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Full Length Article

Mass testing of the JUNO experiment 20-inch PMT readout electronics

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ABSTRACT

The Jiangmen Underground Neutrino Observatory (JUNO) is a multi-purpose, large size, liquid scintillator experiment under construction in China. JUNO will perform leading measurements detecting neutrinos from different sources (reactor, terrestrial and astrophysical neutrinos) covering a wide energy range (from 200 keV to several GeV). This paper focuses on the design and development of a test protocol for the 20-inch PMT underwater readout electronics. The protocol has been employed for 10 months during the mass production and validation of all the electronics that will be installed in JUNO. A total number of 6950 electronic boards were tested with an acceptance yield of 99.1 %.

1. Introduction

The Jiangmen Underground Neutrino Observatory [1] (JUNO) is a 20 ktonnes neutrino medium baseline experiment under construction in southern China. The JUNO experiment has been proposed [2] with the main goals of determining the neutrino mass ordering with a significance of $3\,\sigma$ within the first six years of data taking and measuring the oscillation parameters, Δm^2_{21}, Δm^2_{31}, and $\sin^2\theta_{12}$, with sub-percent precision [3]. To achieve these goals, JUNO is located about 53 km away from two nuclear power plants and will detect electron antineutrinos produced by the beta decays of fission products inside the nuclear cores. JUNO will also be able to address many other topics in particle and astroparticle physics, by detecting neutrinos from natural sources: solar neutrinos, atmospheric neutrinos, geo-neutrinos, neutrinos from core-collapse supernovae, and from the diffuse supernovae neutrino background. An updated overview of the JUNO physics reach can be found here [1].

The JUNO Central Detector (CD) consists of 20 ktonnes of liquid scintillator contained in a spherical acrylic vessel with a 35.4 m diameter, supported by a stainless Steel Truss. A double system of 17 612 20-inch large-PMTs (LPMTs) [4,5] and 25 600 3-inch small-PMTs (SPMTs) [6] is employed to detect the scintillation and Cherenkov light produced by neutrino interactions with the liquid scintillator. The liquid scintillator target is surrounded by a 35-kt pure Water Pool, which is instrumented with 2400 20-inch LPMTs; the Water Pool shields the inner part of the detector from environmental radioactivity, and is part of the muon Veto system, together with the Top Tracker on top of the whole structure.

The JUNO LPMT underwater readout electronic system samples and processes the LPMT output current [7–9]. Spotting hardware failures and evaluating the performance of the underwater readout electronics before the actual installation is of paramount importance, because it will be impossible to repair or to change an electronics module after its deployment. Furthermore, the required loss rate of the electronics channels is less than 0.5% in 6 years [1]. To satisfy this requirement, we follow the strategy: select high reliability components and to detect infant mortality all boards were burnt in. We followed the same procedure used with the previous version of the electronics, as discussed in [7]. To this end, we designed and developed a dedicated test protocol [10,11] to be followed during the mass production, at a dedicated facility in Kunshan, China.

The rest of the paper is organized as follows: in Section 2 we describe the JUNO LPMT readout electronics; in Section 3 we discuss the mass production and the mass testing setup at the dedicated facility in Kunshan; in Section 4 a detailed description of the developed test protocol is presented; conclusions are drawn in Section 5.

2. JUNO LPMT readout electronics

A schematic of the JUNO LPMT electronics is given in Fig. 1. A detailed description can be found in [12]; only details relevant for this work are provided here.

Three LPMTs are connected through 50 Ω, coaxial cables to the *front-end* (FE), or *wet*, electronics [13], which is located very close to the LPMT output, and hosted inside a stainless steel, water-tight box: the Under Water Box (UWBox). In total, the JUNO detector is instrumented with 6681 UWBoxes, 5878 for the CD and 803 for the Water Pool, as part of the JUNO Veto system. Each UWBox contains three High Voltage Units (HVUs), which are programmable modules providing the bias voltage to the LPMT voltage divider, and a motherboard incorporating the front-end and readout electronics components: the Global Control Unit (GCU).

Each GCU implements three readout channels, one for each connected LPMT. The LPMT analog signal reaching the GCU is processed by a custom Front-End Chip (FEC), which duplicates the input signal and injects it in two parallel streams with different gains, referred to as *high-gain stream* and *low-gain stream* (see Fig. 1). The signal from each stream is further converted to a digital waveform by a 14-bit, 1 GS/s, custom Flash Analog-to-Digital Converter (FADC). The digital signal is further processed by a Xilinx Kintex-7 FPGA (XC7K325T), which has the task of generating trigger primitives, reconstructing the charge, timestamp tagging, and temporarily storing the signal before sending it to the data acquisition (DAQ).

The electronics inside the UWBox has two independent connections to the *dry* electronics: a *synchronous link* (S-link) for the connection to the *back-end* (BE) electronics, which provides the clock and synchronization to the boards and handles the trigger primitives; and an *asynchronous link* (A-link) which is fully dedicated to the DAQ and slow-control, or Detector Control System (DCS). A modified dedicated version of the 1588 protocol [14] is used to keep all the boards synchronized and correct time delays due to the cable length difference. Through the A-link, the IPBus Core protocol [15] is used for data transfer [16], slow control monitoring, and electronics configurations. An additional, low-resistance, power cable will bring power to the electronics inside the UWBox.

The three channels of each GCU are independent up to the FPGA. This means that any misbehavior happening before the FPGA will not impact the neighboring channels, while a misbehavior of the FPGA or of the connections to the dry electronics will result in the loss of three channels.

For the purpose of the electronics mass testing described in this work, GCUs were operated in a self-trigger mode, where all channels trigger in parallel and where all readout boards send their locally triggered waveforms to the DAQ, independently of each other, whenever a signal exceeds a given threshold. In this configuration, the BE trigger electronics and the S-link were only used to provide the UWBox with the clock needed to operate properly.

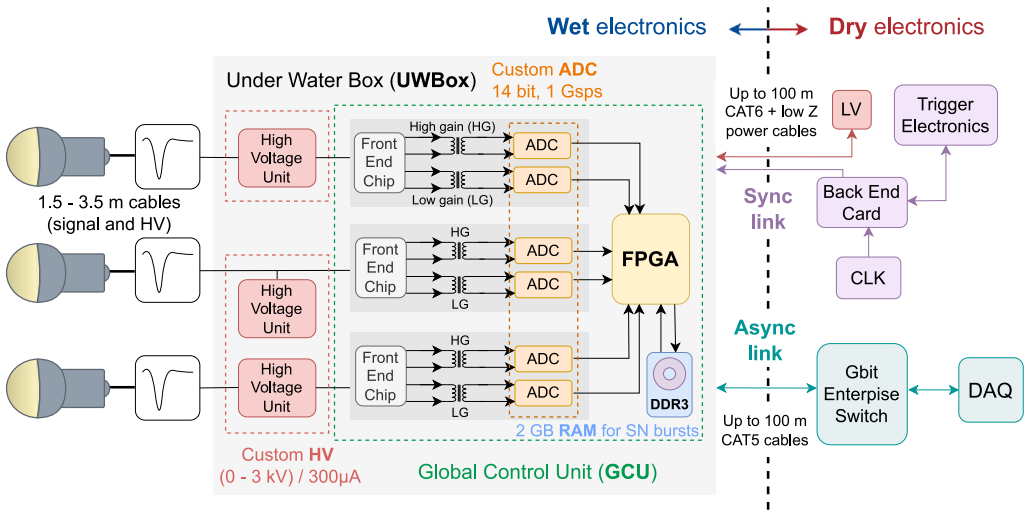


Fig. 1. JUNO LPMT readout electronics schematic [12]. A description of the different parts is given in the text.

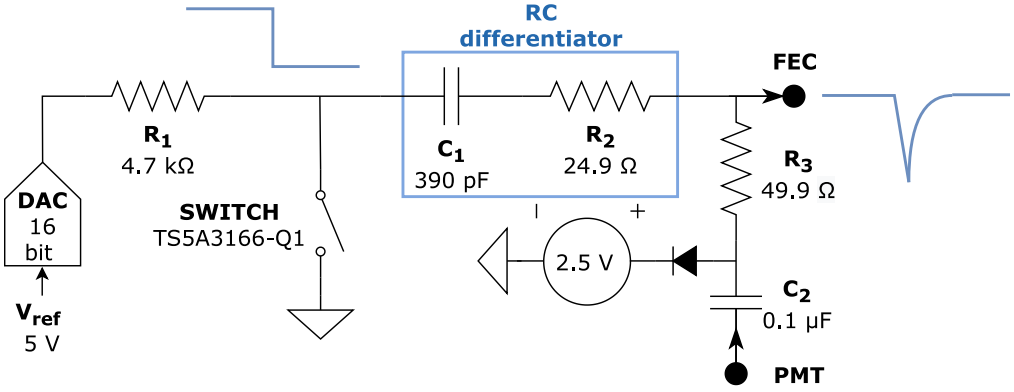


Fig. 2. Schematic of the internal test pulse generator. Each channel is equipped with one internal generator circuit, which is connected directly to the Front-End Chip (FEC). The main components of the circuit are a 16-bit digital-to-analog converter (DAC), a switch, and a RC circuit with $C_1 = 390\,\text{pF}$ and $R_2 = 24.9\,\Omega$. The connection from the PMT to the FEC is also shown; arrows are used to indicate the direction of the signals.

2.1. Internal test pulse generator

Each GCU is equipped with three independent test pulse generator circuits, one per channel; a schematic of the circuit is presented in Fig. 2. The main components of the circuit are a 16-bit digital-to-analog converter (DAC), a switch, and a RC circuit acting as a differentiator, or high-pass filter, with $C_1 = 390\,\text{pF}$ and $R_2 = 24.9\,\Omega$, with a 5 % and 1 % tolerances, respectively; the values of C_1 and R_2 were chosen to produce a signal mimicking a PMT signal.

The amplitude of the generated pulse can be adjusted via the IPbus protocol [15] by changing the input digital amplitude of the DAC (A_{DAC}), which uses a reference voltage of 5 V to convert the digital value to a voltage value. The pulse is generated by closing the switch and connecting the node between the DAC and the differentiator to ground, generating a step voltage, as shown in Fig. 2. The step function goes through a differentiator, or high-pass filter, generating a PMT-like pulse which is injected directly into the FEC of the channel. The switch is also controlled via the IPbus protocol: to generate one pulse, we need to close and then open again the switch, hence two IPbus commands are needed; in this way it is possible to control the frequency at which the switch is closed/opened and the test pulses are generated.

The injected input charge, which is the area of each generated pulse, corresponds to the charge accumulated by the capacitor C_1 under a potential difference equal to the DAC output, evaluated as follows:

$$Q_{\text{in}} = A_{\text{DAC}} \cdot \frac{5\,\text{V}}{2^{16}} \cdot C_1, \tag{1}$$

where Q_{in} is in unit of pC if C_1 and A_{DAC} are in units of pF and DAC counts, respectively. The value $5\,\text{V}/2^{16} \simeq 76\,\mu\text{V/DAC counts}$ is the conversion factor from DAC counts to a tension in volts.

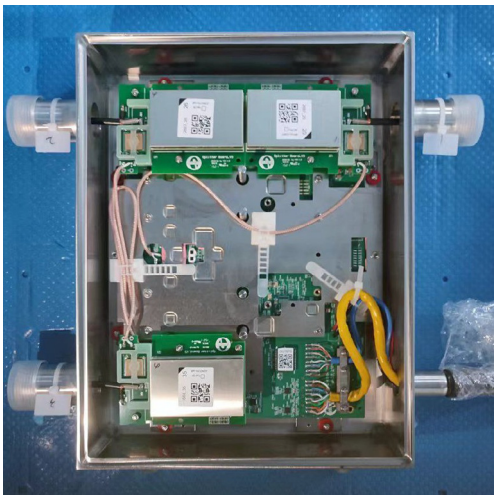
3. Mass production and testing at the Kunshan site

A facility in Kunshan, China, was devoted to the mass production and testing of the 20-inch PMT readout electronics.

3.1. Production process

During mass production, the first step was the welding of the stainless steel bellows to the UWBoxes, followed by a leakage test. Following this, the cables for the S-link, A-link, and the power line were threaded through the bellows. The GCU board and the three HV units were then assembled inside the UWBox and soldered to the cables. The electronics in each box was then tested for at least five days. If it passed the tests, the box was finally laser welded, and – following a further leakage test – was put into store before being sent to the JUNO experimental site. A picture of an assembled UWBox before laser welding is shown in Fig. 3(a).

Before the beginning of the mass production, tests were performed on a small number of boxes to assess the possible damage and risks from the laser welding procedure; it was found that no damage is expected from this procedure. Nonetheless, a shorter version of the tests was performed on each board after the laser welding.



(a) *Assembled UWBox before laser welding.*

(b) *Shelf with UWBoxes in the testing room in Kunshan.*

Fig. 3. (a) Picture of an assembled Underwater Box before laser welding. The three HVUs are clearly visible, one near each of the connectors at which the LPMTs will be connected. The GCU board is located on the bottom. (b) A shelf full of UWBoxes in the testing room at the Kunshan facility. In the front of the picture, a rack with power supplies, switches, and back-end and trigger electronics is also visible.

3.2. Testing of the GCUs

During the test, the assembled UWBoxes and the bellows were located on shelves in a dedicated testing room, as shown in Fig. 3(b); in the front of the picture, a rack with power supplies, switches for the network connection, and the trigger electronics is also visible. The room had space to locate a maximum number of 344 GCUs on nine shelves. All the tests described in Section 4 were performed in parallel on all the GCUs available in the testing room.

The test procedure was automatized in order to minimize human errors during the shifts. Shifts were organized exploiting time zone differences between China, where the boxes were located, and Europe, so that the European part of the collaboration could take part in the mass testing remotely, since it was not possible to travel to China due to COVID-19 restrictions. During daytime in China, local shifters were in charge of assembling between 40 and 60 new UWBoxes per day and replacing them in the testing room. At the end of the Chinese working day, an European shifter took over to perform the tests; in this way it was possible to have shifts covering all 24 h each day. Data analysis on the acquired data from the tests was performed on the following day, in order to provide a fast feedback on the tested boards. The mass testing of all 6950 GCUs lasted for about 10 months from October 2021 to July 2022.

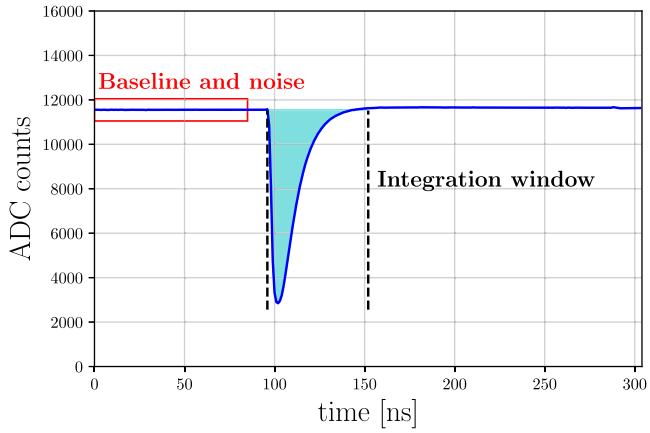


Fig. 4. Example of a digitized waveform from GCU 3133 channel 0, generated with the internal test pulse generator, as described in Section 2.1, and obtained by selecting the high-gain stream. The first 85 samples are used to evaluate the values of the baseline and the noise. The limits of the charge integration window are shown as dashed black lines.

3.3. Network and connection details at the Kunshan site

In the testing room, GCUs were connected to the BECs in batches of 40 in order to provide the clock to the tested boards through the synchronous link. For the asynchronous link, 40 GCUs were connected to a level 1 (L1) switch through a 1 Gb link, for a total of nine L1 switches; L1 switches were then connected to a level 2 (L2) switch through a 4x10 Gb link; the L2 switch was finally connected to the DAQ server via a 4x100 Gb link. The DAQ server consisted of a Dell PowerEdge C6400, with a total of 24 cores and 48 threads, a 2.7 GHz processor and 192 GB RAM. A dedicated local network was used for the communication between the GCUs and the server.

4. Test protocol for the LPMT readout electronics

We designed and implemented the test protocol [10,11] according to the following criteria:

- it had to be controlled remotely and to be run in parallel to the production line;
- it had to be easy to operate, in order to have non-expert shifters being able to join the testing campaign;
- it had to provide the shifter with a fast and visual feedback of the performance of the tested components.

The test protocol was performed on each electronics card after all the components had been fitted, as described in Section 3.1, and before the UWBox was finally sealed. The protocol consisted of several steps:

(1) a ping test (Section 4.3), to check the connection of the board to the local network;
(2) a linearity (Section 4.4) and a stability (Section 4.5) tests investigating the properties of the digitized waveforms to validate the performance and the reliability of the whole readout chain;
(3) a DCS test (Section 4.6) to monitor the temperature and the status of the board.

Each test is presented in more details in the following subsections.

The tests of step (2) were performed separately on the high-gain and on the low-gain streams. Input signals were generated in both cases by the internal test pulse generator, but either the high-gain stream, or the low-gain stream was selected for the readout of the digitized waveform.

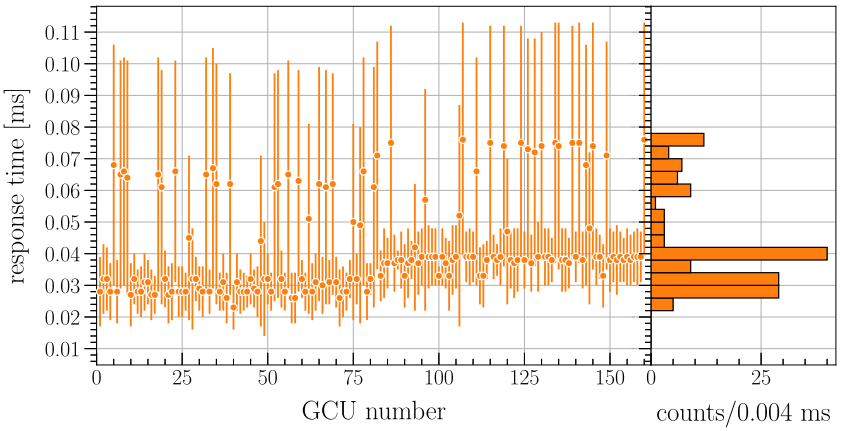


Fig. 5. Ping test results for a batch of 160 GCUs [11]. The plot on the left shows the mean response time and its standard deviation for each GCU; the plot on the right shows the distribution of the response time of the batch of GCUs. A step in the response time is visible around GCU 80, pointing at differences in cable lengths and network configuration between the first 80 GCUs and the other 80 boards of the batch. Large values of the uncertainty are caused by large variations in the ping response time in certain GCUs. This is associated with a longer than usual average delay time, though this parameter is not considered critical.

4.1. Properties of the digitized waveform

Fig. 4 shows an example of a digitized waveform generated by the internal test pulse generator described in Section 2.1, where the high-gain stream was selected. During the tests, the length of the readout window, and hence the length of the waveform, is fixed to 304 samples which correspond to 304 ns, given the FADC sampling frequency of 1 GS/s.

For each digitized waveform, baseline and noise are evaluated. The baseline, B, is defined as the average of the first 85 samples; the noise, σ_{baseline}, is defined as the standard deviation computed on the same samples.

Another property which is monitored during the test is the waveform integrated charge. The waveform integrated charge, Q_{out}, corresponds to the shadowed region in Fig. 4 and it is evaluated offline as in the following equation:

$$Q_{\text{out}} = \sum_{i}^{N_s} \frac{75\,\mu\text{V} \cdot \left(B - N_i\right) \cdot \Delta t_s}{R}, \tag{2}$$

where N_s is the number of samples in the integration window, N_i is the amplitude in ADC counts of the ith bin, B the baseline value as defined above, 75 μV is the voltage corresponding to 1 ADC count, $R = 50\,\Omega$ is the input impedance, and Δt_s is the width of a single bin; in our case $\Delta t_s = 1$ ns. The integration window, shown in Fig. 4, starts 5 ns before the minimum, or peak, of the waveform, and extends out to 50 ns after the minimum.

In Eq. (2), the conversion factor between ADC counts and voltage, 75 μV/ADC count, is a characteristic of the FADCs, and it is the same for the high-gain and low-gain streams. In this way, Eq. (2) does not take into account the gain of the amplification step in the FEC, which in turn has to be determined through the linearity test of the test protocol, as explained in Section 4.4.

4.2. Configuration of the GCUs

The following GCU parameters needed to be set through the slow control before each test:

1. the length of the readout window;
2. the value of the pre-trigger;
3. the value of the trigger threshold;
4. the trigger mode.

For the mass production tests, we fixed the length of the readout window to 304 ns to optimize the total size of the acquired data. The pre-trigger is the time interval between the beginning of the readout window and the moment at which the signal exceeds the threshold, *i.e.*, the region that precedes the pulse.

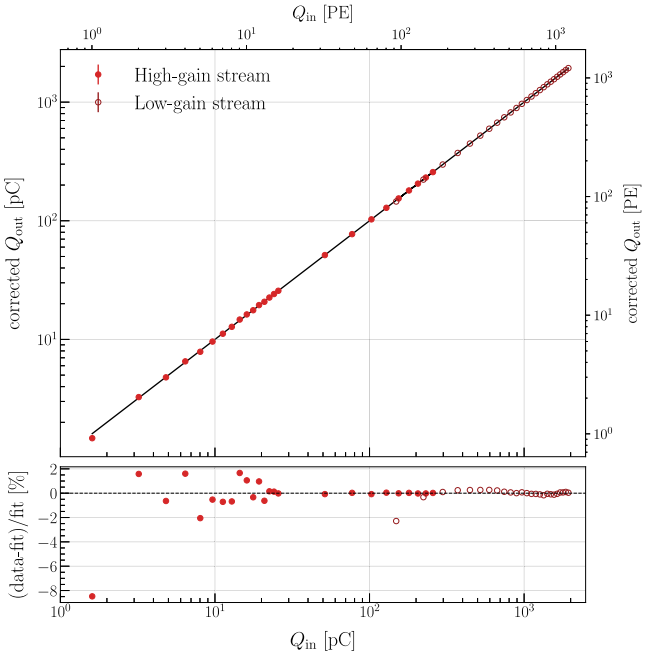
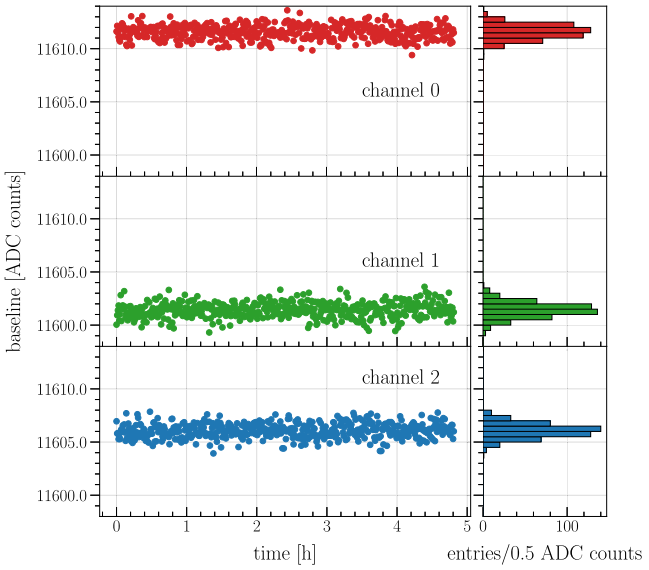


Fig. 6. Results from the linearity test for one channel of a typical GCU for the high-gain (full circles) and low-gain (empty circles) streams. The input charge is evaluated by using Eq. (1), while the output charge is first evaluated through Eq. (2) and then corrected for the gain obtained from the quadratic fit. Charges are also expressed in number of PEs on the secondary axes, where 1 PE = 1.6 pC.

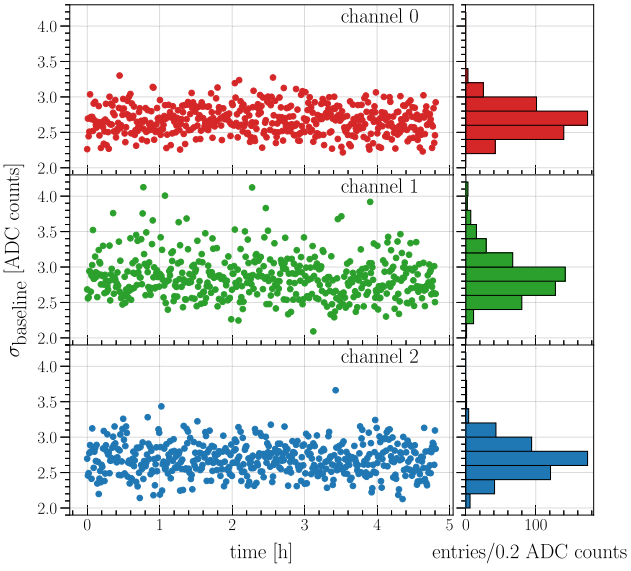
There are two possibilities for the trigger threshold: the threshold is either fixed to a given value in ADC counts, and is the same for all channels; or it is evaluated for each channel in terms of σ_{baseline} from the baseline. During the tests, the trigger threshold was fixed to a common value for all channels. The trigger modes were described in Section 2. During the tests, the trigger mode was set to the locally-triggered configuration in which channels trigger independently from each other with the BE trigger electronics not employed.

4.3. Ping test

The first step of the test protocol is the ping test, meant to check that all the GCUs are properly connected to the local network and



(a) *Results of the stability test for the baseline.*



(b) *Results of the stability test for the noise.*

Fig. 7. Evolution of the (a) baseline and (b) noise over a 5-hour stability run for the three channels of a typical GCU [11]. The plots in the left panel show the baseline and noise evaluated on single waveforms as a function of time; the plots in the right panel show the distribution of the baseline and noise values. For all three channels, both the baseline value and the noise are within the acceptance intervals.

responding. A non-responding board would imply either that the cables are not properly plugged in, which is an easy issue to solve, or that the assembling procedure had not been successful, thus requiring further investigation on the production side.

For this test, we used the default Linux `ping` command and sent 100 56-byte packets in 1 s from the DAQ server to each GCU, so that it was possible to test in a few seconds the connection to the local network of hundreds of boards. The IP addresses were automatically recovered by the input GCU ID number. The `ping` command directly calculates the mean response time and its standard deviation, which were both stored, together with the fraction of lost packets.

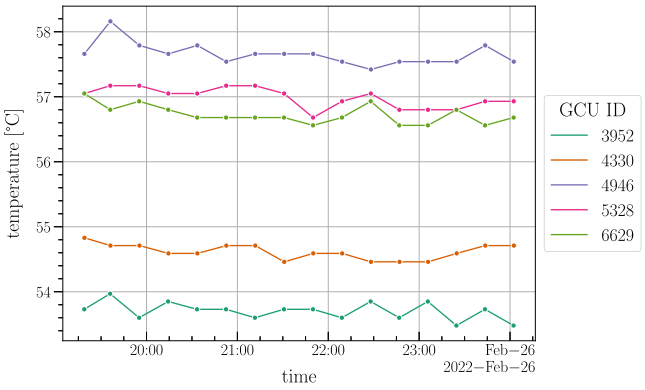


Fig. 8. The figure shows the evolution of the FPGA temperature for 5 GCUs, recorded from the slow control monitoring. The different temperature values are due to the different positions of the GCUs in the testing room in the dedicated facility at Kunshan.

As a quick visual feedback for the shifter, the mean response time and its standard deviation were recovered and plotted versus the GCU ID number; an example with a batch of 160 GCUs is shown in Fig. 5. The mean response time depends on the length of the asynchronous link cables and on the network configuration.

4.4. Linearity test

The linearity test was meant to test the linear response of the two FADCs serving each channel and evaluate the gain factors of the two data streams in the FEC. The test was performed by generating PMT-like signals with the internal test pulse circuit described in Section 2.1. Before this test, the channel linearity was studied with external physics sources and by reading PMT signals on a small set of boxes [12,17].

For the test, values of the test pulse amplitude were chosen to cover a wide range. For the high-gain stream, the range starts at 1 PE up to about 160 PE, before the beginning of the saturation regime. For the low-gain stream, the range starts at about 90 PE up to the maximum possible value of the DAC, corresponding to about 1200 PE. The two ranges overlap, allowing us to check the cross range between the two streams. The frequency of pulse generation and the acquisition time were set to provide more than 2000 waveforms for each linearity point. Parameter settings, test pulse generation, and data acquisition were completely automatized.

Raw data were then processed and saved in `ROOT` [18] files as `TTree` objects. For each channel and each input DAC amplitude, the integrated output charge was evaluated according to Eq. (2); the evaluated values were then collected into a histogram and the mean value was taken as the output charge corresponding to the given input DAC amplitude. Finally, for each channel, a quadratic fit was done for both data streams to extract the gain factor of the two FEC streams, with the fit function defined as:

$$Q_{\text{out}} = c_2 \cdot Q_{\text{in}}^2 + G \cdot Q_{\text{in}} + c_0, \tag{3}$$

where Q_{out} and Q_{in} are the output and input charge defined by Eq. (1) and (2), respectively, G is the dimensionless gain of the FEC stream, c_0 is the intercept, and c_2 is the coefficient of the quadratic term. A quadratic function was used because the response is not perfectly linear, due to the integral non-linearity (INL) which is characteristic of ADCs and DACs; we expect the quadratic term to be subdominant with respect to the linear term. The gain G is expected to be < 1; the reason for this design choice is that the FEC input signal is expected to reach amplitudes exceeding the typical FADC dynamic range, hence the necessity to attenuate and not amplify the signal.

Fig. 6 shows the results of the linearity test for one channel of a typical GCU for the high-gain stream (full circles) and the low-gain stream (empty circles). A quadratic fit was done on both streams, yielding the following results:

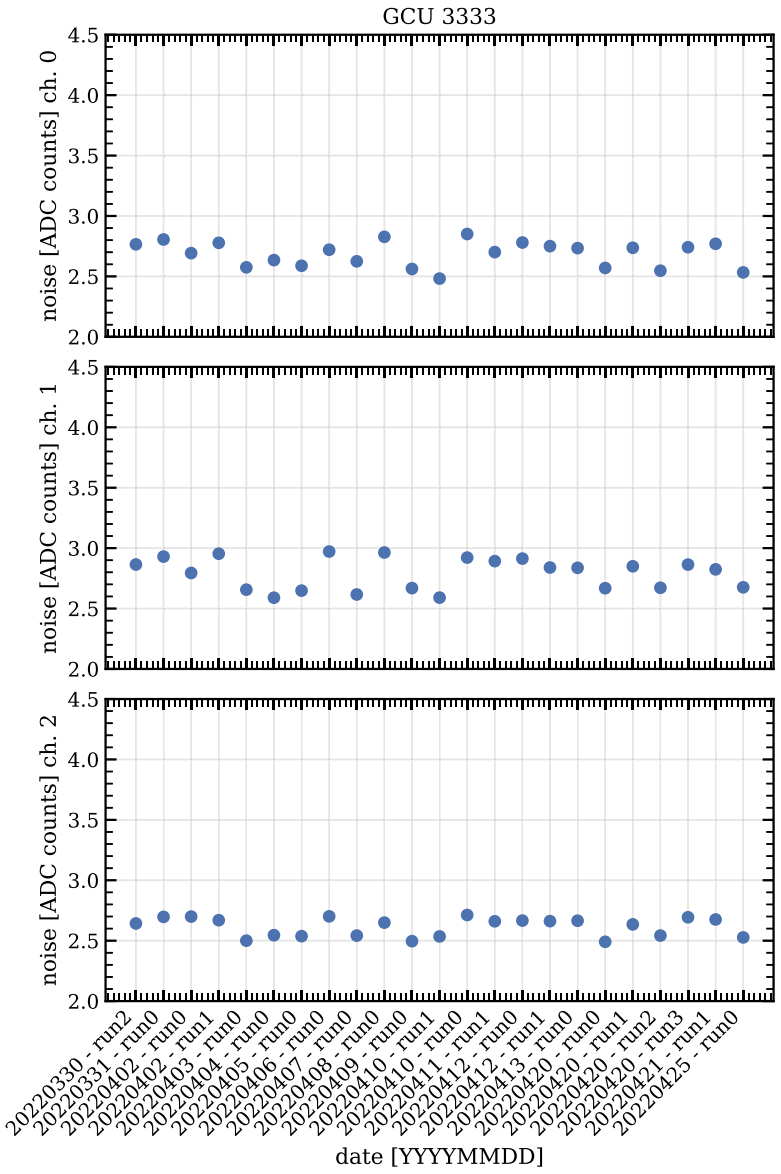


Fig. 9. Results of the stability test from several runs for GCU 3333 are shown. The three panels show the values of the noise for channel 0 (top), channel 1 (middle) and channel 2 (bottom). The noise for all channels is stable and within the acceptance range over a period of more than 25 days.

- in the [1.6, 257] pC high-gain range: $c_0 = (-0.01 \pm 0.02)$ pC, $G = 0.5856 \pm 0.0006$, and $c_2 = (-4.5 \pm 0.3) \times 10^{-5}$ pC^{-1};
- in the [149, 1934] pC low-gain range: $c_0 = (0.90 \pm 0.08)$ pC, $G = 0.0850 \pm 0.0002$, and $c_2 = (-3.3 \pm 0.9) \times 10^{-6}$ pC^{-1}.

The corrected output charge shown in the plot was first evaluated through Eq. (2) and then corrected with the gain obtained from the quadratic fit; as can be seen, after the gain correction the two data streams lie on the same line. The bottom panel shows the residuals of the corrected output charge with respect to a linear fit; the dispersion at low values of the input charge could be explained as low SNR, while the non-linearity at high charge is typical for an ADC. In the figure, input and output charges are expressed in picocoulombs on the primary axes and in terms of number of photo-electrons (PE) on the secondary axes, with $1\,\text{PE} = q_e \cdot G_{\text{PMT}} = 1.6\,\text{pC}$, where q_e is the electron charge, and $G_{\text{PMT}} = 10^7$ is the assumed nominal PMT gain of the 20-inch PMTs in JUNO [1,5].

During the analysis, we also checked for the saturation amplitude of the high-gain stream, while for the low-gain stream we could not reach saturation with the internal test pulse generator. In the high-gain configuration, channels saturate for an input signal of about 16500 DAC counts, corresponding to an input charge of about 450 pC $\simeq$ 280 PE. Data points above the saturation threshold are not used in the linear fit and are not shown in Fig. 6.

4.5. Stability test

The stability test consists in firing the internal test pulse generator with a fixed amplitude over a time period lasting several hours, and to check that the waveform properties listed below do not change. The input amplitude was set to 12000 DAC counts for the high-gain stream and to 45000 DAC counts for the low-gain stream. The frequency of the test pulses was set to 1 Hz, while the data acquisition time was determined by the available time during the shift.

The waveform monitored parameters are: baseline, noise, minimum value of the waveform, and minimum position in the readout window. The baseline and noise are obtained as described in Section 4.1. These quantities were obtained by processing raw data and saved in ROOT files as TTree objects.

As an example, Figs. 7(a) and 7(b) show the results of the stability test for the baseline value and the noise of a typical GCU, respectively.

The values of the baseline and the noise as a function of time are shown for the three channels in three different panels; distributions of the values are shown as well. From Fig. 7(a), we can see that the baseline values for the three channels lie between 11600 and 11615 ADC counts, well within the acceptance range of [11000, 12000] ADC counts. The accepted noise level is between 2 and 4.5 ADC counts, corresponding to about 0.03 PE and 0.08 PE respectively, and, as can be seen in Fig. 7(b), the evaluated values lie within these limits.

4.6. Slow control monitoring

The slow control monitoring is meant to read several internal parameters and sensors installed on the GCU and to monitor the overall status of the board. All sensors were read through the IPbus protocol [15] in parallel to the DAQ and over the same transport layer.

For each GCU, the following parameters were read during the slow control monitoring: the temperature of the FPGA, the temperature and the high voltage value of each HVU, and several FPGA internal reference voltages [19].

As an example, Fig. 8 shows a plot of the evolution of the FPGA temperature for five GCUs. For all GCUs, the FPGA temperature is stable over time. The difference in the absolute values is due to the different positions of the GCUs on the racks in the testing room (see Section 3). The testing room was equipped with an air conditioning system with a constant temperature of about 26 °C.

4.7. Storing of test results into a database

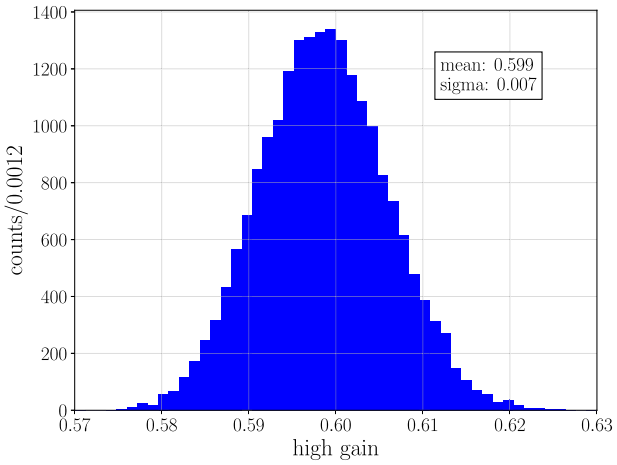
The information on the configuration and parameters used for the tests, together with the results of the tests, are saved in a MySQL database which is available on the local server at the Kunshan site. Storing these kinds of information is important to have an history of the performance of each GCU, and to compare the results during mass production with the tests foreseen for the upcoming installation and commissioning phases.

Fig. 9 is obtained by accessing the local database and shows the value of the noise from the stability test for several days and runs for GCU 3333; each panel shows results for one of the three GCU channels. The runs shown in the figure span a time period of more than 25 days, during which the noise is stable and within the acceptance range.

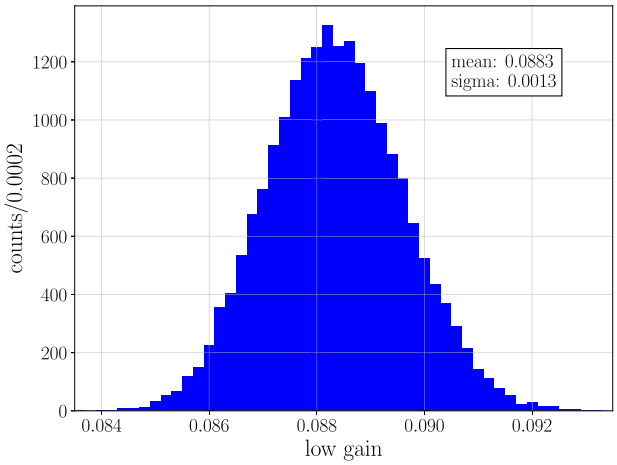
Figs. 10(a) and 10(b) show the distributions of the high-gain and the low-gain values, respectively, obtained in the linearity test by using Eq. (3). The distribution for the high-gain stream has a mean of 0.599 and a standard deviation of 0.007, while the distribution for the low-gain stream has a mean of 0.0883 and a standard deviation of 0.0013.

5. Conclusion

A test protocol was developed to evaluate the performance of the 20-inch PMT readout electronics for the JUNO experiment during mass production. A total of 6950 devices were tested in about ten months. Only eight GCUs were discarded on the basis of the tests presented in this work and the criteria shown in Table 1. Another 56 GCUs were discarded due to issues that arose during the assembling procedure. In total, 6886 GCUs were accepted, while only 64 were rejected, providing a final acceptance yield of 99.1 %. Out of the 6886 accepted cards, 6681 will be used in the CD and Water Pool veto system, 25 will be used by OSIRIS [20], while the remaining 180 will be kept as backup. The test protocol described in this paper will be used as a reference for the upcoming tests during the installation and commissioning phases, where a few adjustments are needed given the different environmental conditions and setup.



(a) *Gain distribution for the high-gain stream.*



(b) *Gain distribution for the low-gain stream.*

Fig. 10. Distributions of the gain obtained from the linearity test for (a) the high-gain stream and (b) the low-gain stream. The distribution of the high gain has mean and standard deviation equal to 0.599 and 0.007, respectively; the distribution of the low gain has mean and standard deviation equal to 0.0883 and 0.0013, respectively. For both histograms, the gains of all the three channels of 6900 GCUs are included, for a total of 20700 entries; the gains from the first 50 tested GCUs are not included.

Table 1
Acceptance range for the baseline, noise, high gain, and low gain, used as acceptance criteria for the evaluation of the performance of each GCU.

Parameter	Acceptance range
Baseline	11,000 – 12,000 ADC counts
Noise	2 – 4.5 ADC counts
High gain	0.5 – 0.65
Low gain	0.05 – 0.095

Declaration of competing interest

The authors declare the following financial interests/personal relationships which may be considered as potential competing interests: Alberto Garfagnini reports financial support was provided by Government of Italy Ministry of Foreign Affairs and International Cooperation. Xiaoshan Jiang reports financial support was provided by National Natural Science Foundation of China.

Data availability

The authors are unable or have chosen not to specify which data has been used.

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