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RESONANT CLASS-E DC-DC CONVERTERS:
an innovative analysis and design approach

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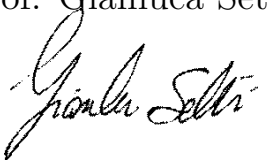

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RESONANT CLASS-E DC-DC CONVERTERS: an innovative analysis and design approach

by
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Abstract

In this thesis, a novel methodology for resonant dc-dc converters analysis and design is introduced and applied to an entire family of class-E topologies. These architectures, exploiting the so-called *soft-switching* technique to allow high frequency operation, are derived from a general resonant topology featuring the minimum number of reactive elements and enable a dramatic reduction of future power conversion systems size and cost. Furthermore, due to their simplicity, they encourage the development of a new, comprehensive analysis method exploiting the exact analytical solution of the differential equations regulating circuit state variables evolution. Such an approach, derived from the well-known state-space modeling theory, permits to overcome the main state-of-the-art limitations due to the non-trivial combination of concepts and techniques from historically disjoint disciplines: power electronics and RF amplifiers design.

The first outcome of this ODE-based methodology is the straightforward computation of a set of dimensionless design curves that, once converter specifications are known, can be readily exploited to get a first lossless design solution. The proposed modeling method is then extended including the main device losses and the possibility to get an accurate estimate of converter efficiency early in the first design phase. Measurements on two PCB prototypes show a remarkable matching with the semi-analytically computed system waveforms without the need for any additional circuital simulation.

Finally, thanks to the versatility of the developed mathematical framework also some advanced features can be investigated, such as the possibility to embed an isolated bidirectional Power-Line Communication (PLC) link with minimum hardware overhead. A new 1 MHz PCB prototype is realized to validate this innovative isolated power/data link solution. Bit error rate measurements, accomplished exploiting two *Tiva C Launchpads* to generate and compare both forward and backward data streams, show that 1 Mb/s maximum data rate is achievable with $BER < 10^{-9}$ in both directions with negligible power conversion efficiency degradation (3-4%).

Acknowledgments

There are several people I would like to thank at the end of this incredible journey. First of all, Prof. Gianluca Setti, for believing in my potential and giving me the possibility to apply for a PhD position at the University of Ferrara three years ago. I am also really grateful to the main supervisor of all my PhD activities, Ing. Fabio Pareschi, for his deep and always positively critical contribution in turning some vague ideas into solid research topics and working circuit prototypes. Many thanks to all the people that sustained me during my US scholarship, especially Prof. Pamela Abshire and Prof. J. Z. Simon from the Institute for System Research, University of Maryland and Ing. Mauro Mangia from the University of Bologna. I cannot forget to mention Prof. Riccardo Rovatti and Prof. Sergio Callegari for invited talks on my research topics at the University of Bologna. A special mention also goes to the two appraisers of my dissertation, Prof. Gabriele Grandi, University of Bologna and Prof. Eduard Alarcón, Technical University of Catalunya, for their valuable comments and suggestions. A very special gratitude goes out to all my colleagues and friends in Texas Instruments, especially Giovanni Frattini, Roberto Massolini, Pierluigi Albertini and Maurizio Granato who helped me developing innovative ideas every single week for the last three years. Last but not the least, I would like to fervently thank all my family, especially my mother Cristina and my father Bruno; there are no words to define what you gave to me throughout the course of my life. Finally, my love Drilona for always supporting me and never let me forget who I really am.

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Chapter 1

Introduction

In 2003 the Roadmapping Initiative of the European Center of Power Electronics (ECPE) started with the aim of defining the main guidelines in the development of new technologies and concepts for the future power electronic systems [1]. After an analysis of the state of technology, a set of performance indices has been defined to implement a quantitative plan of action based on a future vision of society in 2020. The main performance indices considered, reported in Figure 1-1, are actually mutually coupled and usually a compromise between some of them must be accepted.

Traditionally, these trade-offs, exhamined in the definition of roadmap goals, are analyzed recurring only on the experience of the engineers and researchers involved. In

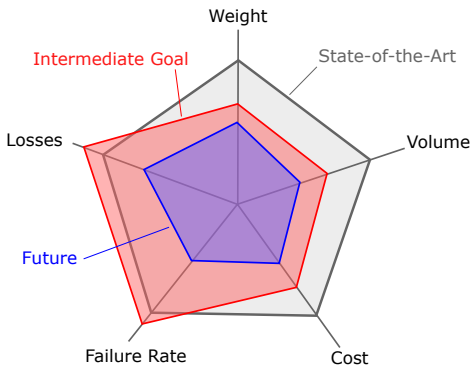


Figure 1-1: State of the art, required future performance and intermediate goals in the development of next generation power electronic systems

this way, what is missing is a clear picture of the relation between a given technology base and the performance achievable exploiting the existing circuits, operating modes and control procedures. An **accurate mathematical modeling of new power converters, along with their parasitics**, would be extremely important to see in advance the effect of a change in the technology base, e.g. an improvement in the figure of merit of the semiconductor devices, on the system performance and consequently drive the development of new technologies and circuital architectures well in time with respect to future market needs.

One of the most important trends is trying to reduce the converter size and cost while mantaining high conversion efficiency. However, higher power density implies higher switching frequency, which potentially leads to increased losses in the circuit (red area in Fig. 1-1). To overcome this limitation **resonant power converters** [2] have been introduced, in the early 80's, with the aim of reducing the impact of frequency dependent losses on efficiency. One of the main issues with this type of *soft-switched* topologies is that there is currently no consolidated design and optimization methodologies to help a faster diffusion in both industrial and consumer applications. In fact, even though this topic has been intensively explored in the past years, it is still very challenging and many aspects remain unsolved, probably due to the fact that it requires to combine concepts and techniques from historically disjoint disciplines such as power electronics and Radio Frequency (RF) amplifiers design [3].

The principal aim of this thesis is to help moving a step forward in resonant converter design through a new comprehensive mathematical modeling approach which can be applied to various converter architectures sharing the same resonant network.

1.1 The Need for HF/VHF Power Converters

There are several advantages connected to a very high switching frequency. Two of them are noteworthy: first, **better transient performance and bandwidth** can be achieved; second, constraints on the values of passive reactive elements are relaxed and, in general, **smaller and less expensive components** are required. This allows to increase the converter power density and supports the ultimate goal of adopting magnetic components small enough to be embedded into a **fully integrated solution**. Furthermore, the converter miniaturization allows to place the power supply closer to the load and to reduce the voltage drop due to parasitic resistances and inductances. This could be particularly beneficial for the rapidly changing load in new generation multi-core microprocessors and ICs in future computers and telecom applications. In such a system, a higher operating frequency also allows the output voltage of the power converter to be tightly regulated with smaller filters. Finally, having miniaturized power supplies can open the way towards a new scenario where the single external power source is replaced with a large number of high-efficiency, low power, small size, distributed power modules. This can particularly simplify the power management for applications, such as mobile phones, where various voltage levels are required within the chip.

Unfortunately, the design of a power converter switching at High or Very High Frequency (HF/VHF) poses several challenges, ranging from device technology improvement to the need for new circuital architectures, design techniques and control strategies.

1.1.1 Device and Packaging Technology

Power semiconductor device technology has greatly improved in the last decades with a simultaneous increase of the switching frequencies. With advances in technology of semiconductors, the commonly adopted figure of merit (FOM) of power semiconductor switches (defined as the product of the on-state resistance R_{DS}^{ON} with the amount of charge Q_G necessary to turn-on the device), which actually represents

an index about the maximum frequency of operation achievable without incurring into intolerable *conduction losses*, has been greatly reduced. It means that with the same R_{DS}^{ON} (i.e. the same conduction loss) less input capacitance would need to be charged to turn-on the device (decreased *gating loss*) or, equivalently, with a given input capacitance a lower R_{DS}^{ON} would help reducing the conduction losses. However, since the gating loss is directly proportional to switching frequency, a further improvement of the FOM of power switches would be really important to increase the performance of future HF Switched-Mode Power Supplies (SMPS). Some interesting research in this direction has been developed at MIT for both discrete and integrated implementations [4, 5].

On the other side, in the last decades no major breakthroughs have been achieved in the **energy storage elements** for high frequency operation, and passive components still dominate the volumes of power converters. Consequenlty, in order to achieve significant benefits from their size reduction radical increases in switching frequency are required. However, at higher frequencies many concerns arise: (a) Inductors and transformers losses grealty increase because both core losses in ferrite materials and copper losses are strongly dependent on frequency. (b) The magnetic permeabilitiy of ferrites also depend on frequency and, as a result, higher switching frequencies do not always lead to smaller sizes of magnetic components. Hence, in order to achieve dramatic reduction in magnetics size either new magnetic materials must be developed or sufficiently high switching frequency will be required to enable coreless inductors and transformers introduction. (c) Capacitor's dielectric loss also increases with frequency and negatively impacts the overall system efficiency. In fact, despite through advanced manufacturing techniques and new materials (especially ceramics) capacitor technologies are already suitable for frequencies of 10 MHz and beyond, further improvements would be important to increase the energy density and reduce the dissipation factor.

Furthermore, along with technology improvements and volume reduction for both semiconductor and passive components, new **integration techniques** must be developed to make them compatible and to cope with increased contact resistances and

parasitic inductances in conductors and interconnections. More advanced and more efficient **thermal management** will also be required to effectively remove the heat through smaller surface areas to satisfy the increasing demand for faster, smaller, cheaper and more reliable HF/VHF power converters. For high frequency and highly distorted signals, conventional **measurement equipments** are no longer suitable due to their limited bandwidth and dynamic frequency response. In addition, the intrusion of probes is becoming more challenging as power converters are shrinking in size and the values of parasitics introduced in the circuit are becoming commensurate with the values of the passives in the circuit. As a consequence, for VHF converters it will be difficult to avoid measurements aberration and new developments in instrumentation technologies will be required.

1.1.2 Converter Topologies

The efficiency drop when operating at HF relies not only on the decrease of device performance but also on some circuit-level considerations, since in conventional hard-switching architectures there are two loss mechanisms that severely increase with the switching frequency. *Switching loss* arises from the non-negligible time in which the voltage across the switching device and the current flowing through it are simultaneously high, as exemplified in Figure 1-2. Plotting the $[V_{sw}(t), I_{sw}(t)]$ loci of a switching device during the whole switching period, the area under the curves can be actually interpreted as the power loss dissipation due to voltage-current overlap. Ideally, when the switching device is turned-off I_{sw} should be already zero before V_{sw} starts rising and, similarly, at turn-on the current starts flowing through the device after V_{sw} is already zero, as sketched in Figure 1-2(c). Unfortunately, the semiconductor switching devices are not ideal components and their capacitive parasitics make the turn-on and turn-off times not negligible with respect to the switching period, especially when the converter is operated at HF. For this reason the actual V_{sw}-I_{sw} loci are more like those depicted in Figure 1-2(a). Addtionally, another limit is given by the energy stored in the parasitic drain-to-source capacitance C_{oss}, that is almost instantaneously dissipated each turn-on, giving rise to an additional power loss proportional to $f_s\, C_{oss}\, {V_{sw}}^2$.

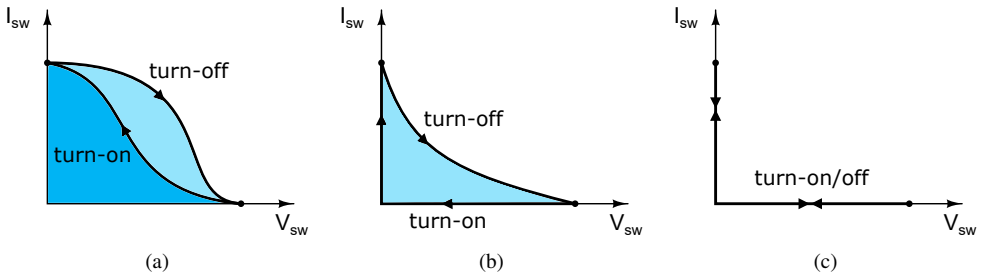


Figure 1-2: Switching converters V_{sw}-I_{sw} loci (a) conventional hard-switched (b) resonant with zero power loss at turn-on (c) ideal. Colored areas represent the amount of switching loss due to voltage-current overlap.

All these effects lower the converter efficiency at HF, and for this reason conventional hard-switching converters operation is actually limited to a few MHz. To overcome this limitation, the switching losses can be mitigated introducing **new converter architectures** such as *resonant* and *quasi-resonant converters*. Roughly speaking, they exploit additional resonant elements to properly shape the current and voltage waveforms of the converter in such a way that the $V_{sw}I_{sw}$ product at the switching instant is reduced as well as the amount of charge stored in the parasitic capacitance C_{oss} thus enabling higher switching frequency to be employed without incurring in excessive efficiency penalty. Acting on the converter topology it is possible to achieve soft-switching conditions but, generally, it is extremely difficult to impose it at both turn-on and turn-off transitions. Usually, a zero-voltage transition at turn-on, depicted in Figure 1-2(b), is preferred.

Furthermore, *gating loss*, which is the power loss necessary to drive the gates of the MOS switching devices, is also directly proportional to the switching frequency and the input capacitance C_{iss}. In a similar way with respect to the power section of the converter, also in the drive circuitry additional resonant reactives can be added to conserve the energy which is used to turn-on the main switching device instead of throwing it away every clock cycle. This approach is commonly employed in the so-called *resonant* and *self-resonant gate drivers* [6, 7, 8].

1.1.3 Analysis and Design Techniques

Along with the research on new circuital topologies which are suitable for HF operation, also **new analysis and design methodologies** must be accordingly developed. In fact, introducing new reactive elements makes the circuit analysis more challenging and even more difficult to find some standard design rules to follow in order to get the desired soft-switching behavior. To overcome the impasse, in the past years, especially for resonant architectures derived from the telecommunication amplifiers, such as the class-E inverter, the followed strategy was to readapt the well-known RF design concepts. However, this kind of approach, consisting in introducing filters and matching networks to justify some assumptions made to simplify the design procedure, is clearly in contrast with the aim of reducing the converter size and cost without too much impact on system performance in overall pursuit of electronic energy management frontends for high efficiency and high power density applications.

The alternative approach proposed in this thesis is to develop a new self-consistent and design-oriented methodology for resonant power converters analysis from scratch:

- First, **converter topology simplification** is addressed and an entire family of resonant converters sharing the same resonant network is presented. The considered resonant tank features the minimum number of reactive elements to get the desired soft-switching behavior, coherently with the aim of reducing size and cost in the future power conversion systems.

- Then, due to its simplicity, it enables the possibility to easily develop a comprehensive mathematical model leading to a **novel unified analysis and design methodology** obtained extending the well-known state-space modelling approach to resonant converters.

Before going into details of the fundamental thesis contributions, in the next sections a brief introduction about the resonant converters derived from class-E RF amplifier topology and the state-space modelling theory, which will be exploited for resonant converters mathematical description, is given.

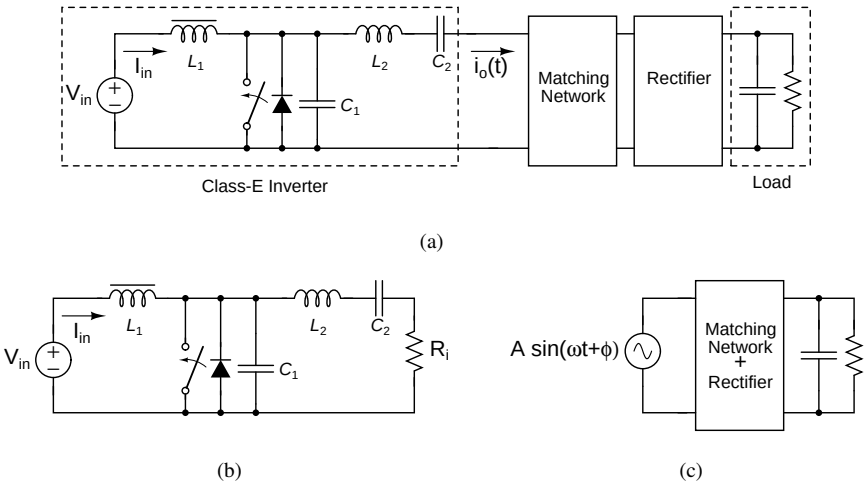


Figure 1-3: RF class-E amplifier inspired dc-dc converter topology (a) Class-E inverter coupled with a rectifying section by means of an impedance matching network. (b) Class-E amplifier with equivalent resistive load. (c) Rectifying stage designed with equivalent sinusoidal source input.

1.2 Resonant Class-E Converters: State-of-the-Art

The idea of applying the RF design concepts to high-frequency dc-dc power conversion was firstly introduced by Gutmann [9] at the early beginning of the '80s. What the author had in mind was a future where the conventional approach of employing a single power source to supply large blocks of electronic circuitry could be substituted by a new scenario with a large number of distributed small power modules. In order to investigate the feasibility of his conviction, he started considering the appllicability of the Class-E amplifier, recently conceived by N. O. Sokal and A. D. Sokal [10], as inverting stage for a dc-dc power converter, as depicted in Figure 1-3(a).

The class-E inverter, depicted separately in Figure 1-3(b), features a large RF choke inductor L_1 to obtain an almost constant dc input current I_{in} (allowing a simplified design procedure), a semiconductor switch with resonant parallel capacitor C_1 and a non-resistive load network that, once properly designed, ensures the desired soft-switching behavior and filters-out all the higher order harmonic contents of the output current. The key features of the class-E with respect to the common class-D

amplifiers can be summarized in the following:

- circuit waveforms are sinusoidally shaped (instead of rectangular-like) allowing to reduce the voltage-current product on the switching device, and consequently the associated power loss, at the switching instants;
- switching time requirements on the semiconductor devices, usually needed to be a small fraction of the switching period to minimize the switching losses, are relaxed;
- harmonic tank circuits are introduced to achieve the desired waveshaping and to provide the required impedance matching with the rectifier section;
- reactive parasitics of both semiconductor devices, passive elements and interconnections can be suitably incorporated into circuit design.

Interestingly, for a given ducty cycle D, depending on the value of the parallel capacitor C_1 and of the network *loaded* Q, defined as

$$Q_L = \frac{\omega_2 L_2}{R_i} = \frac{1}{\omega_2 R_i C_2} \tag{1.1}$$

with $\omega_2 = 1/\sqrt{L_2 C_2}$, three main kinds of transient response voltages can be observed. If Q_L is too low (overdamped) the voltage across the capacitor C_1 never returns to zero. Hence, when the transistor is turned on C_1 must be discharged from some positive voltage V_s to a near-zero value, giving rise to an unwanted power dissipation estimated as $f_s C_1 V_s^2$ which is independent of the switch series resistance. Furthermore, both high voltage and high current occur causing additional power loss and heating on the device that could be irreversibly damaged. On the contrary, with too little damping (Q_L too big) the voltage will go negative until the antiparallel diode, in case of a MOS transistor, will turn on dissipating power (hence reducing efficiency). When optimal values of C_1 and Q_L are chosen, the voltage smoothly goes to zero with also zero time derivative just before transistor turn-on reducing, ideally down to zero, the associated switching loss. These soft-switching techniques are known as **Zero-Voltage Switching (ZVS)** and **Zero-Voltage-Derivative Switching (ZVDS)**

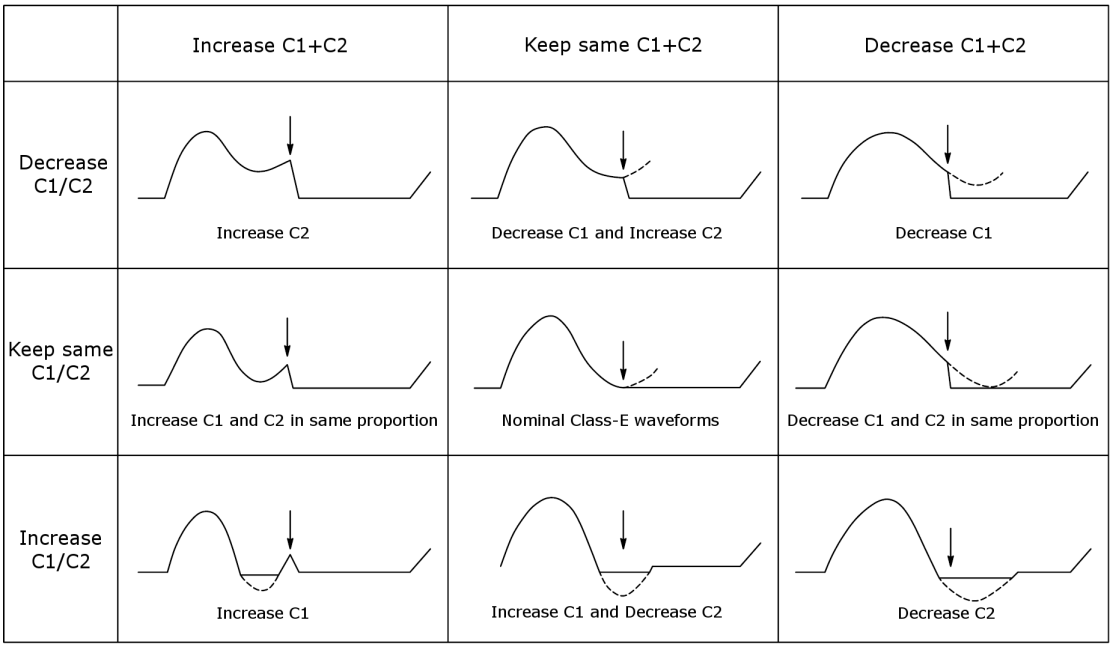


Figure 1-4: C_1 and C_2 adjustment procedure to get the optimal class-E operation. The vertical arrow indicates transistor turn-on.

respectively and when both conditions hold simultaneously at turn-on it is commonly referred to as **optimum class-E operation**. Unfortunately, a trade-off exists between obtaining the desired voltage waveform shaping and reducing the harmonic content delivered to the load R_i (a comprehensive analysis of the class-E inverter with any value of Q_L and duty cycle is provided by Kazimierczuk and Puczko in [11]). A more detailed picture about how to tune the capacitors value to get the desired waveshaping is shown in Figure 1-4.

In order to suitably administrate this trade-off and obtain the desired dc-to-dc conversion avoiding the two above undesirable conditions, an adequate matching network must be introduced when coupling the class-E amplifier with a rectifying stage. It must provide the optimum inverter load value to ensure (a) high efficiency operation and (b) sinusoidal output current $i_o(t)$ of the class-E amplifier to simplify the rectifier stage design procedure. In this way the converter design can be conveniently splitted into two simplified procedures: (a) the rectifier is designed under the hypothesis of sinusoidal input and (b) the inverter is designed with the adapted input resistance of the rectifier as load.

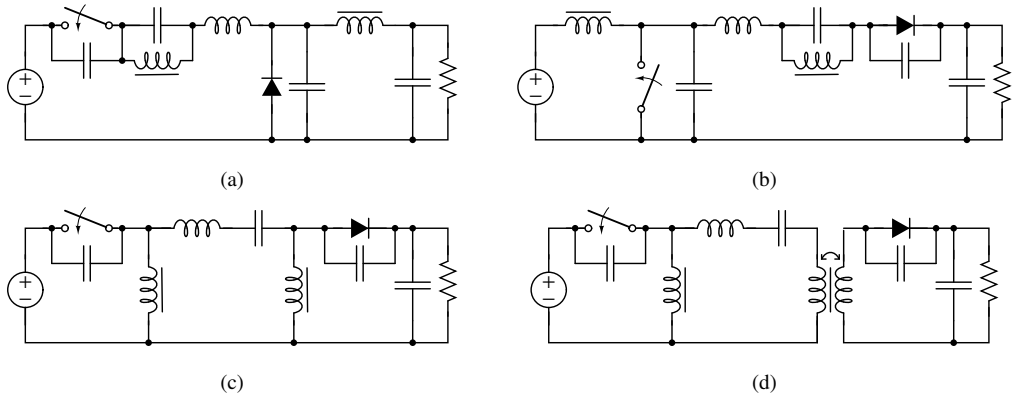


Figure 1-5: Family of class-E^2 dc-dc power converters, taken from [15] (a) buck, (b) boost, (c) buck-boost and (d) isolated buck-boost topologies.

After the first converter topology presented by Gutmann, featuring an harmonically tuned rectifier taken from [12], in the following years many types of matching networks and rectifier topologies have been presented. A class-E converter with full-wave rectifier is proposed in [13], while an isolated solution with inductive impedance inverter is exploited in [14]. Furthermore, in [15] and [16] authors showed that an entire family of isolated and non-isolated converters featuring both class-E inverter and class-E rectifier stages can be drawn. Some of them are reported in Figure 1-5. However, despite a great amount of topologies have been discovered and intensively studied in the past, all of them share the same drawback: the presence of bulky choke inductors and reactive elements in the matching network that need to be employed to make the circuit easier to design dramatically impact the converter size and cost which is obviously in contrast with the main purpose of researching new HF converter architectures.

Among the many recent efforts in class-E converter design improvement, despite most of them removed the large choke inductors, only a very few of them were really aiming at developing a simpler converter topology along with a companion straightforward design procedure. Some of them were targeting the compensation of a variable converter load (the control strategy known as *burst mode*, or simply *on-off control*, is

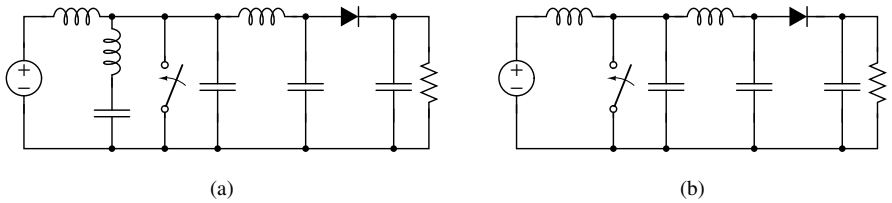


Figure 1-6: Resonant dc-dc converter topologies recently proposed by Perreault *et al.* (a) Φ_2 converter for reducing the transistor peak voltage stress (b) class-E boost converter with minimum component count

applied in [17]), the gating loss reduction by means of new resonant and self-oscillating gate driver topologies [18, 19], and the reduction of peak voltage stress on the switching transistor [20, 21, 22, 23]. In order to achieve this last goal, the so-called Φ_2 topology, depicted in Figure 1-6(a), exploits a second harmonic tank to shape the switch drain voltage into a trapezoidal waveform. One of the few improvements in terms of circuit simplification is found in [24], where the class-E boost converter in Figure 1-6(b) is proposed. Despite featuring a smaller number of elements with respect to previous topologies, the accuracy of the suggested design procedure is still affected by the ancient sinusoidal approximation, resulting in an appreciable difference between the computed solution and SPICE simulation results. As a consequence, additional sweeps across circuit parameters are usually required to identify a suitable design point.

The key idea to make a step forward in resonant converters design is to keep a simple circuit topology featuring a minimal count of reactive components and, at the same time, increase the accuracy of the design procedure removing the hypothesis of sinusoidal coupling. In the next section the mathematical background for resonant converter modeling is introduced, pointing out the clear distinction with respect to the conventional design approach used for hard-switched power supplies.

1.3 Piecewise State-Space Modeling

The behavior of any SMPS consists on the repetitive alternation of different circuit configurations depending on the applied switching pattern. Approximating all devices with their linearized equivalent circuits, each of these circuit states, that will be referred to as *Zones*, can be actually modeled as a linear network consisting of only voltage sources, resistors and energy storage elements (i.e. inductances and capacitances) whose time evolution is regulated by a system of **Ordinary Differential Equations (ODEs)**

$$\mathbf{x}_i'(t) = \mathbf{A}_i\ \mathbf{x}_i(t)\ +\ \mathbf{b}_i \quad i = 1, 2, ... \tag{1.2}$$

where $\mathbf{x}_i(t) \in \mathbb{R}^m$ is the state variables vector, $\mathbf{b}_i \in \mathbb{R}^m$ contains the independent sources of the system, and $\mathbf{A}_i \in \mathbb{R}^{m\times m}$ is the coefficient matrix.

As for all circuital networks, the **state variables of the system** are conveniently chosen to be the currents flowing through inductors and the voltage drops across capacitors. Therefore, the whole converter operation in a switching cycle, $t \in [0, T_s]$, can be piecewisely described collecting the solutions of the ODEs in each time interval Z_i

$$\mathbf{x}(t) \triangleq \mathbf{x}_i(t) \quad t_{i-1} \leq t < t_i \quad i = 1, 2, ...I \tag{1.3}$$

and ensuring the continuity of the state variables at the switching instants t_i (since inductor currents and capacitor voltages cannot change instantaneously)

$$\mathbf{x}_{i+1}(t_i) = \mathbf{x}_i(t_i) \quad i = 1, 2, ...I - 1 \tag{1.4}$$

$$\mathbf{x}_I(t_I) = \mathbf{x}_1(t_0) \tag{1.5}$$

with $t_0 \triangleq 0$ and $t_I \triangleq T_s$. Once Equations (1.4) and (1.5) are satisfied, if the switching pattern is not changed over time (i.e. $\{t_i\} = const$), **steady state operation** is achieved.

Additionally, introducing a suitable variable substitution, it is possible to rewrite

(1.2) into a corresponding set of **homogeneous initial value problems**

$$\begin{cases} \hat{\mathbf{x}}_i'(t-t_i) = \mathbf{A}_i\ \hat{\mathbf{x}}_i(t-t_i) \\ \hat{\mathbf{x}}_i(0) = \hat{\mathbf{x}}_i^0 \end{cases} \tag{1.6}$$

with $\hat{\mathbf{x}}_i(t) = \mathbf{x}_i(t) + {\mathbf{A}_i}^{-1}\ \mathbf{b}_i$ and $i = 1, 2, ...I$. Each of the systems in (1.6) has a unique solution (a more detailed mathematical formulation is provided in the Appendix A), which is given by

$$\hat{\mathbf{x}}_i(t-t_i) = e^{\mathbf{A}_i\,(t-t_i)}\ \hat{\mathbf{x}}_i^0 = \sum_{j=1}^{m} c_{ij}\, e^{\lambda_{ij}\,(t-t_i)}\ \mathbf{v}_{ij} \tag{1.7}$$

where λ_{ij} are the eigenvalues (which can be real or complex) of the matrix $\mathbf{A}_i$, with associated eigenvectors $\mathbf{v}_{ij}$, and $c_{ij} \in \mathbb{C}$ are coefficients that can be computed from the initial conditions $\hat{\mathbf{x}}_i^0$. Hence, once all the eigenpairs $\{\lambda_{ij}, \mathbf{v}_{ij}\}$ are computed for each zone, starting from a guess of the initial conditions $\hat{\mathbf{x}}_1^0$, by means of Equation (1.7) and imposing (1.4) the system waveforms evolution in a single period is easily drawn. Finally, the steady-state solution can be computed repeating this process iteratively with updated initial conditions

$$\mathbf{x}_1^{(k)}(t_0) = \mathbf{x}_I^{(k-1)}(t_I) \tag{1.8}$$

until the stop condition (1.5) is met with the desired accuracy

$$\left\| \mathbf{x}_I^{(k)}(t_I) - \mathbf{x}_1^{(k)}(t_0) \right\| < \varepsilon \tag{1.9}$$

with $\|\cdot\|$ representing the Euclidean distance (i.e. L^2 norm) and ε arbitrarily small number (e.g. 1×10^{-6}).

Interestingly, real and imaginary parts of the eigenvalues λ_{ij} actually represent the natural frequencies of the system, which are determined by the values of the reactive elements in the circuit, and can be collected in a set

$$\mathbb{F} = \{\mathrm{Re}[\lambda_{ij}], \mathrm{Im}[\lambda_{ij}] \mid i = 1, 2, ...I \quad j = 1, 2, ...m\} \tag{1.10}$$

If the supremum of this set is much lower than the converter switching frequency $f_s = 1/T_s$ then all the solutions of the ODEs systems can be well approximated by their first order term, i.e.

$$\sup_{ij} \mathbb{F} \ll 2\pi f_s \implies e^{\mathbf{A}_i t} \approx \mathbf{I} + \mathbf{A}_i t \tag{1.11}$$

This linear approximation is always satisfied for all conventional **hard-switched power converters** and opened the way toward the development of the well-known *state-space averaging method* [25], firstly introduced by R. D. Middlebrook in the middle '70s, which still constitues the leading design strategy for the majority of power conversion systems. However, since the natural frequencies of the circuit are inversely proportional to the passive elements value, when one tries to reduce their impact on converter size and cost the switching frequency must be accordingly increased in such a way that Equation (1.11) still hold. Unfortunately, exploiting the conventional converter architectures, switching loss and gating loss have a detrimental effect on conversion efficiency when switching frequency goes above a few MHz.

To overcome this limitation, **resonant power converters** have been introduced. Since the linear approximation (1.11) doesn't have to be satisfied, a twofold advantage can be achieved:

- with respect to an equivalent hard-switched converter running at the same frequency, smaller passives values are allowed;
- the switching frequency can be further increased thanks to the soft-switching operation opening the way towards further converter miniaturization.

Furthermore, in the new resonant approach, parasitic reactive components (such as MOS output capacitance and transformer leakage inductance) are no more seen as unwanted elements that produce undesirable effects on circuit behavior but they actively participate in normal converter operation and must be included into circuit analysis.

Unfortunately, the analysis of resonant power converters poses several challenges, especially:

- since Equation (1.11) does not hold, the state-space averaging method cannot be applied to find the dc and ac transfer functions;
- the rectifying circuit is no more working in a freewheeling fashion, hence the converter configurations are no more only two but any possible combination of switching devices on/off states must be considered;
- all resonant elements must be accurately designed to met the required soft-switching conditions and only one operating point is the optimal one (e.g. duty cycle cannot be exploited to regulate the output power);
- soft-switching (i.e. state variables continuity) must be ensured for each transition between two zones and an average description across the whole switching period is not sufficient for design puroposes.

As previously described, the commonly adopted analysis and design approach, coming from the conventional RF techniques, is strongly affected by the sinusoidal approximation. In fact, the mismatch between the analytically computed circuit behavior and the actual one, where a non-negligible amount of power out of the first harmonic is transferred to the secondary side, leads to the necessity of subsequent time-domain circuital simulations to refine the initial approximated design point. Moreover, it may become difficult, even for an experienced designer, to understand when an optimal design solution is reached.

Hence, in order to make step forward in **HF/VHF dc-dc converter design**, a completely new approach is summarized in the following **5 steps**:

1. **Remove** any harmonic filtering or matching network and, in general, any additional passive element which is not strictly necessary for resonant operation, thus leading to maximum size and cost reduction;
2. **Follow** the aforementioned state-space analysis method writing the differential equations regualting the converter evolution for all zones;
3. **Identify** a suitable normalization for the converter equations to find out how many the degrees of freedom of the system really are;

4. **Solve** the resulting ODE systems with reduced dimensionality recurring to a numerical optimization tool in order to ensure the desired soft-switching behavior and output power level at steady-state;

5. **Explore** the whole design space and provide additional design curves to help the designer finding a solution which is close to the optimal working point for any specific design case.

1.4 Thesis Organization

The remaining of the thesis is organized in three more chapters.
In Chapter 2 a general **topology** for resonant converters featuring a minimum number of reactive elements is introduced. Subsequently, an entire family of class-E dc-dc converters is derived, showing that, with simple circuital considerations, they can be analyzed exploiting the same set of differential equations.
Chapter 3 is entirely dedicated to the development of a unified **analysis and design** procedure that can be straightforwardly applied to all the class-E converters considered. What will be shown is that by means of a proper normalization the design space can be reduced in such a way that it can be fully explored with minimal computational effort. As a consequence, a set of design curves is introduced, considerably simplifying the power stage design process. Furthermore, the basic circuit model is improved introducing the main device non-idealities such as semiconductor on-state resistance and losses in the reactive elements. This allows to get a first order estimation of the converter efficiency very early during the design process. Results are validated through both numerical examples and PCB prototype measurements showing an almost perfect match with the semi-analytically computed waveforms.
Additionally, in order to further emphasize the proposed modelling technique, in Chapter 4 an **isolated class-E power/data link** is designed and implemented. Finally, conclusions are drawn and future research directions are pointed out.

Chapter 2

Class-E DC-DC Converter Topologies

The resonant converter topologies presented in this thesis are composed of two switching networks connected by means of a LC resonant circuit, as sketched in Figure 2-1. The resonant circuit is made up of two LC loops coupled exploiting a single inductor solution or a transformer providing additional galvanic isolation.

Considering the non-isolated resonant network in Figure 2-1(a), the minimum number of reactive elements needed to enable the resonant operation is actually four: two capacitors and two inductors. In fact, in order to decouple the input and the output, only one between inductors L_1 and L_2 is strictly required. Similarly, for the isolated topology in Figure 2-1(b), if the coupling coefficient of the transformer is nearly 100%, like in the majority of commercially available devices, an extra inductor is needed either on the primary or on the secondary side. On the contrary, when a low-coupling factor transformer is considered, like in some integrated solutions, inductors L_1 and L_2 can be seen as the leakage part of primary and secondary coil inductance respectively and no additional inductors are needed.
Resonant capacitors C_1 and C_2 can be seen as the sum of the parasitic output capacitance of input and output switch networks with additonal capacitors that can be conveniently introduced in the design to get the desired capacitance value and opportunely mask the non-linear effects on the circuit behavior.

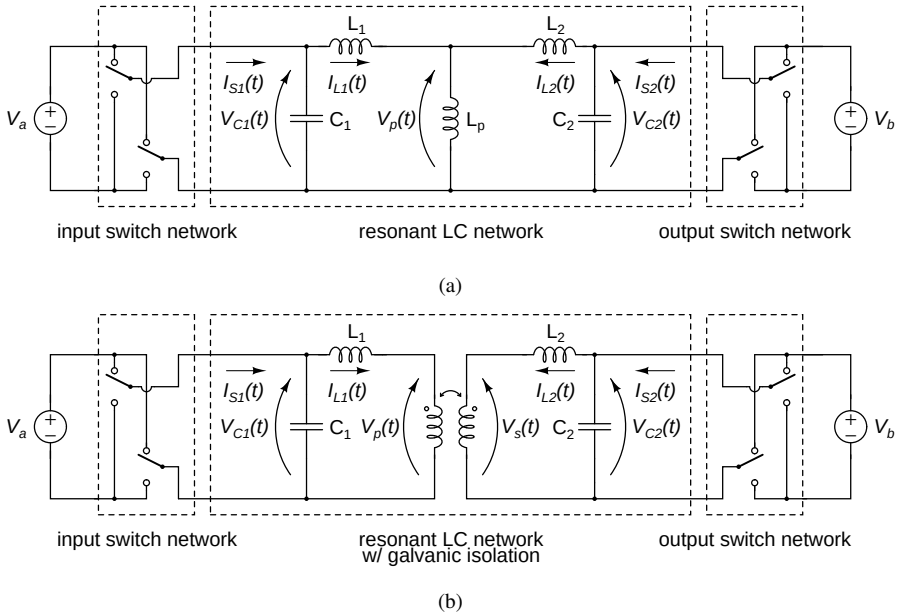


Figure 2-1: Generalized resonant converter topologies (a): non-isolated (b): isolated.

By means of properly designing all these resonant elements, it is possible to achieve soft-switching operation for each of the proposed circuits, enabling efficient power conversion even at very high switching frequencies. In fact, when soft-switching conditions are satisfied, the switching losses become negligible and the theoretical efficiency achievable with ideal lossless devices is 100%.

Despite being a promising solution to increase next generation converter's power density, all resonant topologies are extremely challenging to design and there is still no unified methodology which is simple and fast enough to become a standard one. In order to move a step forward in Resonant Switched-Mode Power Supplies (RSMPS) analysis and design, several isolated and non-isolated resonant topologies will be introduced, with particular emphasis on the fact that all these converters can be actually described as dynamical systems regulated by the same set of ODEs. This represents a great breakthrough with respect to the state-of-the-art since it opens the way towards the development of a **unified analysis, design and optimization approach**.

2.1 Resonant Network Equations

Considering the isolated topology of Figure 2-1(b), the equations regulating the resonant network are written as the Kirchhoff Voltage Laws (KVLs) of the two loops

$$\begin{cases} V_{C_1}(t) = L_1 \dfrac{dI_{L_1}(t)}{dt} + V_p(t) \\ V_{C_2}(t) = L_2 \dfrac{dI_{L_2}(t)}{dt} + V_s(t) \end{cases} \tag{2.1}$$

Transformer voltages can be expressed in matricial form as

$$\begin{pmatrix} V_p(t) \\ V_s(t) \end{pmatrix} = \begin{pmatrix} L_p & \pm M \\ \pm M & L_s \end{pmatrix} \frac{d}{dt} \begin{pmatrix} I_{L_1}(t) \\ I_{L_2}(t) \end{pmatrix} = \begin{pmatrix} L_p & \pm NkL_p \\ \pm NkL_p & N^2 L_p \end{pmatrix} \frac{d}{dt} \begin{pmatrix} I_{L_1}(t) \\ I_{L_2}(t) \end{pmatrix} \tag{2.2}$$

where L_p, L_s and $M = k\sqrt{L_p L_s}$ represent the primary, secondary and mutual inductance (k is known as *coupling coefficient*), and $N = N_s/N_p$ is the secondary-to-primary turn ratio. Merging Equations (2.1) and (2.2) one obtains the following ODE system

$$\begin{cases} V_{C_1}(t) = (L_1 + L_p) \dfrac{dI_{L_1}(t)}{dt} \pm M \dfrac{dI_{L_2}(t)}{dt} \\ V_{C_2}(t) = \pm M \dfrac{dI_{L_1}(t)}{dt} + (L_2 + L_s) \dfrac{dI_{L_2}(t)}{dt} \end{cases} \tag{2.3}$$

The same equations still hold for the non-isolated LC network in Figure 2-1(a) once considered $N = 1$ and $k = 1$ (i.e. $L_p = L_s = M$). The change in sign is still useful for both isolated and non-isolated converters to account for either in-phase or out-of-phase coupling, as it will be explained in the next sections.

Depending on the connection of the switches inside the input and output networks, in each zone they can exhibit:

- **Low-impedance (Lo-Z)**: the voltage across the resonant capacitor is forced to a constant value $V_{Ci}(t) = V_{DC}$, hence no currents flows through it

$$I_{C_i}(t) = C_i \frac{dV_{C_i}(t)}{dt} = 0 \quad \Longrightarrow \quad I_{L_i}(t) = I_{S_i}(t) \qquad i = 1, 2 \tag{2.4}$$

or

- **High-impedance (Hi-Z)**: there is no active power coming out of the voltage source (or delivered to the load), but all the current resonates inside the LC tank

$$I_{S_i}(t) = 0 \quad \Longrightarrow \quad I_{L_i}(t) = -I_{C_i}(t) = -C_i \frac{dV_{C_i}(t)}{dt} \qquad i = 1, 2 \tag{2.5}$$

During the normal operation of conventional hard-switched converters only Lo-Z configurations are possible, where the current flowing through inductors is carried alternatively by the active devices. Conversely, in a resonant converter, depending on the reciprocal state of the input and output switch networks the whole circuit can actually present **three different configurations**:

- **Linear (LIN)**: for Lo-Z input network and Lo-Z output network there is direct power transfer between the input and the output and the circuit is described by a second order differential equation system in the state variables $I_{L_1}(t)$, $I_{L_2}(t)$

$$\begin{cases} (L_1 + L_p) \dfrac{dI_{L_1}(t)}{dt} + nkL_p \dfrac{dI_{L_2}(t)}{dt} \pm V_a = 0 \\ nkL_p \dfrac{dI_{L_1}(t)}{dt} + (L_2 + L_s) \dfrac{dI_{L_2}(t)}{dt} \pm V_b = 0 \end{cases} \tag{2.6}$$

- **Half-Resonant (HR)**: for Hi-Z input (output) network and Lo-Z output (input) network the circuit is described by a third order differential equation system in the state variables $I_{L_1}(t)$, $I_{L_2}(t)$ and $V_{C_1}(t)$ ($V_{C_2}(t)$). With Low-Z input network the energy coming from the voltage source is momentarily stored in the resonant elements

$$\begin{cases} (L_1 + L_p) \dfrac{dI_{L_1}(t)}{dt} + nkL_p \dfrac{dI_{L_2}(t)}{dt} \pm V_a = 0 \\ nkL_p \dfrac{dI_{L_1}(t)}{dt} + (L_2 + L_s) \dfrac{dI_{L_2}(t)}{dt} - V_{C_2}(t) = 0 \\ C_2 \dfrac{dV_{C_2}(t)}{dt} + I_{L_2}(t) = 0 \end{cases} \tag{2.7}$$

while, when the output network is Low-Z, the power is transferred to the load

$$\begin{cases} (L_1 + L_p)\,\dfrac{dI_{L_1}(t)}{dt} + nkL_p\,\dfrac{dI_{L_2}(t)}{dt} - V_{C_1}(t) = 0 \\ nkL_p\,\dfrac{dI_{L_1}(t)}{dt} + (L_2 + L_s)\,\dfrac{dI_{L_2}(t)}{dt} \pm V_b = 0 \\ C_1\dfrac{dV_{C_1}(t)}{dt} + I_{L_1}(t) = 0 \end{cases} \tag{2.8}$$

- **Fully-Resonant (FR)**: for Hi-Z input network and Hi-Z output network the resonant network is completely disconnected from source and load and both primary and secondary side LC tanks are carrying reactive power subjected to a fourth order differential equation system in the four state variables $I_{L_1}(t)$, $I_{L_2}(t)$, $V_{C_1}(t)$ and $V_{C_2}(t)$

$$\begin{cases} (L_1 + L_p)\,\dfrac{dI_{L_1}(t)}{dt} + nkL_p\,\dfrac{dI_{L_2}(t)}{dt} - V_{C_1}(t) = 0 \\ nkL_p\,\dfrac{dI_{L_1}(t)}{dt} + (L_2 + L_s)\,\dfrac{dI_{L_2}(t)}{dt} - V_{C_2}(t) = 0 \\ C_1\dfrac{dV_{C_1}(t)}{dt} + I_{L_1}(t) = 0 \\ C_2\dfrac{dV_{C_2}(t)}{dt} + I_{L_2}(t) = 0 \end{cases} \tag{2.9}$$

  with $n = \pm N$ (± 1 for the non-isolated case) depending on the coupling phase between inverter and rectifier sections.

The alternating of these different operating modes allows the energy to be stored and transferred in a conservative way. Roughly speaking, if the values of L_1, L_2, L_p, L_s, C_1 and C_2 are properly designed, there is no waste of charge during transitions from one zone to another and switching losses can be dramatically reduced. The solution of the aforementioned ODE systems will be presented in the next chapter along with a novel dimensionless design methodology. In the remaining of this chapter several isolated and non-isolated resonant class-E converter topologies derived from the generalized circuits in Figure 2-1 will be introduced and it will be shown that the behavior all of them can be fully described exploiting the Equations (2.6)-(2.9).

2.2 Non-Isolated Class-E Converters

Starting from the resonant circuit in Figure 2-1(a), with two simple one-switch networks it will be shown how to obtain a resonant class-E buck-boost converter with either positive or negative output voltage referred to the common ground. It will be also shown how this circuital scheme can be turned either into an equivalent buck (step-down) or boost (step-up) resonant class-E converter. Interestingly, despite the fact that each of these non-isolated topologies is obtained rearranging the elements in the two loops in different ways, all of them are regulated by the same set of equations.

2.2.1 Buck-Boost Topology

The simpler implementation for input and output switch networks is constituted by a single switch connected in series with the input/output voltage, as depicted in Figure 2-2(a-b). From a topological point of view, if the switch S2 of Figure 2-2(b) is implemented with a rectifying diode, it is actually the same as the conventional hard-switched buck-boost converter depicted in Figure 2-2(c) with additional resonant elements around the pairing inductance L_p. The common drawback of all these circuits is that, once switches are implemented with MOS devices, the source terminal cannot be connected to the ground reference, so either a P-MOS device, or a N-MOS with a bootstrap circuit is required.

These resonant topologies are referred to as **non-inverting** and **inverting class-E buck-boost converter** respectively, since, differently with respect to the standard hard-switching buck-boost, they are capable to produce either a positive or negative output voltage depending on the phase shift between the primary and the secondary switch drives. If passive rectification is employed, the direction in which the diode is connected determines the polarity of the output: positive if the cathode is connected to the output node, negative if the anode is connected to the output node. It is worth noting that this possibility cannot be exploited in the hard-swithing buck-boost because the diode is working in a freewheeling fashion, turning itself on when S1 is off to sustain the inductor current, thus allowing only a negative output voltage.

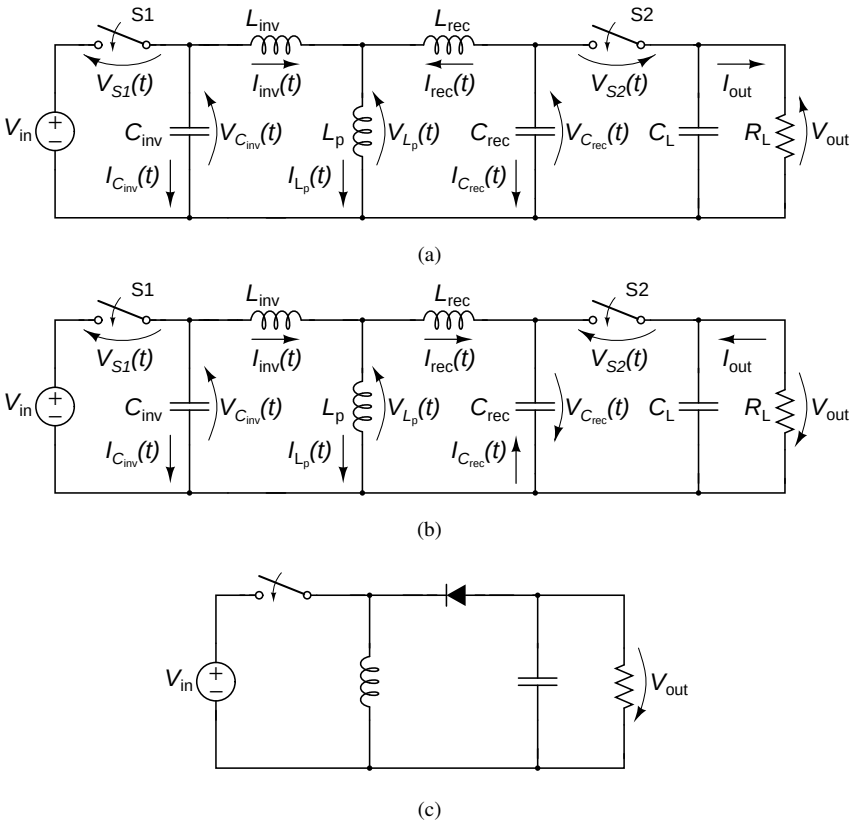


Figure 2-2: Buck-boost converter topologies (a) Non-inverting class-E buck-boost converter. (b) Inverting class-E buck-boost converter. (c) Conventional hard-switched buck-boost converter.

Furthermore both inverting and non-inverting configurations can behave as a step-up ($V_{out} > V_{in}$) or a step-down ($V_{out} < V_{in}$) converter depending on the values of resonant elements in the circuit.

Being $V_{C_{inv}}(t) = V_{in} - V_{S1}(t)$ and $V_{C_{rec}}(t) = V_{out} - V_{S2}(t)$, the loop KVL equations can be written as

$$\begin{cases} (L_{inv} + L_p)\, \dfrac{dI_{inv}(t)}{dt} \pm L_p \dfrac{dI_{rec}(t)}{dt} + V_{S1}(t) - V_{in} = 0 \\ \pm L_p \dfrac{dI_{inv}(t)}{dt} + (L_{rec} + L_p)\, \dfrac{dI_{rec}(t)}{dt} + V_{S2}(t) - V_{out} = 0 \end{cases} \tag{2.10}$$

which are exactly the same as Equations (2.3) with $k = 1$, $N = 1$ (i.e. $M = L_p$), $V_a = V_{in}$ and $V_b = V_{out}$.

Despite the fact that C_{inv} and C_{rec} are not placed in parallel with S1 and S2 respectively, they play the role of masking device parasitics. When the switch S1 is off the inverter side current flowing through the capacitor C_{inv} is $I_{C_{inv}}(t) = -I_{inv}(t)$ and, since $V_{C_{inv}}(t) = V_{in} - V_{S1}(t)$, one gets

$$I_{inv}(t) = -I_{C_{inv}}(t) = -C_{inv} \frac{d}{dt} \left(V_{in} - V_{S1}(t) \right) = C_{inv} \frac{dV_{S1}(t)}{dt} \tag{2.11}$$

On the contrary, when S1 is on $V_{S1}(t) = 0$, $\frac{dV_{C_{inv}}(t)}{dt} = 0$ and all the inverter loop current is carried by the active device. Similar considerations hold also for switch S2 and parallel capacitor C_{rec}: if S2 is on

$$I_{rec}(t) = -I_{C_{rec}}(t) = -C_{rec} \frac{d}{dt} \left(V_{out} - V_{S2}(t) \right) = C_{rec} \frac{dV_{S2}(t)}{dt} \tag{2.12}$$

while in the other case $V_{S2}(t) = 0$, $\frac{dV_{C_{rec}}(t)}{dt} = 0$ and secondary side current flows all through S2. Hence, combining Equations (2.10)-(2.12), it is possible to get the converter description for all zones.

The converter output power, since the average current through the capacitor C_{rec} is zero at steady-state, can be computed once the rectifier current $I_{rec}(t)$ is known

$$P_{out} = V_{out} I_{out} = V_{out} \left(-\frac{1}{T_s} \int_0^{T_s} I_{rec}(t)\, dt \right) = -\, V_{out}\, \langle I_{rec}(t) \rangle \tag{2.13}$$

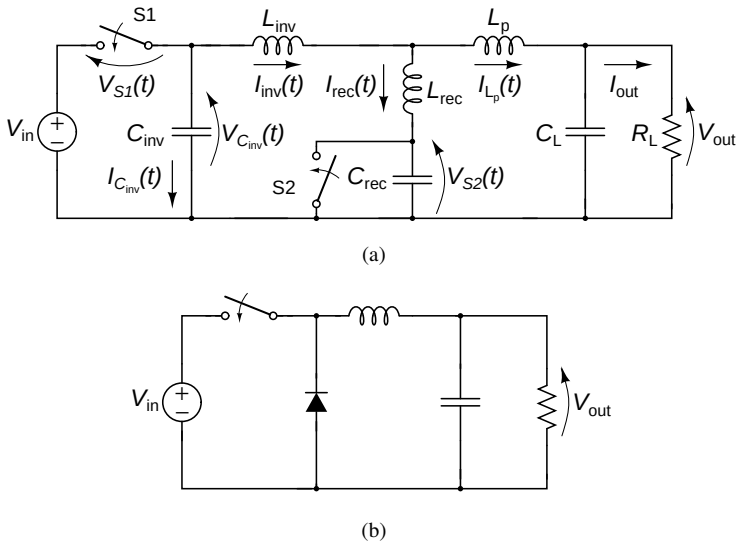


Figure 2-3: Non-isolated buck topologies:
(a) Class-E buck converter. (b) Conventional hard-switched buck converter.

where the brackets $\langle \cdot \rangle$ represent the average value computed over a period T_s after steady-state is reached. A class-E buck-boost topology without primary inductor L_{inv}, with low side switching devices and separated ground references was firstly presented in [**26**] and implemented with high quality factor components in [**27**] in order to validate the modeling equations and a new design method which will be thoroughly explained in the next chapter.

2.2.2 Buck Topology

The circuit shown in Figure 2-3(a) is a **class-E buck converter** since, with respect to the common ground level, the potential V_{in} at the input node is always higher than the potential V_{out} at the output.

The resonant buck converter is obtained from the conventional hard-switched buck architecture in Figure 2-3(b) once added the two LC resonant tanks L_{inv}-C_{inv} and L_{rec}-C_{rec}. Similar resonant or quasi-resonant topologies appeared many times in the recent literature and what is most interesting is that almost all of them can

be obtained removing one or more passive elements from the schematic of Figure 2-3(a). Just to cite some of them, authors in [28] proposed a ZVS buck converter with non-resonant rectifier (i.e., without C_{rec}) and where the L_{rec} is not used. In [29] and [30] only the version with L_{inv} was taken into account while a more comprehensive overview of different ZVS converter topologies was presented in [31], including that of Figure 2-3(a) in the two alternatives where only one inductor among L_{inv} and L_{rec} is present.

The analysis of the circuit starts considering the KVL at the outer loop

$$V_{in} = V_{S1}(t) + L_{inv}\,\frac{dI_{inv}(t)}{dt} + L_p\,\frac{dI_{L_p}(t)}{dt} + V_{out} \tag{2.14}$$

and rectifier loop

$$V_{out} = V_{S2}(t) + L_{rec}\frac{dI_{rec}(t)}{dt} - L_p\,\frac{dI_{L_p}(t)}{dt} \tag{2.15}$$

Being also $I_{L_p}(t) = I_{inv}(t) - I_{rec}(t)$, the two equations above become

$$\begin{cases} (L_{inv} + L_p)\,\dfrac{dI_{inv}(t)}{dt} - L_p\,\dfrac{dI_{rec}(t)}{dt} + V_{S1}(t) - (V_{in} - V_{out}) = 0 \\ -L_p\,\dfrac{dI_{inv}(t)}{dt} + (L_{rec} + L_p)\,\dfrac{dI_{rec}(t)}{dt} + V_{S2}(t) - V_{out} = 0 \end{cases} \tag{2.16}$$

which correspond to the equations of an equivalent resonant inverting buck-boost converter having input voltage equal to $V_{in} - V_{out}$ and output voltage V_{out}. Capacitor C_{inv} still masks S1 parasitic output capacitance and equations for both resonant capacitors remain exactly as computed in (2.11) and (2.12) for the isolated buck-boost topologies.

Conversely, the output power is now computed from the current $I_{L_p}(t)$ as

$$P_{out} = V_{out}I_{out} = V_{out}\left(\frac{1}{T_s}\int_0^{T_s} I_{L_p}(t)\,dt\right) = V_{out}\left\langle I_{L_p}(t)\right\rangle \tag{2.17}$$

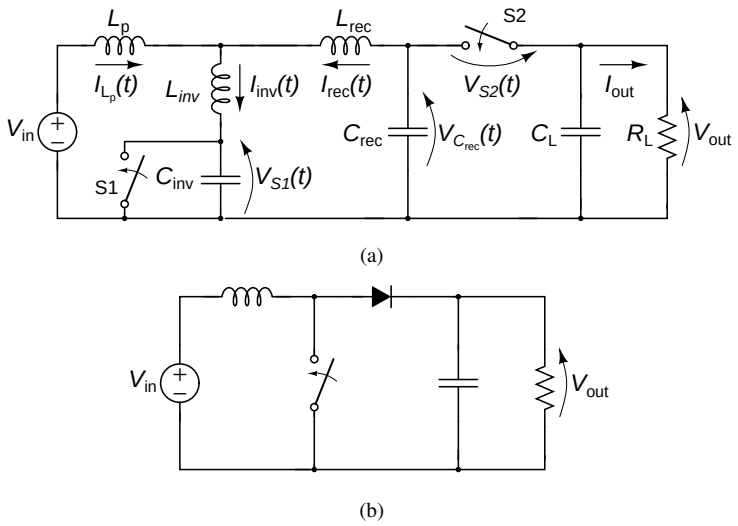


Figure 2-4: Non-isolated boost topologies:
(a) Class-E boost converter. (b) Conventional hard-switched boost converter.

2.2.3 Boost Topology

The topology in Figure 2-4(a) represents a **class-E boost converter** since, with respect to the common ground level, the potential V_{in} at the input node is always lower than the potential V_{out} at the output.

This topology recalls the standard hard-switched boost converter when the resonant network made of L_{inv}, L_{rec}, C_{inv} and C_{rec} is added. In the two alternative implementations with L_{inv} or L_{rec} only, it is actually one of the most commonly used in the literature due to its simplicity (for example, there is no need for a bootstrap circuit for driving S1). In their overview of different ZVS converter topologies in [31], authors included both implementations. The dc-dc converter in [32] is a boost circuit presenting a small variation with respect to that of Figure 2-4(a), where only L_{rec} is present while in [33] a ZVS inverter side is combined with a non-resonant rectifier (i.e., without resonant elements L_{rec} and C_{rec}). In [19] the Φ_2 converter was introduced. This converter is basically the same of the resonant boost converter presented here with $L_{inv} = 0$ and additional LC resonant circuit whose aim is to reduce the peak value of the voltage across the main switch. The recently proposed converter in

[24] by Burkhart *et al.* is a fully resonant 75 MHz 12 V-30 V boost converter featuring ZVS and ZVDS whose topology is substantially the same with no L_{inv}.

This time the converter analysis is carried out considering inverter and outer loop equations which are

$$V_{in} = L_p \frac{dI_{L_p}(t)}{dt} + L_{inv} \frac{dI_{inv}(t)}{dt} + V_{S1}(t) \tag{2.18}$$

and

$$V_{out} = V_{S2}(t) + L_{rec} \frac{dI_{rec}(t)}{dt} - L_p \frac{dI_{L_p}(t)}{dt} + V_{in} \tag{2.19}$$

respectively. As for the resonant buck topology, $I_{L_p}(t) = I_{inv}(t) - I_{rec}(t)$ and the two equations above are conveniently rearranged in the following system of differential equations

$$\begin{cases} (L_{inv} + L_p) \dfrac{dI_{inv}(t)}{dt} - L_p \dfrac{dI_{rec}(t)}{dt} + V_{S1}(t) - V_{in} = 0 \\ -L_p \dfrac{dI_{inv}(t)}{dt} + (L_{rec} + L_p) \dfrac{dI_{rec}(t)}{dt} + V_{S2}(t) - (V_{out} - V_{in}) = 0 \end{cases} \tag{2.20}$$

which can be seen as the equations regulating the behavior of a resonant inverting buck-boost converter with input voltage V_{in} and output voltage equal to $V_{out} - V_{in}$. Furthermore, resonant capacitor C_{rec}, despite being not in parallel with the switch S2, is capable to mask its parasitic capacitance as explained in for the buck-boost topology and Equations (2.11)-(2.12) still hold. Furthermore, since for the resonant boost converter $\langle I_{out} \rangle = \langle -I_{rec}(t) \rangle$, the expression for output power is the same of (2.13).

2.3 Isolated Class-E Converters

Galvanic isolation is useful and sometimes mandatory in many applications, such as isolated gate drivers, industrial process monitoring and noise sensitive measurements. In such a case, the pairing inductor L_p is replaced with a pair of coupled inductors

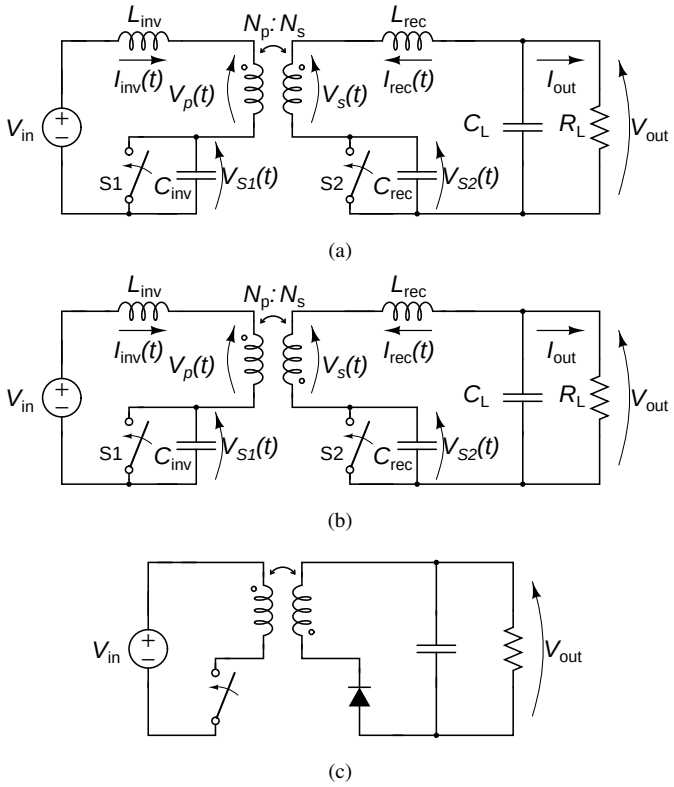


Figure 2-5: Isolated converter topologies (a): Class-E with in-phase coupling. (b): Class-E with 180° out-of-phase coupling. (c): Conventional hard-switched flyback converter.

L_p and L_s with turn ratio $N = N_s/N_p$ and coupling coefficient k. Starting from the isolated resonant network in Figure 2-1(b), if a single switch solution is considered a **class-E isolated buck-boost converter** can be obtained, while exploiting multi-switch input and output networks one can design either half-bridge or full-bridge resonant converters.

The proposed isolated class-E resonant converters are depicted in Figure 2-5(a-b). The only difference between Figure 2-5(a) and Figure 2-5(b) is the connection of the secondary winding of the transformer which can be either in-phase or 180° out-of-phase respectively. The former has been presented in [**34**] along with a ODE-based analysis and design methodology that will be discussed in the next chapter. The latter, when the switch S2 is replaced with a rectifying diode, is topologically the

same of a conventional flyback converter with additional passive elements L_{inv}, L_{rec}, C_{inv} and C_{rec} to enable resonant operation.

A clear advantage of the isolated alternatives, with respect to their non-isolated counterparts in Figure 2-2(a-b), is that the switching devices can be moved to the low side of the circuit, allowing them to be connected to ground. Despite the resonant capacitors have been drawn in parallel to switching devices to underline their role of masking semiconductor parasitics, the set of differential equations remains exactly the same firstly introduced in (2.3)

$$\begin{cases} \left(L_{inv} + L_p\right) \dfrac{dI_{inv}(t)}{dt} + nkL_p \dfrac{dI_{rec}(t)}{dt} + V_{S1}(t) - V_{in} = 0 \\ nkL_p \dfrac{dI_{inv}(t)}{dt} + \left(L_{rec} + N^2 L_p\right) \dfrac{dI_{rec}(t)}{dt} + V_{S2}(t) - V_{out} = 0 \end{cases} \tag{2.21}$$

with $\pm M = \pm NkL_p = nkL_p$ and $L_s = N^2 L_p$.

Similarly to the non-isolated buck-boost resonant converters, when the primary switch S1 is on the voltage $V_{S1}(t)$ is constrained to zero and all the primary loop current is flowing through the device while, when it is turned off, $I_{inv}(t)$ starts flowing through the parallel resonant capacitor C_{inv}, hence

$$\begin{cases} V_{S1}(t) = 0, & \text{if S1 is on} \\ I_{inv}(t) = C_{inv} \dfrac{dV_{S1}(t)}{dt}, & \text{if S1 is off} \end{cases} \tag{2.22}$$

Similar equations hold for the secondary side loop, where the capacitor C_{rec} carries all the loop current $I_{rec}(t)$ when the secondary switch is off, so

$$\begin{cases} V_{S2}(t) = 0, & \text{if S2 is on} \\ I_{rec}(t) = C_{rec} \dfrac{dV_{S2}(t)}{dt}, & \text{if S2 is off} \end{cases} \tag{2.23}$$

Finally, the computation of the output power, as for the respective buck-boost topologies, is still related to the average value of the secondary side current $I_{rec}(t)$ by the formula in (2.13).

2.4 Design Example

In the following chapters the attention will be focused on the class-E converters, maily due to their switching network simplicity, but being aware that similar consideration would be possible also for many other resonant topologies. In order to sum up the relation between the equation parameters and the class-E resonant topology considered, the following generalized loop equations and Table 2.1 are given:

$$\begin{cases} (L_{inv} + L_p)\,\dfrac{dI_{inv}(t)}{dt} + nkL_p\,\dfrac{dI_{rec}(t)}{dt} + V_{S1}(t) - V_a = 0 \\ nkL_p\,\dfrac{dI_{inv}(t)}{dt} + \left(L_{rec} + n^2 L_p\right)\,\dfrac{dI_{rec}(t)}{dt} + V_{S2}(t) - V_b = 0 \end{cases} \tag{2.24}$$

For isolated converters, the loop voltages V_a and V_b represent input and output voltage respectively while n and k can be computed knowing the ratio between primary and secondary winding turns along with their coupling coefficient. If secondary is reverse coupled the parameter n needs to be changed in sign. Non-inverting and inverting non-isolated buck-boost converters are described by the same equations of their isolated counterparts when considering ideal coupling between primary and secondary coils (no leakage inductance, i.e. $k = 1$) and unitary turn ratio ($N_s/N_p = 1$). Buck and boost topologies equations have $n = -1$ and $k = 1$ like the inverting buck-boost but primary loop voltage V_a has to be changed into $V_{in} - V_{out}$ in the former and the secondary loop voltage V_b has to be changed into $V_{out} - V_{in}$ in the latter. In other words, if with given reactive elements L_p, L_{inv}, L_{rec}, C_{inv} and C_{rec} one can design a class-E inverting buck-boost converter having $V_{in} = V_a$ and $V_{out} = V_b$, then it is possible, with the same valued resonant elements, to design either a resonant boost converter with $V_{in} = V_a$ and $V_{out} = V_a + V_b$ or a resonant buck converter having $V_{in} = V_a + V_b$ and $V_{out} = V_b$.

As a proof of concept, a simple example is given starting from the converter depicted in Figure 2-6(a). It is a class-E inverting buck-boost converter running at 5 MHz with $V_{in} = V_a = 3\,\mathrm{V}$ and $V_{out} = V_b = 9\,\mathrm{V}$. Resonant elements $L_p = 1\,\mu\mathrm{H}$, $L_{rec} = 1\,\mu\mathrm{H}$, $C_{inv} = 1.4\,\mathrm{nH}$, $C_{rec} = 915\,\mathrm{pF}$ (L_{inv} is removed) have been properly

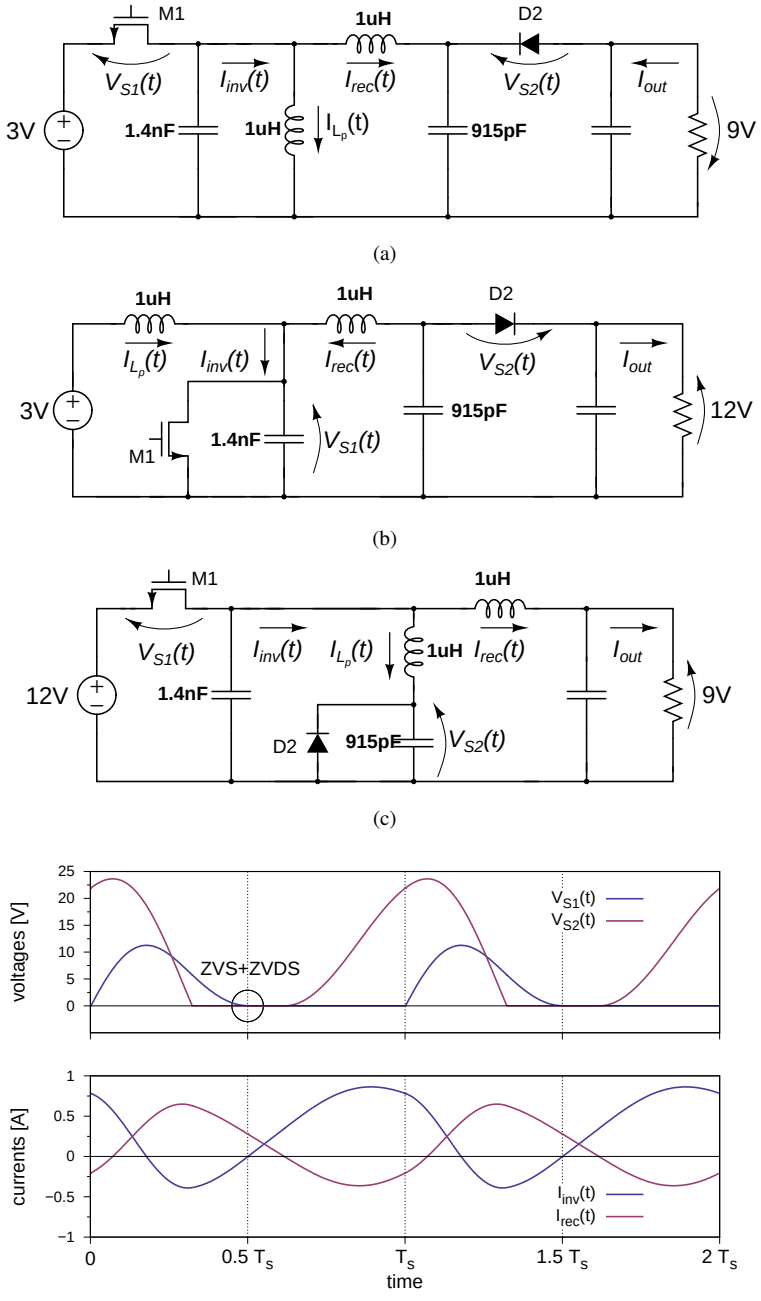


Figure 2-6: Class-E resonant converters design example:
(a) inverting buck-boost, (b) boost and (c) buck topologies. (d) Common voltage and current waveforms for all circuits.

Table 2.1: ODE parameters vs resonant topology

$_{topology}\backslash^{parameters}$	V_a	V_b	n	k
Non-Isolated Class-E				
buck-boost	V_{in}	V_{out}	1	1
inv. buck-boost	V_{in}	V_{out}	-1	1
buck	$V_{in} - V_{out}$	V_{out}	-1	1
boost	V_{in}	$V_{out} - V_{in}$	-1	1
Isolated Class-E				
in-phase	V_{in}	V_{out}	N_s/N_p	$M/(NL_p)$
180° out-of-phase	V_{in}	V_{out}	$-N_s/N_p$	$M/(NL_p)$

designed to achieve ZVS/ZVDS conditions and passive rectification is implemented with the diode D2. The nominal output power is

$$P_{out}^{BB} \approx 900\,\mathrm{mW}$$

Keeping the same valued resonant elements it is possible to design either a 3 V-to-12 V class-E boost converter, as in Figure 2-6(b), or a 12 V-to-9 V class-E buck converter, shown in Figure 2-6(c), working with the same switching frequency. Despite having different topologies and different input and output voltages, all these converters are actually regulated by the same set of differential equations and hence also all the waveforms in the circuit, such as the voltages across the MOS and the rectifying diode and the currents $I_{inv}(t)$ and $I_{rec}(t)$, drawn in Figure 2-6(d), are exactly the same. On the contrary, the output power is not the same. In fact, despite all three converters share the same inverter and rectifier currents, the output current of the inverting buck-boost

$$I_{out}^{BB} = -\langle I_{rec}(t)\rangle = P_{out}^{BB}/V_{out}^{BB} \approx 100\,\mathrm{mA}$$

is the same of the boost converter but having the latter different output voltage the

resulting power is

$$P_{out}^{BOOST} = -V_{out}^{BOOST} \langle I_{rec}(t) \rangle = (V_a + V_b)\, I_{out}^{BB} = \left(\frac{V_a}{V_b} + 1 \right) P_{out}^{BB} \approx 1.2\,\mathrm{W} \quad (2.25)$$

For the buck converter the output power is computed from (2.17), knowing that $I_{L_p}(t) = I_{inv}(t) - I_{rec}(t)$, so

$$P_{out}^{BUCK} = V_{out}^{BUCK} \langle I_{inv}(t) - I_{rec}(t) \rangle = V_b \left(\langle I_{inv}(t) \rangle + I_{out}^{BB} \right)$$

and also that, under the hypothesis of negligible losses in the circuit, $P_{in}^{BB} = V_a \langle I_{inv}(t) \rangle \approx P_{out}^{BB}$

$$P_{out}^{BUCK} \approx V_b \left(\frac{P_{out}^{BB}}{V_a} + I_{out}^{BB} \right) = \left(\frac{V_b}{V_a} + 1 \right) P_{out}^{BB} \approx 3.6\,\mathrm{W} \quad (2.26)$$

Concluding, in this chapter, a resonant network with minimum component count has been presented with the aim of introducing an entire family of dc-dc power converters suitable for HF operation. Among them a subset of single-switch converters is represented by the class-E family, composed of both isolated and non-isolated topologies. Interestingly, the differential equations regulating the circuit behavior are substantially the same for all class-E members once some simple consideration, reported in Table 2.1 and Equations (2.25)-(2.26), are taken into account. In the following, a unified and comprehensive dimensionless ODE-based analysis and design methodology for this class of RSMPS will be presented. The proposed approach represents a step further in resonant converter design since it reduces the design effort but also improves the accuracy of the achieved solution, giving a solid background for any additional optimization purpose.

Chapter 3

Unified Class-E Analysis and Design Methodology

Despite being a promising solution for increasing the compactness of next generation power converters, all resonant topologies have been always limited by the fact that there is no consolidated design procedure which is simple, fast and accurate enough to become a standard one. As already discussed in Chapter 1, the commonly adopted approach is to split the converter design into two simplified procedures relying on the hypothesis to have a "sinusoidal coupling" between inverter and rectifier sections. Unfortunately, this approach has **two main disadvantages**: (a) the overall **converter size** is impacted by the need for a matching network adapting the input impedance of the rectifier to enable class-E inverter soft-switching operation, (b) the **design accuracy** is severely compromised by the sinusoidal approximation and additional time-consuming circuital simulations are needed to refine the inital solution. To overcome the impasse, the proposed approach is to forget about the common RF design concepts and develop a completely new methodology based on the following guidelines: (a) simplify the converter architecture as much as possible, leveraging the resonant topologies introduced in the last chapter; (b) take advantage of the simplified topology to develop a new, unified analysis and design procedure from scratch.

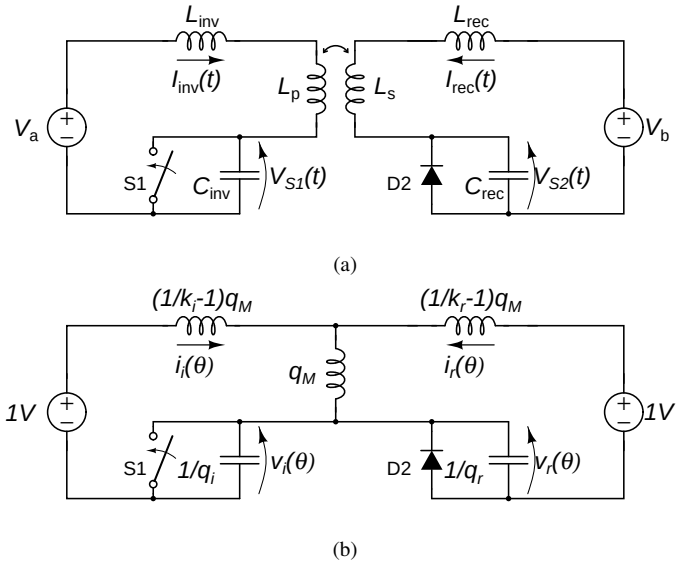


Figure 3-1: Class-E converter model and its equivalent dimensionless circuit (a): generalized model with rectifying diode as secondary side switch. (b): equivalent lossless normalized circuit with input voltage $V_{in} = 1\,\mathrm{V}$, output voltage $V_{out} = 1\,\mathrm{V}$, output power $P_{out} = 1\,\mathrm{W}$ and switching angular frequency $\omega_s = 1\,\mathrm{Hz}$.

3.1 Lossless Methodology

As a first step, a lossless model of the converter power section, depicted in Figure 3-1(a), is considered. Here, all reactive elements are taken as ideal, with zero parasitic series resistance and infinite resonance frequency, while the active devices are ideal open circuits in the off-state and short circuits in the on-state with negligible parasitic capacitances. As a consequence, it will be supposed to have $P_{out} = P_{in}$. Furthermore, the output capacitor is supposed to be big enough to keep the output voltage almost constant (i.e. negligible output ripple) is such a way that the load can be conveniently substituted with a voltage source. The following analysis is referred to the class-E topologies presented in the last chapter when the secondary switch S2 is implemented with a rectifying diode with negligible forward voltage ${V_D}^{ON} = 0$. However, the very same approach can be easily applied to synchronous switched class-E topologies and also to half-bridge and full-bridge resonant converters having the same resonant network with minor modifications.

3.1.1 Lossless ODE Analysis

The starting point for converter analysis are the **generalized class-E differential equations** (2.24)

$$\begin{cases} (L_{inv} + L_p)\,\dfrac{dI_{inv}(t)}{dt} \pm M\,\dfrac{dI_{rec}(t)}{dt} + V_{S1}(t) - V_a = 0 \\ \pm M\,\dfrac{dI_{inv}(t)}{dt} + (L_{rec} + L_s)\,\dfrac{dI_{rec}(t)}{dt} + V_{S2}(t) - V_b = 0 \end{cases} \tag{3.1}$$

where $M = NkL_p$ represents the mutual inductance as a function of the turn ratio, coupling coefficient and primary inductance while the "$\pm$" sign takes into account the different coupling between inverter and rectifier sides.

The first analysis step is **normalization**. New normalized state variables, distinguished using lower-case notation, are introduced as

$$\begin{aligned} i_i(t) &= I_{inv}(t)/I_a \quad i_r(t) = I_{rec}(t)/I_b \\ v_i(t) &= V_{S1}(t)/V_a \quad v_r(t) = V_{S2}(t)/V_b \end{aligned} \tag{3.2}$$

where virtual currents I_a and I_b are defined from the converter output power P_{out} as

$$I_a = P_{out}/V_a, \quad I_b = P_{out}/V_b. \tag{3.3}$$

Converter loop equations (3.1) are divided by the voltages V_a and V_b respectively, obtaining

$$\begin{cases} (L_{inv} + L_p)\,\dfrac{I_a}{V_a}\,\dfrac{di_i(t)}{dt} \pm M\,\dfrac{I_b}{V_a}\,\dfrac{di_r(t)}{dt} + v_i(t) = 1 \\ \pm M\,\dfrac{I_a}{V_b}\,\dfrac{di_i(t)}{dt} + (L_{rec} + L_s)\,\dfrac{I_b}{V_b}\,\dfrac{di_r(t)}{dt} + v_r(t) = 1 \end{cases} \tag{3.4}$$

Capacitor's equations in (2.22) and (2.23) hold for all class-E topologies considered and, similarly to (3.4), they can be normalized as

$$\begin{cases} i_i(t) = C_{inv}\,\dfrac{V_a}{I_a}\,\dfrac{dv_i(t)}{dt} \\ i_r(t) = C_{rec}\,\dfrac{V_b}{I_b}\,\dfrac{dv_r(t)}{dt} \end{cases} \tag{3.5}$$

Defining also the **angular time** $\theta = 2\pi\, f_s\, t = \omega_s t$ and the following **dimensionless design variables**

$$\begin{aligned} k_i &= \pm\,\xi\,\frac{M}{L_{inv}+L_p},\quad k_r = \pm\,\xi^{-1}\,\frac{M}{L_{rec}+N^2 L_p},\\ q_M &= \pm\,\frac{\omega_s\, M\, P_{out}}{V_a\, V_b},\quad q_i = \frac{1}{\omega_s R_a C_{inv}},\quad q_r = \frac{1}{\omega_s R_b C_{rec}} \end{aligned} \tag{3.6}$$

where $\xi = V_a/V_b$, $R_a = V_a/I_a = V_a^2/P_{out}$ and $R_b = V_b/I_b = V_b^2/P_{out}$, it is possible to reduce the full set of normalized equations to the following

$$\begin{cases} \dfrac{q_M}{k_i}\,\dfrac{di_i(\theta)}{d\theta} + q_M\,\dfrac{di_r(\theta)}{d\theta} + v_i(\theta) = 1 \\ q_M\,\dfrac{di_i(\theta)}{d\theta} + \dfrac{q_M}{k_r}\,\dfrac{di_r(\theta)}{d\theta} + v_r(\theta) = 1 \end{cases} \tag{3.7}$$

$$\begin{cases} v_i(\theta) = 0, & \text{if S1 is on} \\ i_i(\theta) = \dfrac{1}{q_i}\dfrac{dv_i(\theta)}{d\theta}, & \text{if S1 is off} \end{cases} \qquad \begin{cases} v_r(\theta) = 0, & \text{if D2 is on} \\ i_r(\theta) = \dfrac{1}{q_r}\dfrac{dv_r(\theta)}{d\theta}, & \text{if D2 is off} \end{cases} \tag{3.8}$$

Equations (3.7) and (3.8) can be summarized introducing two boolean variables m_{OFF} and d_{OFF} which can be either equal to zero, when the corresponding switching device is on, or equal to one when it is off.

$$\begin{cases} \dfrac{q_M}{k_i}\,\dfrac{di_i(\theta)}{d\theta} + q_M\,\dfrac{di_r(\theta)}{d\theta} + m_{OFF}\; v_i(\theta) = 1 \\ q_M\,\dfrac{di_i(\theta)}{d\theta} + \dfrac{q_M}{k_r}\,\dfrac{di_r(\theta)}{d\theta} + d_{OFF}\; v_r(\theta) = 1 \\ m_{OFF}\, i_i(\theta) = \dfrac{1}{q_i}\dfrac{dv_i(\theta)}{d\theta} \\ d_{OFF}\, i_r(\theta) = \dfrac{1}{q_r}\dfrac{dv_r(\theta)}{d\theta} \end{cases} \tag{3.9}$$

This kind of approach has a **twofold advantage**:

First, the dimensionality of the system is greatly reduced. In fact the equations in (3.6) actually represent a remapping of the original design space into a reduced set

of normalized design variables

$$\begin{aligned} &\{V_{in}, V_{out}, P_{out}, f_s, D, M, L_p, L_s, L_{inv}, L_{rec}, C_{inv}, C_{rec}\} \in \mathbb{R}^{12} \\ &\Longrightarrow \{D, k_i, k_r, q_M, q_i, q_r\} \in \mathbb{R}^6 \end{aligned} \tag{3.10}$$

where D is the main switch duty cycle.

Second, the normalized system (3.9), fully describing the circuit behavior, is completely independent of the switching frequency and of the output voltage and power. In this way, for a given value of D, once computed the normalized design variables k_i, k_r, q_M, q_i and q_r which satisfiy the soft-switching conditions at steady-state, it is possible to easily realize multiple designs with different switching frequency and output power level by simply exploiting the following de-normalizing equations, retrieved from (3.6):

$$\begin{aligned} L_p &= \frac{V_a\, V_b}{\omega_s\, N\, k\, P_{out}}\, |q_M|, \\ L_{inv} = \left(\frac{\xi\, N\, k}{|k_i|} - 1\right) L_p, \quad L_{rec} &= \left(\frac{k}{\xi\, N\, |k_r|} - 1\right) N^2 L_p, \\ C_{inv} = \frac{1}{\omega_s\, R_a\, q_i}, \quad C_{rec} &= \frac{1}{\omega_s\, R_b\, q_r}. \end{aligned} \tag{3.11}$$

After defining the equations that regulate the state variables evolution during circuit operation, the second step of analysis consists in computing the complete set of steady-state waveforms as a **piecewise solution of the normalized ODE system**. The resonant nature of these converters reflects on the fact that both switching devices can be on (or off) simultaneously, so all the four on/off combinations are actually possible during the switching period. The typical converter switching behavior for both in-phase and out-of phase coupling is shown in Figure 3-2. The switching period $\theta \in [0, 2\pi]$ can be divided into four **Zones**, that will be referred to as

$$Z_i = \{\, \theta \,|\, \theta_{i-1} \leq \theta < \theta_i \} \quad i = 1, 2, 3, 4$$

with $\theta_0 = 0$ and $\theta_4 = 2\pi$. Consequently, the state variables in each zone will be

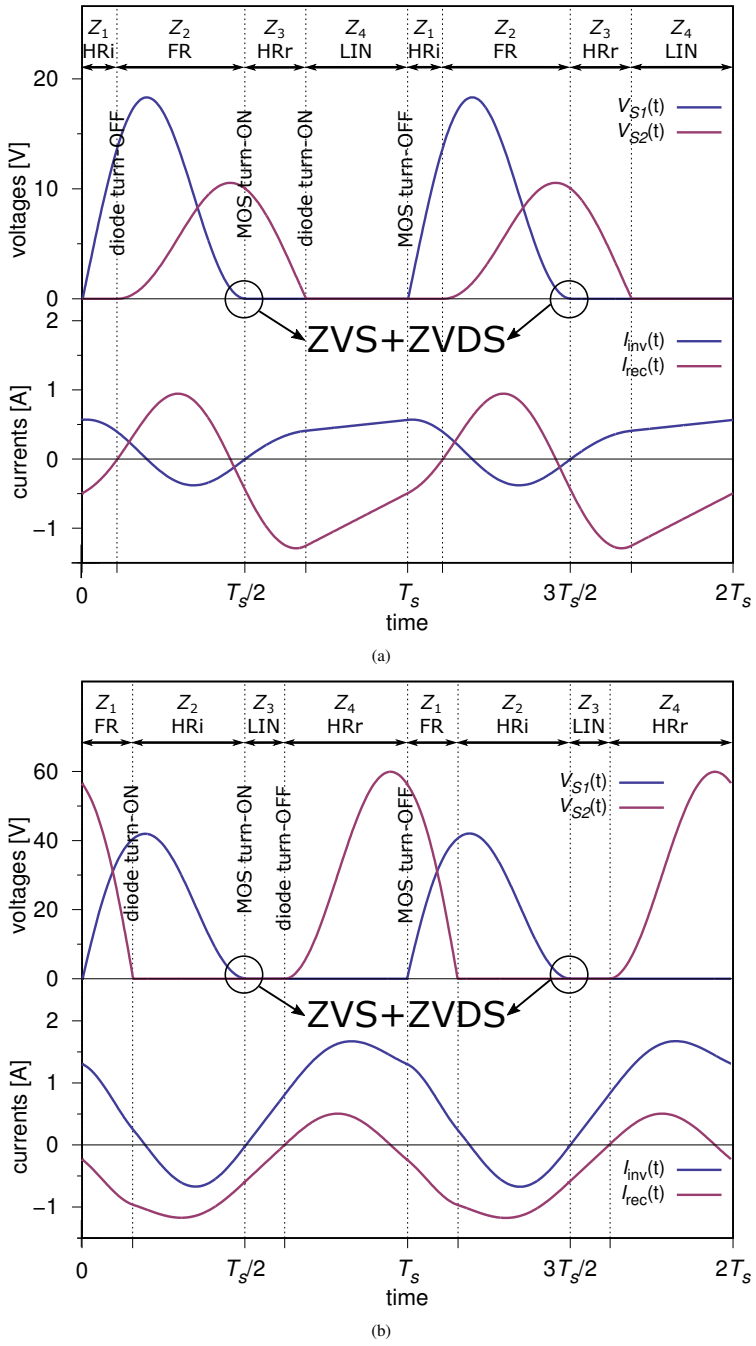


Figure 3-2: Resonant converter voltage and current waveforms for (a) in-phase coupled secondary side and (b) 180° out-of-phase coupled secondary side.

identified with the notation below

$$\mathbf{x}_i(\theta) \triangleq \begin{pmatrix} {i_i}^{(i)}(\theta) \\ {i_r}^{(i)}(\theta) \\ {v_i}^{(i)}(\theta) \\ {v_r}^{(i)}(\theta) \end{pmatrix} \triangleq \begin{pmatrix} i_i(\theta) \ : \theta \in Z_i \\ i_r(\theta) \ : \theta \in Z_i \\ v_i(\theta) \ : \theta \in Z_i \\ v_r(\theta) \ : \theta \in Z_i \end{pmatrix} \tag{3.12}$$

As an example, considering to have in-phase coupling and choosing as a time reference the instant in which the primary side switch M1 is turned off ($\theta = \theta_0 = 0$), the converter evolution in Figure 3-2(a) is obtained as follows (please note that a detailed computation of the ODE system solutions is reported in the Appendix B).

Zone 1 (HRi): For $\theta \in Z_1$ the MOS switch is off ($m_{OFF} = 1$) while the rectifying diode is still conducting ($d_{OFF} = 0$), hence ${v_r}^{(1)}(\theta) = 0 \ \ \forall\, \theta \in Z_1$ and the converter behavior is regulated by a third order ODE system in the state variables ${i_i}^{(1)}(\theta)$, ${i_r}^{(1)}(\theta)$ and ${v_i}^{(1)}(\theta)$

$$\begin{cases} \dfrac{q_M}{k_i} \dfrac{d{i_i}^{(1)}(\theta)}{d\theta} + q_M \dfrac{d{i_r}^{(1)}(\theta)}{d\theta} + {v_i}^{(1)}(\theta) - 1 = 0 \\ q_M \dfrac{d{i_i}^{(1)}(\theta)}{d\theta} + \dfrac{q_M}{k_r} \dfrac{d{i_r}^{(1)}(\theta)}{d\theta} - 1 = 0 \\ \dfrac{d{v_i}^{(1)}(\theta)}{d\theta} - q_i \, {i_i}^{(1)}(\theta) = 0 \end{cases} \tag{3.13}$$

subject to the initial conditions

$$\begin{cases} {i_i}^{(1)}(0) = {i_i}^0 \\ {i_r}^{(1)}(0) = {i_r}^0 \\ {v_i}^{(1)}(0) = {v_i}^0 = 0 \end{cases} \tag{3.14}$$

where ${i_i}^0$ and ${i_r}^0$ are unknowns to be determined. The equations (3.13) can be easily decoupled by substitution into the following second order ODE system and first order

differential equation:

$$\begin{cases} q_M \left(\dfrac{1}{q_i} - k_r\right) \dfrac{di_i{}^{(1)}(\theta)}{d\theta} + v_i{}^{(1)}(\theta) + k_r - 1 = 0 \\ \dfrac{dv_i{}^{(1)}(\theta)}{d\theta} - q_i\, i_i{}^{(1)}(\theta) = 0 \end{cases} \tag{3.15}$$

$$q_M \frac{di_i{}^{(1)}(\theta)}{d\theta} + \frac{q_M}{k_r} \frac{di_r{}^{(1)}(\theta)}{d\theta} - 1 = 0 \tag{3.16}$$

The generic solution for (3.15) and (3.16) is

$$\mathbf{x}_1(\theta) = \begin{pmatrix} \beta_0/q_i \left(c_2 \cos(\beta_0\,\theta) - c_1 \sin(\beta_0\,\theta)\right) \\ -k_r\beta_0/q_i \left(c_2 \cos(\beta_0\,\theta) - c_1 \sin(\beta_0\,\theta)\right) + \dfrac{k_r}{q_M}\theta + c_3 \\ c_1 \cos(\beta_0\,\theta) + c_2 \sin(\beta_0\,\theta) + 1 - k_r \\ 0 \end{pmatrix} \tag{3.17}$$

where $\beta_0 = \sqrt{\dfrac{k_i\, q_i}{q_M\,(1 - k_i k_r)}} \in \mathbb{R}$ and the coefficients c_1, c_2 and c_3 can be computed from the initial conditions $\mathbf{x}_1(\theta_0) = (i_i^0,\, i_r^0,\, 0,\, 0)^\intercal$.

Zone 2 (FR): At $\theta = \theta_1$ the diode current falls down to zero, the device turns-off ($m_{OFF} = 1$, $d_{OFF} = 1$) and Z_2 starts. The value of θ_1 can be (numerically) computed from (3.17) by solving $i_r{}^{(1)}(\theta_1) = 0$ under the constraint $0 < \theta_1 < \theta_2 = 2\pi(1 - D)$, and the state variables evolution is regulated by a fourth order system of differential equations

$$\begin{cases} \dfrac{q_M}{k_i} \dfrac{di_i{}^{(2)}(\theta)}{d\theta} + q_M \dfrac{di_r{}^{(2)}(\theta)}{d\theta} + v_i{}^{(2)}(\theta) - 1 = 0 \\ q_M \dfrac{di_i{}^{(2)}(\theta)}{d\theta} + \dfrac{q_M}{k_r} \dfrac{di_r{}^{(2)}(\theta)}{d\theta} + v_r{}^{(2)}(\theta) - 1 = 0 \\ \dfrac{dv_i{}^{(2)}(\theta)}{d\theta} - q_i\, i_i{}^{(2)}(\theta) = 0 \\ \dfrac{dv_r{}^{(2)}(\theta)}{d\theta} - q_r\, i_r{}^{(2)}(\theta) = 0 \end{cases} \tag{3.18}$$

subject to the initial conditions

$$\begin{cases} {i_i}^{(2)}(\theta_1) = {i_i}^{(1)}(\theta_1) \\ {i_r}^{(2)}(\theta_1) = {i_r}^{(1)}(\theta_1) \\ {v_i}^{(2)}(\theta_1) = {v_i}^{(1)}(\theta_1) \\ {v_r}^{(2)}(\theta_1) = 0 \end{cases} \tag{3.19}$$

Solutions are made of the superposition of two sinusoidal tones and can be computed from the eigenvalues

$$\lambda_{1,2} = \pm j\beta_1,\ \lambda_{3,4} = \pm j\beta_2$$

(with $\beta_1, \beta_2 \in \mathbb{R}$) and eigenvectors

$$\mathbf{v}_{1,2} = \begin{pmatrix} \pm j\mathrm{v}_{11} & \pm j\mathrm{v}_{12} & \mathrm{v}_{13} & 1 \end{pmatrix}^{\intercal},\ \mathbf{v}_{3,4} = \begin{pmatrix} \pm j\mathrm{v}_{31} & \pm j\mathrm{v}_{32} & \mathrm{v}_{33} & 1 \end{pmatrix}^{\intercal}$$

(with $v_{11}, v_{12}, v_{13}, v_{31}, v_{32}, v_{33} \in \mathbb{R}$) of the matrix $\mathbf{A} = \begin{pmatrix} 0 & \dfrac{k_i}{q_M\,(1 - k_i k_r)} \\ -q_i & 0 \end{pmatrix}$ as

$$\mathbf{x}_2(\delta\theta) = \begin{pmatrix} c_2\mathrm{v}_{11}\cos(\beta_1\,\delta\theta) - c_1\mathrm{v}_{11}\sin(\beta_1\,\delta\theta) + c_4\mathrm{v}_{31}\cos(\beta_2\,\delta\theta) - c_3\mathrm{v}_{31}\sin(\beta_2\,\delta\theta) \\ c_2\mathrm{v}_{12}\cos(\beta_1\,\delta\theta) - c_1\mathrm{v}_{12}\sin(\beta_1\,\delta\theta) + c_4\mathrm{v}_{32}\cos(\beta_2\,\delta\theta) - c_3\mathrm{v}_{32}\sin(\beta_2\,\delta\theta) \\ c_1\mathrm{v}_{13}\cos(\beta_1\,\delta\theta) + c_2\mathrm{v}_{13}\sin(\beta_1\,\delta\theta) + c_3\mathrm{v}_{33}\cos(\beta_2\,\delta\theta) + c_4\mathrm{v}_{33}\sin(\beta_2\,\delta\theta) + 1 \\ c_1\cos(\beta_1\,\delta\theta) + c_2\sin(\beta_1\,\delta\theta) + c_3\cos(\beta_2\,\delta\theta) + c_4\sin(\beta_2\,\delta\theta) + 1 \end{pmatrix} \tag{3.20}$$

where $\delta\theta = \theta - \theta_1$ and real coefficients c_1, c_2, c_3 and c_4 that can be computed from the initial conditions $\mathbf{x}_2(0) = \left({i_i}^{(1)}(\theta_1), {i_r}^{(1)}(\theta_1), {v_i}^{(1)}(\theta_1), 0\right)^{\intercal}$.

Zone 3 (HRr): Z_3 begins at $\theta = \theta_2 = 2\pi(1 - D),\ 0 < D < 1$, when the MOS switch is instantaneously turned-on ($m_{OFF} = 0$, $d_{OFF} = 1$). Then, the primary side current, previously resonating through the capacitor C_{inv}, now starts flowing through the active device; hence ${v_i}^{(3)}(\theta) = 0 \quad \forall\, \theta \in Z_3$ and the state variables evolution is

regulated by the third order system

$$\begin{cases} \dfrac{q_M}{k_i}\,\dfrac{di_i{}^{(3)}(\theta)}{d\theta} + q_M\,\dfrac{di_r{}^{(3)}(\theta)}{d\theta} - 1 = 0 \\ q_M\,\dfrac{di_i{}^{(3)}(\theta)}{d\theta} + \dfrac{q_M}{k_r}\,\dfrac{di_r{}^{(3)}(\theta)}{d\theta} + v_r{}^{(3)}(\theta) - 1 = 0 \\ \dfrac{dv_r{}^{(3)}(\theta)}{d\theta} - q_r\, i_r{}^{(3)}(\theta) = 0 \end{cases} \tag{3.21}$$

subject to the initial conditions

$$\begin{cases} i_i{}^{(3)}(\theta_2) = i_i{}^{(2)}(\theta_2) \\ i_r{}^{(3)}(\theta_2) = i_r{}^{(2)}(\theta_2) \\ v_r{}^{(3)}(\theta_2) = v_r{}^{(2)}(\theta_2) \end{cases} \tag{3.22}$$

Solutions can be easily retrieved from (3.17) due to the circuit symmetry

$$\mathbf{x}_3(\delta\theta) = \begin{pmatrix} -k_i\beta_3/q_r\,(c_2\cos(\beta_3\,\delta\theta) - c_1\sin(\beta_3\,\delta\theta)) + \dfrac{k_i}{q_M}\theta + c_3 \\ \beta_3/q_r\,(c_2\cos(\beta_3\,\delta\theta) - c_1\sin(\beta_3\,\delta\theta)) \\ 0 \\ c_1\cos(\beta_3\,\delta\theta) + c_2\sin(\beta_3\,\delta\theta) + 1 - k_i \end{pmatrix} \tag{3.23}$$

where $\beta_3 = \sqrt{\dfrac{k_r\,q_r}{q_M\,(1-k_ik_r)}} \in \mathbb{R}$ and the coefficients c_1, c_2 and c_3 can be computed from the initial conditions $\mathbf{x}_3(0) = \left(i_i{}^{(2)}(\theta_2),\, i_r{}^{(2)}(\theta_2),\, v_i{}^{(2)}(\theta_2),\, v_r{}^{(2)}(\theta_2)\right)^{\mathsf{T}}$.

Zone 4 (LIN): Finally, Z_4, where both switching devices are on ($m_{OFF} = 0$, $d_{OFF} = 0$), begins at $\theta = \theta_3$ when the reverse voltage of the diode falls down to zero. The value of θ_4 can be computed by solving $v_r{}^{(3)}(\theta_3) = 0$, with $\theta_2 < \theta_3 < \theta_4 = 2\pi$. The circuit evolution is regulated by a second order ODE system

$$\begin{cases} \dfrac{q_M}{k_i}\,\dfrac{di_i{}^{(4)}(\theta)}{d\theta} + q_M\,\dfrac{di_r{}^{(4)}(\theta)}{d\theta} - 1 = 0 \\ q_M\,\dfrac{di_i{}^{(4)}(\theta)}{d\theta} + \dfrac{q_M}{k_r}\,\dfrac{di_r{}^{(4)}(\theta)}{d\theta} - 1 = 0 \end{cases} \tag{3.24}$$

subject to the initial conditions

$$\begin{cases} {i_i}^{(4)}(\theta_3) = {i_i}^{(3)}(\theta_3) \\ {i_r}^{(4)}(\theta_3) = {i_r}^{(3)}(\theta_3) \end{cases} \tag{3.25}$$

The current solution is made of two straight line waveforms

$$\mathbf{x}_4(\delta\theta) = \begin{pmatrix} \dfrac{k_i\,(1-k_r)}{q_M\,(1-k_i k_r)}\,\delta\theta + c_1 \\ \dfrac{k_r\,(1-k_i)}{q_M\,(1-k_i k_r)}\,\delta\theta + c_2 \\ 0 \\ 0 \end{pmatrix} \tag{3.26}$$

where $\delta\theta = \theta - \theta_3$ and the coefficients c_1 and c_2 can be computed from the initial conditions. Finally, Z_4 ends at $\theta = \theta_4 = 2\pi$ when the MOS switch is turned-off and the described behavior is repeated periodically.

In conclusion, the normalized analytic evolution of the converter in a clock period can be computed zone by zone starting from the **initial conditions**

$$IC = [i_i(0),\ i_r(0),\ v_i(0),\ v_i(0)]^{\intercal} = \left[{i_i}^0,\ {i_r}^0\ 0,\ 0\right]^{\intercal} \tag{3.27}$$

once the **six dimensionless parameters**

$$D,\ k_i,\ k_r,\ q_M,\ q_i,\ q_r \tag{3.28}$$

are known. Among them, k_i and k_r are influenced by the voltage ratio ξ and by the amount of inductance in the inverter and rectifier branches, q_i and q_r are related to the design of the resonant capacitors in order to get the desired soft-switching operation and q_M is proportional to the product $\omega_s\,M\,P_{out}$. If in-phase coupling is considered ($q_M > 0$, $k_i > 0$, $k_r > 0$), then the zone sequence is exactly the one presented while, if secondary side is reverse coupled ($q_M < 0$, $k_i < 0$, $k_r < 0$) the right zone sequence

will be the one depicted in Figure 3-2(b). It is worth noting that also other zone sequences are possible but mostly in rather unpractical situations such as when the system is not in a steady-state condition, or when the considered quality factors of the components are extremely low. In all realistic cases the succession of zones are those depicted in Fig. 3-2.

3.1.2 Design Curves

The third step, after calculating the analytic expression of the state variable waveforms for each zone and identifying the parameters at designer's disposal (i.e. degrees of freedom), is to put the constraints for class-E operation into a mathematical form.

Stationary condition

Steady-state is achieved when the value of the currents flowing through the inductors at the end of each switching period are equal to those at the beginning

$$\Delta i_i \triangleq i_i(2\pi) - i_i^{\,0} = 0, \quad \Delta i_r \triangleq i_r(2\pi) - i_r^{\,0} = 0 \tag{3.29}$$

and the average current flowing into the load capacitor C_L is zero, so that the average output voltage is unchanged across switching periods justifying the assumption to replace it with an ideal voltage source

$$\frac{1}{2\pi}\int_0^{2\pi} I_{C_L}(\theta)\, d\theta = 0 \tag{3.30}$$

Depending on the converter topology considered, Equation (3.30) can be rewritten as:

$$\frac{I_b}{2\pi}\int_0^{2\pi} i_r(\theta)\, d\theta + I_{out} = 0 \tag{3.31}$$

for the resonant isolated and non-isolated buck-boost and boost converters; or

$$\frac{1}{2\pi}\left(I_a\int_0^{2\pi} i_i(\theta)\, d\theta - I_b\int_0^{2\pi} i_r(\theta)\, d\theta\right) - I_{out} = 0 \tag{3.32}$$

for the resonant buck converter, with $I_{out} = P_{out}/V_{out}$.

Notably, the first constraint (3.29) is automatically satisfied letting the piecewise system evolve for k switching periods until a stationary condition is detected

$$\|(\Delta i_i,\ \Delta i_r)_k\| < \varepsilon \tag{3.33}$$

with ε as low as it is required to achieve the desired solution accuracy. It is worth noting that continuity conditions on switch voltages, since $v_i(0) = v_i(2\pi) = 0$ and $v_r(0) = v_r(2\pi) = 0$, are always automatically satisfied for in-phase zone sequence while in case of out-of-phase coupling also $\Delta v_r \triangleq v_r(2\pi) - v_r(0)$ must be considered.

Zero Voltage Switching (ZVS)

ZVS condition is needed to reduce the voltage-current product at the switching instants and also ensures that there is no energy inside the resonant capacitor to be discharged at MOS turn-on ($\theta = \theta_2$). It is satisfied when

$$v_i(\theta_2) = 0 \tag{3.34}$$

When both (3.29) and (3.34) are satisfied the state variables are continuous across the whole period T_s, and there is no power loss due to parallel capacitor discharge. Note that the ZVS condition at the secondary side is always automatically satisfied due to the presence of the diode.

Zero Voltage-Derivative Switching (ZVDS)

ZVDS is obtained when $dv_i(\theta)/d\theta = 0$ for $\theta = \theta_2$. Since the voltage derivative is proportional to the inverter side current due to the capacitor constitutive relation in (3.8), this is equivalent to ask that

$$i_i(\theta_2) = 0 \tag{3.35}$$

It is worth mentioning that this is actually not a strictly required constraint for converter operation but can help reducing the switching loss since the intial current

through S1 after turn-on rises gradually from zero and the achieved design is also much more robust with respect to parameters variability.

Equations (3.31)/(3.32), (3.34) and (3.35) represent a system of **three non-linear equations in the six dimensionless variables D, $\mathbf{k_i}$, $\mathbf{k_r}$, $\mathbf{q_M}$, $\mathbf{q_i}$ and $\mathbf{q_r}$**. Hence, three among the six variables are actually degrees of freedom at designer's disposal while the remaining three must be computed to ensure optimum class-E operation. Since it is usually preferred to set the values of inductors with respect to the value of capacitors, which can be easily placed in parallel to obtain the desired amount of capacitance, a particularly convenient choice is to take as **design constants** the duty cycle and the normalized inductors values

$$\mathbf{k} = (D, k_i, k_r)$$

and numerically solve the system in the three **design variables**

$$\mathbf{q} = (q_M, q_i, q_r)$$

to get the desired class-E working point.

The main advantage of the dimensionless approach is that after normalizing the system of equations it is possible to see how many the actual degrees of freedom of the system really are and understand their relation with the other physical quantities such as frequency, inductance, voltage and power. Starting from a dimensionless design point, in fact, a designer can simply ensure the optimum class-E operation by taking the dimensionless solution and denormalize it with the actual values of V_{in}, V_{out}, P_{out} and f_s (in case of an isolated topology, also the values of N and k have to be used in the denormalization process) exploiting the relations in (3.11). This opens the way toward the **complete exploration of the whole design space** solving the constraints for all possible values of $\mathbf{k}$. For $D = 0.5$, the design curves in Figure 3-3 have been computed exploiting the *MATLAB Optimization Toolbox* from *MathWorks*® for both (a) in-phase and (b) out-of-phase coupled secondary side. A

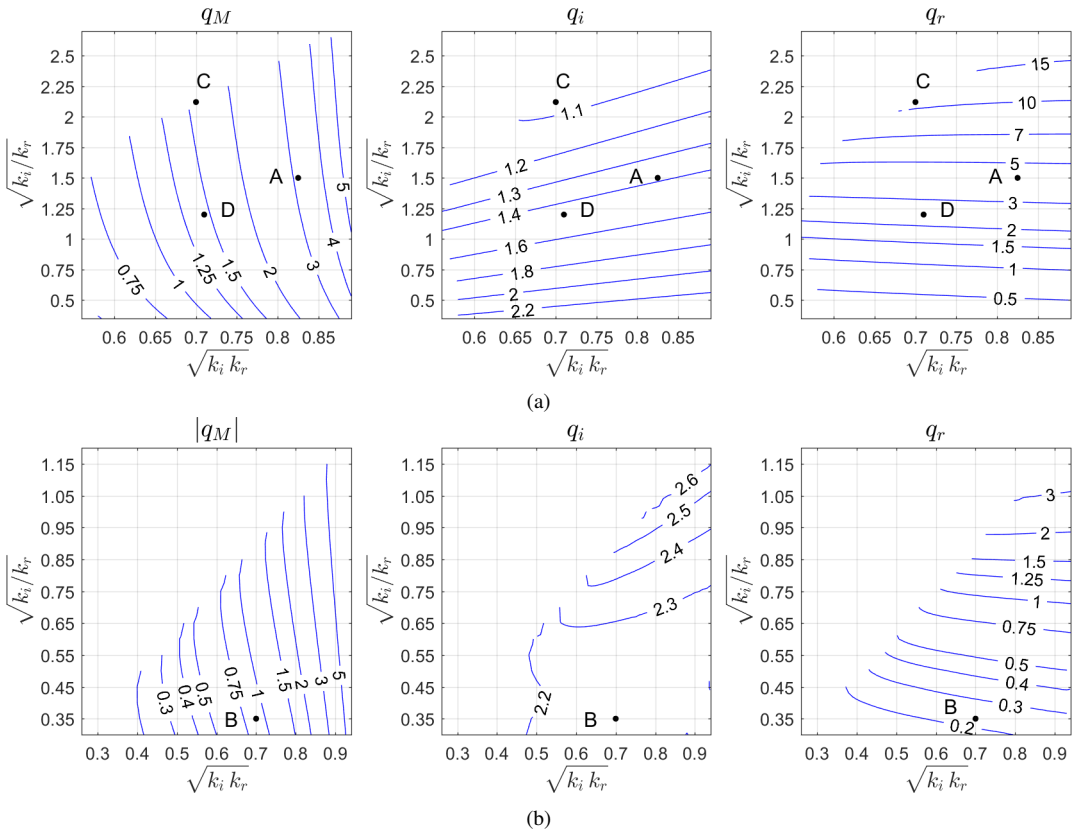


Figure 3-3: Lossless design curves for non-isolated and isolated resonant class-E converters with $D = 0.5$ and (a) in-phase coupling or (b) 180° out-of-phase coupling.

first version of class-E design curves, with a slightly different normalization, was presented in [**34**]. Recent developments introduced in this document demonstrate that, with respect to that work, the system dimensionality can be further reduced including the voltage ratio ξ inside the values of k_i and k_r. Additionally, in this thesis, for both computational and graphical reasons the design space is represented in a new coordinate space identified applying the following $\mathbb{R}^5 \rightarrow \mathbb{R}^5$ transformation

$$(k_i, k_r, q_M, q_i, q_r) \rightarrow \left(\sqrt{k_i\, k_r}, \sqrt{k_i/k_r}, q_M, q_i, q_r\right)$$

All the portions of the $\left(\sqrt{k_i\, k_r}, \sqrt{k_i/k_r}\right)$ plane where contours are shown represent the feasible design space where class-E operating conditions at steady-state can be satisfied. The values of q_i and q_r are inversely proportional to the amount of capacitance needed to ensure soft switching transitions, and they are indicators of the maximum parasitic capacitance that can be introduced with the active devices for given design specifications. For example, with both in-phase and out-of-phase topologies, one can clearly observe that the value of q_r rapidly increases with $\sqrt{k_i/k_r}$ and hence it becomes more challenging to design the secondary active device in such a way that the capacitance introduced in the circuit does not exceed $1/\left(\omega_s\, R_b\, q_r\right)$. Even more important is the role of the other dimensionless parameter q_M, which is directly proportional to the product $\omega_s M P_{out}$. For example, a design with a lower q_M (i.e. moving from the right to the left on the x-axis) will lead to a lower output power for a given frequency and coupling inductance. In the following two design examples will be provided to better clarify the resonant converter design procedure based on this set of curves.

3.1.3 Lossless Design Example

Given the converter specifications as

$$V_{in} = 5\,\mathrm{V},\ V_{out} = 3.3\,\mathrm{V},\ f_s = 1\,\mathrm{MHz},\ P_{out} \geq 500\,\mathrm{mW},$$

there are several options to implement a dc-to-dc power conversion stage with the resonant topologies presented hitherto. Among them, (A) isolated class-E converter

and (B) non-isolated class-E buck converter solutions will be investigated and a step-by-step procedure to clarify the whole design process will be described into detail by means of useful numerical examples.

Design (A): Class-E isolated 5 V-to-3.3 V converter

If galvanic isolation is a required feature, the resonant converter can be realized implementing one of the isolated topologies of Figure 2-5(a-b). For this example in-phase coupled topology is chosen. Furthermore, in order to allow a simpler transformer implementation 1:1 turn ratio is preferred ($N = 1$). Under the hypothesis to have a transformer with low coupling coefficient, for example $k = 0.825$, both inverter and rectifier inductors L_{inv} and L_{rec} are not necessary. Hence, the other free dimensionless parameters are computed from the input/output voltage ratio and the transformer coupling coefficient as

$$\xi = \frac{V_{in}}{V_{out}} \approx 1.5, \quad k_i = k\,\xi, \quad k_r = k/\xi,$$

$$\sqrt{k_i\,k_r} = k = 0.825, \quad \sqrt{k_i/k_r} = \xi = 1.5.$$

From the design curves in Figure 3-3(a) (marker "A") one gets

$$q_M \approx 3.16, \quad q_i \approx 1.4, \quad q_r \approx 4.25.$$

The transformer inductance upper bound is retrieved from (3.11) as

$$L_p = \frac{V_{in}\,V_{out}}{2\pi f_s k P_{out}}\,q_M \leq 19.9\,\mu\text{H}.$$

Finally, rounding the inductance L_p to $18\,\mu$H, the effective output power and the capacitor values are calculated as

$$P_{out} = \frac{V_{in}\,V_{out}}{2\pi f_s k L_p}\,q_M \approx 550\,\text{mW},$$

$$C_{inv} = \frac{P_{out}}{2\pi f_s {V_{in}}^2 q_i} \approx 2.56\,\text{nF}, \quad C_{rec} = \frac{P_{out}}{2\pi f_s {V_{out}}^2 q_r} \approx 1.9\,\text{nF}.$$

Design (B): Class-E 5 V-to-3.3 V buck converter

An alternative implementation is obtained exploiting the resonant buck topology. Since it is a non-isolated converter one must set $N = 1$, $k = 1$ and calculate outer and secondary loop voltages from Table 2.1 as $V_a = V_{in} - V_{out} = 1.7\,\mathrm{V}$ and $V_b = V_{out} = 3.3\,\mathrm{V}$. Then the input/output ratio is computed as

$$\xi = N\,V_a/V_b = 1.7\,\mathrm{V}/3.3\,\mathrm{V} \approx 0.5.$$

If one decide to not implement inductor L_{rec} and choose the same valued inductors for both L_p and L_{inv}, then $k_i = -0.5\,\xi = -0.25$ and $k_r = -1/\xi = -2$, which means

$$\sqrt{k_i\,k_r} \approx 0.7, \quad \sqrt{k_i/k_r} \approx 0.35.$$

From the design curves in Figure 3-3(b) (marker "B") the dimensionless parameters are extracted as

$$q_M \approx -0.92, \quad q_i \approx 2.25, \quad q_r \approx 0.234.$$

Inductance is computed exploiting again (3.11) paying attention that the effective output power of a buck topology must be scaled by $(V_b/V_a + 1)$ as outlined in (2.26)

$$L_p = L_{rec} = \left(\frac{V_b}{V_a} + 1\right) \frac{V_{in}\,V_{out}}{2\pi f_s P_{out}}\,|q_M| \leq 4.89\,\mu\mathrm{H}.$$

In this case the closest standard value for inductors is $4.7\,\mu\mathrm{H}$ and the resulting effective output power is

$$P_{out} = \left(\frac{V_b}{V_a} + 1\right) \frac{V_{in}\,V_{out}}{2\pi f_s L_p}\,|q_M| \approx 510\,\mathrm{mW}.$$

Finally, capacitor values are calculated as

$$C_{inv} = \frac{P_{out}/\left(\frac{V_b}{V_a}+1\right)}{2\pi f_s {V_{in}}^2\,q_i} \approx 4.4\,\mathrm{nF}, \quad C_{rec} = \frac{P_{out}/\left(\frac{V_b}{V_a}+1\right)}{2\pi f_s {V_{out}}^2\,q_r} \approx 10.5\,\mathrm{nF}.$$

3.2 Lossy Methodology

One of the main disadvantages of resonant dc-dc converters is that **any resistive parasitic in the circuit can significantly alter the designed waveforms**. Consequently, besides the power loss directly due to the dissipation in the resistive parasitics themselves, there is an additional loss contribution due to the fact that the converter operates away from the ZVS and ZVDS conditions and the overall system efficiency is much more severely impacted. In order to overcome this drawback, the unified design methodology presented is improved taking into account the main circuit losses such as those related to switching devices on-resistance, rectifying diode voltage drop and finite resonant elements quality factor.

3.2.1 Component Modeling

In order to develop an accurate mathematical model also for dc-dc converters having efficiency that is far less than 100%, for each device a simple equivalent circuit that includes non-idealities and parasitic effects is presented.

The MOS transistor is modeled as an open circuit when in the off-state and with an equivalent channel resistance R_{DS}^{ON} when it is turned-on. Similarly, the diode is modeled as an open circuit when it is off while its equivalent on-state circuit is made up of a voltage source ${V_D}^{ON}$ with a series resistance ${R_D}^{ON}$ to take into account the relation between the device voltage and the current flowing through it. Considering the parallel connection of a MOS device, a diode and a capacitor, one obtains the **resonant switch** depicted in Figure 3-4(a-c) which can be modeled with an equivalent Thevenin circuit, including the linearized active devices and the resistance R_C, connected in parallel with the resonant capacitor C. Considering a voltage $V_{sw}(t)$ applied between the terminals of this subcircuit, a current $I_{sw}(t)$ will flow following the relation

$$I_{sw}(t) = I_C(t) + I_d(t) = C\frac{dV_{sw}(t)}{dt} + \frac{V_{sw}(t) + V_d}{R_d} \tag{3.36}$$

Depending on the on/off state of MOS and diode the equivalent circuit elements V_d and R_d can have different values: (a) if diode is off $V_d = 0$ and if also MOS is

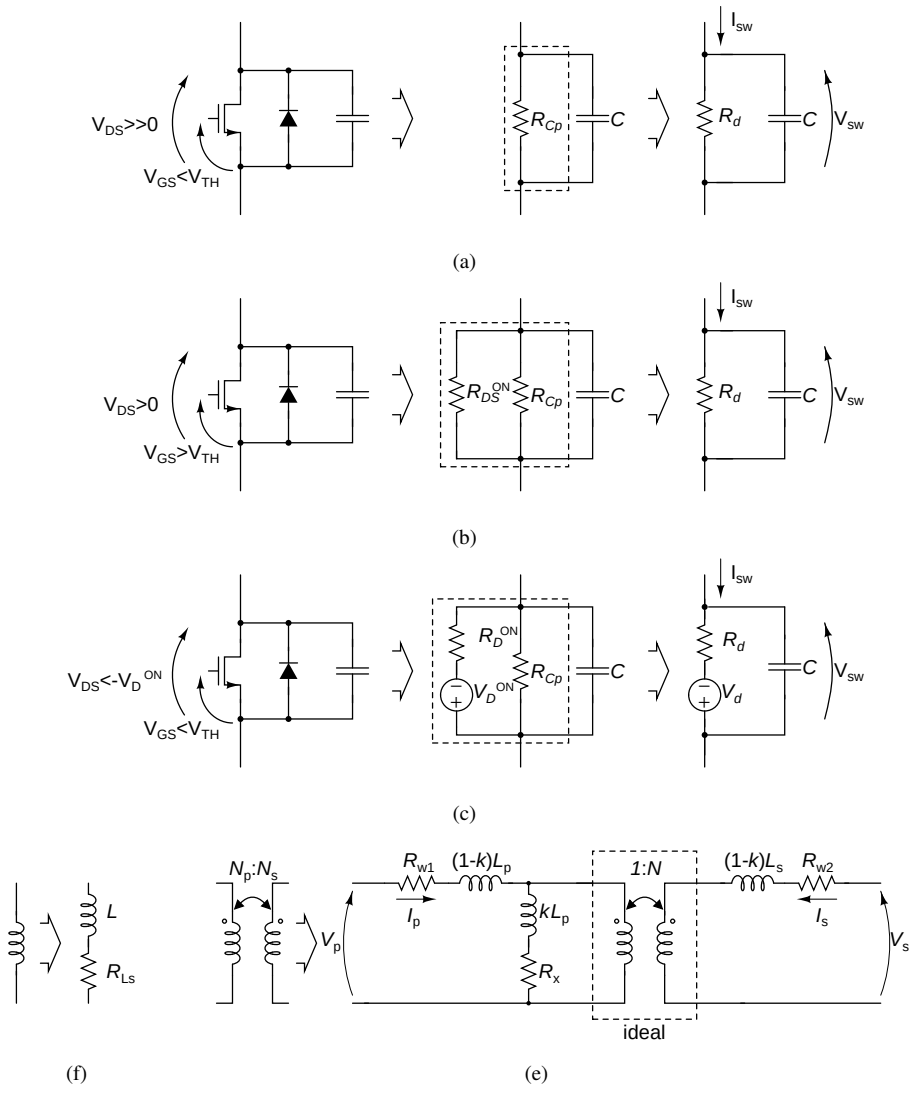


Figure 3-4: Lossy devices models: Resonant switch model when (a) the MOS is OFF, (b) the MOS is ON or (c) antiparallel diode is ON. (d) Resonant inductor model and (e) 1:N transformer with both winding and core losses modeled with series resistances.

off then $R_d = R_{Cp}$; (b) if MOS is on and diode off $R_d = R_{DS}^{ON} /\!\!/ R_{Cp}$, while (c) if MOS is off and diode on $V_d = R_{Cp}/(R_{Cp} + R_D^{ON})V_D^{ON}$ and $R_d = R_D^{ON} /\!\!/ R_{Cp}$. Note that both diode and parallel capacitor can be seen either as the inner bulk diode and the output capacitance of the MOS device, commonly referred to as C_{oss}, or as external components opportunely connected to "mask" these parasitics. For example, an external schottky diode would have a smaller forward voltage compared to the diode inside the MOS thus preventing it to turn-on. Likewise, an external capacitor much bigger than the C_{oss} would reduce the impact of its non-linearity on the circuit behavior.

Under the hypothesis that reactive elements are all operating well below their resonance frequency, and that the power dissipation on parasitic elements is mainly related to the first harmonic of current/voltage excitation then these parasitics can be simply modeled as series or parallel resistors. The capacitor parasitics are modeled with an equivalent parallel resistance R_{Cp}, as depicted in Figure 3-4(a-c), which is related to the quality factor Q_C by the formula

$$R_{Cp} = \omega_s C Q_C.$$

To take into account also the finite quality factor of inductors an equivalent series resistance R_{Ls} is introduced, whose value can be computed once the quality factor Q_L is known as

$$R_{Ls} = \frac{\omega_s L}{Q_L}.$$

The transformer is modeled adding two series resistors $R_{w1} = \omega_s L_p/Q_{L_p}$ and $R_{w2} = \omega_s L_s/Q_{L_s}$ to account for ohmic loss in the windings and an additional resistor $R_x = R_M/N = \omega_s M/(NQ_M)$ in series with the magnetizing inductance $L_x = kL_p$ referred to the primary side to model the power loss in the ferromagnetic core. The transformer matrix description is then updated as follows:

$$\begin{pmatrix} V_p(t) \\ V_s(t) \end{pmatrix} = \begin{pmatrix} L_p & \pm M \\ \pm M & L_s \end{pmatrix} \frac{d}{dt} \begin{pmatrix} I_p(t) \\ I_s(t) \end{pmatrix} + \omega_s \begin{pmatrix} L_p/Q_{L_p} & \pm M/Q_M \\ \pm M/Q_M & L_s/Q_{L_s} \end{pmatrix} \begin{pmatrix} I_p(t) \\ I_s(t) \end{pmatrix} \quad (3.37)$$

Once all the lossy circuit elements have been modeled, the differential equation system describing the state variables evolution must be consequently rewritten and new analytic solutions must be found and properly combined to define a new lossy approach to resonant converters analysis. This step will be of crucial importance to have a first approximation of the system efficiency early during the design process opening the way towards several optimization strategies.

3.2.2 Lossy ODE Analysis

Including all the lossy models for both switching devices and resonant elements the new class-E equivalent circuit in Figure 3-5(a) is drawn. Inductors $L_i = L_{inv} + (1-k)L_p$ and $L_r = L_{rec} + (1-k)L_s$ are introduced to include both the the transformer leakage inductance and the primary and secondary inductances L_{inv} and L_{rec}. Similarly, the primary side and secondary side resistances R_i and R_r take into account the parasitic resistance of the inductors L_{inv} and L_{rec} respectively, but also the winding resistance of the transformer and any other resistive parasitic connected in series with the input and output voltage sources

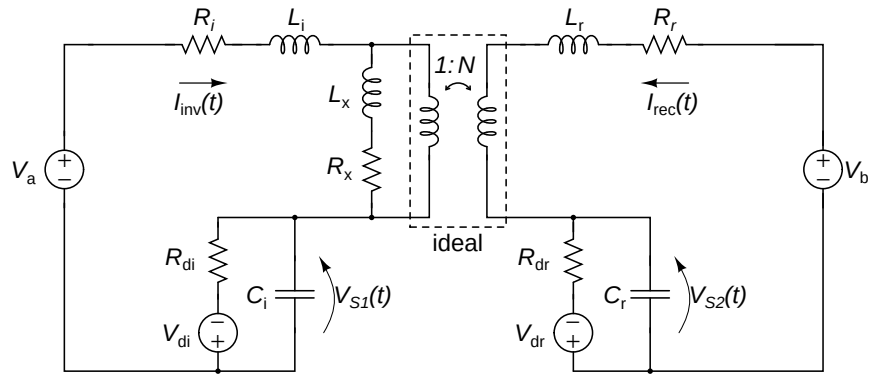
$$R_i = \omega_s \left(L_{inv}/Q_{L_{inv}} + L_p/Q_{L_p} \right) + R_{si}, \quad R_r = \omega_s \left(L_{rec}/Q_{L_{rec}} + L_s/Q_{L_s} \right) + R_{sr}.$$

Primary and secondary side KVLs are updated as follows

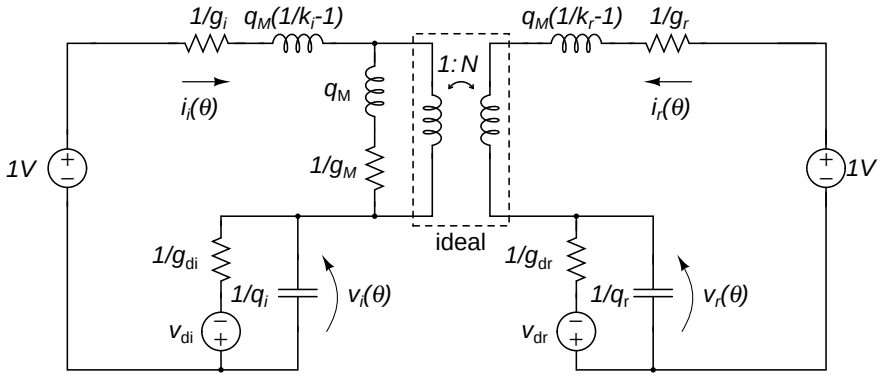
$$\begin{cases} (L_{inv} + L_p)\, \dfrac{dI_{inv}(t)}{dt} \pm M\, \dfrac{dI_{rec}(t)}{dt} + R_i\, I_{inv}(t) \pm R_M\, I_{rec}(t) + V_{S1}(t) - V_a = 0 \\ \pm M\, \dfrac{dI_{inv}(t)}{dt} + (L_{rec} + L_s)\, \dfrac{dI_{rec}(t)}{dt} \pm R_M\, I_{inv}(t) + R_r\, I_{rec}(t) + V_{S2}(t) - V_b = 0 \end{cases} \tag{3.38}$$

Equations for both primary and secondary resonant switches are written explicitly from (3.36)

$$\begin{cases} C_i R_{di} \dfrac{dV_{S1}(t)}{dt} - R_{di} I_{inv}(t) + V_{S1}(t) + V_{di} = 0 \\ C_r R_{dr} \dfrac{dV_{S2}(t)}{dt} - R_{dr} I_{rec}(t) + V_{S2}(t) + V_{dr} = 0 \end{cases} \tag{3.39}$$



(a)



(b)

Figure 3-5: Lossy class-E converter equivalent circuit (a) before and (b) after normalization.

Then, similarly to the lossless methodology, both (3.38) and (3.39) are normalized dividing the first equation by V_a and the second by V_b. Introducing also the same normalized state variables (3.2) and dimensionless design variables (3.6) one gets a new **fourth order ODE system describing the lossy converter behavior**.

$$\begin{cases} \dfrac{q_M}{k_i}\dfrac{di_i(\theta)}{d\theta} + q_M\dfrac{di_r(\theta)}{d\theta} + i_i(\theta)/g_i + \dfrac{q_M}{Q_M}\,i_r(\theta) + v_i(\theta) - 1 = 0 \\ q_M\dfrac{di_i(\theta)}{d\theta} + \dfrac{q_M}{k_r}\dfrac{di_r(\theta)}{d\theta} + \dfrac{q_M}{Q_M}i_i(\theta) + i_r(\theta)/g_r + v_r(\theta) - 1 = 0 \\ \dfrac{1}{q_i}\dfrac{dv_i(\theta)}{d\theta} - i_i(\theta) + g_{di}(Z_i)\,(v_i(\theta) + v_{di}(Z_i)) = 0 \\ \dfrac{1}{q_r}\dfrac{dv_r(\theta)}{d\theta} - i_r(\theta) + g_{dr}(Z_i)\,(v_r(\theta) + v_{dr}(Z_i)) = 0 \end{cases} \tag{3.40}$$

with $g_i = R_a/R_i$, $g_r = R_b/R_r$. Notably, going the quality factor Q_M and the conductances g_i, g_r, g_{di}, g_{dr} to infinity the equations in (3.40) can be reduced to the lossless system in (3.9).

Furthermore, it is important to stress that the equivalent voltages $v_{di,r}(Z_i)$ and conductances $g_{di,r}(Z_i)$ of the resonant switches change zone by zone to account for different circuit configurations but, interestingly, after including the non-idealities in the circuit model, the converter evolution is always described by a fourth order ODE system

$$\mathbf{x}'(\theta) = \mathbf{A}\mathbf{x}(\theta) + \mathbf{b} \tag{3.41}$$

in the four state variables $\mathbf{x}(\theta) = (i_i(\theta),\ i_r(\theta),\ v_i(\theta),\ v_r(\theta))^\intercal$. The eigenvalues and eigenvectors of the matrix $\mathbf{A}$ determine the nature of the solution in the different zones, which is reported with more details in Appendix C. Similarly to the procedure presented for the lossless case, the state variables evolution can be drawn zone by zone and a piecewise solution in the entire clock period is simply obtained imposing the state variables continuity at each switching instant and computing the coefficients c_1, c_2, c_3 and c_4 from the initial conditions.

HRi Zone ($\theta_{prev} < \theta < \theta_{next}$):

In this zone the primary side switch is off and the corresponding equivalent circuit is the one depicted in Figure 3-4(a). The primary side current is all flowing through the parallel of the resonant capacitor C_i with its parasitic resistance $R_{C_i} = \omega_s\, C_i\, Q_{C_i}$, hence

$$v_{di}^{HRi} = 0,\ g_{di}^{HRi} = R_a/R_{C_i}$$

On the contrary, the secondary side diode is on and it is modeled with the circuit in Figure 3-4(c). If the series resistance of the diode ${R_D}^{ON}$ is very small compared to the impedance of the parallel resonant capacitor with its parasitic resistance $Z_{C_r} = (\omega_s C_r)^{-1} /\!\!/ R_{C_r} \approx (\omega_s C_r)^{-1}$, like in the most of the cases, then the rectifying current is mainly flowing through the diode and $v_r(t) \approx -{v_D}^{ON} = -{V_D}^{ON}/V_b$. Anyway, in general

$$v_{dr}^{HRi} = {v_D}^{ON} R_{C_r} / \left(R_{C_r} + {R_D}^{ON}\right),\ g_{dr}^{HRi} = R_b / \left(R_{C_r} /\!\!/ {R_D}^{ON}\right) \tag{3.42}$$

The detailed computation of the evolution can be found in (C.7). The end of the zone can be detected when the rising voltage ${v_r}^{(1)}(\theta)$ becomes greater than a diode threshold $-{v_D}^{ON}$ causing the diode to turn-off. However, depending on the amount of losses introduced in the circuit, it is also possible that this instant comes after the turn-on of the primary side switch at $\theta_M = 2\pi(1-D)$. Consequently, the end condition for Z_1 can be expressed as

$$\theta_{next} = min\left(\theta_M, {\theta_D}^{OFF}\right) \tag{3.43}$$

with ${\theta_D}^{OFF} = \theta > \theta_{prev} \,|\, {v_r}^{(1)}(\theta) = -{v_D}^{ON}$.

FR Zone ($\theta_{prev} < \theta < \theta_{next}$):

Here both MOS primary switch and diode at the secondary side are turned-off. All the primary and secondary side currents are flowing through resonant capacitors C_i and C_r respctively, and the equivalent model for both devices is the one in Figure 3-4(a).

Then,

$$v_{di}^{FR} = 0,\ g_{di}^{FR} = R_a/R_{C_i} = R_a/\left(\omega_s\, C_i\, Q_{C_i}\right) \tag{3.44}$$

$$v_{dr}^{FR} = 0,\ g_{dr}^{FR} = R_b/R_{C_r} = R_b/\left(\omega_s\, C_r\, Q_{C_r}\right). \tag{3.45}$$

The solution of the system in fully resonant conditions is computed in (C.8). The zone ends once the first switching device is turned-on. The MOS switch is externally turned on at $\theta_M = 2\pi(1-D)$ while diode turns on when the reverse voltage $v_r(\theta)$ falls below $-{v_D}^{ON}$. Hence,

$$\theta_{next} = min\left(\theta_M, {\theta_D}^{ON}\right) \tag{3.46}$$

with ${\theta_D}^{ON} = \theta > \theta_{prev} \,|\, {v_r}^{(2)}(\theta) = -{v_D}^{ON}$.

HRr Zone ($\theta_{prev} < \theta < \theta_{next}$):

This zone, which is complementary with respect to *HRi*, is characterized by a conducting MOS switch at the primary side and a high-impedance secondary side. If the on-state resistance of the MOS switch is negligible with respect to the impedance $Z_{C_i} = (\omega_s C_i)^{-1} /\!\!/ R_{C_i} \approx (\omega_s C_i)^{-1}$ of the resonant capacitor C_i, then ${v_i}^{(3)}(\theta) \approx 0\ \forall\ \theta \in Z_3$. In any case the general equivalent model of the two resonant switches is

$$v_{di}^{HRr} = 0,\ g_{di}^{HRr} = R_a/\left(R_{C_i} /\!\!/ {R_{DS}}^{ON}\right) = R_a/\left(\left(\omega_s\, C_i\, Q_{C_i}\right) /\!\!/ {R_{DS}}^{ON}\right)$$

on the primary side while, being the diode on the secondary side off, the current flows all through the resonant capacitor C_r and

$$v_{dr}^{HRr} = 0,\ g_{dr}^{HRr} = R_b/R_{C_r} = R_b/\left(\omega_s\, C_r\, Q_{C_r}\right)$$

This zone ends at θ_3, when the voltage ${v_r}^{(3)}(\theta)$ turns negative and the diode is switched on before MOS turn-off, otherwise a new period begins at $\theta = 2\pi$. Mathematically it can be written as

$$\theta_{next} = min\left(2\pi, {\theta_D}^{ON}\right) \tag{3.47}$$

with ${\theta_D}^{ON} = \theta > \theta_{prev} \,|\, {v_r}^{(3)}(\theta) = -{v_D}^{ON}$.

LIN Zone ($\theta_{prev} < \theta < \theta_{next}$):

Here both switching devices are on and the equivalent circuit parameters to put in the expression of **A** are

$$v_{di}^{LIN} = 0,\ g_{di}^{LIN} = R_a / \left(R_{C_i} /\!/ {R_{DS}}^{ON}\right)$$

$$v_{dr}^{LIN} = {v_D}^{ON} R_{C_r} / \left(R_{C_r} + {R_D}^{ON}\right),\ g_{dr}^{LIN} = R_b / \left(R_{C_r} /\!/ {R_D}^{ON}\right).$$

Solution for this zone is given in (C.6). Finally, the ending of this zone actually depends on two possible events: MOS turn-off at $\theta = \theta_4 = 2\pi$ and diode turn-off when secondary side voltage reaches the diode threshold. Therefore, the next instant of converter evolution is computed as

$$\theta_{next} = min\left(2\pi, {\theta_D}^{OFF}\right) \tag{3.48}$$

with ${\theta_D}^{OFF} = \theta > \theta_{prev} \,|\, {v_r}^{(4)}(\theta) = -{v_D}^{ON}$. Additionally, once the time domain evolution for all zones is drawn, the steady state behavior can be computed repeating this procedure periodically with updated initial conditions at $\theta = \theta_0$ until a stop criterion is detected.

Similarly to the lossless system previously described, imposing the values of D, k_i, k_r, steady-state constraint on state-variables

$$\|(\Delta i_i,\ \Delta i_r\ \Delta v_i,\ \Delta v_r)\| < \varepsilon, \tag{3.49}$$

with $\Delta v_i \triangleq v_i(2\pi) - v_i(0)$, $\Delta v_r \triangleq v_r(2\pi) - v_r(0)$, ZVS/ZVDS constraints (3.34)-(3.35) and output steady-state constraint (3.30), it is possible to numerically compute the optimum class-E operation design point of the system with losses.

Starting from the converter specifications such as V_{in}, V_{out} and P_{out}, once the design constants **k** have been chosen, for a given set of quality factors for both active devices and reactives, the proposed analysis and design methodology is summarized

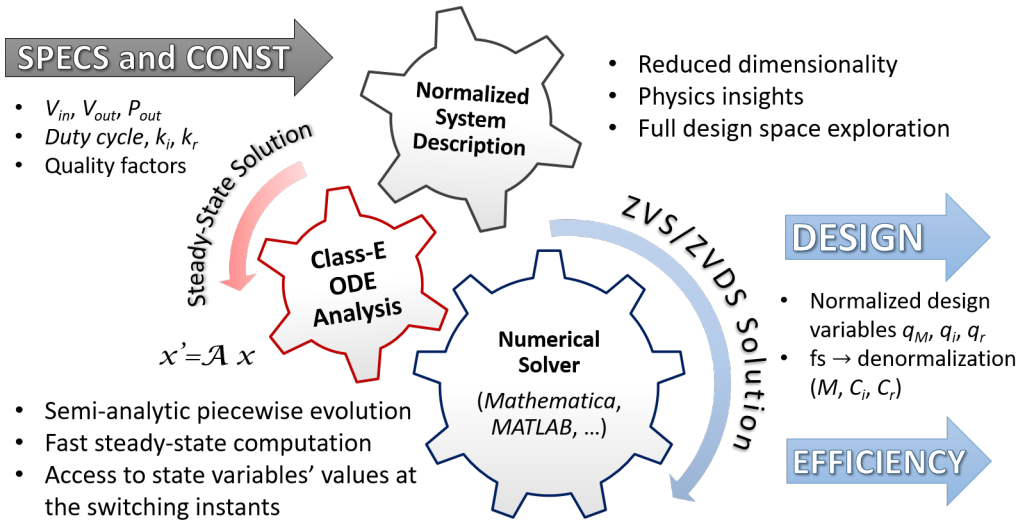


Figure 3-6: Class-E resonant converter dimensionless analysis and design approach

in the following three points, as also exemplified by Figure 3-6:

- Depending on the resonant network topology, differential equations for each converter switch configuration are written and organized in matricial form. They are subsequently normalized to find out the actual design space dimensionality. There are two main advantages derived from **normalization**: first, the normalizing equations give a phisics insight view of the relation between the dimensionless parameters and the real world values of inductances, capacitances, frequency, voltage and power; second, the reduced number of variables permits to extensively explore all the design space opening the way towards a broad variety of optimization opportunities.

- Then, each differential equation system is solved analytically, and the obtained solutions are used to build-up a piecewise **semi-analytical converter simulator**. The main difference with respect to a conventional circuit simulator like SPICE is that the circuit currents and voltages waveforms are not computed exploiting step-by-step numerical integration methods but, leveraging the analitically computed solutions, the state variables values must be actually evaluated only at the switching instants to link the solutions together. The

result is a much faster steady-state computation while still having the control of the state variables values at the switching instants to impose ZVS and ZVDS operating conditions. The related drawback is the lack of flexibility. In fact, if the converter resonant network topology is changed, new normalized equations and analytical solutions must be computed accordingly.

- Finally, recurring to any **numerical optimization tool** such as *MATLAB* or *Mathematica*, the semi-analytical converter evolution is iterated changing the values of $\mathbf{q}$ unitl

$$\left\| \left(v_i(\theta_2),\ i_i(\theta_2),\ \frac{1}{2\pi} \int_0^{2\pi}\ I_{C_L}(\theta)\, d\theta \right) \right\| < \varepsilon$$

  with ε arbitrarily small number (e.g. 1×10^{-6}). The last step is clearly denormalization of dimensionless design variables into real world quantities. In particular, from $\mathbf{q} = (q_M, q_i, q_r)$ the values of the resonant capacitors C_i and C_r are obtained along with the result of the product $f_s\, M\, P_{out}$. This means that only two between these factors can be freely chosen while the third must be computed to match the value of q_M.

The superior computation speedup achieved permits to repeat such a procedure exploring all possible values of the design constants $\mathbf{k}$ in a reasonable amount of time. Such an approach finally leads to the possibility to explore and compare a great amount of design solutions pursuing for improved system compactness or maximum conversion efficiency. In fact, once the average value of the input current $i_i(\theta)$ is known, also the **power section efficiency** can be accurately estimated during the numerical optimization process starting from the general definition (please note that gate driving losses will not be included)

$$\eta = \frac{P_{out}}{P_{in}} = \frac{V_{out}\, I_{out}}{V_{in}\, I_{in}} \tag{3.50}$$

which can be expanded in different ways depending on the topology considered: isolated/non-isolated buck-boost, buck or boost.

- For the **class-E isolated and non-isolated buck-boost converters**, since $I_{in} = \langle I_{inv}(t) \rangle = I_a \langle i_i(\theta) \rangle = P_{out}/V_a \langle i_i(\theta) \rangle$ and $V_a = V_{in}$,

$$\eta^{BB} = \frac{P_{out}}{V_{in} \dfrac{I_a}{2\pi} \displaystyle\int_0^{2\pi} i_i(\theta)\, d\theta} = \frac{2\pi}{\displaystyle\int_0^{2\pi} i_i(\theta)\, d\theta} = \frac{1}{\langle i_i(\theta) \rangle} \tag{3.51}$$

- for the **class-E boost converter**, being $I_{in} = \left\langle I_{L_p}(t) \right\rangle = I_a \langle i_i(\theta) \rangle + I_{out}$, $V_{in} = V_a$ and $V_{out} = V_a + V_b$, one obtains

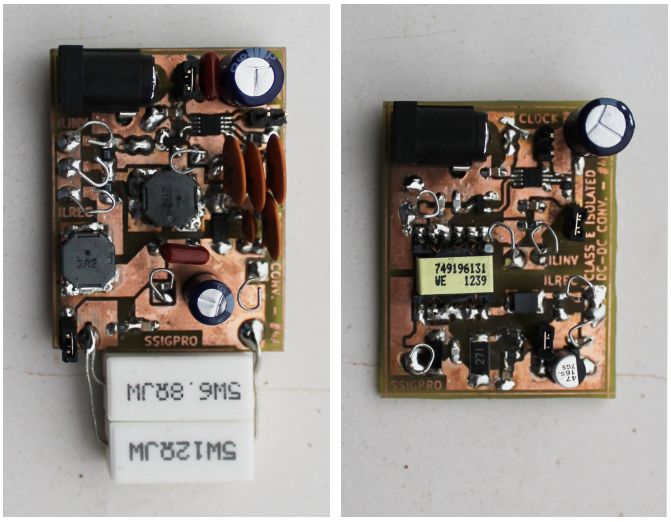
$$\begin{aligned} \eta^{BOOST} &= \frac{V_{out}\, I_{out}}{V_{in} \left(\dfrac{I_a}{2\pi} \displaystyle\int_0^{2\pi} i_i(\theta)\, d\theta + I_{out} \right)} = \\ &= \frac{V_a + V_b}{V_b \langle i_i(\theta) \rangle + V_a} = \frac{\xi + 1}{\langle i_i(\theta) \rangle + \xi} \end{aligned} \tag{3.52}$$

- for the **class-E buck converter**, since $I_{in} = \langle I_{inv}(t) \rangle = I_a \langle i_i(\theta) \rangle$ and $V_a = V_{in} - V_{out}$, then

$$\begin{aligned} \eta^{BUCK} &= \frac{P_{out}}{V_{in} \dfrac{I_a}{2\pi} \displaystyle\int_0^{2\pi} i_i(\theta)\, d\theta} = \\ &= \frac{V_a}{(V_a + V_b) \langle i_i(\theta) \rangle} = \frac{1}{(1 + 1/\xi) \langle i_i(\theta) \rangle} \end{aligned} \tag{3.53}$$

3.3 Design Examples and PCB Prototypes

The proposed modelling, analysis and design approach is validated through implementation and measurements of two dc-dc converters realized with off-the-shelves components. The first one has a non-isolated topology, a low switching frequency and it is built with low-quality inductors and capacitors. The second one is isolated, running at higher frequency and designed with high-quality reactive elements. The pictures of the two prototypes, whose design was firstly presented in **[34]**, are shown in Figure 3-7(a) and Figure 3-7(b), respectively. The design procedure is composed of two steps: the first design step (lossless) is performed neglecting any kind of loss



(a) (b)

Figure 3-7: Photograph of the designed prototypes. (a) 2.5 W non-isolated dc-dc converter; and (b) 500 mW isolated dc-dc converter.

in the circuit in order to get, with the help of the design curves of Figure 3-3, a first approximation of the component values, and consequently an indication of their parasitics. Then one takes into account all circuit non idealities (diode voltage drop, inductor and capacitor quality factors *etc.*) and apply the lossy methodology to reach the final accurate design point. In both cases measurements perfectly match the expected theoretical results.

Design (C): Low-efficiency non-isolated buck-boost converter

Let us consider a 2.5 W non-isolated buck-boost converter, with $V_{in} = 5\,\mathrm{V}$ and $V_{out} = 3.3\,\mathrm{V}$, operating at approximately 500 kHz. The desired voltage ratio imposes $\xi \approx 1.5$ and, since only L_{rec} is implemented then $k_i = \xi$. The two additional degrees of freedom are set as $k_r = 0.5/\xi$ (i.e. $L_p = L_{rec}$) and $D = 0.5$ (i.e., $\theta_2 = \pi$). If one initially assumes that all circuit elements are ideal, *i.e.*, $v_D^{ON} = 0$ and all quality factors equal to infinity, the design solution is exactly the one indicated with the marker "C" in Figure 3-3(a):

$$\begin{aligned} &\sqrt{k_i\,k_r} \approx 0.7, \quad \sqrt{k_i/k_r} \approx 2.1, \\ &q_M \approx 1.67,\ q_i \approx 1.1,\ q_r \approx 10. \end{aligned} \tag{3.54}$$

Then q_M, q_i, q_r can be denormalized using Equations (3.11) to get

$$L_p = L_{rec} = 3.47\,\mu\text{H},\ C_{inv} = 29.3\,\text{nF},\ C_{rec} = 6.46\,\text{nF}.$$

Given a first approximation of circuit elements values, it is possible to search for discrete components available and get a realistic indication of their parasitics. In order to validate the proposed circuit modelling and design methodology even for low efficiency converters, passive elements with very low quality factors at the desired operating frequency are chosen: $Q_{L_p} = Q_{L_{rec}} \approx 36$, $Q_C \approx 28$ (quality factor measurements with *Hewlett Packard 4284A Precision LCR Meter*). In order to simplify the circuit implementation, the converter is implemented with an N-MOS transistor separating the primary and the secondary grounds. Then, a IRLML0030TR transistor by International Rectifier, with $R_{DS}^{ON} \approx 27\,\text{m}\Omega$ and a DB24307 Schottky barrier diode from Panasonic with ${V_D}^{ON} \approx 0.3\,\text{V}$ and ${R_D}^{ON} \approx 30\,\text{m}\Omega$ were used. Finally, two $20\,\text{m}\Omega$ current sensing resistors have been added, one on the inverter and one on the rectifier branches. Exploiting the optimization capabilities inside the *Wolfram Mathematica* software, the lossy system dimensionless solution has been found

$$q_M = 1.37,\ q_i = 0.87,\ q_r = 4.54.$$

Remarkably, it is quite different with respect to its lossless counterpart (3.54), mainly due to the low quality factors of inductors and capacitors. This confirms how important is the consideration and the correct estimation of parasitics in this kind of converters. Denormalization leads to

$$L_p = L_{rec} = 2.85\,\mu\text{H},\ C_{inv} = 37.3\,\text{nF},\ C_{rec} = 16.1\,\text{nF}$$

In order to further simplify the converter implementation, the last degree of freedom given by the oscillation frequency is exploited, noticing that by slightly increasing f_s

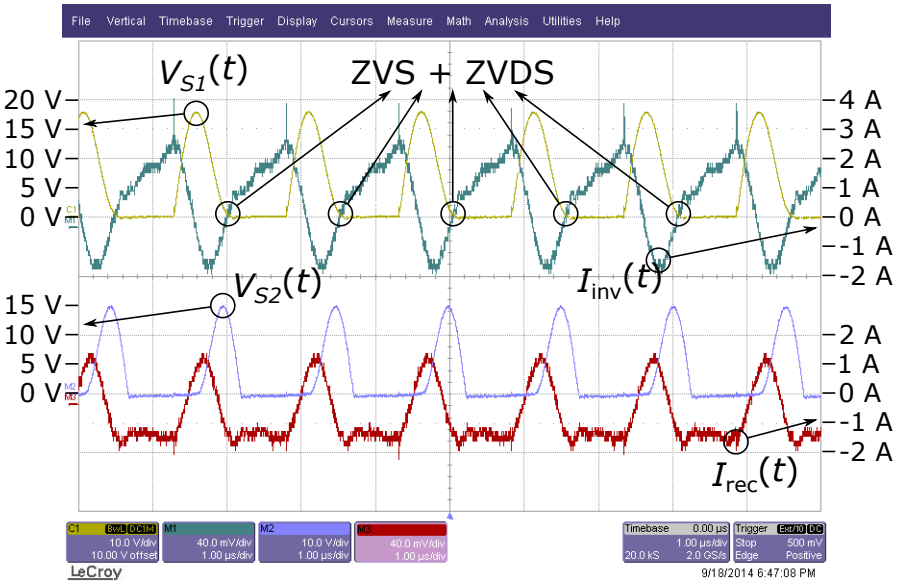


Figure 3-8: Measured current and voltage waveforms for the 2.5 W non-isolated dc-dc converter prototype showing almost perfect ZVS/ZVDS characteristics.

from 500 kHz to 650 kHz, one gets

$$L_p = L_{rec} \approx 2.2\,\mu\text{H},\ C_{inv} = 28.7\,\text{pF},\ C_{rec} = 12.4\,\text{pF}$$

In this way, two inductors with a standard commercial values for L_p and L_{rec} can be used, while $C_{inv} = 30\,\text{pF}$ and $C_{rec} = 12.2\,\text{pF}$ can be well approximated placing a few commercial capacitors in parallel.

Measurements, performed exploiting *Aim-TTi PL303-P Power Supply*, *Aim-TTi LCD 1705 Multimeter*, *LeCroy WaveSurfer WS 452* and *LeCroy WaveRunner WR 104 Xi-A*, show a very good matching with the expected results. Output voltage and current measured from the prototype are in the expected range ($V_{out} \approx 3.1\,\text{V}$ and $I_{out} \approx 680\,\text{mA}$). Also the measured efficiency (59%) agrees with the theoretical one (58%) computed accordingly to (3.51). The measured waveforms for $V_{S1}(t)$, $V_{S2}(t)$, $I_{inv}(t)$ and $I_{rec}(t)$ are plotted in Fig. 3-8, underlining a very good behavior in terms of both ZVS and ZVDS.

Design (D): High-efficiency isolated class-E converter

The second prototype is a 500 mW isolated dc-dc converter, with $V_{in} = 5\,\mathrm{V}$, $V_{out} = 12\,\mathrm{V}$, operating at approximately $f_s = 1\,\mathrm{MHz}$. Also a 1:2 (i.e. $N = 2$) transformer with in-phase coupled secondary side is considered. Being $\xi = V_{in}/V_{out} = 0.42$, if $L_{inv} = 0\,\mathrm{H}$ then k_i is given only by the transformer turn ratio and coupling coefficient $k_i = Nk\xi$. Differently, on the other side $k_r = NkL_p/\left(\xi(L_{rec} + N^2L_p)\right)$ is also influenced by the rectifying inductance L_{rec}. If the transformer considered features a very high coupling then $k_i \approx N\xi = 0.84$. As in the previous example, one can start with the assumption of ideal devices and $L_s = N^2L_p = L_{rec}$ (i.e. $k_r = k/\left(2\xi N\right) \approx 0.6$), that leads from Figure 3-3(a) (see marker "D") to

$$\begin{aligned} &\sqrt{k_i\,k_r} \approx 0.71, \quad \sqrt{k_i/k_r} \approx 1.2, \\ &q_M = 1.4,\ q_i = 1.46,\ q_r = 2.29 \end{aligned} \tag{3.55}$$

that is denormalized to

$$L_p = 13.5\,\mu\mathrm{H},\ L_{rec} = N^2L_p = 54\,\mu\mathrm{H},\ C_{inv} = 2.15\,\mathrm{nF},\ C_{rec} = 241\,\mathrm{pF}.$$

The best fit for commercial transformer is a $10.9\,\mu\mathrm{H}$ *WE-FLEX* transformer by Würth Elektronik, with coupling coefficient $k \approx 0.98$ and quality factor $Q_M \approx Q_{L_p} \approx Q_{L_s} \approx 45$. Consequently, a smaller value also for the inductor, i.e., $L_{\mathrm{rec}} = 33\,\mu\mathrm{H}$ with a quality factor $Q_{L_{rec}} \approx 47$, is used. Furthermore $k_i \approx 2 \times 0.98 \times 0.42 \approx 0.82$ and $k_r = \dfrac{2 \times 0.98}{0.42}\dfrac{10.9}{33 + 4 \times 10.9} \approx 0.66$. In this prototype ceramic capacitors with C0G dielectric are considered, ensuring extremely high performance ($Q_C > 1000$) so that an almost infinite quality factor can be assumed. The same N-MOS of the previous example is used, while the rectifying diode chosen for this prototype is a ES1B by Vishay, with $V_D^{ON} \approx 0.7\,\mathrm{V}$ and $R_D^{ON} \approx 3\,\Omega$. Finally, the design is completed with two current sensing resistors, a $0.1\,\Omega$ at the primary side and a $5.1\,\Omega$ at the secondary side. With the help of *Mathematica* the new solutions, accounting for all circuit losses

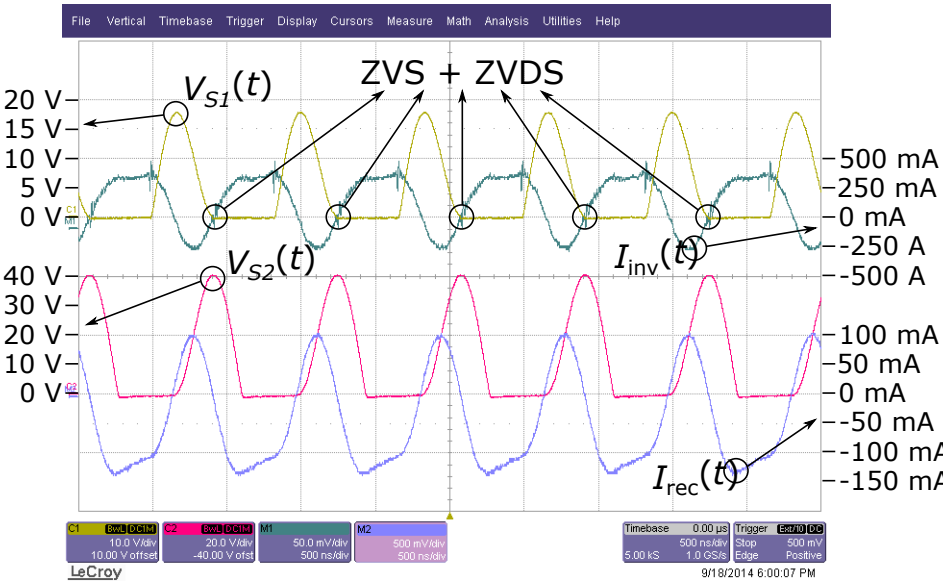


Figure 3-9: Measured current and voltage waveforms for the 500 mW isolated dc-dc converter prototype showing almost perfect ZVS/ZVDS characteristics..

modeled, have been computed:

$$q_M = 1.38,\ q_i = 1.29,\ q_r = 1.35 \tag{3.56}$$

Due to the high quality factor of the components used, the new solution is not very far from the lossless design in (3.55), which is suitably used as a starting point for the numerical optimization. Then, by slightly increasing the operating frequency to $f_s = 1.22\,\text{MHz}$, (3.56) is denormalized as

$$L_p \approx 10.9\,\mu\text{H},\ L_{rec} \approx 33\,\mu\text{H},\ C_{inv} \approx 2\,\text{nF},\ C_{rec} \approx 335\,\text{pF}$$

With the same setup used with the previous prototype, a new set of measurement are performed on this new board. Output voltage $V_{out} = 11.8\,\text{V}$ and output current $I_{out} = 40.3\,\text{mA}$, with a 75% efficiency, are very similar to the theoretically expected ones (12.0 V, 41.7 mA, 77%). Measured converter waveforms are plotted in Fig. 3-9. Also in this case the ZVS/ZVDS matching with respect to expected theoretical results is extremely good, proving the excellent performance of the proposed methodology for both designing and predicting the performance of a resonant power stage.

Conclusion

The new analysis and design approach presented in this chapter represents an exceptional breakthrough with respect to the state-of-the-art resonant converter design techniques, which are mostly based on strongly simplifying assumptions, since:

- it allows to **simplify the converter topology** and remove reactive elements that are not strictly necessary for the resonant operation;
- it can be **applied to several isolated and non-isolated class-E topologies** and can be easily extended to other resonant converters sharing the same resonant network;
- it dramatically **reduces the design time** providing a high accuracy solution that doesn't need to be refined with additional circuital simulations;
- it takes into account the main circuit non-idealities giving a **very good approximation of the conversion efficiency** achievable;
- the dimensionless analysis allows a **comprehensive design space exploration** giving the possibility to straightforwardly find the optimization path based on design specifications and technological constraints;
- it can be leveraged to rapidly test the feasibility of more "fancy" circuital solutions such as the implementation of a **power line communication technique to transfer power and data within the same isolation channel** as it will be explained in the next chapter.

Chapter 4

Isolated Bi-directional Communication Channel

Galvanic isolation is often required in many power conversion systems, especially those for industrial and safety-critical applications such as telecommunications and medical equipment. Additionally, dc-dc converters providing isolated output power benefit designers who need isolated gate drivers or noise reduction in analog circuitry. Some applications, such as sensors for industrial process monitoring and testing, where high voltages, magnetic fields and noise are commonly present, also demand for reliable isolated data links capable of **sending information across the isolation barrier**. Furthermore, an isolated data channel is always required for isolated power supplies with primary side feedback control [35].

The conventional approach is to use independent interfaces for power and data transfer. While transformers are always the preferred solution for power conversion, the data interface can be implemented with optocouplers, extra pulse micro-transformers, or high-voltage capacitors, as sketched in Figure 4-1.

The main benefits of **optical coupling** are that light is inherently immune to external electric or magnetic fields, and optocoupling allows for transfer of steady-state information. The disadvantages include speed limitations (which depend on how quickly the LED can turn on and off), power dissipation (up to 10 mA of input current for high-speed digital transfers), and the degradation of the LED over time, which may

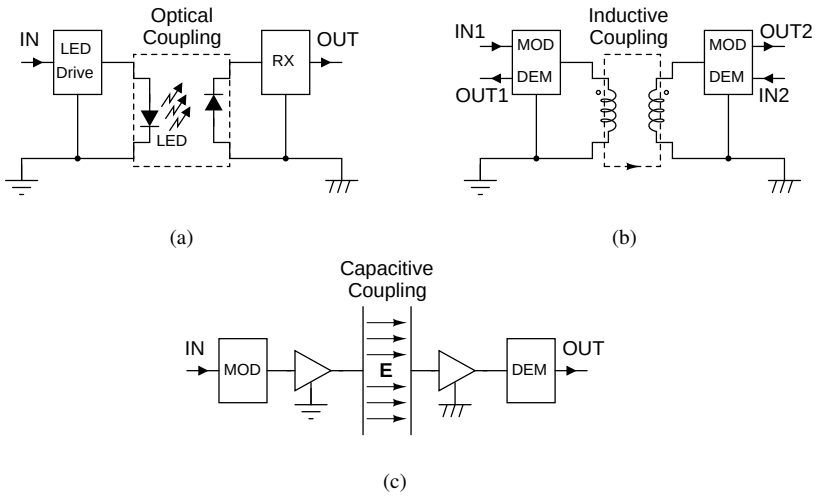


Figure 4-1: Conventional data isolation techniques (a) optocoupling, (b) inductive coupling and (c) capacitive coupling.

lead to no longer functional coupling [36]. Despite these drawbacks, optical coupling has been the leading isolation techinque for the last decades in many applications ranging from telecommunications to robotics and power conversion systems.

In the last years, both **inductive and capacitive coupling** are replacing optoisolators in the most of commercial products and solutions thanks to their superior efficiency and reliability. The former, despite its susceptibility to external magnetic fields, with careful transformer design, allows common-mode noise rejection, while the latter enables cost-effective integrated isolation circuits. In both cases, almost 100% power efficiency can be achieved and there is no performance degradation over time. The main concern is that both inductive and capacitive coupling pass signals within a certain range of frequencies and amplitudes with tolerable distortion and proper signal processing is required to keep the signal within the usable bandwidth.

There are already several products on the market that include both isolated power and data inside a single-package solution, such as the *ISOpro* family of digital isolators from Silicon Laboratories (capacitive isolation) [37], the *isoPower* micro-transformer technology developed by Analog Devices [38, 39, 40] (protected by patents [41, 42, 43]) and the RS232 transceiver from Linear Technology (coupled inductors) [44], but all of them exploit separate isolation devices for power and data.

Only a couple of works in the literature tried to address the problem of Power Line Communication (PLC) between the two sides of an isolated power converter. The first of them implements a bidirectional communication strategy in a full-bridge converter changing the switching phase of the bridge at the primary side to transmit a forward data stream and introducing an impedance modulator circuit on the secondary side for backward communication [45]. The second one exploits switching frequency modulation and output voltage amplitude modulation to send bidirectional data in an isolated PWM gate driver [46]. Surprisingly, it seems that no work has been published about power line communication in isolated resonant converters yet.

The purpose of this last part of the thesis is to leverage the analysis and design methodology introduced in the previous chapter to develop a novel power line communication technique to be exploited in resonant converters with **minimal impact in terms of size/cost** and negligible power efficiency degradation. The proposed solution is capable of sending **high-rate bidirectional data** across the same isolation barrier used for power transfer. Since it doesn't require neither dedicated isolation devices nor additional signal processing to adapt the data stream to the bandwidth of the isolation channel, the overall system compactness and reliability can be greatly improved with respect to currently available industrial solutions.

4.1 Operating Principle

The converter topology considered is an isolated resonant class-E with 1:1 in-phase coupling where only the seondary side inductance L_{rec} is implemented. The proposed communication architecture is the same for both forward (i.e. primary to secondary) and backward (i.e. secondary back to primary) communication and it is depicted in Figure 4-2. It consists in adding two switched capacitors C_f and C_b, in parallel to C_{inv} and C_{rec} respectively, that are attached or detached every clock cycle depending on the bit to transmit. Hence, there is no need for signal conditioning but the PAM bitstream signal can be directly applied to the gate of the auxiliary MOSFETS used to modulate the total capacitance value. The resulting change in converter voltage

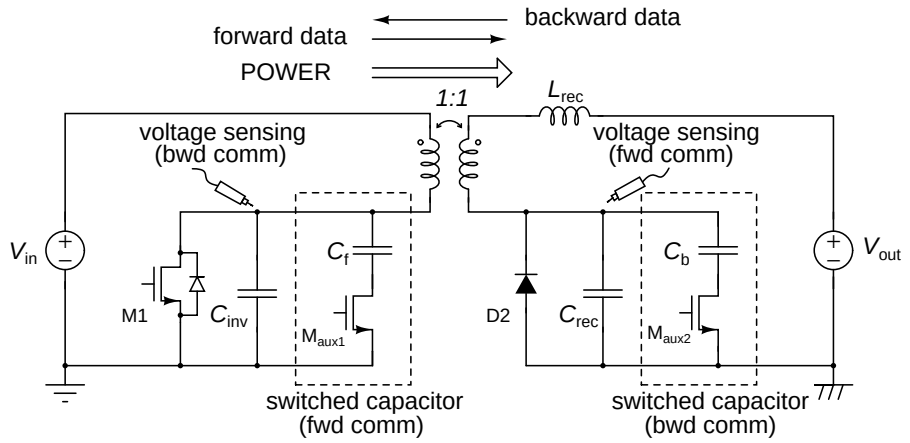


Figure 4-2: Schematic of the proposed isolated class-E converter implementing a bi-directional PLC scheme

waveforms can be detected at the opposite side of the transformer with properly designed sensing circuits to recover the original data stream.

Unfortunately, in such a system data and power transfer are not orthogonal mechanisms but they mutually influence each other, so some concerns arise:

- The datastream transmission alters the converter normal behavior. If the converter configuration is changed every clock cycle to achieve high-rate (1 bit/cycle) transmission capability, it never reaches the steady state and both ZVS and ZVDS conditions cannot be perfectly met. Furthermore, also the amount of power delivered to the load is strongly influenced by the datastream being transmitted.

- The converter behaves like a channel with memory that may be incompatible with 1 bit/cycle data transmission. In fact, the values of the state variables of the circuit at the beginning of each period depend on the bits previously transmitted and some bit sequences could be critical for the receiver.

Consequently, it is of fundamental importance to develop a design strategy in order to cleverly administrate the **trade-off between power conversion efficiency and communication performance**.

The proposed design approach is summarized as follows:

- The equivalent dimensionless circuit model and analysis methodology presented in the previous chapter are extended to monitor the converter **state variables evolution across multiple switching periods** when the resonant capacitor values are changed accordingly to the bitstream to be transmitted.

- The **memory of the system** m must be estimated and a suitable bitsequence to be used in the design phase has to be identified to account for all possible combinations of bits with length $m+1$.

- **Resonant capacitor values** C_{inv}, C_{rec}, C_f and C_b must be accurately designed in such a way that:

  - the converter is still able to deliver the desired amount of power to the output with negligible performance degradation with respect to an equivalent class-E converter without communication capabilities and

  - the families of waveforms obtained for "0" and "1" bit transmission are clearly separated (*open eye pattern*), accordingly to the sensing strategy chosen, proving the robustness with respect to circuit parameters spread and noise variations.

4.2 Modeling

In order to describe the communicating class-E converter, the dimensionless model developed in Chapter 3 must be updated as follows:

- At the beginning of each period analysis the value of primary and secondary capacitances is changed accordingly to the bit to transmit and the direction (i.e. backward or forward) of the datastream. Then, the associated dimensionless variables q_i and q_r are redefined as follows:

$$q_i\left(B_k^{FWD}\right) = \begin{cases} q_{i1}, & \text{if } B_k^{FWD} \text{ is "0"} \\ q_{i1} /\!/ q_{i2}, & \text{if } B_k^{FWD} \text{ is "1"} \end{cases} \tag{4.1}$$

$$q_r\left(B_k^{BWD}\right) = \begin{cases} q_{r1}, & \text{if } B_k^{BWD} \text{ is “0”} \\ q_{r1} /\!\!/ q_{r2}, & \text{if } B_k^{BWD} \text{ is “1”} \end{cases} \tag{4.2}$$

with

$$q_{i1} = \frac{1}{\omega_s R_a C_{inv}}, \quad q_{r1} = \frac{1}{\omega_s R_b C_{rec}}$$
$$q_{i2} = \frac{1}{\omega_s R_a C_{inv2}}, \quad q_{r2} = \frac{1}{\omega_s R_b C_{rec2}}$$

The value of C_{inv2} and C_{rec2} can be computed under a first harmonic approximation as

$$C_{inv2} = \frac{C_f}{1 + (\omega_s R_m C_f)^2}, \quad C_{rec2} = \frac{C_b}{1 + (\omega_s R_m C_b)^2} \tag{4.3}$$

where R_m is the sum of the on-resistance of the auxiliary MOS that connect and disconnect the switched capacitors and the parasitic series resistance of the switched capacitor itself, that can be computed from the quality factor Q_C as

$$R_{Cs} = \frac{1}{\omega_s C Q_C} \tag{4.4}$$

Under the same hypotheses also the equivalent parallel resistances can be approximated as

$$\begin{aligned} R_{C_i} &= (\omega_s C_{inv} Q_{C_{inv}}) /\!\!/ B_k^{FWD} \left(R_m + \frac{1}{\omega_s^2 R_m C_f^2}\right), \\ R_{C_r} &= (\omega_s C_{rec} Q_{C_{rec}}) /\!\!/ B_k^{BWD} \left(R_m + \frac{1}{\omega_s^2 R_m C_b^2}\right) \end{aligned} \tag{4.5}$$

In order to avoid backward-to-forward and forward-to-backward interference, bidirectional communication is obtained by time-division multiplexing (**half-duplex**) following the scheme reported in Figure 4.2. During the backward communication slot capacitors C_{inv} and C_f on the primary side are connected in parallel while the secondary side capacitor C_b is connected and disconnected depending on the sequence of bits to transmit. Similarly, during forward communication, capacitor C_b is kept connected to the circuit while the bitstream

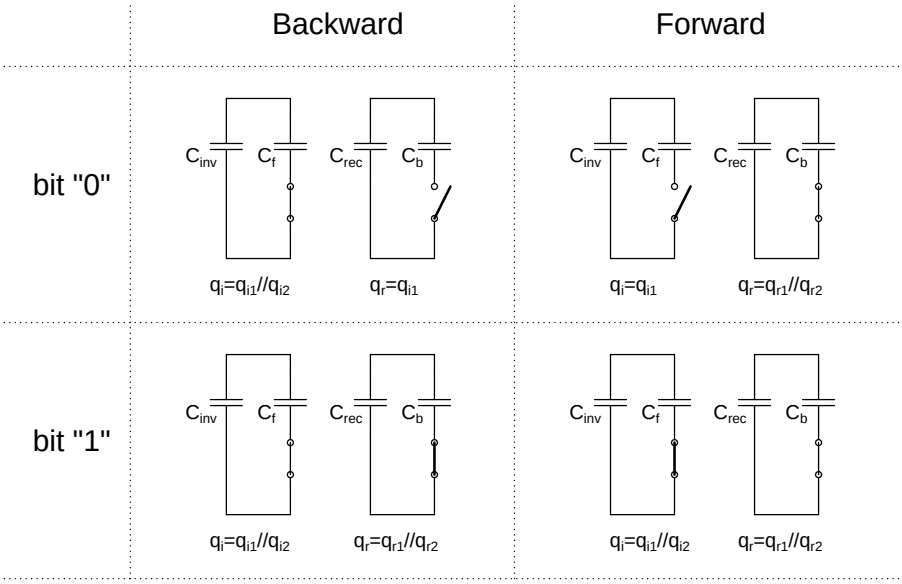


Figure 4-3: Bidirectional communication switching configurations

controls the configuration of the capacitor C_f on the primary side.

- During both backward and forward communication, the voltage $V_{S1}(t)$ can go negative turning on the body diode of M1 which conducts for a non-negligible amount of time before clock rising edge. This actually represents an **additional Half-Resonant zone**, referred to as *HRd*, that has to be modeled and introduced in the circuit analysis. Exploiting the model depicted in Figure 3-4(c), the equivalent Thevenin parameters are easily computed as follows

$$v_{di}^{HRd} = {v_D}^{ON} R_{C_i} / \left(R_{C_i} + {R_D}^{ON} \right), \; g_{di}^{HRd} = R_a / \left(R_{C_i} /\!/ {R_D}^{ON} \right) \tag{4.6}$$

- The **steady-state cannot be strictly reached** since the converter configuration is changed cycle by cycle. To overcome this limitation, the converter behavior is no more obtained iterating on a single circuit configuration but it is analyzed iterating an entire sequence of bits of given length L. This actually represents an extension of the concept of steady-state, where the matching of the initial conditions of the system at the beginning and at the end of such a

sequence have to be considered. As it will be explained in the next section, it is important to properly choose this **design sequence** in such a way that a theoretical converter model (considered for design purposes) transmitting such a sequence periodically represents a good approximation of the real converter behavior in actual operating conditions (infinite sequence of bits).

4.3 The Memory of the System

Since the transmitted bit is (potentially) changed every clock period k, steady state, i.e.

$$\mathbf{x}_k^0 = \left(i_i^{\,0},\ i_r^{\,0}\right)_k = \left(i_i(2\pi),\ i_r(2\pi)\right)_k ,$$

is never achieved cycle by cycle and all circuit waveforms in every switching period depend on:

- the system **initial conditions** $\mathbf{x}_k^0$, i.e. the state variables $i_i(\theta)$ and $i_r(\theta)$ at $\theta = 0$ (assuming that $v_i(0) \approx v_i(2\pi) \approx 0$ and $v_r(0) \approx v_r(2\pi) \approx -v_D^{ON}$), that can be straighforwardly represented in a two-dimensional space, and
- the **switched capacitor configuration** (i.e. the bit being transmitted).

Letting the system evolve for k switching periods with random bit transmission every clock cycle and collecting the initial conditions $\mathbf{x}_k^0$ at the beginning of each period a cloud of points can be obtained. The frontier $\overline{\mathbf{X}}^{\mathbf{0}}$ of a set of points obtained for $k \to \infty$ (excluding the first generated points which are biased by the starting conditions that can be out of $\overline{\mathbf{X}}^{\mathbf{0}}$) encloses all the possible initial conditions of the system and, the single period analysis function, described in the previous chapter, can be defined as

$$f_E\left(\mathbf{k},\mathbf{q}\right) : \mathbf{X^0}\left(\mathbf{k},\mathbf{q}\right) \longrightarrow \mathbf{X^0}\left(\mathbf{k},\mathbf{q}\right)$$

(with $\mathbf{X^0}$ representing the set enclosed by $\overline{\mathbf{X}}^{\mathbf{0}}$) which actually represents and extended definition of **steady state** for this kind of system. What is needed to analyze the converter behavior while communicating a bidirectional stream of bits is a bitsequence

of length L which is able to explore a representative discrete subset of $\mathbf{X^0}$, i.e.

$$\mathbf{\Omega} = \{\mathbf{D}_{(\mathbf{x}_k^0,\varepsilon)} | k = 1, ..., L\} \supset \mathbf{X^0} \tag{4.7}$$

where $\mathbf{D}_{(\mathbf{x}_k^0,\varepsilon)}$ is a closed disk of radius ε centered in $\mathbf{x}_k^0$.

Despite the fact that it is not the main focus of this work to examine in depth all these mathematical aspects, a rough estimation about how well a given sequence s_L can approximate the actual converter behavior is computed comparing the discrete set of initial conditions X_L^0 generated by s_L with another discrete set X_∞^0 obtained with a very large number of random bits to get an estimation of ε as

$$\varepsilon = \sup_i \ \{\inf_k \{\mathrm{d}_{ik}|\ k = 1, ..., K \to \infty\} \, | i = 1, ..., L\} \tag{4.8}$$

with d_{ik} representing the euclidean distance between a point in X_L^0 with another point in X_∞^0. For a sufficiently small value of ε the bitstream s_L is representative of the entire behavior of the power-line communicating converter and the memory of the system is estimated as $m_\varepsilon \approx L - 1$. Obviously a trade-off between ε and L exists: the smaller L (faster computation) the bigger ε (worse approximation), the bigger L (slower computation) the smaller ε (better approximation).

A useful choice to generate a bitstream s_{L-1}, with $L = 2^l$, is to consider the maximum length sequence (MLS or *m-sequence*) generated by a linear feedback shift register (LFSR) of length l. Such a sequence is periodic and it is the shortest that contains all the possible combinations of l bits, except the all-zero vector. For this reason it is particularly useful to characterize the behavior of the communicating converter under study without requiring too much computational effort (good trade-off betwee L and ε), as highlighted in Figure 4-4 for a 5-bit and a 8-bit Galois LFSR (GLFSR). A more detailed explanation about how to generate MLSs of different length is provided in Appendix D.

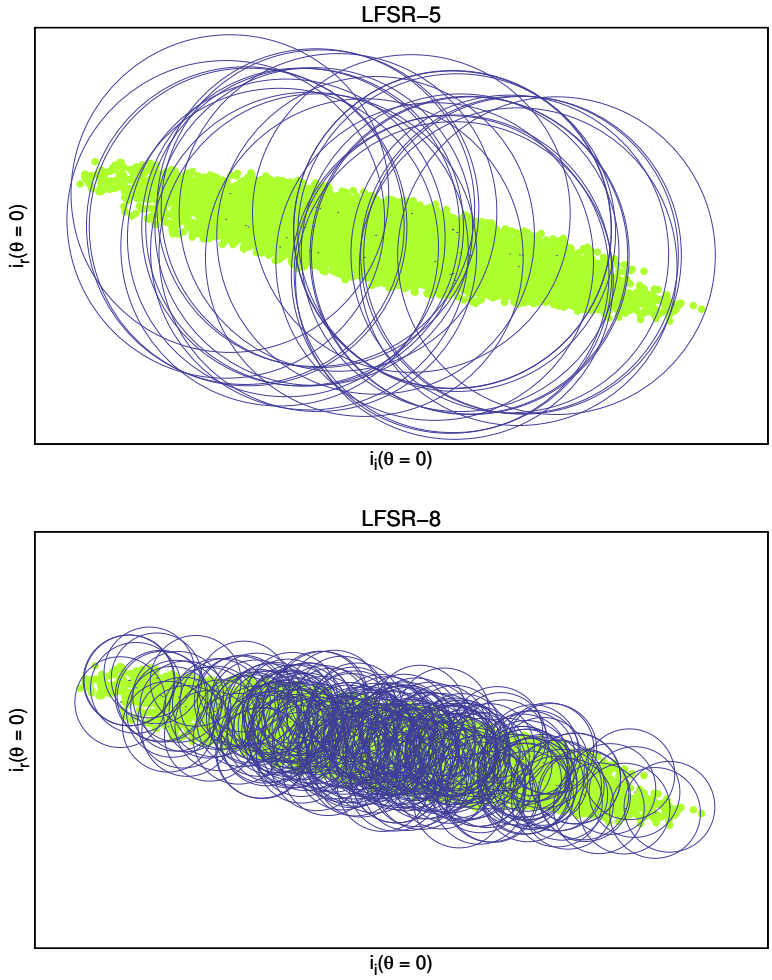


Figure 4-4: A 2D representation, computed with *Wolfram Mathematica*, of the state variables' initial conditions explored by a class-E isolated converter with backward communication (i.e. secondary side capacitance modulation) during normal operation. Green points: set of initial conditions X_∞^0 obtained with 10k random bits transmission, Blue lines: set of disks of radius ε centered in the initial conditions obtained transmitting a MLS generated with a GLFSR of length 5 (a) or 8 (b).

4.4 Backward Communication

Sending data in the opposite direction with respect to power flow is of great interest since it can be exploited in several ways, such as feedback control loop for load regulation or to collect data from an isolated sensor node which needs to be also powered-up.

4.4.1 Working Principle

The proposed approach to implement such a backward communication channel is to connect (or disconnect) an additional resonant capacitor C_b in parallel with C_{rec} at the secondary side every clock cycle during the conducting phase of the rectifying diode. In this way, the behavior of the converter is not altered until the diode switch-off, when the secondary side current starts flowing through the resonant capacitor(s) and the primary side voltage waveform $v_i(\theta)$ changes accordingly, as sketched in Figure 4-5(a). Once a threshold voltage v_{th} is opportunely chosen in such a way that

$$-v_D^{ON} \leq v_{th} < 0 \tag{4.9}$$

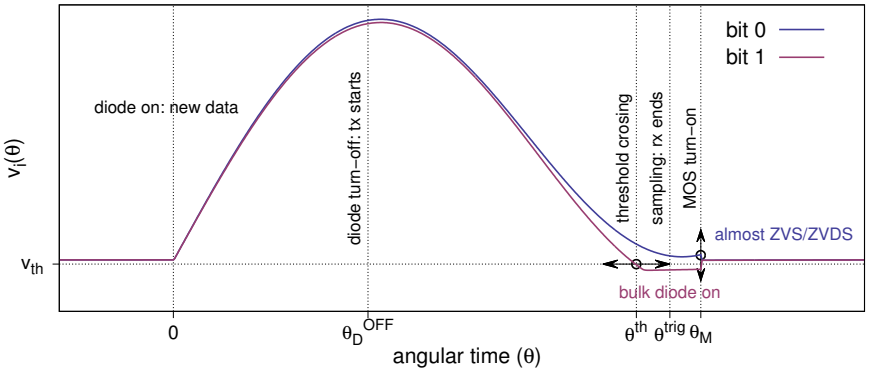
then also a threshold crossing time can be defined for each period k as

$$\theta_k^{th} = \begin{cases} \theta_M = 2\pi(1-D), & \text{if } \{\theta \in]0, \theta_M[\mid v_i(\theta) \leq v_{th}\} = \varnothing \\ \inf\left[\{\theta \in]0, \theta_M[\mid v_i(\theta) \leq v_{th}\}\right], & \text{otherwise} \end{cases} \tag{4.10}$$

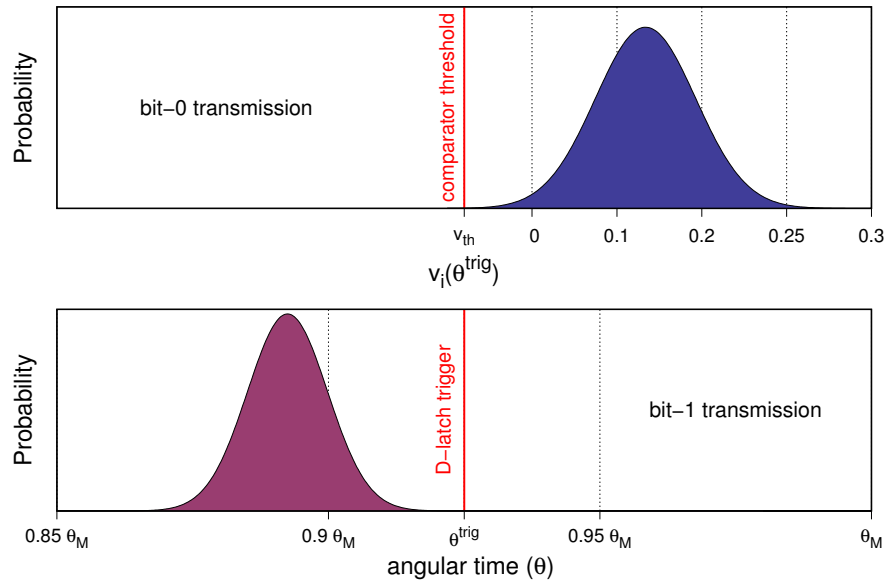
and the received bit can be decided based on the following rule

$$B_k^{BWD} = \begin{cases} 0, & \text{if } \theta^{trig} < \theta_k^{th} \leq \theta_M \\ 1, & \text{if } \theta_k^{th} \leq \theta^{trig} < \theta_M \end{cases} \tag{4.11}$$

where θ^{trig} represents the sampling instant. Roughly speaking, when the "0" bit is transmitted (C_b is left disconnected) the voltage $v_i(\theta)$ should not cross the zero-volt level and the optimal class-E operation (i.e. ZVS and ZVDS) is almost preserved.



(a)



(b)

Figure 4-5: Backward communication waveshaping. (a) Typical $v_i(\theta)$ voltage waveforms: if "0" is sent the ZVS/ZVDS behavior is almost preserved, while for "1" transmission the antiparallel bulk diode turns-on setting $v_i(\theta) \approx -v_D^{ON}$. (b) Spreading of the sampled voltage $v_i(\theta^{trig})$ and the angular time crossing instant θ^{th} due to the memory of the system.

Differently, when the "1" bit is transmitted (capacitor C_b connected to the circuit), after diode turn-off the voltage $v_i(\theta)$ at the primary side goes down with significant slope until it becomes negative first crossing the voltage threshold v_{th} and then turning on the body diode of M1. Subsequently, the voltage is forced to $-v_D^{ON}$ (Zone *HRd* starts) until the MOS is turned-on at $\theta = \theta_M$. This actually produce an unwanted power loss due to the diode conduction and a trade-off exists between the achievable conversion efficiency and the robustness of the communication technique.

4.4.2 Circuit Design

The design of the backward communicating class-E converter starts from the conventional converter solution (i.e. without communication capabilities) obtained following the methodology presented in Chapter 3. A statistical estimation of the converter evolution is then obtained simulating the periodic transmission of a MLS of bits and changing the values of the the dimensionless variables q_i, q_{r1} and q_{r2} (i.e. $C_{inv} + C_f$, C_{rec} and C_b) to impose the desired statistical characteristics. Assuming that the variables $v_i(\theta^{trig})$ and θ^{th} are Gaussian distributed with mean μ_0, μ_1 and standard deviation σ_0, σ_1 respectively, the new design constraints can be expressed as follows:

- slightly positive voltage switching for **"0" bit transmission**

$$\mu_0 - \gamma\,\sigma_0 \geq v_{th}, \quad \gamma \geq 1 \tag{4.12}$$

- threshold crossing time sufficiently before MOS turn-on for **"1" bit transmission**

$$\mu_1 + \sigma_1 \leq \rho\,\theta_M, \quad \rho < 1 \tag{4.13}$$

Finally, the values of the threshold voltage v_{th} and the trigger instant θ^{trig} must be properly set to ensure correct bitstream reconstruction at the receiver side.

It is worth noting that the computation of the switched capacitors values is a critical task, especially for C_b: if it is taken too small then the time window $[\mu_1 + \sigma_1, \theta_M]$ will become too narrow for sensing, but also a very big value would be a

problem because it will cause the voltage $v_i(\theta)$ to become negative even for "0" bit transmission. However, if this trade-off is carefully handled, two desirable features can be observed:

- two families of waveforms can be clearly distinguished in the last part of the first-half period just before MOS turn-on (*open eye pattern*), making possible to straightforwardly implement the sensing circuitry and correctly receive the transmitted bits;

- the soft-switching operation is mostly preserved and still very good preformance in terms of power efficiency is ensured.

4.4.3 Bit Error Probability

To evaluate the Bit Error Probability (BEP), one needs to consider the "0" bit and the "1" bit transmission separately, as outlined in Figure 4-5(b). For the former, we focus on the distribution of the noramlized drain-to-source voltage $v_i(\theta)$ at the sampling instant θ^{trig}, which should be always greater than the threshold voltage v_{th} (drawn as a red line). A first approximation of the error probability when "0" is transmitted is given by:

$$P_{eBWD}^{1|0} = P\left[v_i(\theta^{trig}) < v_{th} \,|\, B_k^{BWD} = 0\right] \approx \frac{1}{2}\,\mathrm{erfc}\left(\frac{\mu_0 - v_{th}}{\sqrt{2}\sigma_0}\right) \tag{4.14}$$

In the other case, one needs to consider the distribution of the angular time θ^{th} at which $v_i(\theta)$ crosses the threshold v_{th}. The probability of wrong detection when "1" is transmitted can be estimated as

$$P_{eBWD}^{0|1} = P\left[\theta_k^{th} > \theta^{trig} \,|\, B_k^{BWD} = 1\right] \approx \frac{1}{2}\,\mathrm{erfc}\left(\frac{\theta^{trig} - \mu_1}{\sqrt{2}\sigma_1}\right) \tag{4.15}$$

Finally, combining (4.14) and (4.15), the probability of wrong detection for backward communication is obtained, under the hypothesis to have equal probability that a "0"

Table 4.1: Forward Communication Decoding Rule

B_{k-1}^{FWD} / $\mathbf{B_k^{FWD}}$	**0**	**1**
0	Nominal: $\Theta_k \approx 2\pi$	Long: $\Theta_k > \tau_2 > 2\pi$
1	Short: $\Theta_k < \tau_1 < 2\pi$	Nominal: $\Theta_k \approx 2\pi$

or a "1" is sent, as

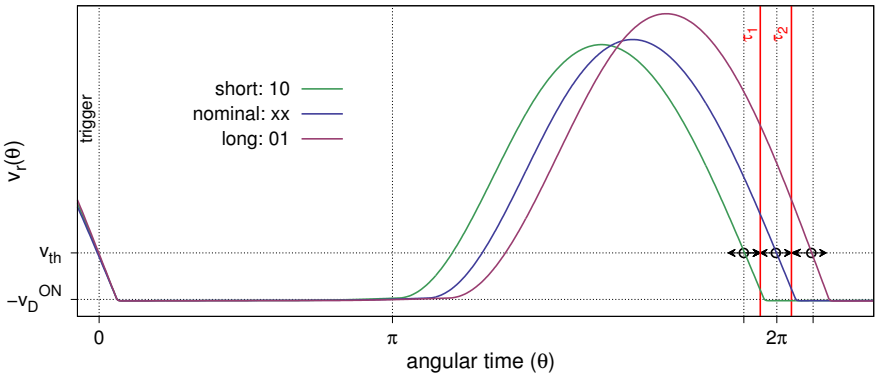
$$P_{eBWD} = P_{eBWD}^{1|0}\, P\left[B_k^{BWD} = 0\right] + P_{eBWD}^{0|1}\, P\left[B_k^{BWD} = 1\right] \approx \\ \approx \frac{1}{4}\left[\text{erfc}\left(\frac{\mu_0 - v_{th}}{\sqrt{2}\sigma_0}\right) + \text{erfc}\left(\frac{\theta^{trig} - \mu_1}{\sqrt{2}\sigma_1}\right)\right] \tag{4.16}$$

4.5 Forward Communication

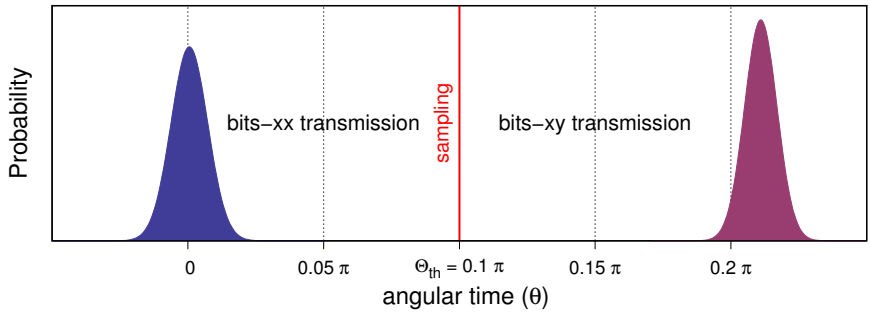
Sending high-rate information in the same direction as power could be exploited in several ways, such as for real-time configuration and updating of isolated sensor nodes in industrial process monitoring.

4.5.1 Working Principle

Similarly to backward communication, data can be easily sent from the primary to the secondary side of the converter adding a switched capacitor C_f in parallel to C_{inv}. In this case, during the on-state of the main MOS device, C_f is connected to the circuit when the bit "1" is transmitted or it is left floating if the bit to send is "0". The most visible effect is a **cycle-to-cycle jitter** of the clock signal recovered at the secondary side from the diode reverse voltage $v_r(\theta)$, as depicted in Figure 4-6. Defined, for each clock cycle k, the **angular time distance $\mathbf{\Theta_k}$** of the recovered clock rising edge ($v_r(\theta)$ falling edge) with respect to the the same rising edge in period $k-1$, then the new received bit B_k^{FWD} is retrieved knowing the value of B_{k-1}^{FWD} and applying the decision rule in Table 4.1. The relationship between the transmitted and the received data stream is inherently differential: if the bit is equal to the previously transmitted



(a)



(b)

Figure 4-6: Forward communication secondary side period length modulation. (a) Typical $v_r(\theta)$ voltage waveform: if the current bit is equal to the previously transmitted one then the period is the nominal one (i.e. 2π), otherwise it can be shorter (if the last two bits are "10") or longer ("01"). (b) Period length distributions of $\Delta\Theta_k = \text{Abs}\left[\Theta_k - 2\pi\right]$ showing a clear separation between the two cases and the optimum threshold Θ_{th} standing in the middle.

one then the period detected at the secondary side should be the nominal one (i.e. 2π), while if it is different the measured period can be either smaller or greater than 2π. In both case the main MOS bulk diode can conduct for a non-negligible amount of time before gate rising edge causing an undesirable power loss.

4.5.2 Bi-directional Communication Circuit Design

The design of a bidirectional communicating class-E converter can be achieved starting from the design of the circuit with backward communication only and then computing how to conveniently split the primary side resonant capacitance into a fixed part C_{inv} and a switching part C_f.

Under the hypothesis that $\Delta\Theta_k = \mathrm{Abs}\left[\Theta_k - 2\pi\right]$ is distributed with two Gaussian density functions, with mean μ_{xx}, μ_{xy} and standard deviation σ_{xx}, σ_{xy} respectively, the forward communication design consists in ensuring a sufficient separation between them, i.e.

$$(\mu_{xy} - \sigma_{xy}) - (\mu_{xx} + \sigma_{xx}) \geq \phi\,\pi, \quad 0 < \phi < 1 \tag{4.17}$$

Finally, the capacitor dimensionless design variables q_{i1}, q_{i2}, q_{r1} and q_{r2} are tuned all together to ensure that the desired amount of power is delivered to the load under **GLFSR-l backward/forward half-duplex operation**

$$\langle i_r(\theta) \rangle \,|_{[0,2L\pi]} - 1 = 0 \tag{4.18}$$

Administrating the trade-off between the constraints (4.12), (4.13), (4.17), (4.18), the power loss due to non-perfect ZVS at the primary side and larger RMS currents due to the non-steady-state operation it is possible to obtain very good communication performance with negligible efficiency drop $(3 - 4\%)$.

4.5.3 Bit Error Probability

In order to compute the forward communication BEP, the distribution of the recovered clock period length, sketched in Figure 4-6(b), is considered. Particularly, the current

normalized angular period $\Delta\Theta_k$ must be compared with a suitably defined threshold $\Theta_{th} = 2\pi - \tau_1 = \tau_2 - 2\pi$ and the extimation of erroneous detection can be expressed as follows

$$P_{eFWD}^{xx|xy} = P\left[\Delta\Theta_k < \Theta_{th} | B_k^{FWD} = xy\right] \approx \frac{1}{2}\text{erfc}\left(\frac{\mu_{xy} - \Theta_{th}}{\sqrt{2}\sigma_{xy}}\right) \tag{4.19}$$

$$P_{eFWD}^{xy|xx} = P\left[\Delta\Theta_k > \Theta_{th} | B_k^{FWD} = xx\right] \approx \frac{1}{2}\text{erfc}\left(\frac{\Theta_{th} - \mu_{xx}}{\sqrt{2}\sigma_{xx}}\right) \tag{4.20}$$

where the bit pairs "xx" and "xy" indicate that the last transmitted/received bit is respectively equal or different in comparison to the previous one. The overall BEP considering both "0" and "1" bit transmission with equal probability is

$$\begin{aligned} P_{eFWD} &= P_{eFWD}^{xx|xy}\, P\left[B_k^{FWD} = xy\right] + P_{eFWD}^{xy|xx}\, P\left[B_k^{FWD} = xx\right] \approx \\ &\approx \frac{1}{4}\left[\text{erfc}\left(\frac{\mu_{xy} - \Theta_{th}}{\sqrt{2}\sigma_{xy}}\right) + \text{erfc}\left(\frac{\Theta_{th} - \mu_{xx}}{\sqrt{2}\sigma_{xx}}\right)\right] \end{aligned} \tag{4.21}$$

4.6 Circuit Implementation and Experimental Results

In order to validate the proposed bi-directional communication over power approach a PCB prototype has been designed and realized with off-the-shelf devices. The core of the system is a **1- MHz class-E isolated converter**, whose design is achieved following the procedure presented in Chapter 3. The converter specifications and design values are summarized in Table 4.2. Two **Tiva C LaunchPad Evaluation Boards** from *Texas Instruments*, running with an internal 80 MHz clock, are connected to the circuit and used as transmitter/receiver module for both backward and forward communication, as depicted in Figure 4-7. The primary side Tiva (**A**), powered-up with the common input voltage V_{in}, generates the main system clock V_g at 1 MHz and, depending on the current time slot, (a) generates an output bitstream signal V_{tx}^{FWD} to drive the gate of M_{aux1} (forward communication) or (b) samples the output of the backward communication receiver (V_{rx}^{BWD}). Similarly, the secondary

Table 4.2: Power section specifications and device values

Specifications	
$V_{in} = 5\,\mathrm{V}$, $V_{out} = 5\,\mathrm{V}$, $P_{out}^{MAX} = 1.2\,\mathrm{W}$, $f_s = 1\,\mathrm{MHz}$	
Semiconductor Devices	
Main MOS	$R_{DS}^{ON} = 40\,\mathrm{m\Omega}, \quad C_{oss} \approx 120\,\mathrm{pF}$
Rect. Diode	$V_D^{ON} = 0.7\,\mathrm{V}, \quad R_D^{ON} = 300\,\mathrm{m\Omega}, \quad C_j \approx 100\,\mathrm{pF}$
Aux MOS	$R_{DS}^{ON} = 2\,\Omega, \quad C_{oss} \approx 6\,\mathrm{pF}$
Magnetic Components	
Transformer	$Lp = 8.5\,\mu\mathrm{H}, \quad N = 1, \quad k = 0.98, \quad Q_{L_p} \approx Q_M \approx 45$
Rect. Inductor	$L_{rec} = 3.3\,\mu\mathrm{H}, \quad Q_{L_{rec}} \approx 50$
Resonant Capacitors	
Primary side	$C_{inv} = (2.7 + 2)\,\mathrm{nF}, \quad C_f = 2\,\mathrm{nF}$
Secondary side	$C_{rec} = (1.5 + 1.5 + 1.5)\,\mathrm{nF}, \quad C_b = 2\,\mathrm{nF}$

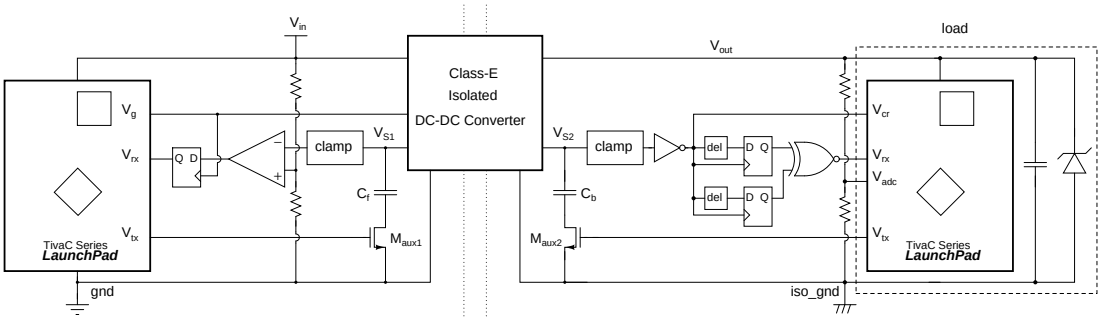


Figure 4-7: Simplified PCB schematic showing the connections between the dc-dc converter power sections, the switched capacitors needed to send backward and forward data, the clock recovery and the sensing circuits and the *Tiva C Launchpads* used to generate the stream of bits to be transmitted.

side Tiva (**B**), supplied by the isolated output voltage V_{out} of the dc-dc converter, (a) takes a recovered clock signal V_{cr} as input and synchronously (b) generates a backward bitstream signal V_{tx}^{BWD} to drive the gate of $\mathrm{M2_{aux2}}$ or (c) samples the output of the forward communication receiver (V_{rx}^{FWD}). Furthermore, it monitors the supplied voltage V_{out} (opportunely scaled) and exploits the backward communication capabilities to implement **on-off (burst-mode) load regulation**.

4.6.1 Backward Communication

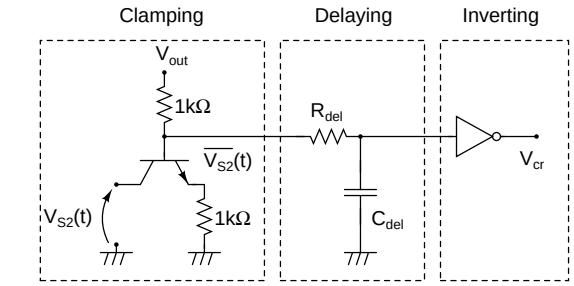
Starting from the dimensionless solution of the converter without communication capabilities ($q_i = 1.34$, $q_r = 1.67$) the new values of $q_i = q_{i1} /\!\!/ q_{i2}$, q_{r1} and q_{r2} must be found to satisfy the constraints (4.12) and (4.13). Recurring to numerical optimization, for a steady-state converter transmitting a GLFSR-7 backward sequence and setting $\theta^{trig} = \theta_M = \pi$, $v_{th} = -v_D^{ON}$, $\gamma = 2$, $\rho = 0.45$ (5% of the period), $\phi = 0.1$ (5% of the period), the following result is found

$$q_i^{BWD} = 2.85, \;\; q_{r1}^{BWD} = 1.85, \;\; q_{r2}^{BWD} = 5.27, \tag{4.22}$$

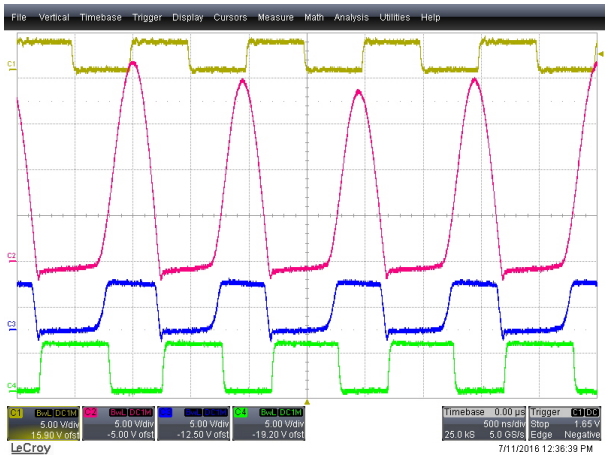
which can be easily denormalized as

$$C_{inv}^{BWD} \approx 2.7\,\mathrm{nF}, \; C_{rec}^{BWD} \approx 4.1\,\mathrm{nF}, C_b^{BWD} \approx 1.4\,\mathrm{nF}. \tag{4.23}$$

In order to send a synchronous backward data stream a clock signal is needed also on the isolated side. A straightforward way to retrieve it from the resonant waveforms available at the rectifier side is to clamp the cathode-to-anode voltage across the diode. The clamping circuit implemented, depicted in Figure 4-8, is made of a NPN bipolar junction transistor and two $1\,\mathrm{k\Omega}$ resistors. When the voltage $V_{S2}(t)$ is lower than the supply voltage V_{out} (used for powering-up all the circuitry) both the base-collector and base-emitter junctions are forward biased (saturation mode) and the voltage $\overline{V_{S2}(t)}$ resembles $V_{S2}(t)$ except for a $0.6 - 0.7\,\mathrm{V}$ amplitude shift due to the base-collector forward voltage drop V_{BC}^{ON}. Conversely, when $V_{S2}(t)$ becomes higher



(a)



(b)

Figure 4-8: Implemented clock recovery circuitry. (a) Circuit schematic (b) Measured waveforms. Yellow: primary side gate signal $V_g(t)$ (clock reference); Red: secondary side diode reverse voltage $V_{S2}(t)$; Blue: clamped voltage $\overline{V_{S2}}(t)$; Green: recovered clock signal $V_{cr}(t)$

than V_{out}, while the base-emitter junction is still forward biased, the base-collector one is now reverse biased and the transistor operates in the forward-active mode. Consequently, the voltage at the output of the clamping circuit can be expressed as follows:

$$\overline{V_{S2}}(t) = \begin{cases} V_{S2}(t) + V_{BC}^{ON} & \text{if } V_{S2}(t) + V_{BC}^{ON} \leq V_{out} \\ V_{out} & \text{if } V_{S2}(t) + V_{BC}^{ON} > V_{out} \end{cases} \tag{4.24}$$

Since we want the transmitted data to change on the rising edge of the clock signal when the diode is already turned on, it is useful to insert an RC delay circuit (to ensure that the diode is fully turned on when the capacitor is switched) followed by an inverter. The obtained clock signal is used as input for the Synchronous Serial Interface (SSI) module of the *TM4C123GH6PM* microcontroller embedded on the *Tiva B* device, whose output direcly drives the gate of $\mathrm{M_{aux2}}$.

On the receiver side, the sensing strategy for retrieving the backward transmitted bitstream from the voltage $V_{S1}(t)$ is shown in Figure 4-9. It involves the same clamping circuit used for clock recovery, followed by an analog comparator and a D-latch. Here, the clamping circuit architecture plays a key role in adapting the voltage $V_{S1}(t)$ to become suitable as input for the comparator. All the sensing circuitry is powered-up with the input voltage V_{in} and the clamped waveform can be expressed as:

$$\overline{V_{S1}}(t) = \begin{cases} V_{S1}(t) + V_{BC}^{ON} & \text{if } V_{S1}(t) + V_{BC}^{ON} \leq V_{in} \\ V_{in} & \text{if } V_{S1}(t) + V_{BC}^{ON} > V_{in} \end{cases} \tag{4.25}$$

Assuming that the forward voltage of the base-collector junction is almost equal to the forward voltage of the MOSFET body diode (i.e $V_{BC}^{ON} \approx V_{D}^{ON}$), the voltage $\overline{V_{S1}}(t)$ is in the range $[0 - V_{in}]$. When the transmitted bit is "1", the clamped voltage goes below $V_{th} \approx 0.3\,\mathrm{V}$, the comparator output V_{cmp}, which is normally low, is asserted high and it is then sampled by the D-latch at the rising edge of the clock signal V_{trig}. After that, when the main clock signal V_g goes high, turning-on the main MOS switch, $V_{S1}(t)$ is forced to zero so $\overline{V_{S1}} > V_{th}$ and the comparator output is reset (*Return To Zero*). Otherwise, if the bit "0" is sent, the clamped voltage remains higher than V_{th},

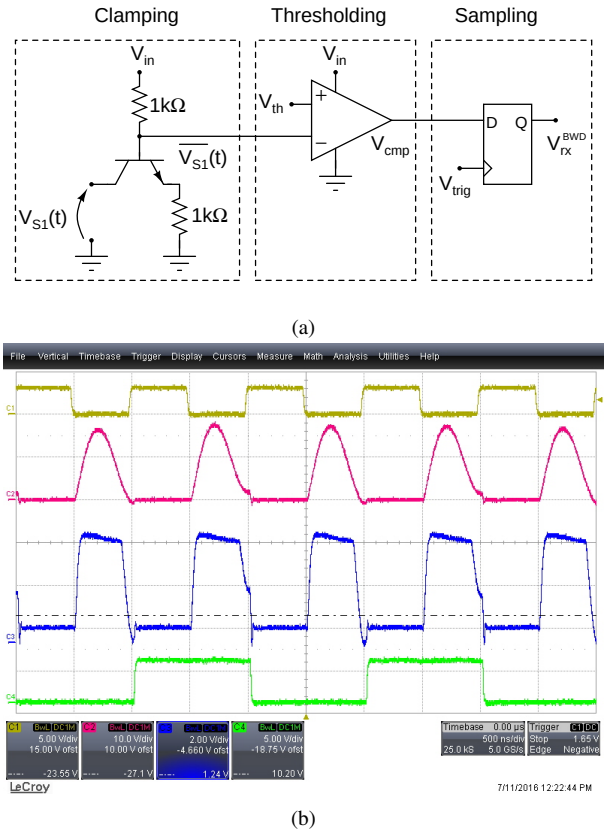


Figure 4-9: Implemented backward communication receiver. (a) Circuit schematic (b) measured waveforms. Yellow: primary side gate signal $V_g(t)$ (clock reference); Red: main MOS drain-to-source voltage $V_{S1}(t)$; Blue: clamped voltage $\overline{V_{S1}}(t)$; Green: received bitstream $V_{rx}^{BWD}(t)$

and no output pulse is generated by the analog comparator.

The backward communicating system has been firstly simulated applying the proposed methodology with a sequence of 10000 random bits, allowing to estimate by fitting the parameters $\mu_0 = 0.134$, $\sigma_0 = 0.059$, $\mu_1 = 2.804$ and $\sigma_1 = 0.023$ (obtained with a worst case approximation of $v_{th} = V_{th}/V_{in} = -v_D^{ON} = -0.08$ and $\theta^{trig} = \theta_M = \pi$) and computing the expected backward bit error probability as $\mathrm{E}[P_{eBWD}] < 0.7 \times 10^{-4}$. Secondly, the implemented system has been tested comparing the received bitstream with the ground truth sent to the same *Tiva A* by means of an optocoupler. The real-time comparison of the two streams is made in software and after an error is detected a LED status is changed. Observing the system running for more than 17 minutes no errors have been detected in nominal working conditions (i.e. $\mathbf{P_{eBWD} < 10^{-9}}$).

4.6.2 Bi-directional Communication

Once computed the values of q_i, q_{r1} and q_{r2} for backward communication, what is left is to determine how to conveniently split $q_i = q_{i1}\, q_{i2} / (q_{i1} + q_{i2})$ in order to satisfy the constraint (4.17) and make forward communication work properly. The main intent is to obtain two period length distributions which are separate enough to allow a correct reconstruction of the transmitted bitstream at the secondary side. Additionally, under the hypothesis that the converter is continuously switching between backward and forward communication time slots during normal operation, the desired amount of average power must be still delivered to the load. Starting from the values computed in (4.22), the circuit design is re-optimized considering a **16-bit packet interleaved half-duplex transmission of a GLFSR-7 stream both in backward and forward direction** to ensure that constraints (4.12), (4.13), (4.17) and (4.18) are all simultaneously satisfied. The new computed parameters are

$$q_{i1}^{BiDIR} = 1.95, \quad q_{i2}^{BiDIR} = 3.96, \quad q_{r1}^{BiDIR} = 1.69, \quad q_{r2}^{BiDIR} = 3.91, \tag{4.26}$$

which lead to the following capacitor values

$$\begin{aligned} C_{inv}^{BiDIR} &\approx 3.9\,\text{nF},\ C_{f}^{BiDIR} \approx 2\,\text{nF}, \\ C_{rec}^{BiDIR} &\approx 4.5\,\text{nF},\ C_{b}^{BiDIR} \approx 2\,\text{nF}. \end{aligned} \tag{4.27}$$

In order to retrieve the forward transmitted data stream the period of the recovered clock signal V_{cr} obtained with the circuit of Figure 4-8 should be measured and compared with two reference periods of length $T_{1,2} = (1 \mp \Theta_{th}/(2\pi))\,T_s$ every clock cycle. The decoding algorithm can be straightforwardly implemented with two delay lines followed by two D-latches and a logic XNOR gate, as shown in Figure 4-10. If the current V_{cr} rising edge comes more than T_1 seconds but less than T_2 seconds after the previous rising edge then the latch L1 samples a logic "1" while the latch L2 samples a logic "0". In such a case the output of the XNOR gate V_{Δ} is a logic "0" which means that the currently transmitted bit is equal to the previous one. In the other two cases, i.e. when the current bit is changed with respect to the last transmitted one, L1 and L2 both sample the same logic value, then the output of the receiver is a logic "1". Finally, starting from a guess on the first transmitted bit, all the following can be computed as

$$B_k^{FWD} = \left(B_{k-1}^{FWD} + V_{\Delta}\right)_{\%2} \tag{4.28}$$

where $(\cdot)_{\%2}$ is the modulo-2 operator. Bit error rate measurements show that also forward communication is perfeclty working under nominal conditions ($\mathbf{P_{eFWD} < 10^{-9}}$).

4.6.3 ON-OFF Control

One of the main concerns in isolated power converters is how to implement the feedback control loop. The proposed power line communication strategy offers a unique opportunity to exploit a single transformer to get both power transfer and a feedback communication channel. In order to demonstrate the applicability of such a solution, a simple communication protocol has been implemented in both *Tiva B transmitter*

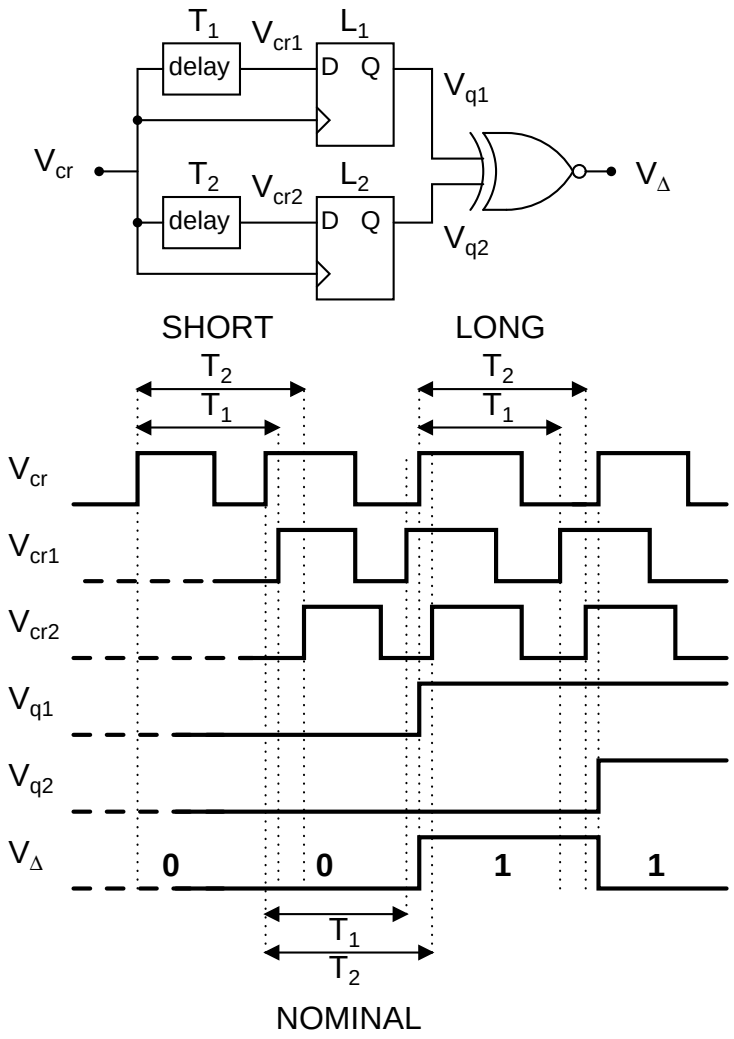


Figure 4-10: Schematic and characteristic waveforms of the proposed forward communication receiver.

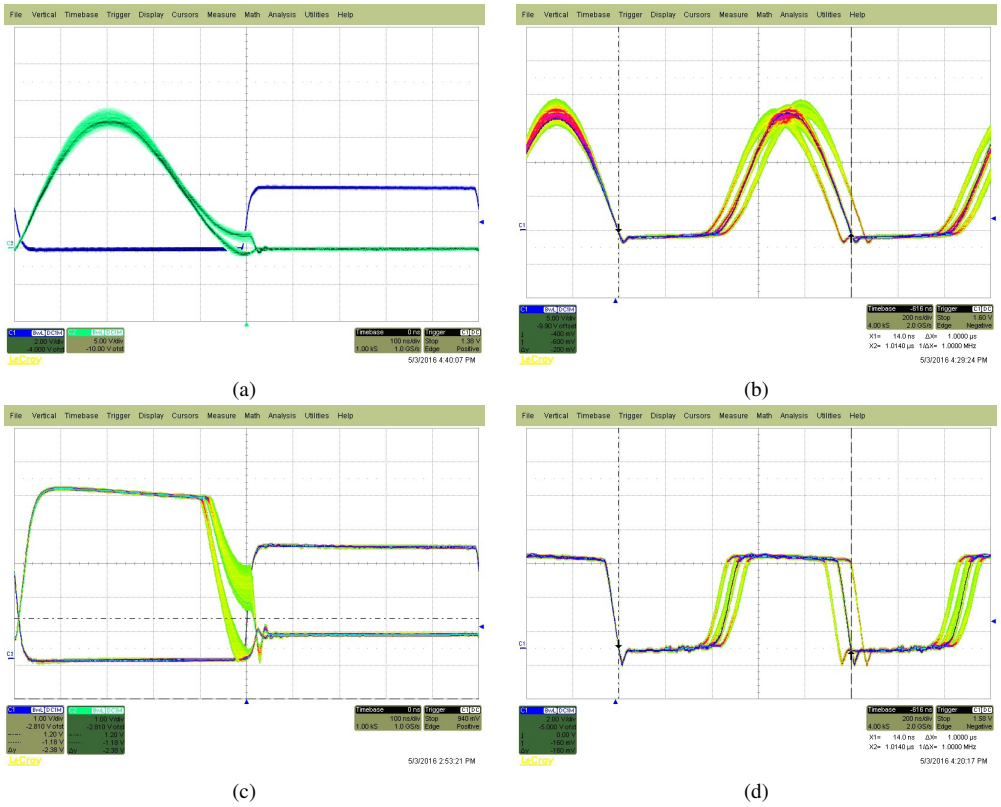
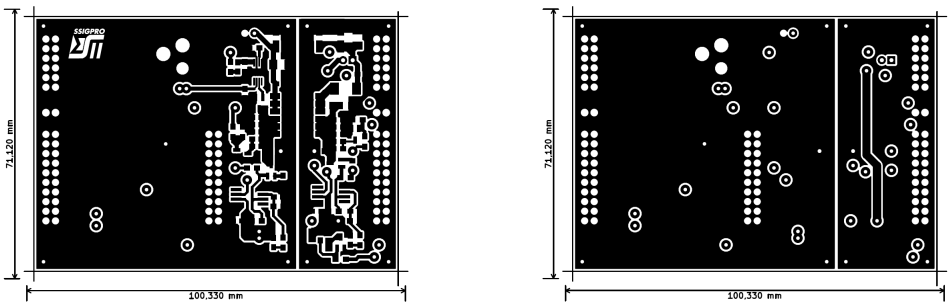


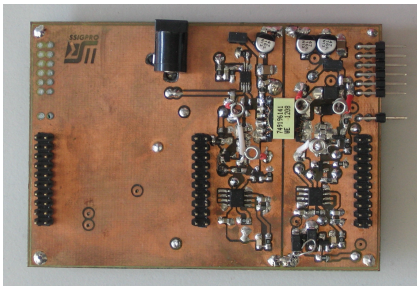
Figure 4-11: Oscilloscope waveforms showing how converter waveforms are modulated to obtain backward and forward communication capabilities. (a) Primary side MOS drain-to-source voltage $V_{S1}(t)$ and clock signal; (b) Secondary side diode reverse voltage $V_{S2}(t)$ triggered on the first falling edge; (c) voltage $V_{S1}(t)$ after clamping, comparator threshold v_{th} (dashed line) and clock signal; (d) clamped diode reverse voltage $V_{S2}(t)$ triggered on the first falling edge.

Figure 4-12: Class-E converter with backward communication channel used to regulate the output voltage. Yellow: main clock signal V_g showing on-off converter modulation; Red: regulated output voltage V_{out}

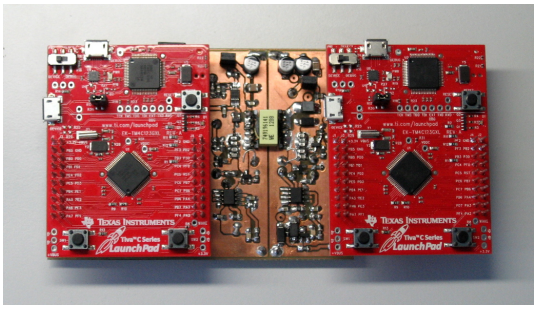
and *Tiva A receiver*. When output voltage regulation is disabled, the class-E dc-dc converter is always on and the maximum output voltage is constrained by a 5.6 V zener diode always connected between V_{out} and isolated ground to protect the *Tiva B* board. When load regulation is enabled, the output voltage V_{out} is periodically sampled by the *TM4C123GH6PM* ADC module and compared by sofware with two thresholds. Since V_{out} is clearly well above the nominal value of 5 V, a particular bit packet is sent backward to the primary side controller specifying a suitable on-off modulation scheme to regulate the power delivered to the load. As depicted in Figure 4-12, this process is iterated until the output voltage value falls between the two given hysteresis thresholds. Then, if the amount of current required by the load increases/decreases (for example when a LED is turned on in the *Tiva B*) then the feedback control loop reacts communicating how to adjust the on-off ratio at the primary side until V_{out} is brought back to 5 V.



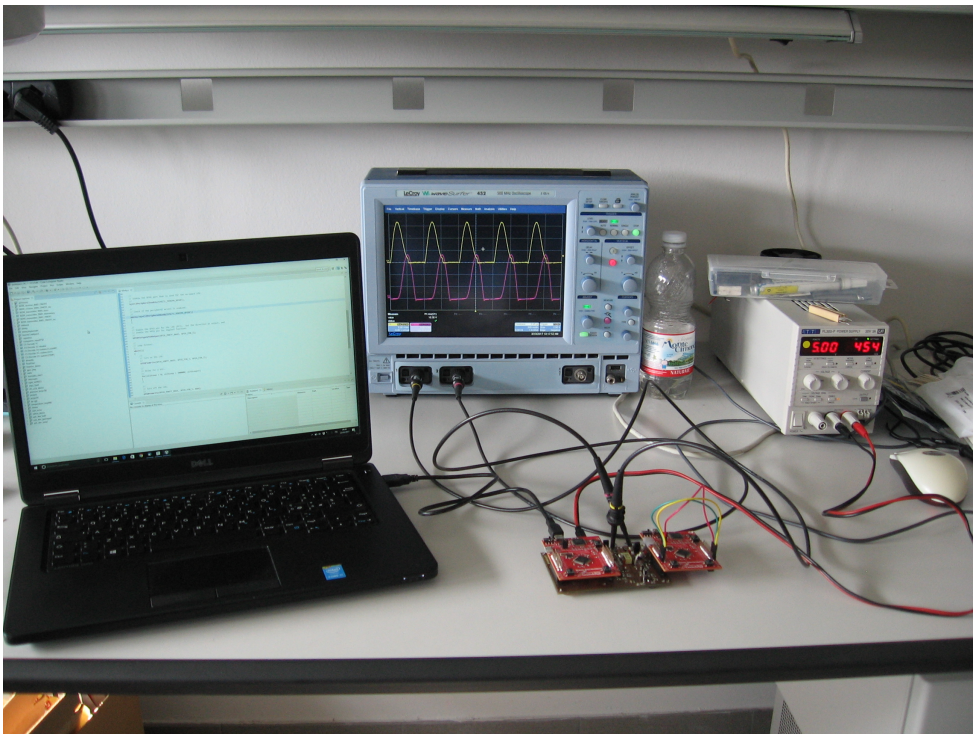
(a)



(b)



(c)



(d)

Figure 4-13: PCB prototype of a 1.2 W 5 V-5 V isolated class-E converter with bidirectional communication over power (a) PCB layout (left to right: top layer, bottom layer) (b) Custom PCB and (c) full-system photographs. (d) Laboratory experimental setup.

Conclusion and Future Work

The main purpose of the research presented in this dissertation was to introduce a **novel analysis and design methodology for resonant dc-dc power converters**. In fact, despite being particularly attractive due to their capability of ensuring high efficiency operation even for high switching frequency, there is still no consolidated design methodology which is fast and accurate enough to encourage their diffusion.

The proposed approach, applied to **several isolated and non-isolated class-E topologies**, consists in directly solving the differential equation systems describing the circuit behavior for all possible switch configurations and then combine them to get the complete evolution of converter waveforms across the whole switching period. Such an approach enables a **tremendous topology simplification** since there is no more need for filters and matching networks commonly used following the conventional RF design principles. In order to demonstrate the transversal applicability of the proposed methodology, it is extended to buck, boost, buck-boost and isolated buck-boost topologies showing that they are actually described by the same set of differential equations and can be analyzed within the same mathematical framework. Once the ODE systems have been solved analytically, the design solution can be readily computed numerically, with the aid of any optimization tool like *MATLAB* or *Mathematica*, to impose the desired soft-switching behavior. Considering a lossless circuit, a **set of normalized design curves** is provided in order to fastly get the ZVS/ZVDS solution (starting from converter specifications) which can be also used to rapidly explore and compare a great amount of design alternatives. In fact, since the degrees of freedom of the system are greatly reduced after normalizing equations, it is possible to **fully explore all the converter design space** with minimal effort opening the way towards several circuit optimizations.

Additionally, when the **resistive parasitics are introduced** in the modelling equations to account for semiconductor devices on-state resistance and reactive elements finite quality factor, also converters having a great amount of losses, such as

new miniaturized integrated power modules, can be accurately designed and their **efficency can be estimated** at an early design stage. This can lead to enormous benefits to the designers trying to optimize a power converter in a multidimensional performance space where many trade-offs (such as the one between efficiency and size/cost) exist. In order to validate the proposed methodology two **PCB prototypes** have been realized and measured showing 59 % and 75 % efficiency respectively, which are very similar to those predicted by the mathematical computations. Furthermore, for both prototypes, implemented without the need of any circuital simulator to refine the semi-analitically computed design point, the circuit current and voltage waveforms are almost perfectly resembling the theoretical ones proving that a superior level of accuracy has been reached.

Finally, the same ODE-based analysis has been exploited to statistically characterize the behavior of an isolated class-E converter where the resonant capacitors values are modulated to implement a **new bidirectional power line communication technique**. Then, with minimal hardware overhead (just a couple of switched capacitors), a robust and high-speed (1 bit/cycle) bidirectional communication channel exploiting the same transformer used for power transfer has been succesfully implemented and tested. Prototype measurements confirm that the proposed solution can achieve a bit error rate as low as 10^{-9} for both backward and forward communication (under nominal working conditions) with a minimal impact on converter efficiency (3-4 %).

For future developments, the proposed ODE-based methodology can be applied as is to other double-ended resonant topologies such as the half-bridge and full-bridge converters or it can be extended to other isolated or non-isolated converters featuring different resonant networks. In such a case, the analytic solutions of the ODE system must be coherently updated and new design curves can be drawn. Furthermore, if an integrated converter design is targeted, the FOM of semiconductor devices and the dependency of gate driving losses, inductance and quality factor on switching frequency can be combined with the established mathematical framework to get a superior level of modelling, design and optimization capabilities. This can also facilitate

understanding the impact that a new semiconductor or integrated passive technology could have on next generation miniaturized power conversion systems performance allowing to foresee the future roadmap trends. Current and future influence of the thesis contributions encompasses several emergent fields such as concurrent data/power links as evidenced in the work, but also resonant inductive coupling wireless power transfer, high power density medium-to-high power converter frontends for electrical vehicles as well as bioimplants and energy-harvesting-enabled self-powered wireless sensor networks and Internet of Things.

Milano, March 29$^{\text{th}}$, 2017

Appendix A

The Eigenanalysis Method

The solution $\mathbf{x}(t) = e^{\mathbf{A}t}\,\mathbf{x}(0)$ of the linear system

$$\mathbf{x}'(t) = \mathbf{A}\,\mathbf{x}(t) \tag{A.1}$$

can be obtained entirely by eigenanalysis of the matrix $\mathbf{A}$. Especially, having the matrix $\mathbf{A} \in \mathbb{R}^{m\times m}$ a list of eigenpairs

$$(\lambda_1, \mathbf{v}_1)\,,\ (\lambda_2, \mathbf{v}_2)\,,\ ...,\ (\lambda_m, \mathbf{v}_m)\ , \tag{A.2}$$

a computationally useful case (while it is not required for the eigenvalues to be distinct, and they can be real or complex) is when the eigenvectors $\mathbf{v}_i$ are all independent. In such a situation the following mathematical formulations can be derived.

A.1 The Eigenanalysis Method for $m = 2$

Supposing that $\mathbf{A}$ is a 2×2 real matrix with eigenpairs

$$(\lambda_1, \mathbf{v}_1)\,,\ (\lambda_2, \mathbf{v}_2) \tag{A.3}$$

Despite the fact that both eigenvalues λ_i and eigenvectors $\mathbf{v}_i$ can be either real or complex valued, the general solution of (A.1) can be written as

$$\mathbf{x}(t) = \sum_{i=1}^{2} c_i \, e^{\lambda_i t} \, \mathbf{v}_i \; = \; c_1 \, e^{\lambda_1 t} \, \mathbf{v}_1 + c_2 \, e^{\lambda_2 t} \, \mathbf{v}_2 \tag{A.4}$$

or, equivalently, in the vector-matrix form as

$$\mathbf{x}(t) \; = \mathbf{V} \begin{pmatrix} e^{\lambda_1 t} & 0 \\ 0 & e^{\lambda_2 t} \end{pmatrix} \mathbf{c} \; = \; \mathbf{V} \; \mathbf{diag}\left(e^{\lambda_1 t}, \, e^{\lambda_2 t}\right) \mathbf{c} \tag{A.5}$$

with $\mathbf{V} = (\mathbf{v}_1 \; \mathbf{v}_2) \in \mathbb{C}^{2\times 2}$ being the augmented matrix with eigenvectors as columns and $\mathbf{c} = (c_1 \; c_2)^\intercal \in \mathbb{C}^2$ coefficients to be computed from the initial conditions $\mathbf{x}^0 \triangleq \mathbf{x}(0)$. In fact, being the eigenvectors independent, $\mathbf{V}$ is invertible and setting $t = 0$ in (A.5) one obtains

$$\mathbf{c} = \mathbf{V}^{-1} \, \mathbf{x}(0). \tag{A.6}$$

Merging (A.5) and (A.6), the matrix exponential is readily defined by

$$\mathbf{x}(t) = e^{\mathbf{A}t} \, \mathbf{x}^0 \; = \; \mathbf{V} \; \mathbf{diag}\left(e^{\lambda_1 t}, \, e^{\lambda_2 t}\right) \; \mathbf{V}^{-1} \mathbf{x}^0. \tag{A.7}$$

Justification of (A.4)

Substituting (A.4) into (A.1) and considering the eigenpair relation $\lambda_i \, \mathbf{v}_i = \mathbf{A} \, \mathbf{v}_i$

$$\begin{aligned} \mathbf{x}'(t) = c_1 \, \left(e^{\lambda_1 t}\right)' \, \mathbf{v}_1 + c_2 \, \left(e^{\lambda_2 t}\right)' \, \mathbf{v}_2 \; = \\ = \; c_1 \, e^{\lambda_1 t} \, \lambda_1 \, \mathbf{v}_1 + c_2 \, e^{\lambda_2 t} \, \lambda_2 \, \mathbf{v}_2 \; = \\ = \; c_1 \, e^{\lambda_1 t} \, \mathbf{A} \, \mathbf{v}_1 + c_2 \, e^{\lambda_2 t} \, \mathbf{A} \, \mathbf{v}_2 \; = \\ = \; \mathbf{A} \, \left(c_1 \, e^{\lambda_1 t} \, \mathbf{v}_1 + c_2 \, e^{\lambda_2 t} \, \mathbf{v}_2\right) \; = \\ = \; \mathbf{A} \, \mathbf{x}(t) \end{aligned} \tag{A.8}$$

Equation (A.7) is immediately useful when eigenvalues are real, otherwise in case

of complex conjugate eigenvalues

$$\lambda_1 = \alpha + j\beta, \quad \lambda_2 = \alpha - j\beta \tag{A.9}$$

with $\beta > 0$ and $\mathbf{v}_2 = \overline{\mathbf{v}_1}$, the exponential matrix can be conveniently rewritten as

$$e^{\mathbf{A}t} = e^{\alpha t}\,\mathbf{V}\begin{pmatrix} \cos(\beta t) & \sin(\beta t) \\ -\sin(\beta t) & \cos(\beta t) \end{pmatrix}\mathbf{V}^{-1} \;=\; e^{\alpha t}\,\mathbf{V}\,\mathbf{R}(-\beta t)\,\mathbf{V}^{-1} \tag{A.10}$$

where $\mathbf{V} = (\mathrm{Re}\,[\mathbf{v}_1]\;\; \mathrm{Im}\,[\mathbf{v}_1]) = (\mathbf{v}_R\;\mathbf{v}_I)$ and $\mathbf{R}(\varphi)$ is the well-known *rotation matrix*.

Justification of (A.10)

The formula is established by showing that the matrix $\mathbf{\Phi}(t) = \mathbf{V}\,\mathbf{R}(-\beta t)\,\mathbf{V}^{-1}$ satisfies (a) $\mathbf{\Phi}(0) = \mathbf{I}$ and (b) $\mathbf{\Phi}'(t) = \mathbf{A}\,\mathbf{\Phi}(t)$. Then, by definition, $\mathbf{\Phi}(t) = e^{\mathbf{A}t}$.

The identity (a) is verified as follows:

$$\mathbf{\Phi}(0) = \mathbf{V}\,\mathbf{R}(0)\,\mathbf{V}^{-1} \;=\; \mathbf{V}\,e^{0}\,\mathbf{I}\,\mathbf{V}^{-1} = \mathbf{I} \tag{A.11}$$

To demonstrate (b) the eigenpair relation $\mathbf{A}\,\mathbf{v}_1 = \lambda_1\,\mathbf{v}_1$ is expanded into real and imaginary parts

$$\begin{aligned} \mathbf{A}\,\mathbf{v}_R &= \alpha\,\mathbf{v}_R - \beta\,\mathbf{v}_I \\ \mathbf{A}\,\mathbf{v}_I &= \alpha\,\mathbf{v}_I + \beta\,\mathbf{v}_R \end{aligned} \tag{A.12}$$

that can be rewritten in matrix form as

$$\mathbf{A}\,\mathbf{V} \;=\; \mathbf{V}\begin{pmatrix} \alpha & \beta \\ -\beta & \alpha \end{pmatrix} \tag{A.13}$$

Then,

$$\begin{aligned} &\mathbf{\Phi}'(t)\,\mathbf{\Phi}^{-1}(t) = \mathbf{V}\,\mathbf{R}'(-\beta t)\,\mathbf{V}^{-1}\,\mathbf{V}\,\mathbf{R}^{-1}(-\beta t)\,\mathbf{V}^{-1} \;= \\ &= \mathbf{V}\,\mathbf{R}'(-\beta t)\,\mathbf{R}^{-1}(-\beta t)\,\mathbf{V}^{-1} \;=\; \mathbf{V}\begin{pmatrix} \alpha & \beta \\ -\beta & \alpha \end{pmatrix}\mathbf{V}^{-1} \;= \mathbf{A} \end{aligned} \tag{A.14}$$

A.2 The Eigenanalysis Method for $m = 3$

Let's suppose now that the matrix $\mathbf{A}$ is 3×3 with eigenpairs

$$(\lambda_1, \mathbf{v}_1)\,,\ (\lambda_2, \mathbf{v}_2)\,,\ (\lambda_3, \mathbf{v}_3) \tag{A.15}$$

If the eigenvalues are all real the solution can be easily derived from (A.5) as

$$\mathbf{x}(t) \,=\, \mathbf{V}\ \mathbf{diag}\left(e^{\lambda_1 t},\, e^{\lambda_2 t},\, e^{\lambda_3 t}\right)\ \mathbf{c}. \tag{A.16}$$

with $\mathbf{V} = (\mathbf{v}_1\ \mathbf{v}_2\ \mathbf{v}_3)$. When there is a complex conjugate pair of eigenvalues $\lambda_1 = \overline{\lambda_2} = \alpha + j\beta$, $\beta > 0$, then as shown for the 2×2 case it is possible to extract a real solution from the complex formula (A.16) as

$$\mathbf{x}(t) = \mathbf{V} \begin{pmatrix} e^{\alpha t}\cos(\beta t) & e^{\alpha t}\sin(\beta t) & 0 \\ -e^{\alpha t}\sin(\beta t) & e^{\alpha t}\cos(\beta t) & 0 \\ 0 & 0 & e^{\lambda_3 t} \end{pmatrix} \mathbf{c} \tag{A.17}$$

with $\mathbf{V} = (\mathrm{Re}\,[\mathbf{v}_1]\ \ \mathrm{Im}\,[\mathbf{v}_1]\ \ \mathbf{v}_3)$. In both cases the coefficient vector $\mathbf{c}$ can be computed from the initial conditions as

$$\mathbf{c} = (c_1\ c_2\ c_3)^\intercal = \mathbf{V}^{-1}\mathbf{x}^0. \tag{A.18}$$

A.3 The Eigenanalysis Method for a Generic $m \times m$ Matrix

The general solution formula can be easily generalized from the 2×2 and 3×3 cases to the general case of an $m \times m$ matrix. The vector-matrix form of the general solution is

$$\mathbf{x}(t) = (\mathbf{v}_1,\ ...,\ \mathbf{v}_m)\ \ \mathbf{diag}\left(e^{\lambda_1 t},\, ...,\, e^{\lambda_m t}\right)\ \ (c_1,\ ...,\ c_m)^\intercal \tag{A.19}$$

This form is real provided all eigenvalues are real. Oppositely, a real form can be made from a complex form by following the example of a 3×3 matrix. The plan is to list all complex eigenvalues first, in pairs, λ_1, $\overline{\lambda_1}$, ..., λ_p, $\overline{\lambda_p}$. Then the real eigenvalues ρ_1, ..., ρ_q are listed, $2p + q = m$. Define

$$\mathbf{V} = (\mathrm{Re}\left[\mathbf{v}_1\right],\ \mathrm{Im}\left[\mathbf{v}_1\right], ..., \mathrm{Re}\left[\mathbf{v}_{2p-1}\right],\ \mathrm{Im}\left[\mathbf{v}_{2p-1}\right], \mathbf{v}_{2p+1}, ..., \mathbf{v}_m) \tag{A.20}$$

and

$$\mathbf{R}_{\lambda_i}(t) \ = \ e^{\alpha_i t} \begin{pmatrix} \cos(\beta_i t) & \sin(\beta_i t) \\ -\sin(\beta_i t) & \cos(\beta_i t) \end{pmatrix} \tag{A.21}$$

where $\lambda_i = \alpha_i + j\beta_i, \beta_i > 0, i = 1, 2, ..., p$. Then the real vector-matrix form of the general solution is

$$\mathbf{x}(t) = \mathbf{V}\ \mathbf{diag}\left(R_{\lambda_1}(t), ..., R_{\lambda_p}(t), e^{r_1 t}, ..., e^{r_q t}\right)\ \mathbf{c} \tag{A.22}$$

with $\mathbf{c} = (c_1, ..., c_m)^\intercal = \mathbf{V}^{-1}\ \mathbf{x}^0$.

Appendix B

Lossless System Solutions

Depending on the different configurations of the input and output switch networks the resonant converter is regulated by a second, third or fourth order differential equation system. In the following an analytic solution for each *zone*, which depends on the initial conditions $\mathbf{x}(0)$ and on the dimensionless design variables $(k_i, k_r, q_M, q_i, q_r)$, is found.

B.1 Linear (LIN) Zone

When both the switches are on there is no current flowing through the capacitors and the effective resonant network is made of only inductors producing linear current waveforms. The equations regulating the circuit evoution are the following

$$\begin{cases} \dfrac{q_M}{k_i}\dfrac{di_i(\theta)}{d\theta} + q_M\dfrac{di_r(\theta)}{d\theta} - 1 = 0 \\ q_M\dfrac{di_i(\theta)}{d\theta} + \dfrac{q_M}{k_r}\dfrac{di_r(\theta)}{d\theta} - 1 = 0 \end{cases} \tag{B.1}$$

which can be easily decoupled by substitution into two independent first order differential equations

$$\frac{di_x(\theta)}{d\theta} = \frac{k_x\,(1-k_y)}{q_M\,(1-k_xk_y)} \tag{B.2}$$

where the (x, y) notation is introduced to include both inverter side and rectifier side equations into a single formula. Solutions can be found by integration as

$$i_x(\theta) = \frac{k_x\,(1 - k_y)}{q_M\,(1 - k_x k_y)}\theta + c_x \tag{B.3}$$

where the constant c_x is found from the initial condition $i_x(0)$.

B.2 Half-Resonant (HR) Zone

The solution of the converter equations when only one among S1 and S2 is on can be conveniently splitted into two easier problems, as already explained in Chapter 3. If we refer to the current and voltage on the resonant side (i.e. the side of the converter with switch network being an open circuit) as $i_x(\theta)$ and $v_x(\theta)$ respectively, then the first part of the problem can be conveniently rewritten as

$$\begin{cases} q_M \left(\dfrac{1}{k_x} - k_y\right) \dfrac{di_x(\theta)}{d\theta} + v_x(\theta) + k_y - 1 = 0 \\ \dfrac{dv_x(\theta)}{d\theta} - q_x\, i_x(\theta) = 0 \end{cases} \tag{B.4}$$

where $k_x \equiv k_i$, $k_y \equiv k_r$ and $q_x \equiv q_i$ if S1 is off (S2 on); $k_x \equiv k_r$, $k_y \equiv k_i$ and $q_x \equiv q_r$ otherwise (S1 on, S2 off).

After defining the state variable vector $\mathbf{x}(\theta) = \begin{pmatrix} i_x(\theta) \\ v_x(\theta) \end{pmatrix}$, the system can be rearranged in canonical form as

$$\mathbf{x}'(\theta) = \mathbf{A}\mathbf{x}(\theta) + \mathbf{b}$$

with

$$\mathbf{A} = \begin{pmatrix} q_M \left(\dfrac{1}{k_x} - k_y\right) & 0 \\ 0 & 1 \end{pmatrix}^{-1} \begin{pmatrix} 0 & -1 \\ q_x & 0 \end{pmatrix} = \begin{pmatrix} 0 & \dfrac{k_x}{q_M\,(1 - k_x k_y)} \\ -q_x & 0 \end{pmatrix}$$

$$\mathbf{b} = \begin{pmatrix} q_M\left(\frac{1}{k_x} - k_y\right) & 0 \\ 0 & 1 \end{pmatrix}^{-1} \begin{pmatrix} 1 - k_y \\ 0 \end{pmatrix} = \begin{pmatrix} \frac{k_x\,(1-k_y)}{q_M\,(1-k_x k_y)} \\ 0 \end{pmatrix}$$

Solution of (B.4), can be easily retrieved after computing the eigenvalues λ_i and associated eigenvectors $\mathbf{v}_i$ of the matrix $\mathbf{A}$, which must be also invertible.

$$\mathbf{x}(\theta) = \hat{\mathbf{x}}(\theta) - \mathbf{A}^{-1}\mathbf{b} = \begin{pmatrix} \mathbf{v}_1 & \mathbf{v}_2 \end{pmatrix} \begin{pmatrix} e^{\lambda_1\theta} & 0 \\ 0 & e^{\lambda_2\theta} \end{pmatrix} \begin{pmatrix} c_1 \\ c_2 \end{pmatrix} - \begin{pmatrix} 0 \\ k_y - 1 \end{pmatrix} \tag{B.5}$$

where $\hat{\mathbf{x}}(\theta)$ is the solution of the corresponding homogeneus system and the complex conjugate coefficients $c_1 = c_R + jc_I$ and $c_2 = c_R - jc_I$ can be computed from the initial conditions $\mathbf{x}^0 \triangleq \mathbf{x}(0)$. If $k_x q_x / q_M > 0$ and $k_x k_y < 1$ then $\beta = \sqrt{\frac{k_x\, q_x}{q_M\,(1-k_x k_y)}} \in \mathbb{R}$ and eigenvalues are complex conjugate (real part is zero because no losses are taken into account)

$$\lambda_{1,2} = \pm j\,\beta \quad \mathbf{v}_{1,2} = \begin{pmatrix} \pm j\beta/q_x \\ 1 \end{pmatrix} \tag{B.6}$$

Since the matrices $\mathbf{A}$ and $\mathbf{b}$ are real, the solution will be real as well and can be easily obtained recurring to some complex algebra manipulations

$$\hat{\mathbf{x}}(\theta) = \begin{pmatrix} c_1\,\mathrm{v}_{11}\,e^{\lambda_1\theta} + c_2\,\mathrm{v}_{21}\,e^{\lambda_2\theta} \\ c_1\,\mathrm{v}_{12}\,e^{\lambda_1\theta} + c_2\,\mathrm{v}_{22}\,e^{\lambda_2\theta} \end{pmatrix} =$$

$$= \begin{pmatrix} (c_R + jc_I)\,\mathrm{v}_{11}\,e^{\lambda_1\theta} + (c_R - jc_I)\,\mathrm{v}_{21}\,e^{\lambda_2\theta} \\ (c_R + jc_I)\,\mathrm{v}_{12}\,e^{\lambda_1\theta} + (c_R - jc_I)\,\mathrm{v}_{22}\,e^{\lambda_2\theta} \end{pmatrix} =$$

$$= \begin{pmatrix} j\beta/q_x(c_R + jc_I)\,e^{j\beta\theta} - j\beta/q_x(c_R - jc_I)\,e^{-j\beta\theta} \\ (c_R + jc_I)\,e^{j\beta\theta} + (c_R - jc_I)\,e^{-j\beta\theta} \end{pmatrix} =$$

$$= \begin{pmatrix} -c_I\beta/q_x\left(e^{j\beta\theta} + e^{-j\beta\theta}\right) + jc_R\beta/q_x\left(e^{j\beta\theta} - e^{-j\beta\theta}\right) \\ c_R\left(e^{j\beta\theta} + e^{-j\beta\theta}\right) + jc_I\left(e^{j\beta\theta} - e^{-j\beta\theta}\right) \end{pmatrix} =$$

$$= \begin{pmatrix} \beta/q_x\left(c_b\cos(\beta\theta) - c_a\sin(\beta\theta)\right) \\ c_a\cos(\beta\theta) + c_b\sin(\beta\theta) \end{pmatrix}$$

with $c_a = 2c_R \in \mathbb{R}$ and $c_b = -2c_I \in \mathbb{R}$. Then,

$$\mathbf{x}(\theta) = \hat{\mathbf{x}}(\theta) - \begin{pmatrix} 0 \\ k_y - 1 \end{pmatrix} = \begin{pmatrix} \beta/q_x \left(c_b \cos(\beta\theta) - c_a \sin(\beta\theta) \right) \\ c_a \cos(\beta\theta) + c_b \sin(\beta\theta) + 1 - k_y \end{pmatrix} \tag{B.7}$$

Hence, in such a special case, the solution can be written directly once defined the matrix $\mathbf{V} = (\mathrm{Re}\,[\mathrm{v}_1] \;\; \mathrm{Im}\,[\mathrm{v}_1]) \in \mathbb{R}^{2\times 2}$ as also explained in Appendix A

$$\hat{\mathbf{x}}(\theta) = \mathbf{V}\, \mathbf{R}(-\beta\theta)\, \mathbf{c} = \mathbf{V} \begin{pmatrix} \cos(\beta\theta) & \sin(\beta\theta) \\ -\sin(\beta\theta) & \cos(\beta\theta) \end{pmatrix} \begin{pmatrix} c_a \\ c_b \end{pmatrix} \tag{B.8}$$

where $\mathbf{R}(\varphi)$ is the well-known *rotation matrix*. Once solved the first part of the problem, the second one becomes a trivial task, because $i_x(\theta)$ is known and $i_y(\theta)$ can be computed by simply integrating both sides of the following equation

$$\frac{q_M}{k_y} \frac{di_y(\theta)}{d\theta} = -q_M \frac{di_x(\theta)}{d\theta} + 1 \tag{B.9}$$

which leads to

$$i_y(\theta) = -k_y i_x(\theta) + \frac{k_y}{q_M}\theta + c_3 \tag{B.10}$$

where the real coefficient c_3 is computed from the initial condition $i_y(0)$.

B.3 Full-Resonant (FR) Zone

When both S1 and S2 are open circuits the resonant network is freely oscillating following a fourth order ODE system

$$\begin{cases} \dfrac{q_M}{k_i} \dfrac{di_i(\theta)}{d\theta} + q_M \dfrac{di_r(\theta)}{d\theta} = -v_i(\theta) + 1 \\ q_M \dfrac{di_i(\theta)}{d\theta} + \dfrac{q_M}{k_r} \dfrac{di_r(\theta)}{d\theta} = -v_r(\theta) + 1 \\ \dfrac{1}{q_i} \dfrac{dv_i(\theta)}{d\theta} = i_i(\theta) \\ \dfrac{1}{q_r} \dfrac{dv_r(\theta)}{d\theta} = i_r(\theta) \end{cases} \tag{B.11}$$

that can be conveniently rewritten in matricial form as $\mathbf{x}'(\theta) = \mathbf{A}\mathbf{x}(\theta) + \mathbf{b}$ with

$$\mathbf{x}(\theta) = \begin{pmatrix} i_i(\theta) \\ i_r(\theta) \\ v_i(\theta) \\ v_r(\theta) \end{pmatrix}$$

$$\mathbf{A} = \mathbf{M}^{-1}\mathbf{L}_0 = \mathbf{M}^{-1} \begin{pmatrix} 0 & 0 & -1 & 0 \\ 0 & 0 & 0 & -1 \\ 1 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 \end{pmatrix} =$$

$$= \begin{pmatrix} 0 & 0 & -\dfrac{k_i}{q_M\,(1-k_ik_r)} & \dfrac{k_ik_r}{q_M\,(1-k_ik_r)} \\ 0 & 0 & \dfrac{k_ik_r}{q_M\,(1-k_ik_r)} & -\dfrac{k_r}{q_M\,(1-k_ik_r)} \\ q_i & 0 & 0 & 0 \\ 0 & q_r & 0 & 0 \end{pmatrix}$$

$$\mathbf{b} = \mathbf{M}^{-1}\mathbf{l}_0 = \mathbf{M}^{-1} \begin{pmatrix} 1 \\ 1 \\ 0 \\ 0 \end{pmatrix} = \begin{pmatrix} \dfrac{k_i\,(1-k_r)}{q_M\,(1-k_ik_r)} \\ \dfrac{k_r\,(1-k_i)}{q_M\,(1-k_ik_r)} \\ 0 \\ 0 \end{pmatrix}$$

and

$$\mathbf{M} = \begin{pmatrix} \dfrac{q_M}{k_i} & q_M & 0 & 0 \\ q_M & \dfrac{q_M}{k_r} & 0 & 0 \\ 0 & 0 & \dfrac{1}{q_i} & 0 \\ 0 & 0 & 0 & \dfrac{1}{q_r} \end{pmatrix}$$

The eigenvalues of the matrix $\mathbf{A}$ are the following

$$\lambda_{1,2} = \pm j\sqrt{\frac{\gamma^-}{2q_M(1-k_ik_r)}} = \pm j\beta_1 \quad \lambda_{3,4} = \pm j\sqrt{\frac{\gamma^+}{2q_M(1-k_ik_r)}} = \pm j\beta_2 \qquad \text{(B.12)}$$

with $\gamma^{\pm} = k_i q_i + k_r q_r \pm \sqrt{(k_i q_i - k_r q_r)^2 + 4k_i^2 k_r^2 q_i q_r} \in \mathbb{R}$. It can be easily proven that, having $q_M/k_i > 0$, $q_M/k_r > 0$, $q_i > 0$ and $q_r > 0$, $\lambda_{1,2}$ and $\lambda_{3,4}$ are two couples of complex conjugates eigenvalues with zero real part. The corresponding eigenvectors are

$$\mathbf{v}_{1,2} = \begin{pmatrix} \pm j\mathrm{v}_{11} & \pm j\mathrm{v}_{12} & \mathrm{v}_{13} & 1 \end{pmatrix}^{\intercal} = \left(-\lambda_{1,2} \, \frac{\gamma^- - 2k_r q_r}{2k_i k_r q_i q_r}, \;\; \frac{\lambda_{1,2}}{q_r}, \;\; \frac{\gamma^+ - 2k_i q_i}{2k_i k_r q_r}, \;\; 1 \right)^{\intercal}$$

$$\mathbf{v}_{3,4} = \begin{pmatrix} \pm j\mathrm{v}_{31} & \pm j\mathrm{v}_{32} & \mathrm{v}_{33} & 1 \end{pmatrix}^{\intercal} = \left(-\lambda_{3,4} \, \frac{\gamma^+ - 2k_r q_r}{2k_i k_r q_i q_r}, \;\; \frac{\lambda_{3,4}}{q_r}, \;\; \frac{\gamma^- - 2k_i q_i}{2k_i k_r q_r}, \;\; 1 \right)^{\intercal}$$

Then, the same approach used to get Equation (B.8) can be extended to the FR case as follows

$$\hat{\mathbf{x}}(\theta) = \mathbf{V} \begin{pmatrix} \mathbf{R}(-\beta_1 \theta) & \mathbf{0} \\ \mathbf{0} & \mathbf{R}(-\beta_2 \theta) \end{pmatrix} \mathbf{c} \tag{B.13}$$

with the eigenvector matrix is defined as $\mathbf{V} \in \mathbb{R}^{4\times 4}$ is in the form

$$\mathbf{V} = \begin{pmatrix} \mathrm{Re}\,[\mathrm{v}_1] & \mathrm{Im}\,[\mathrm{v}_1] & \mathrm{Re}\,[\mathrm{v}_3] & \mathrm{Im}\,[\mathrm{v}_3] \end{pmatrix} = \begin{pmatrix} 0 & \mathrm{v}_{11} & 0 & \mathrm{v}_{31} \\ 0 & \mathrm{v}_{12} & 0 & \mathrm{v}_{32} \\ \mathrm{v}_{13} & 0 & \mathrm{v}_{33} & 0 \\ 1 & 0 & 1 & 0 \end{pmatrix} \tag{B.14}$$

and $\mathbf{c} = (c_a \; c_b \; c_c \; c_d)^{\intercal}$ are computed from the initial conditions

$$\hat{\mathbf{x}}(0) = \mathbf{x}(0) + \mathbf{A}^{-1}\mathbf{b} = \mathbf{x}^0 + \begin{pmatrix} 0 & 0 & -1 & -1 \end{pmatrix}^{\intercal}$$

Finally, the solution can be written explicitly as

$$\mathbf{x}(\theta) = \begin{pmatrix} c_b \mathrm{v}_{11} \cos(\beta_1\theta) - c_a \mathrm{v}_{11} \sin(\beta_1\theta + c_d \mathrm{v}_{31} \cos(\beta_2\theta) - c_c \mathrm{v}_{31} \sin(\beta_2\theta) \\ c_b \mathrm{v}_{12} \cos(\beta_1\theta) - c_a \mathrm{v}_{12} \sin(\beta_1\theta) + c_d \mathrm{v}_{32} \cos(\beta_2\theta) - c_c \mathrm{v}_{32} \sin(\beta_2\theta) \\ c_a \mathrm{v}_{13} \cos(\beta_1\theta) + c_b \mathrm{v}_{13} \sin(\beta_1\theta) + c_c \mathrm{v}_{33} \cos(\beta_2\theta) + c_d \mathrm{v}_{33} \sin(\beta_2\theta) + 1 \\ c_a \cos(\beta_1\theta) + c_b \sin(\beta_1\theta) + c_c \cos(\beta_2\theta) + c_d \sin(\beta_2\theta) + 1 \end{pmatrix} \tag{B.15}$$

Appendix C

Lossy System Solutions

Once the power converter is modeled as a piecewise linear system which also includes the main device non-idealities, as described in Chapter 3, the number of state variables for each zone is constant and it is determinied by the number of reactive elements in the circuit. In fact, introducing the series resistances of the semiconductor switches, the voltages $v_i(\theta)$ and $v_r(\theta)$ are no more constrained to zero when the corresponding devices are on and they remain in the pool of system state variables

$$\mathbf{x}(\theta) = (i_i(\theta),\ i_r(\theta),\ v_i(\theta),\ v_r(\theta))^{\mathsf{T}} \tag{C.1}$$

Hence, considering the resonant network in Figure 3-5, **each zone is described by a fourth order ODE system** which can be written as

$$\mathbf{M}\,\mathbf{x}'(\theta) = \mathbf{L}(Z_i)\,\mathbf{x}(\theta) + \mathbf{l}(Z_i) \quad i = 1, 2, 3, 4 \tag{C.2}$$

or, equivalently,

$$\mathbf{x}'(\theta) = \mathbf{A}(Z_i)\,\mathbf{x}(\theta) + \mathbf{b}(Z_i) \quad i = 1, 2, 3, 4 \tag{C.3}$$

with

$$\mathbf{A}(Z_i) = \mathbf{M}^{-1}\,\mathbf{L}(Z_i) =$$

$$= \mathbf{M}^{-1} \begin{pmatrix} -\dfrac{1}{g_i} & -\dfrac{q_M}{Q_M} & -1 & 0 \\ -\dfrac{q_M}{Q_M} & -\dfrac{1}{g_r} & 0 & -1 \\ 1 & 0 & -g_{di}(Z_i) & 0 \\ 0 & 1 & 0 & -g_{dr}(Z_i) \end{pmatrix} \tag{C.4}$$

$$\mathbf{b}(Z_i) = \mathbf{M}^{-1}\,\mathbf{l}(Z_i) = \mathbf{M}^{-1} \begin{pmatrix} 1 \\ 1 \\ -g_{di}(Z_i)\; v_{di}(Z_i) \\ -g_{dr}(Z_i)\; v_{dr}(Z_i) \end{pmatrix} \tag{C.5}$$

Even if it is not possible to provide a full mathematical demonstration, depending on the values of $g_{di}(Z_i)$ and $g_{dr}(Z_i)$, the matrix $\mathbf{A}$ can have:

- four real negative eigenvalues,
- a couple of complex conjugate eigenvalues and two real negative eigenvalues or
- two couples of complex conjugate eigenvalues.

C.1 Linear (LIN) Zone

When both S1 and S2 are on, the matrix $\mathbf{A}$ has four real negative eigenvalues $-\lambda_i$, $i = 1, 2, 3, 4$ and corresponding eigenvectors $\mathbf{v}_i$ are real as well. The solution of the homogeneous system can be written as

$$\hat{\mathbf{x}}(\theta) = \mathbf{V}\;\mathbf{diag}\Big(e^{-\lambda_1\theta}, e^{-\lambda_2\theta}, e^{-\lambda_3\theta}, e^{-\lambda_4\theta}\Big)\,\mathbf{c} =$$

$$= \begin{pmatrix} & & & \\ \mathbf{v}_1 & \mathbf{v}_2 & \mathbf{v}_3 & \mathbf{v}_4 \\ & & & \end{pmatrix} \begin{pmatrix} e^{-\lambda_1\theta} & 0 & 0 & 0 \\ 0 & e^{-\lambda_2\theta} & 0 & 0 \\ 0 & 0 & e^{-\lambda_3\theta} & 0 \\ 0 & 0 & 0 & e^{-\lambda_4\theta} \end{pmatrix} \begin{pmatrix} c_1 \\ c_2 \\ c_3 \\ c_4 \end{pmatrix} \tag{C.6}$$

C.2 Half-Resonant (HR) Zone

If only one switch between S1 and S2 is on, the the matrix $\mathbf{A}$ features a couple of complex conjugate eigenvalues $\lambda_{1,2} = -\alpha_0 \pm j\beta_0$, $\alpha_0 > 0$, $\beta_0 > 0$, with associated complex conjugate eigenvectors $\mathbf{v}_R \pm j\mathbf{v}_I$ and two real negative eigenvalues $-\lambda_{3,4} < 0$, with assciated eigenvectors $\mathbf{v}_3$ and $\mathbf{v}_4$. The solution of the homogeneous system is

$$\hat{\mathbf{x}}(\theta) = \begin{pmatrix} \mathbf{v}_R & \mathbf{v}_I & \mathbf{v}_3 & \mathbf{v}_4 \end{pmatrix} \begin{pmatrix} e^{-\alpha_0\theta}\,\mathbf{R}(-\beta_0\theta) & \mathbf{0} \\ \mathbf{0} & \mathbf{diag}\left(e^{-\lambda_3\theta}, e^{-\lambda_4\theta}\right) \end{pmatrix} \mathbf{c} \tag{C.7}$$

where $\mathbf{R}(\varphi)$ is the rotation matrix and $\mathbf{0} \in \mathbb{R}^{2\times 2}$ is the all-zero matrix.

C.3 Full-Resonant (FR) Zone

The full-resonant zone, where the resonant tank is completely disconnected from the input and output swtich networks, is characterized by a matrix $\mathbf{A}$ having two couples of complex conjugate eigenvalues $\lambda_{1,2} = -\alpha_1 \pm j\beta_1$, with associated complex conjugate eigenvectors $\mathbf{v}_{1,2} = \mathbf{v}_{R1} \pm j\mathbf{v}_{I1}$, and $\lambda_{3,4} = -\alpha_2 \pm j\beta_2$, $\alpha_1 > 0$, $\alpha_2 > 0$, $\beta_1 > 0$, $\beta_2 > 0$, with associated complex conjugate eigenvectors $\mathbf{v}_{3,4} = \mathbf{v}_{R2} \pm j\mathbf{v}_{I2}$. The solution of the homogeneous system is

$$\hat{\mathbf{x}}(\theta) = \begin{pmatrix} \mathbf{v}_{R1} & \mathbf{v}_{I1} & \mathbf{v}_{R2} & \mathbf{v}_{I2} \end{pmatrix} \begin{pmatrix} e^{-\alpha_1\theta}\,\mathbf{R}(-\beta_1\theta) & \mathbf{0} \\ \mathbf{0} & e^{-\alpha_2\theta}\,\mathbf{R}(-\beta_2\theta) \end{pmatrix} \mathbf{c} \tag{C.8}$$

Appendix D

Galois Linear Feedback Shift Registers (GLFSR)

Linear Feedback Shift Registers (LFSR) are a collection of cyclic binary states where the current state is a linear combination of its predecessor. A simple eXclusive-OR (XOR) of particular bits (the tap positions), and a shifting behavior allows for a uniform serial computation until the start state repeats.

In the Galois configuration, named after the French mathematician Évariste Galois, when the system is clocked, bits that are not taps are shifted one position to the right unchanged. The taps, on the other hand, are XOR'd with the output bit before they are stored in the next position. The arrangement of taps for feedback in an LFSR can be expressed as a polynomial modulo-2. This means that the coefficients of the polynomial must be 1s or 0s. This is called the *feedback polynomial* or *reciprocal characteristic polynomial*.

For example, if the taps are at the 7^{th} and 6^{th} bits (as shown in Figure D-1), the

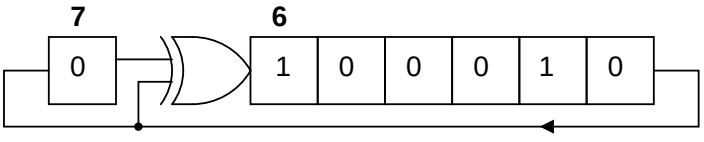


Figure D-1: A 7-bit Maximal Length Galois LFSR

feedback polynomial is

$$g(x) = x^7 + x^6 + 1. \tag{D.1}$$

The total number of unique states depends on the tap positions. If the tap positions are *maximal*, then for a LFSR of length m there are $2^m - 1$ possible states, spanning all non-zero bit binary numbers. It is known that if $g(x)$ divides $p(x) = x^{2m-1}+1$ and $deg(g(x)) = m$, then $g(x)$ is said to be *primitive* and correlates to tap positions leading to a *Maximal Length Sequence (MLS)*. This process for larger registers can be very tedious. Fortunately, tap positions for larger length LFSR are known, and publicly available.

LFSRs are particularly attractive due to their quick hardware implementations and are useful in digital electronics where can be used for testing hardware in a pseudorandom manner since, as stated, they can span all non-zero m-bit binary numbers. In addition they find application in noise generation, or scramblers, but the most common use of LFSR is in cryptography. In this thesis the 7-bit LFSR depicted in Figure D-1 is exploited to generate a design sequence for a power-line communicating isolated dc-dc converter. Such a sequence must contain all the possible bit combinations of $m + 1$ bits, where m is the estimated memory of the system, in order to give a good approximation of the converter behavior in real operating conditions with minimum computational effort.

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