Nonlinear Modeling of GaAs pHEMTs for Millimeter-Wave Mixer Design

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Abstract—The present paper is focused on the extraction of a GaAs pHEMT nonlinear model meant for mixer design. The model is based on an equivalent circuit that is analytically extracted from DC and multi-bias and –frequency S-parameter measurements and then implemented in a nonlinear RF circuit simulator by using look-up tables. The model accuracy is extensively verified by comparing device measurements and simulations under a wide range of operating conditions. Furthermore, to corroborate the validity of the model, the design of a Q-band up-converter is considered.

Keywords: design; equivalent circuit; microwave measurements; mixer; modeling; pHEMTs.

1. Introduction

High-frequency equivalent circuit modeling of active solid-state devices is a very attractive field of on-going research because of its crucial role for a fast and reliable development of both device fabrication and circuit design processes. Nowadays, there is considerable and growing interest in the determination of nonlinear models able to reproduce the device behavior under realistic RF operating conditions [1]-[3]. This is due to the increasing number of telecommunication applications that need the device to operate in a highly nonlinear regime, such as power amplifiers and mixers [4]-[8].

In this context, the purpose of this paper is to analytically extract and fully validate a nonlinear high-frequency model for GaAs pseudomorphic high electron mobility transistors (pHEMTs) for cold-FET mixer design. As well known, the core of the device model is its intrinsic section representing the actual nonlinear transistor. To implement the model in a commercial circuit simulator, the nonlinear intrinsic section can be represented by analytical functions [9]-[16] and/or look-up tables [17]-[25]. In the present case, the lookup table approach is adopted because of its key advantage of being a straightforward representation without requiring complex model functions, which can be very challenging and time consuming to construct and fit. It is worth noting that the determination of the model at negative V_{DS} is a critical step for mixer applications [26]-[30]. In light of that, the present model accounts for potential asymmetries as the model extraction is performed also at negative V_{DS} without the need of assuming a symmetric behavior of the device. Furthermore, the standard formulae for determining the transconductance and its delay at positive V_{DS} are modified for their extraction at negative V_{DS}. Specifically, the sign of g_m is changed at negative V_{DS} and such a π phase shift is subtracted before evaluating τ.

The paper is organized into five parts. Section 2 is dedicated to presenting the advanced tested pHEMTs fabricated in GaAs technology with a gate length of 0.15 μm. The two investigated devices have different gate width: 200 μm and 300 μm. Section 3 is aimed at describing the procedure for determining and implementing the equivalent circuit model, while Section 4 is devoted to its validation based on the comparison between measurements and simulations. Subsequently, Section 5 shows the comparison between measured and simulated performance of a Q-band up-converter designed and realized by using the 0.15 x 300 μm^2 transistor modeled in the present study. The Q-band ranges from

33 to 50 GHz and is widely used for several applications in satellite and terrestrial microwave communications and radio astronomy. Finally, conclusive remarks are given in Section 6.

2. Device characterization

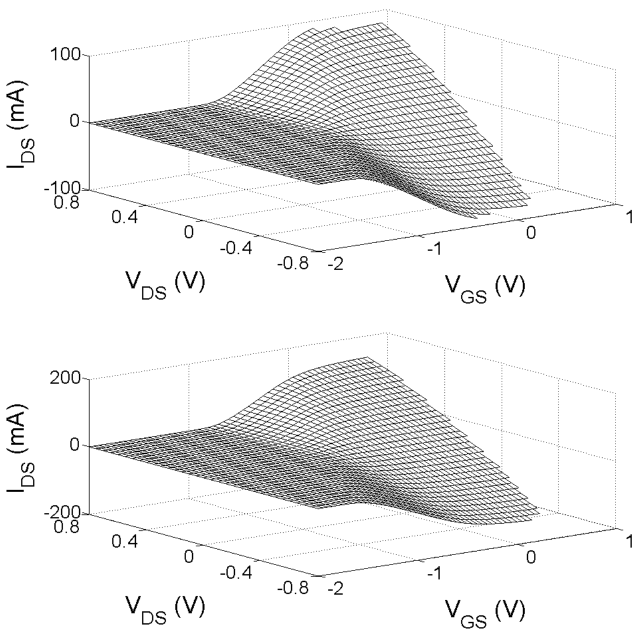
The two studied transistors are on-wafer GaAs pHEMTs fabricated by TriQuint Semiconductor [31]. The two devices have a gate length of 0.15 μm and a gate width of 200 μm and 300 μm, respectively. To improve their microwave performance, the layouts of the two devices are based on four interdigitated fingers with lengths of 50 μm and 75 μm, respectively. Furthermore, to minimize discontinuities between the transmission lines and the actual transistor, tapers are used at both gate-source and drain-source ports.

Device characterization is based on multi-bias scattering (S-) parameters measured from 2.5 GHz to 65 GHz. To put in evidence the wide range of bias points used for S-parameter measurements, Fig. 1 reports the corresponding measured values of I_D versus V_{GS} and V_{DS}. It should be highlighted that a small step of 50 mV has been used for both gate and drain voltages to guarantee good interpolation properties of the intrinsic look-up table model. This is because the intrinsic multi-bias small-signal equivalent circuit obtained from S-parameter measurements is used to build the nonlinear model, which is implemented by means of a symbolically defined device (SDD) component available in Agilent's advanced design system (ADS) circuit simulator [32]. Furthermore, it should be underlined that, based on the presented modeling technique, the model parameters are calculated from the measurements with appropriate scripts developed in MATLAB software. The S-parameter measurements on the device are achieved by using a TRL on-wafer calibration followed by matrix manipulations to remove the contributions of the input and output tapers. In particular, the shift of the reference planes is obtained by using the following formula based on the transmission (T-) parameters, known also as the chain parameters, as they are very helpful when working with networks connected in cascade [33]:

$$[T_{DUT}] = [T_{INPUT\_TAPER}]^{-1}[T_{DUT+TAPERS}][T_{OUTPUT\_TAPER}]^{-1} \quad (1)$$

where the behavior of the tapers is accurately determined by electromagnetic simulations.

Hence, the extrinsic effects arising from the tapers are disregarded in the present model since the model extraction is based on the S-parameter measurements after de-embedding the taper contributions. On the other hand, off-wafer calibrations are used for the nonlinear measurements devoted to the model validation at both low and high frequencies. This implies that the calibration reference planes have been set at the probe tips. The contributions associated to the path from the probe tips to the taper ends have to be considered at microwave frequencies; therefore they are properly modelled by using electromagnetic simulations. On the contrary, these access structures can be totally neglected at low frequencies (i.e., in the megahertz range) since they produce inductive and capacitive effects that are of the order of 100 pH and 50 fF respectively, whereas their resistive losses are below 50 mΩ.



(a) (b)

Fig. 1. Behavior of I_D versus V_{DS} and V_{GS} for two GaAs pHEMTs with different gate widths: 200 μm (a) and 300 μm (b).

3. Equivalent circuit extraction

Fig. 2 shows the small-signal equivalent circuit used for the tested GaAs pHEMTs. This circuit can be divided into two main sections: the extrinsic part, whose elements are assumed to be bias-independent, and the intrinsic section, whose elements are bias dependent. The values of the circuit elements are determined from S-parameter measurements. In particular, the extrinsic elements are firstly extracted from "cold" S-parameters (i.e., V_{DS} = 0 V) [34]-[40]. Successively, de-embedding of the extrinsic elements from the measurements is carried out with simple matrix manipulations, and the intrinsic elements are calculated from the intrinsic admittance (Y-) parameters at each investigated bias point by using well known formulae [33]. It should be highlighted that the transconductance and its delay are obtained at negative V_{DS} by modifying the standard formulae used for positive V_{DS}. In particular, at negative V_{DS} the sign of g_m must be changed and this π phase shift has to be subtracted before calculating τ:

$$G = g_m e^{-j\omega\tau} = (Y_{21} - Y_{12})\left[1 + j\frac{\mathrm{Re}(Y_{11}+Y_{12})}{\mathrm{Im}(Y_{11}+Y_{12})}\right] \begin{cases} for \quad V_{DS} > 0 & \begin{cases} g_m = |G| \\ \tau = -\dfrac{1}{\omega}\angle G \end{cases} \\ for \quad V_{DS} < 0 & \begin{cases} g_m = -|G| \\ \tau = -\dfrac{1}{\omega}(\angle G - \pi) \end{cases} \end{cases}$$

(2)

The bias dependences of the intrinsic g_m and C_{gs} for the two tested devices are illustrated in Fig. 3. Subsequently, the achieved multi-bias small-signal equivalent circuit is used as the starting point to build the large-signal model shown in Fig. 4. As can be seen, the transconductance delay τ is approximated with the transcapacitance (i.e., $C_m = g_m\tau$) by using only the first term in the Taylor series expansion for the function $e^{-j\omega\tau}$ (i.e., $e^{-j\omega\tau} = g_m - j\omega C_m$) [41], [42]. The conduction gate and drain currents are obtained from the measured DC values. Dedicated DC measurements at high values of the gate voltage are used to obtain the gate Schottky diode forward characteristics. The intrinsic circuit elements are stored in look-up tables versus the intrinsic voltages with the exception of the conduction gate current that is modeled with an analytical function approach. This is because the better extrapolation capability of the analytical functions allows predicting more accurately the exponential current growth when the gate voltage is increased beyond the analyzed bias range. In particular, the standard diode model available in ADS has been adopted [32]. To model the forward conduction of the gate Schottky junction the ideality factor N and the inverse saturation current I_s have been identified by using the DC measurements performed at sufficiently high gate voltage, keeping the drain voltage constant to 0 V. After de-embedding these data from the resistive parasitic effects, we use them to identify the requested parameters through the optimization tool provided by ADS. To reproduce the reverse conduction, the breakdown voltage provided by the foundry has been considered.

It should be pointed out that low-frequency dispersion effects have not been included in the model [43]-[50], since the thermal phenomena can be disregarded under the low power-dissipation of mixer application and the trapping mechanisms are negligible for the studied GaAs pHEMTs which are based on a well-established technology.

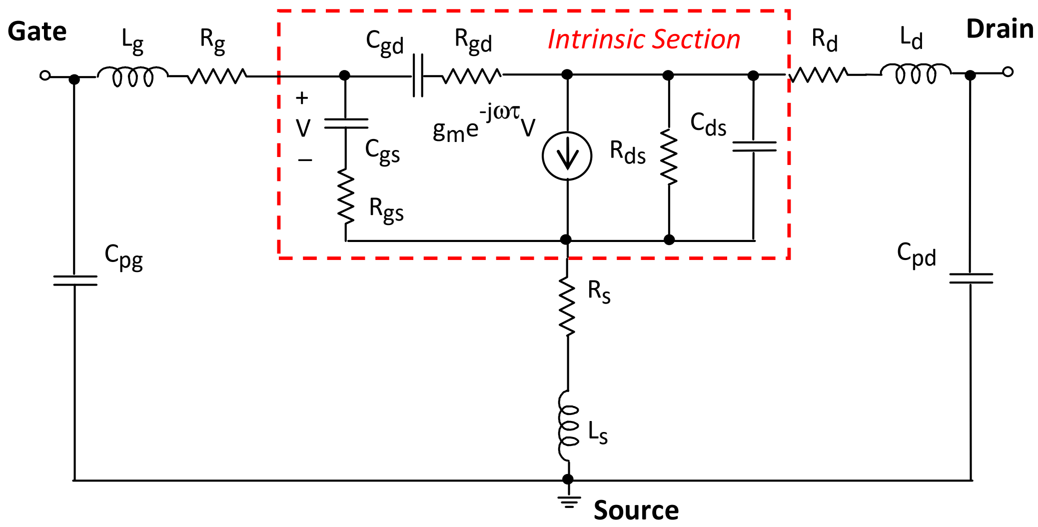


Fig. 2. Small-signal equivalent circuit for GaAs pHEMT. The intrinsic section is highlighted by a dashed box.

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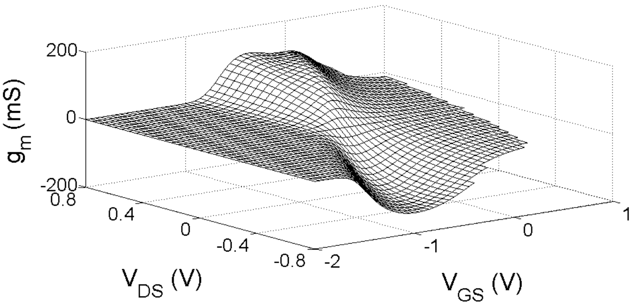
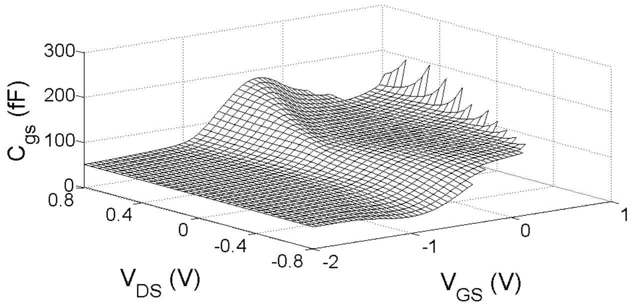
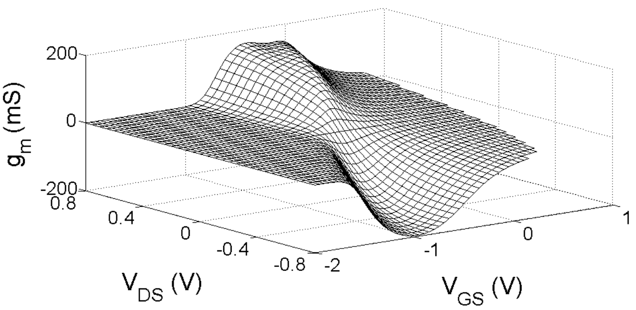
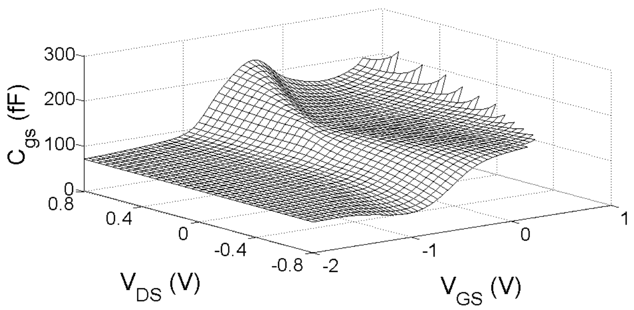




(a) (b)





(c) (d)

Fig. 3. Behavior of g_m and C_{gs} versus V_{DS} and V_{GS} for two GaAs pHEMTs with different gate widths: 200 μm (a, b) and 300 μm (c, d).

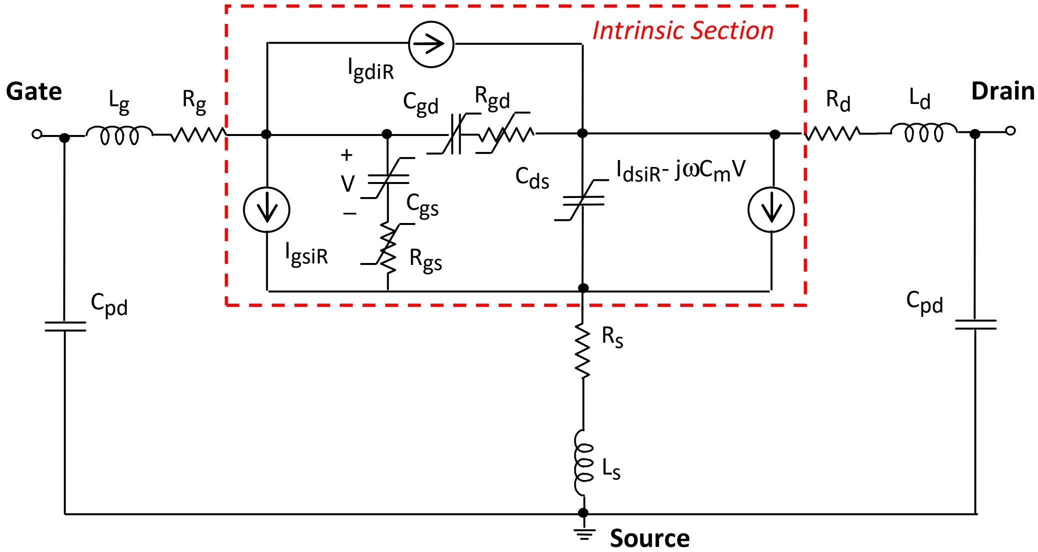


Fig. 4. Large-signal equivalent circuit for GaAs pHEMT. The intrinsic section is highlighted by a dashed box.

4. Equivalent circuit validation

The obtained nonlinear model can reproduce accurately the measured S-parameters over the full investigated frequency range up to 65 GHz. As an illustrative example, Fig. 5 shows the good agreement between measured and simulated S-parameters for the tested devices at three different bias conditions: V_{DS} = 0 V and V_{GS} = -1 V, V_{DS} = 0.5 V and V_{GS} = -0.8 V, V_{DS} = -0.5 V and V_{GS} = -0.5 V. The model accuracy is confirmed by the low percentage errors E_{ij} between measured and simulated S-parameters (see Table I). The values of E_{ij} are achieved as follows:

$$E_{ij} = \frac{1}{N_f} \sum_f 100 \left| \frac{S_{ijMEASURED}(f) - S_{ijSIMULATED}(f)}{S_{ijMEASURED}(f)} \right| \quad (3)$$

where N_f is the frequency point number that is equal to 201 for the present study. It should be pointed out that the percentage error associated to S_{12} may reach very high values, due to its extremely small magnitude especially at low frequencies. Furthermore, Fig. 6 illustrates that the model can mimic very

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well the behavior of the real and imaginary parts of the measured S-parameters versus V_{GS} with $V_{DS} = 0$ V at the high frequency of 40 GHz.

Fig. 7 presents the result of the nonlinear validation at low frequencies. In particular, it is shown that the model can accurately predict the measured drain voltage and current time-domain waveforms under cold-FET mixer application (i.e., $V_{DS} = 0$ V and $V_{GS} = -1$ V) with a fundamental frequency (f_0) of 2 MHz for the tested GaAs pHEMTs. At such low frequency the nonlinear capacitive effects are negligible and then the achieved accuracy of the present model without a dedicated low-frequency dispersion network confirms that the impact of dispersive effects on the conduction drain current can be disregarded.

To validate the nonlinear model at high frequencies, the results of the simulations are compared with measurements performed by means of a large-signal network analyzer (LSNA) working up to 50 GHz. Fig. 8 reports the comparison between measured and simulated input and transfer loci for the device with a gate width of 300 μm at $f_0 = 10$ GHz, $V_{DS} = 0$ V, and V_{GS} going from -1.1 V to -0.6 V with a step of 0.1 V. Fig. 9 illustrates the comparison between measured and simulated input and transfer loci for the device with a gate width of 200 μm at 15 GHz, $V_{DS} = 0$ V, V_{GS} -1 V, and for four different values of input power: -10.8 dBm, -5.8 dBm, -0.8 dBm, and 4.2 dBm. Furthermore, Fig. 10 shows measured and simulated output power and b_2/a_1 phase versus input power for the device with a gate width of 300 μm at $V_{DS} = 0$ V, $V_{GS} = -1$ V, and for two different values of the fundamental frequency: 38 GHz and 42 GHz.

The observed good agreement between model simulations and measurements under different operating conditions confirms the robustness of the extracted model.

TABLE I. The percentage errors between measured and simulated S-parameters for the two tested devices at three different bias conditions.

Gate Width (μm)	V_{DS} (V)	V_{GS} (V)	E_{11} (%)	E_{21} (%)	E_{12} (%)	E_{22} (%)
200	0	-1	4.4	4.6	4.6	4.3

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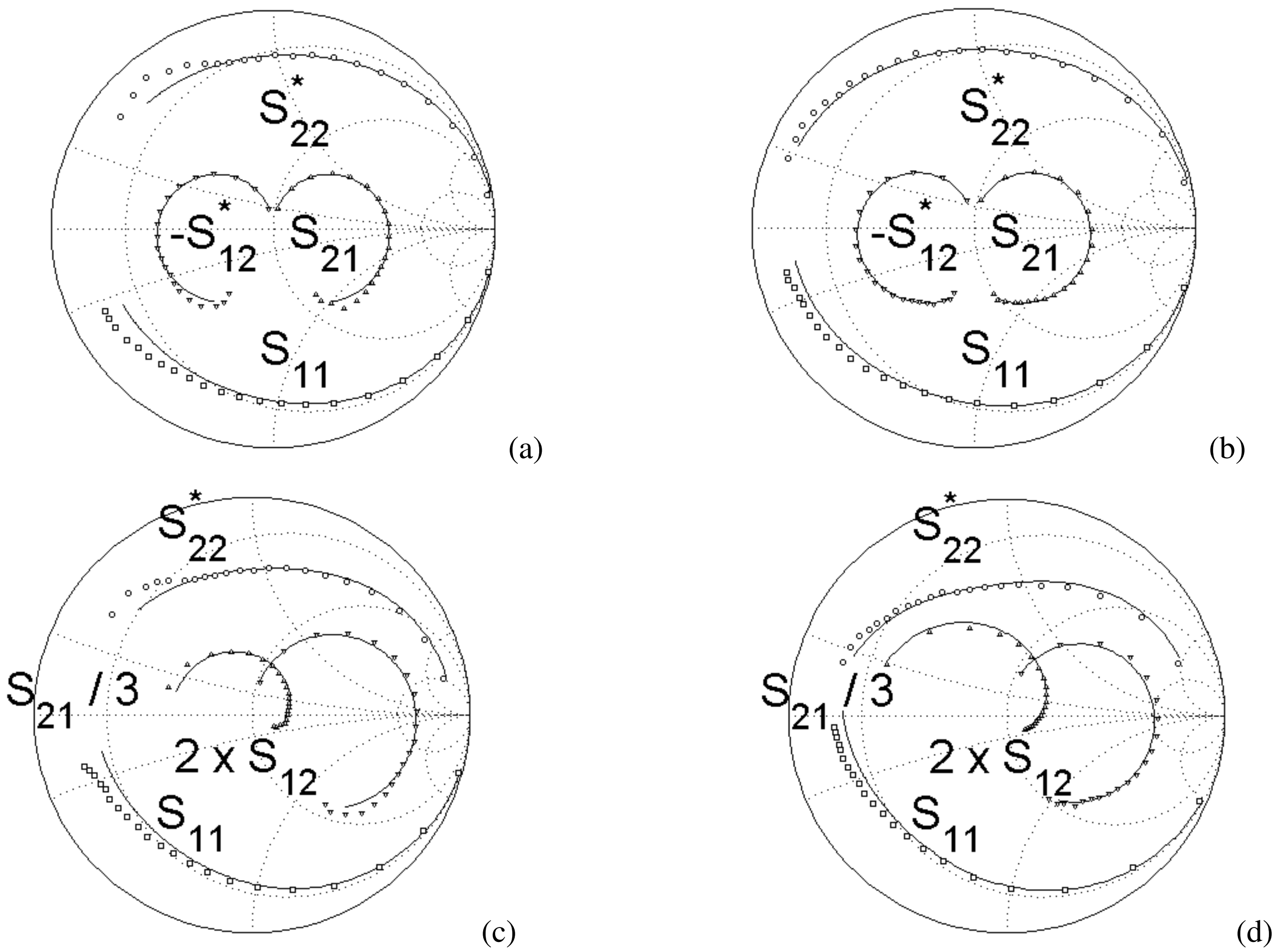
300	0	-1	3.6	3.4	3.4	4.1
200	0.5	-0.8	4.8	6.3	4.2	4.7
300	0.5	-0.8	4.4	8.2	3.2	5.6
200	-0.5	-0.5	5.2	5.6	22.2	7.3
300	-0.5	-0.5	3.7	9.9	32.6	6.2



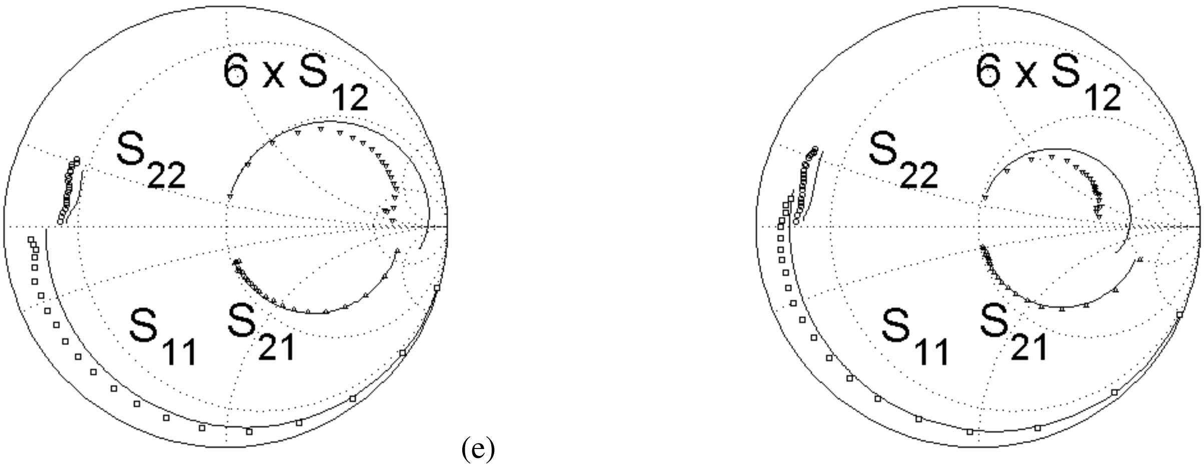
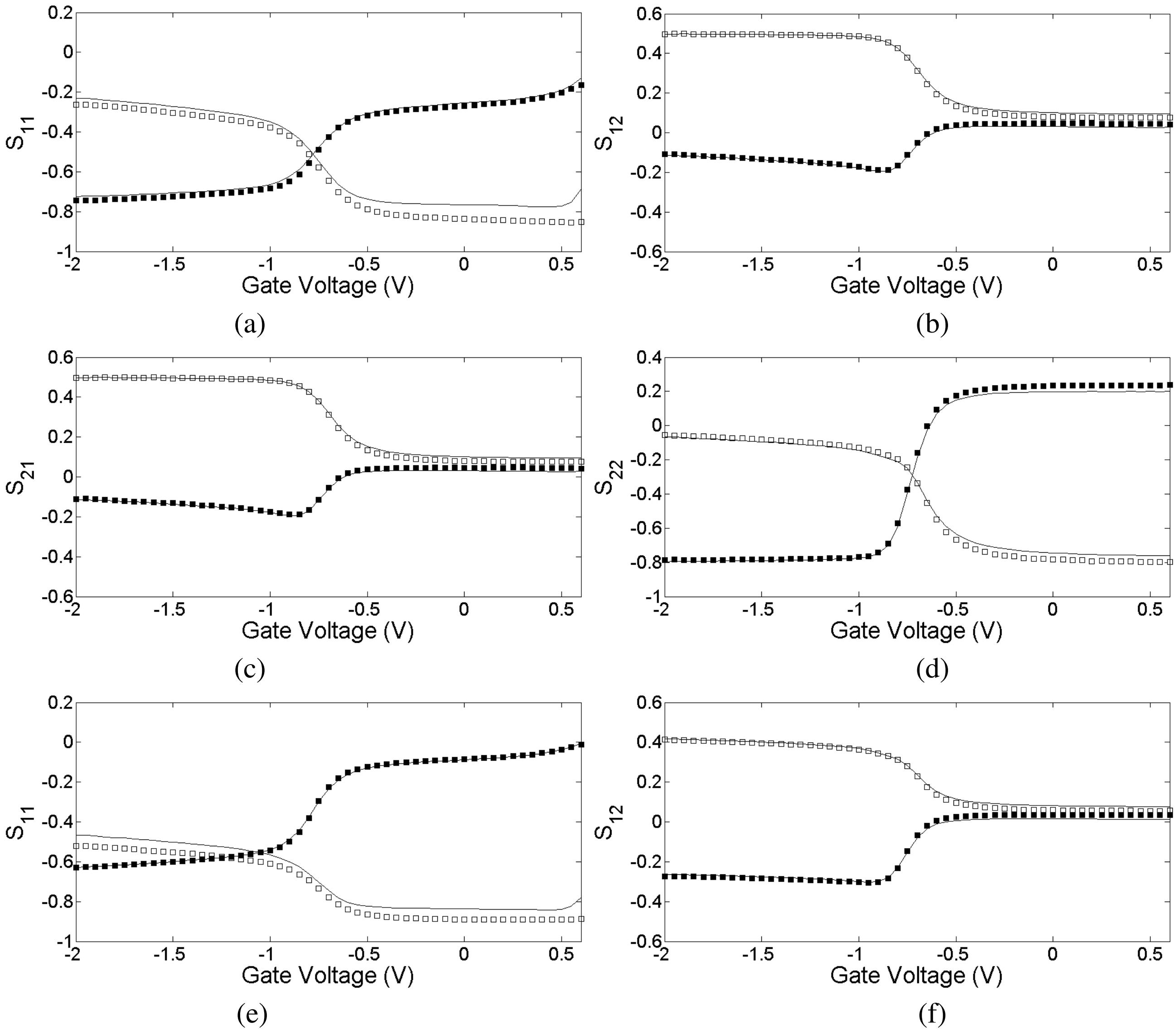
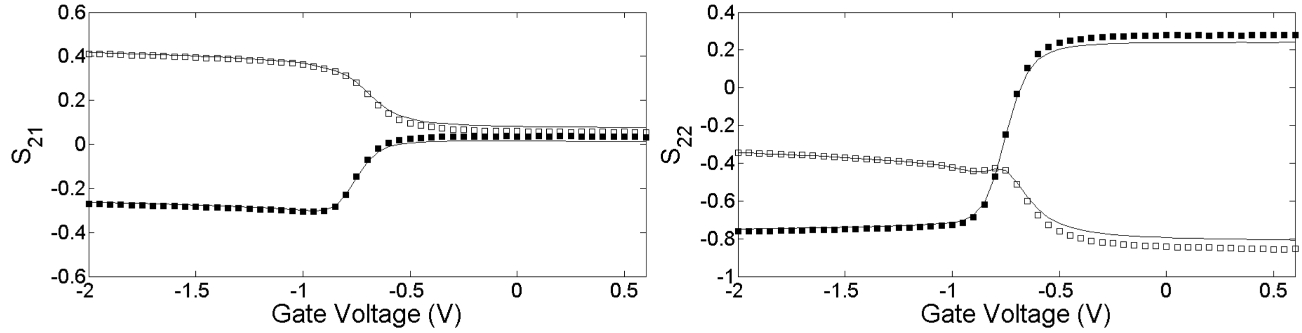


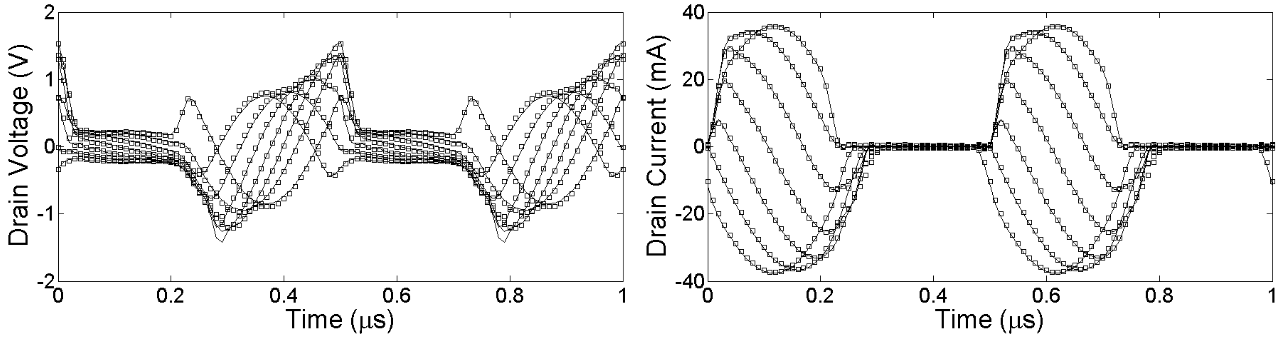
Fig. 5. Comparison between measured (symbols) and simulated (lines) S-parameters from 2.5 GHz to 65 GHz for two GaAs pHEMTs with different gate widths: 200 μm (a, c, e) and 300 μm (b, d, f). The three analyzed bias conditions are: V_{DS} = 0 V and V_{GS} = -1 V (a, b), V_{DS} = 0.5 V and V_{GS} = -0.8 V (c, d), V_{DS} = -0.5 V and V_{GS} = -0.5 V (e, f).



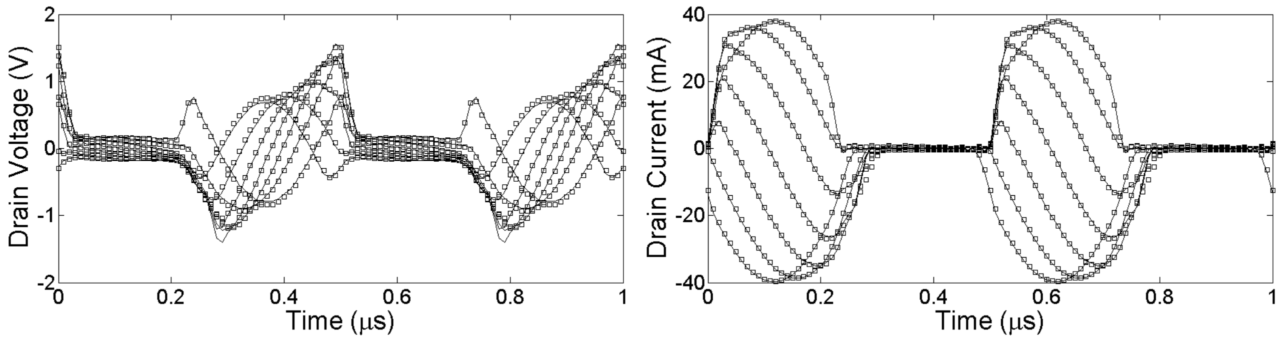


(g) (h)

Fig. 6. Comparison between measured (symbols) and simulated (lines) S-parameters versus V_{GS} from -2 V to 0.6 V with 50 mV step at 40 GHz and V_{DS} = 0 V for two GaAs pHEMTs with different gate widths: 200 μm (a, b, c, d) and 300 μm (e, f, g, h). The real and imaginary parts of the measured S-parameters are, respectively, represented with white and black symbols.

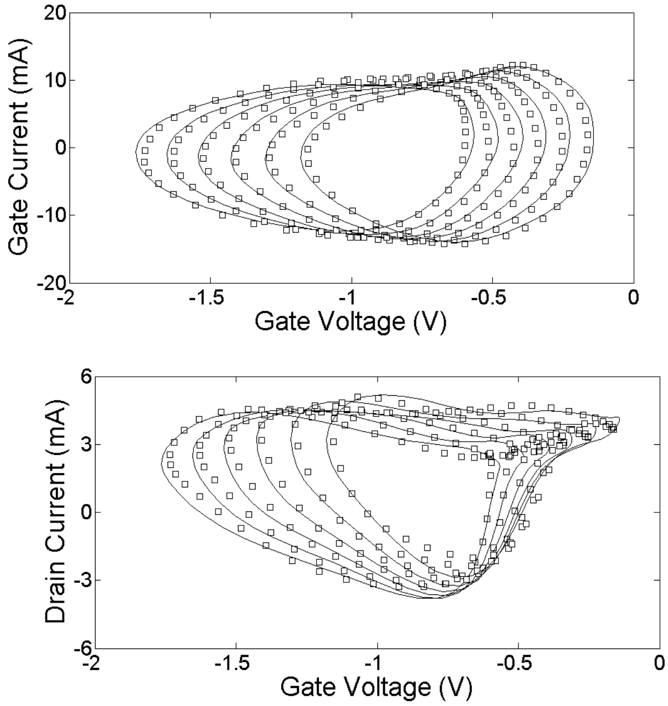


(a) (b)



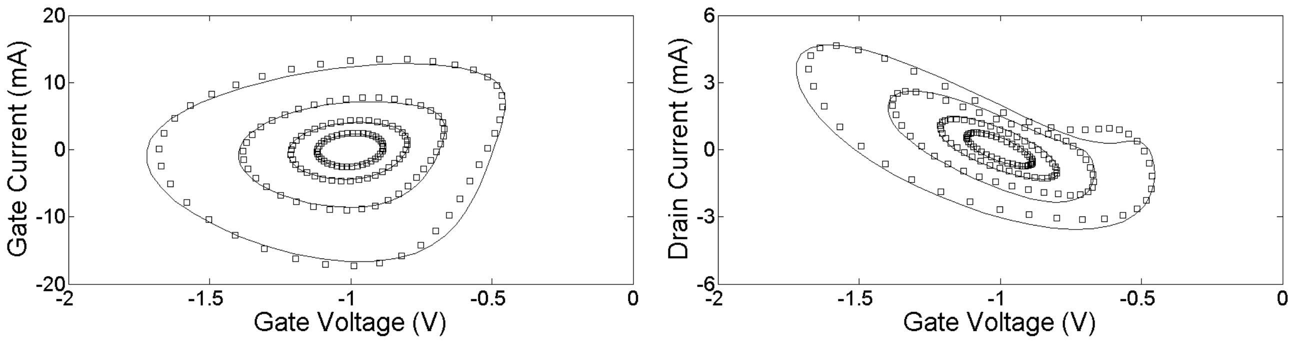
(c) (d)

Fig. 7. Comparison between measured (symbols) and simulated (lines) drain voltage and current time-domain waveforms at f_0 = 2 MHz, V_{DS} = 0 V, and V_{GS} = -1 V for two GaAs pHEMTs with different gate widths: 200 μm (a, b) and 300 μm (c, d). The amplitude of the input and output incident waves and their relative phase are respectively: A_g = 1.5 V, A_d = 1.5 V, and $\Delta\Phi$ = 0°, 30°, 60°, 90°, 120°, 150°, 180°.



(a) (b)

Fig. 8. Comparison between measured (symbols) and simulated (lines) input (a) and transfer (b) loci for a GaAs pHEMT with a gate width of 300 μm at f_0 = 10 GHz, V_{DS} = 0 V, and V_{GS} from -1.1 V to -0.6 V with a step of 0.1 V.



(a) (b)

Fig. 9. Comparison between measured (symbols) and simulated (lines) input (a) and transfer (b) loci for a GaAs pHEMT with a gate width of 200 μm at f_0 = 15 GHz, V_{DS} = 0 V, V_{GS} = -1V and with four different values of the input power: -10.8 dBm, -5.8 dBm, -0.8 dBm, and 4.2 dBm.

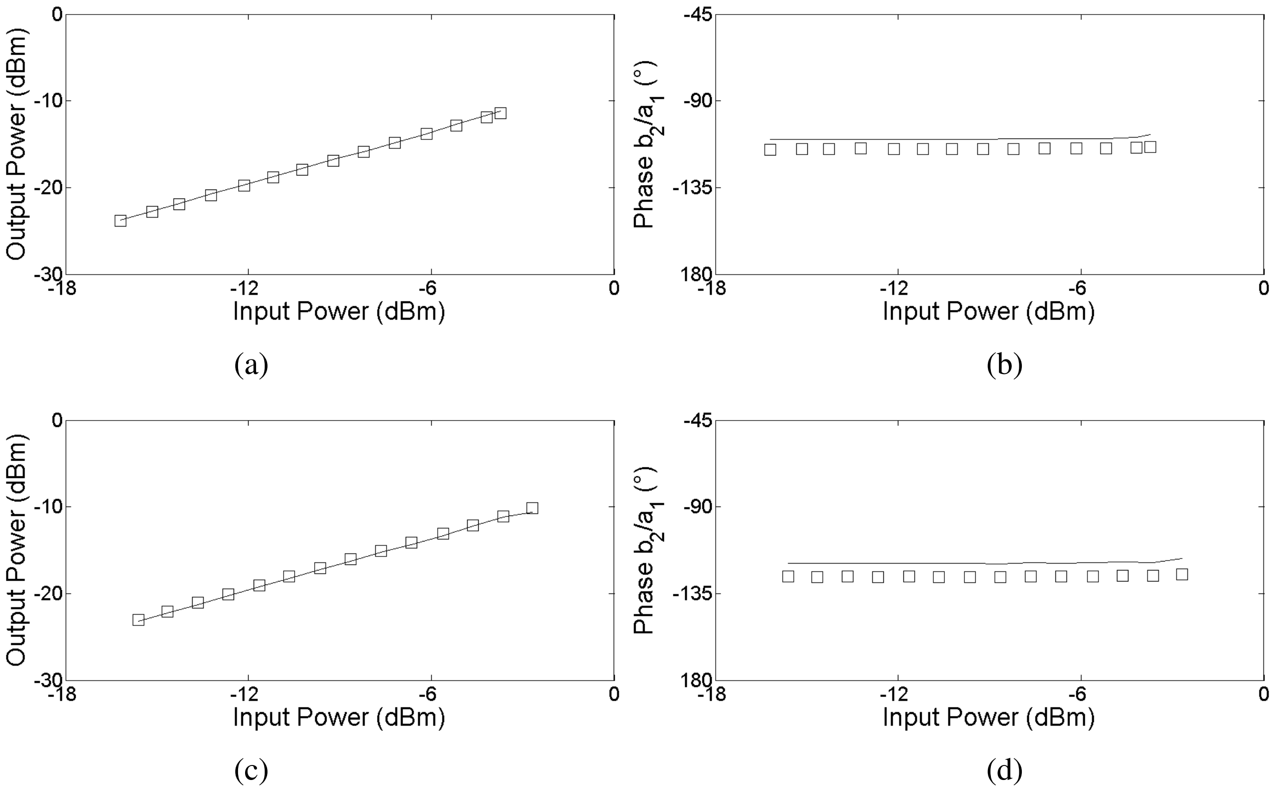


Fig. 10. Comparison between measured (symbols) and simulated (lines) output power and b_2/a_1 phase versus input power for a GaAs pHEMT with a gate width of 300 µm at f_0 = 38 GHz (a) and 42 GHz (b), V_{DS} = 0 V, and V_{GS} = -1 V.

5. Model validation based on cold-FET mixer design

To definitely validate the developed model, simulations and measurements of a cold-FET mixer are reported. The mixer is part of a packaged Q–band up-converter (see Fig. 11), which integrates on the same MMIC two single balanced cold-FET mixers in I/Q configuration, a frequency quadrupler, which is able to convert the X-band LO input into the Q-band pump signal (PS) required for the mixers, and a four-stage RF driver, cascaded to the cold FET mixers [51]. A photograph of the designed up-converter is presented in Fig. 12. In order to better relate the cold-FET model accuracy with the measurements, the comparisons are performed between the stand alone measured mixer and the corresponding simulated circuit. In Figs. 13 and 14 the simulated performance of the designed up-converter is compared with the data obtained from scalar measurements. In particular, the conversion gain and the

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image rejection are reported in Figs. 13 and 14, respectively. Also in this case, the model prediction capability is successfully confirmed.

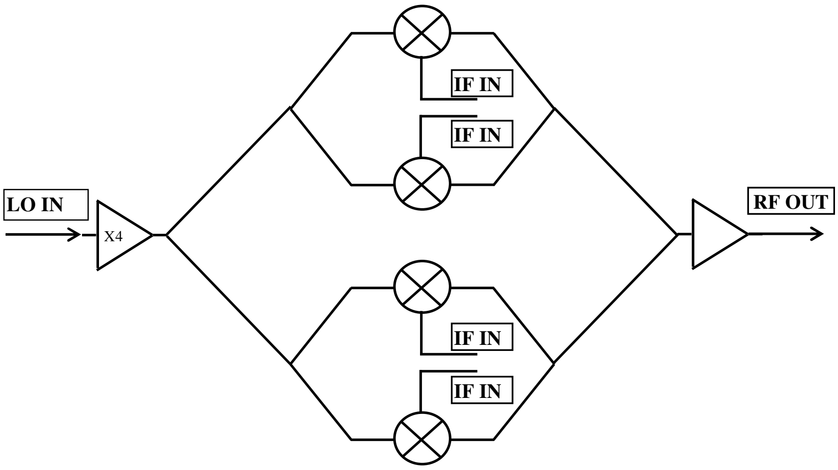

Fig. 11. Block diagram of the designed Q-band up-converter.

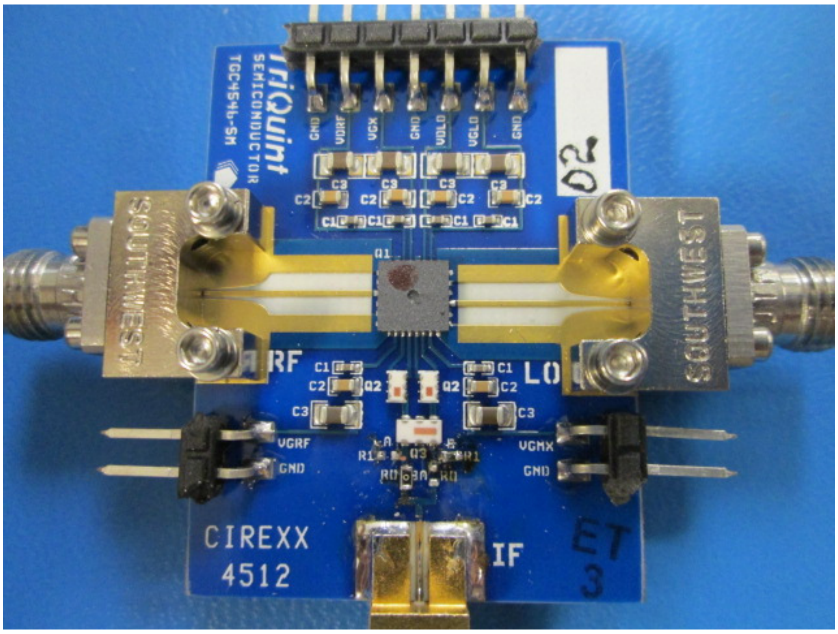

Fig. 12. Photograph of the designed Q-band up-converter.

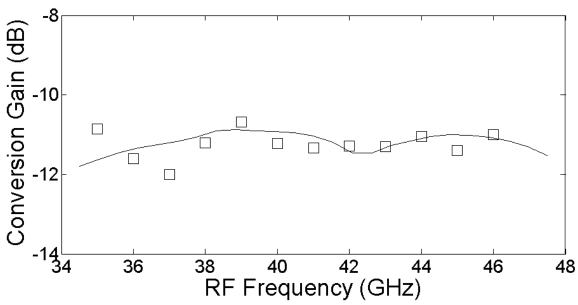

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Fig. 13. Comparison between measured (symbols) and simulated (lines) conversion gain of the up-converter with an LO power of 14 dBm and an IF frequency of 2.5 GHz.

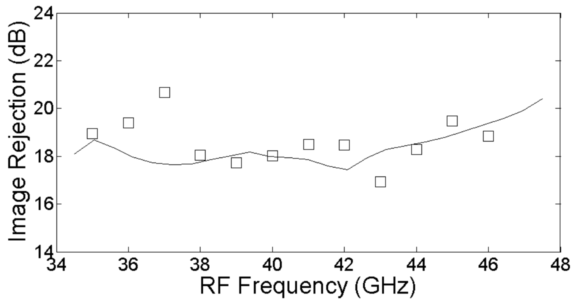

Fig. 14. Comparison between measured (symbols) and simulated (lines) image rejection of the up-converter with an LO power of 14 dBm and an IF frequency of 2.5 GHz.

6. Conclusion

This study has been devoted to the extraction of a nonlinear equivalent circuit of GaAs pHEMTs for mixer design. The developed approach, which is based on a straightforward extraction technique and transistor representation, leads to accurate and robust results. The model has been determined by using a purely analytical approach without any optimization and its representation has been based on look-up tables. The robustness of the achieved model has been confirmed by its capability to accurately predict the measured nonlinear device behavior for different gate widths and under different operating conditions: bias point, frequency, and input power level. Finally, to definitely validate the developed modeling approach, the extracted model has been used for the design of a packaged Q–band up-converter based on cold-FET mixer and a good agreement has been obtained between its measured and simulated performance.

Acknowledgments

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