

# Impact of inter-cell and intra-cell variability on forming and switching parameters in RRAM arrays

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**Abstract**—The inter-cell variability of the initial state and the impact of d.c. and pulse forming on inter-cell variability as well as on intra-cell variability in TiN/HfO<sub>2</sub>/Ti/TiN 1T-1R devices in 4 kbit memory arrays were investigated. Nearly 78% of devices on particular arrays were d.c. formed with a wordline voltage  $V_{WL} = 1.4$  V and a bitline voltage  $V_{BL} = 2.3$  V, whereas 22% devices were not formed due to the combined effect of the extrinsic process-induced inter-cell variability of the initial state and intrinsic inter-cell variability after d.c. forming. Furthermore, pulse-induced forming with pulse widths on the order of 10  $\mu$ s ( $V_{WL} = 1.4$  V,  $V_{BL} = 3.5$  V) caused for 86% of devices a low resistance state. Using a retry algorithm, we achieve 100 % of formed devices. To assess and confirm the nature of the variability during forming operation and during cycling the quantum point-contact (QPC) model was considered. The modeling results demonstrate a relationship between the forming and the device performance. The cells requiring large energy for forming operation, due to impurities in the HfO<sub>2</sub> deposition during array processing, are those subject to poor switching performance, larger variability, and faster wear-out. Devices formed by pulse-retry algorithm show (i) shorter endurance and (ii) higher variability during cycling.

**Index Terms**—4 kbit RRAM array, Inter-cell variability, Intra-cell variability, Hafnium dioxide (HfO<sub>2</sub>), Pulse-induced forming, Quantum point-contact (QPC) model.

## I. INTRODUCTION

RECENT advances in the performance of resistive random access memory (RRAM) have led to significant interest in system-on-chip applications in Si-based CMOS technologies, in particular for microcontrollers in wireless sensor nodes and in automotive electronics [1], [2]. For sensor nodes, the integration of energy-efficient microcontrollers with RRAM could provide the prospect of completely autonomous systems. In electric cars, energy-efficient microcontrollers for internal states storage in complex control units are inevitable due

to the relatively low energy supply resources. Hence, recent hardware-based approaches focus on the integration of HfO<sub>2</sub>-based RRAM in a microcontroller unit [3]. HfO<sub>2</sub> is one of the most promising transition metal oxides for RRAM with an ideal CMOS back-end-of-line compatibility. Thus considerable progress has been made in 1T-1R device integration as well as in understanding the physical/chemical properties of the resistance change behavior. Although memory arrays in the 1T-1R architecture demonstrated excellent performance parameters [4]–[7], the inter-cell variability (variations between cells) and intra-cell variability (cycle-to-cycle variations of any given cell) still prevents RRAM manufacturing from fast commercialization. While the intra-cell variability can be optimized for the particular memory cells, the inter-cell variability in memory arrays must be minimized [8]. Hence, several investigations on the extrinsic process-induced and intrinsic microscopic origin of the inter-cell and intra-cell variability after forming have been carried out in the recent past [9]–[14]. In this work, however, we first investigate the inter-cell variability of the initial state in memory arrays and then study the impact of d.c. and pulse forming on inter-cell variability as well as on intra-cell variability. To assess and confirm the nature of the variability during forming operation and during cycling the quantum point-contact (QPC) model was considered.

## II. DEVICES AND EXPERIMENTS

The bottom metal electrode of 150 nm TiN with a sheet resistance of 10-50  $\Omega$ /sq was prepared by physical vapor deposition (PVD) sputtering. 9 nm HfO<sub>2</sub> was deposited at 320 °C by the reaction of O<sub>2</sub> and tetrakis(ethylmethyamido)hafnium (Hf(NMeEt)<sub>4</sub>) onto TiN in an atomic vapor deposition (AVD) chamber. Finally, HfO<sub>2</sub> was capped by 7 nm ionized metal plasma (IMP) Ti and 150 nm PVD TiN [15]. To investigate the impact of inter-cell and intra-cell variability, 4kbit RRAM arrays with 600 × 600 nm<sup>2</sup> MIM area and with 890 × 965 nm<sup>2</sup> 1T-1R area were processed [16]–[18]. Memory array characterization was performed for 20 packaged memory arrays on a dedicated automated Active Technologies RIFLE system [16].

## III. RESULTS AND DISCUSSION

### A. Inter-cell variability in initial state and after d.c. forming

In this section, we present the influence of the d.c. forming process on the inter-cell variability. Forming was a prerequisite to induce stable resistance changes in our devices. This process

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TABLE I  
SUMMARY OF DC FORMING, PULSE-INDUCED FORMING, PULSE-RETRY FORMING, DC-RETRY FORMING, SET/RESET AND READ VOLTAGES.

	Bitline (BL) voltage $V_{BL}$	Sourceline (SL) voltage $V_{SL}$	Wordline (WL) voltage $V_{WL}$	Bitline (BL) pulse width $t_{BL, pulse}/$ Bitline (BL) sweep time
d.c. forming	0 V - 2.3 V	0 V	1.4 V	23 s
d.c. Set	0 V - 2.3 V	0 V	1.4 V	23 s
d.c. Reset	0 V	0 V - 2.3 V	2.2 V	23 s
Pulse-induced forming	3.5 V	0 V	1.4 V	10 $\mu$ s
Pulse-retry forming	3.5 V	0 V	1.4 V	10 $\mu$ s
d.c. retry forming	0 V - 3.5 V	0 V	1.4 V	-
Pulse set cycling	3 V	0 V	1.4 V	10 $\mu$ s
Pulse reset cycling	0 V	3 V	2.2 V	10 $\mu$ s
Reading	0.3 V	0 V	1.4 V	-

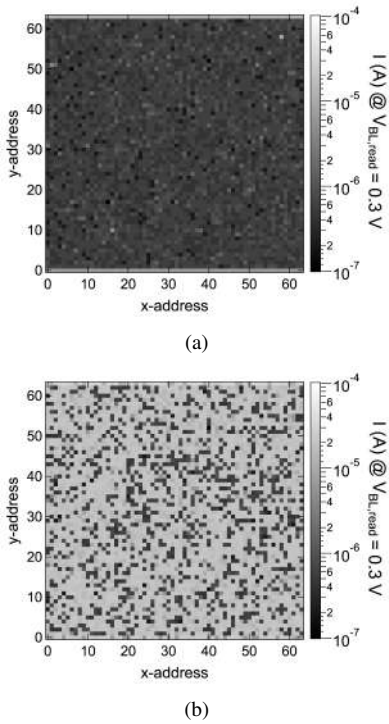


Fig. 1. Current distributions for a  $64 \times 64$  bit (4 kbit) RRAM array with 1T-1R devices with  $600 \times 600 \text{ nm}^2$  MIM area. (a) Initial state. (b) After forming in d.c. step sweep. The gate-source voltage was set to  $V_{WL} = 1.4 \text{ V}$  with a bitline voltage sweep to  $V_{BL} = 2.3 \text{ V}$  with ramp rate  $dV/dt = 0.1 \text{ V s}^{-1}$ . Current reading was performed at  $V_{WL} = 1.4 \text{ V}$  and  $V_{BL, read} = 0.3 \text{ V}$ .

consists in the application of a d.c. step sweep on the bitline (BL) to  $V_{BL} = 2.3 \text{ V}$  as well as grounding the sourceline (SL)  $V_{SL} = 0 \text{ V}$ . In contrast to d.c. voltage sweeps, current-driven d.c. step sweeps result in more reliable transitions into the bipolar switching mode in 1R devices by avoiding overshoot issues [19]. To prevent hard breakdown, the saturation current of the select transistor is controlled by the wordline (WL) voltage at  $V_{WL} = 1.4 \text{ V}$ . Table I summarizes the forming, set/reset and reading parameters in this work. In general, the forming process produces a non-destructive soft breakdown and progressive breakdown regime of the dielectric and requires a sufficiently high electric field across the  $\text{HfO}_2$  film thickness [20], [22], [23]. Due to the stochastic nature of the forming process or due to process-induced variations, the inter-

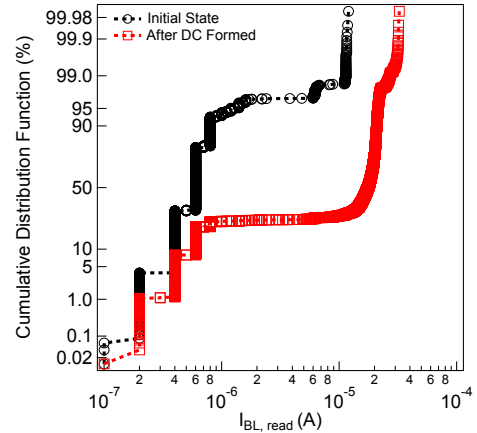


Fig. 2. Statistical current distributions of the initial state and after forming in d.c. step sweep. Current reading was performed at  $V_{WL} = 1.4 \text{ V}$  and  $V_{BL, read} = 0.3 \text{ V}$ .

cell variability of memory elements in a 4 kbit memory array cannot be neglected. To address this point, we first show in Fig. 1 the current distribution in the initial state which is defined by the combination of the Ti and  $\text{HfO}_2$  film thicknesses [18] and the current distribution after d.c. forming.

Statistical analysis in a cumulative distribution function plot in Fig. 2 reveals that only 78 % of the devices (red curve) were successfully formed by the d.c. step sweep, whereas 22% devices were not formed due to the high inter-cell variability of the initial state current. The thickness inhomogeneity of the PVD Ti layer with  $\sigma < 5\%$  standard deviation over the whole wafer diameter is believed not to play a central role in the inter-cell variability of the initial currents in Fig. 2 since the memory array with circuitry area is  $365 \times 752 \text{ } \mu\text{m}^2$ . When compared with Ti, the thickness inhomogeneity of the  $\text{HfO}_2$  film with  $\sigma < 2\%$  standard deviation should also be insignificant for the initial current inter-cell variability [24]. One reason could be the root mean square surface roughness of  $\text{HfO}_2$  films due to the columnar structure of the TiN bottom metal electrode [25], although a post-metallization annealing (PMA) step was applied which was reported to reduce the surface roughness [26]. To support this hypothesis it is shown in Fig. 3 the different root mean square values of the roughness profiles extracted from TiN and  $\text{HfO}_2$  films used in RRAM arrays processing. The randomly distributed inter-cell variability after

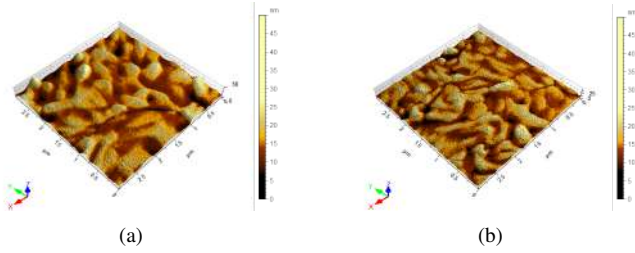


Fig. 3. Roughness profile of the TiN (a) and HfO<sub>2</sub> (b) films used in the array processing.

forming in d.c. step sweep is often related to intrinsic processes which involve microscopic transport of oxygen vacancies and permutations of filamentary clusters [9], [27], [28].

### B. Inter-cell variability in initial state and after pulse-induced forming

Recently, the pulse-induced forming has attracted wide attention as an alternative to d.c. forming. This pulse forming mode may reduce the operation current and the energy per unit volume imparted to the dielectric [29], [30]. Moreover, the forming time for the whole memory array can be reduced. To understand the pulse-induced forming process in more detail, we varied the forming parameters, namely  $V_{WL}$ ,  $V_{BL}$ , and the voltage pulse width  $t_{BL, pulse}$  on an adjacent memory array. For  $V_{WL} = 1.4$  V,  $V_{BL} = 3.5$  V, and  $t_{BL, pulse} = 10$   $\mu$ s, devices were formed, which is comparable to d.c. forming (see Fig. 2).  $V_{WL}$ ,  $V_{BL}$  in conjunction with  $t_{BL, pulse}$  are critical parameters to initiate the pulse-induced forming process. Simplified analytical models reproduce the statistical distribution of the forming voltage  $V_{BL}$  for each device in the memory array [31], [32]. The pulse-induced forming energy density (voltage  $\times$  current  $\times$  time/area) imparted to the dielectric for each cell reaches an average value of  $1.9 \times 10^{-9}$  J/ $\mu$ m<sup>2</sup> in comparison to  $3.7 \times 10^{-3}$  J/ $\mu$ m<sup>2</sup> after d.c. forming.

From a physical point of view, the pulse-induced forming may be appreciated with the shape of the created conductive filament: while pulses with low  $V_{WL}$  and  $V_{BL}$  voltages or short pulse width  $t_{BL, pulse}$  create narrow filaments showing low currents, higher  $V_{WL}$  and  $V_{BL}$  voltages or long pulse width  $t_{BL, pulse}$  create stable and wider filaments [33]. The filament diameter and areal density may be correlated with the concentration of oxygen vacancies that are supposed to participate in the filament formation process. The oxygen vacancies are predominantly produced at the Ti metal electrode as the result of redox processes of the oxide by the Ti metal electrode [34]–[36].

We applied thereafter these parameters to a fresh memory array. Figures 4(a) and 4(b) show the current distributions of the initial state and after pulse-induced forming. Statistical analysis in a cumulative distribution function plot in Fig. 5 reveals that 86 % of the devices were formed by the pulse process. A retry-algorithm was then implemented to form the remaining devices. The retry operations have been mostly required on cells with low initial currents. One reason could be that devices with a lower initial current need a higher energy density imparted to the dielectric to be formed. Forming with

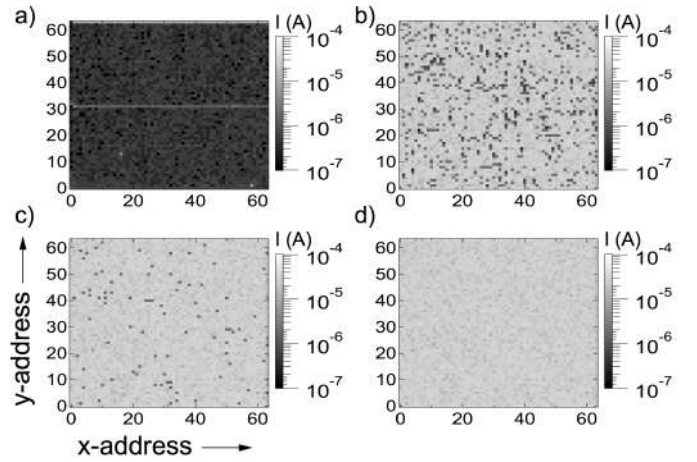


Fig. 4. Current distributions for a  $64 \times 64$  bit (4 kbit) RRAM array with 1T-1R devices with  $600 \times 600$  nm<sup>2</sup> MIM area. (a) Initial state. (b) After pulse-induced forming.  $V_{WL}$  was set to 1.4 V with  $V_{BL} = 3.5$  V and  $t_{BL, pulse} = 10$   $\mu$ s: total 86 % formed. (c) After applying a retry-algorithm to unformed devices: total 97.6 % formed. (d) After d.c. forming of the devices not formed by the retry step: total 100 % formed. Current reading was performed at  $V_{WL} = 1.4$  V and  $V_{BL, read} = 0.3$  V.

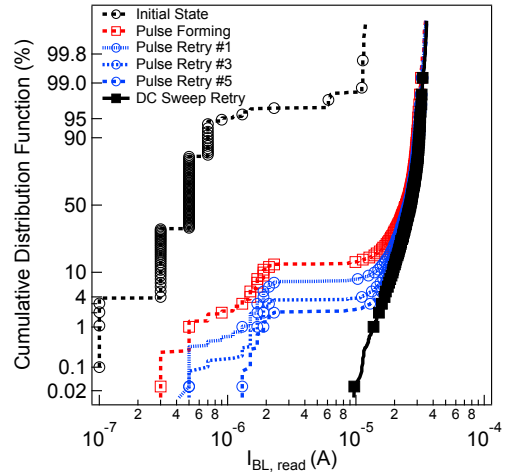


Fig. 5. Statistical current distributions of the initial state, after pulse-induced forming and after application of retry-algorithms. Current reading was performed at  $V_{WL} = 1.4$  V and  $V_{BL, read} = 0.3$  V.

the same parameters as before was applied 5 times on BLs with unformed devices. This increased the fraction of formed devices in the array to 97.6% (Figs. 4(c) and 5). The remaining 2.4 % devices could be formed by a d.c. forming step (Figs. 4(d) and 5). After forming, positive  $V_{SL}$  step sweeps with  $V_{WL} = 2.2$  V and  $V_{BL} = 0$  V reset the devices to the high resistance OFF state. Positive  $V_{BL}$  step sweeps with  $V_{WL} = 1.4$  V and  $V_{SL} = 0$  V set the devices to the low resistance ON state (Table I). The OFF/ON resistance contrast on repeated switching cycles remains typically between 1.4 to 10.

### C. Intra-cell variability in set/reset endurance and after bake

We performed set/reset pulse operations after pulse forming and after pulse-retry forming to evaluate the cycling endurance (Fig. 6). 70 % of the devices formed with the first forming

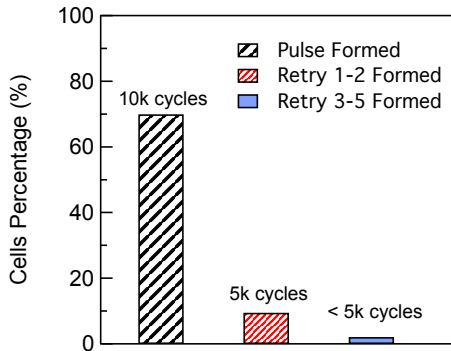


Fig. 6. Set/reset cycling endurance after pulse-induced forming and after pulse-retry forming.

pulse show the highest endurance, whereas almost 16 % of them evidenced resistance switching issues after a possible over-forming process [40].

As the number of forming-retry pulses increases, the resistance switching capability of the conductive filament is strongly impacted: retry-formed cells show lower cycling endurance compared to single-pulse formed cells. The retrieved endurance of  $10^4$  cycles is significantly lower than what retrieved for similar arrays [33], [41] and this could be attributed to the impact of impurities in the metal-organic AVD precursor, in particular to carbon [36]. To support such a consideration, Fig. 7 shows a XPS depth profile measurement of a 50 nm thick  $\text{HfO}_2$  deposited on a silicon substrate. Since the cells embedded into the array are too small for the analysis, XPS profile has been measured on cells with a higher  $\text{HfO}_2$  stack, but processed with the same deposition parameters used for the MIM cells in the array. A high presence of carbon and nitrogen atoms can be observed: these impurities are caused by the liquid metal-organic precursor, used for the AVD deposition process. Their presence severely limits the oxide performance and wears the cells in the array faster than any other degradation mechanism.

To evaluate the relationship between forming conditions and endurance, formed cells with a single pulse, after 1, 3, 5 forming-retry pulses and after d.c. step sweep were considered (Tab. I). Figures 8 (a) and 8 (b) show the average and minimum (i.e. considering the worst-case condition) read window calculated during cycling for each cell subset [16]. For all cell subsets both average and minimum read window decrease with increasing number of cycles.

Figure 9 (a) shows the ON state (LRS) intra-cell variability during cycling, which indicates decrease for each cell subset. The highest variability is observed on cells formed after 5 pulse-retry algorithms and after d.c. step sweeps. Similar behavior is observed for the OFF state (HRS) intra-cell variability during cycling in Fig. 9 (b). The reduction of the intra-cell variability during cycling is given by the fact that a consecutive set/reset operation brings all cells toward a uniform wear-out condition of the conducting filament, therefore reducing the fluctuations due to structural modifications of the conduction path in the memory cells [11].

In order to investigate the reason underlying different

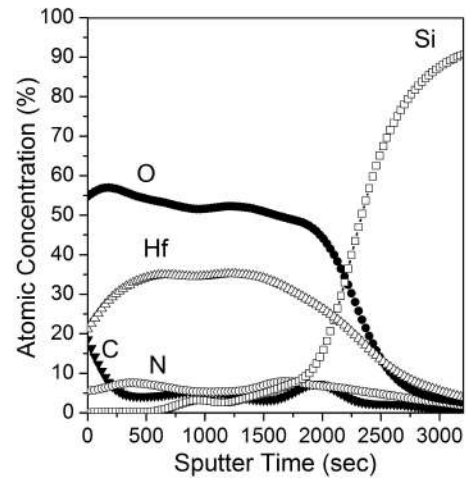


Fig. 7. XPS depth profile measurement of a 50 nm thick  $\text{HfO}_2$  RRAM cell.

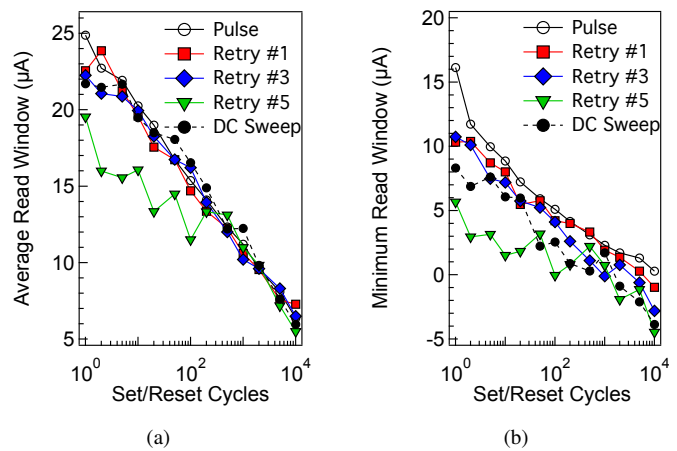


Fig. 8. (a) Average and (b) minimum read window after a single pulse, after 1, 3, 5 forming-retry pulses and after d.c. step sweep.

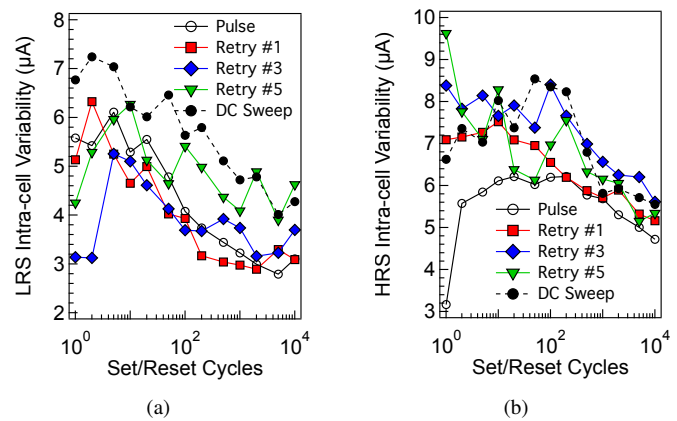


Fig. 9. Intra-cell variability during  $10^4$  pulse set/reset cycling for (a) LRS and (b) HRS.



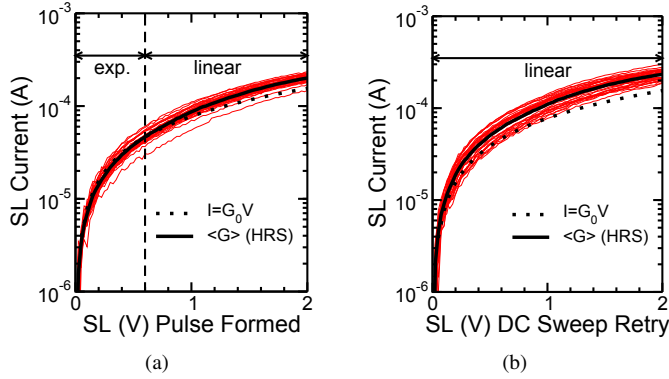


Fig. 10. HRS I-V curves measured on cycled devices after Reset on cells formed with a single pulse (a) and with DC sweep retry operation (b).

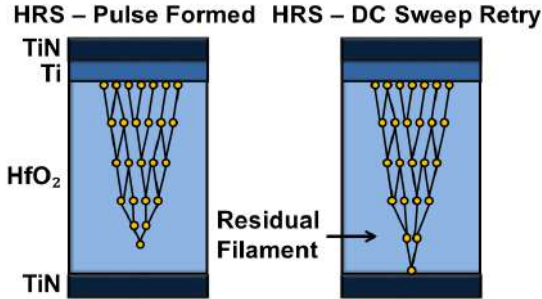


Fig. 11. Schematic showing the conductive filament shape after reset (HRS) for Pulse and DC Retry formed cells.

degradation speed for different forming retry times, I-V measurements of the Reset operation have been performed at endurance cycle  $10^4$ . Fig. 10 shows HRS I-V curves of the cells formed with a single pulse (a) or with DC sweep retry operations (b). The black dashed line shows the limit  $I = G_0 V$  with  $G_0 = 2e^2/h$  equal to the quantum conductance unit corresponding to the creation of a single mode nanowire according to Quantum Contact Point (QPC) model [20], where  $e$  is the electron charge and  $h$  the Planck's constant. The average  $\langle G \rangle$  curves measured after Reset is shown for sake of comparison. Within this framework, in case of  $I > G_0 V$  the presence of a residual conductive filament has to be taken into account. Cells formed with a single pulse show lower average conductance values after Reset, even after cycling. Moreover, on single pulse formed cells an exponential ( $V_{SL} < 0.6V$ ) plus linear ( $V_{SL} > 0.6V$ ) current behavior can be observed since  $\langle G \rangle$  is very close to  $I = G_0 V$  limit, whereas only linear behavior is observed on  $\langle G \rangle$  of DC sweep retry formed cells. This indicates that for single pulse formed cells, the filament geometry after cycling in reset condition still evidences a potential barrier giving rise to direct tunneling transport through a material barrier or through a residual confinement barrier (QPC) [30] (i.e., the exponential part of the curve), whereas for DC sweep retry formed cells only the ohmic component is present due to worn-out filament (see Fig. 11). Fig. 12 shows the cumulative distribution of conductance values measured after Reset operation of cells formed at different retry steps: cells formed with a higher number of retry operations show higher conductance values and intra-

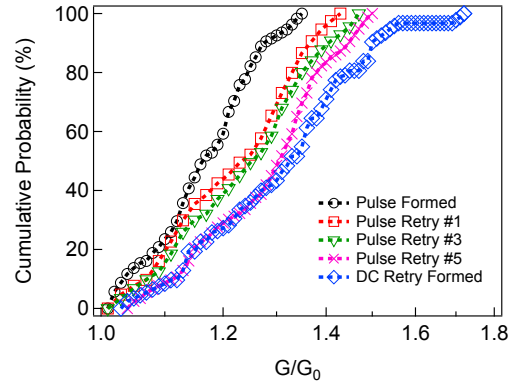


Fig. 12. Cumulative distribution of conductance values measured after Reset on cycled cells.

cell variability. More retry steps allow the cells to reach a more stable state resulting in higher conductance values yet displaying lower switching capabilities. More energy is indeed required in these cells in order to create the conductive filament compared to single pulse formed cells, hence it can be expected that even during cycling a higher set/reset energy was required to create/disrupt the filament on such cells. Due to such lack of energy, a higher intra-cell variability is observed since set/reset operations were not correctly performed on all retry-formed cells.

Figure 13 shows the cumulative distribution function plots for the first (a) and for the  $10^4$  (b) cycle for pulsed set/reset operations. A 24-hour temperature bake at  $125^\circ\text{C}$  has been applied before and after set/reset cycling on different arrays. The LRS and HRS average currents do not show any relevant variation after bake for both fresh and cycled devices (Tab. II).

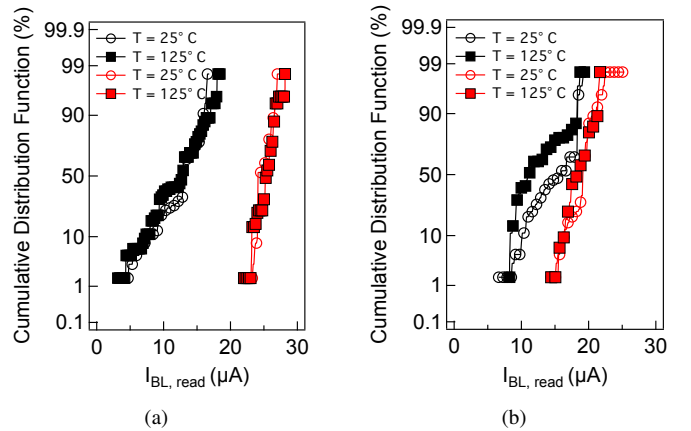


Fig. 13. Statistical current distributions of the temperature bake at cycle (a) 1 and after (b)  $10^4$  set/reset cycles for the LRS state (red curves) and for the HRS state (black curves) obtained with the following set/reset pulse conditions:  $V_{BL/SL} = 3V$  and  $t_{BL, pulse} = 10 \mu\text{s}$  (Tab. I).

#### IV. CONCLUSION

This paper has presented results on the inter-cell variability of the initial state and the impact of d.c. and pulse forming on inter-cell as well as on intra-cell variability in 4kbit memory arrays. 100 % of devices in a memory array must be formed

TABLE II  
HRS/LRS STATISTICS BEFORE AND AFTER A 24 HOURS TEMPERATURE  
BAKE AT 125 °C.

	Cycle 1		Cycle 10 <sup>4</sup>	
	$\mu$ ( $\mu$ A)	$\sigma$ ( $\mu$ A)	$\mu$ ( $\mu$ A)	$\sigma$ ( $\mu$ A)
HRS (25 °C)	11.9	3.7	13.1	3.0
HRS (125 °C)	11.8	3.7	12.1	4.1
LRS (25 °C)	25.2	1.1	18.5	2.7
LRS (125 °C)	25.3	1.3	18.5	1.8

to guarantee a product maturity level for RRAM, however, we observe that on particular arrays only 78 % are d.c. formed. The insights suggest a combination of the extrinsic process-induced variability of the initial state and intrinsic variability after forming as origin. Pulse-induced forming was achieved by choosing 10  $\mu$ s pulses as well as by  $V_{BL} = 3.5$  V and  $V_{WL} = 1.4$  V. These parameters were applied to the memory array. Using a retry algorithm, we achieve 100 % of pulse-formed devices. However, the endurance of retry-formed devices decreased faster compared to pulse-formed devices with a single pulse. One possible physical explanation for the endurance degradation could be impurities in the metal-organic AVD precursor. The fitting of the I-V curves after different pulse forming steps by using the QPC model offers a route to the understanding of the degradation process within a physical framework.

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