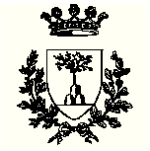

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DOTTORATO DI RICERCA IN
"SCIENZE DELL'INGEGNERIA"

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DESIGN TECHNIQUES FOR HIGH-EFFICIENCY MICROWAVE POWER AMPLIFIERS

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Per una vita a colori, insieme…

Contents

Preface: vii

Prefazione: ix

Chapter 1 *Microwave power amplifier design techniques* 1

Introduction 3

1.1 Load-Pull design approach 4

1.2 Iterative Harmonic balance analysis approach 7

1.3 Nonlinear modeling for microwave power amplifier design 9

Conclusion 11

References 13

Chapter 2 *A new approach to microwave power amplifier design* 17

Introduction 19

2.1 A low-frequency large-signal measurement setup 20

2.1.1 Investigation of low-frequency dispersion by exploiting the proposed setup 22

2.1.2 Large-signal measurements for high-efficiency operation 26

2.2 The proposed design approach 31

2.2.1 Class-A power amplifier design example 37

2.2.2 Wideband Class-AB power amplifier design example 40

2.3 Power amplifier design accounting for input large-signal matching 44

2.3.1 Power amplifier design and realization 45

Conclusion 49

References 50

Chapter 3 *High-efficiency power amplifier design* 53

Introduction 55

3.1 Design scenario for class-F and class-E power amplifiers 56

3.2 Class-F power amplifier design 58

3.3 Class-E power amplifier design 67

Conclusion 73

References 74

Chapter 4 *Degradation phenomena of electron devices in microwave power amplifier design* 77

Introduction 79

4.1 The innovative measurement system 80

4.2 Analysis of the gate current as a suitable indicator for GaAs FET degradation 81

4.2.1 Theoretical overview 82

4.2.2 Experimental results and considerations 83

4.3 Empirical study of performance degradation of X-band GaN HEMTs 92

4.3.1 DC characterization 92

4.3.2 Low-frequency large-signal characterization 94

4.3.3 Small-signal characterization 96

Conclusions 98

References 99

General conclusion 101

List of publications 103

Ringraziamenti 105

Preface

The increasingly diffusion of wireless devices during the last years has established a sort of "second youth" of analog electronics related to telecommunication systems. Nowadays, in fact, electronic equipments for wireless communication are exploited not only for niche sectors as strategic applications (e.g., military, satellite and so on): as a matter of fact, a large number of commercial devices exploit wireless transmitting systems operating at RF and microwave frequencies.

As a consequence, increasing interest has been focused by academic and industrial communities on RF and microwave circuits and in particular on power amplifiers, that represent the core of a wireless transmitting system. In this context, more and more challenging performance are demanded to such a kind of circuit, especially in terms of output power, bandwidth and efficiency.

The present thesis work has been focused on RF and microwave power amplifier design that, as said before, represents one of most actual and attractive research theme. Several aspects of such topic have been covered, from the analysis of different design techniques available in literature to the development of an innovative design approach, providing many experimental results related to realized power amplifiers. Particular emphasis has been given to high-efficiency power amplifier classes of operation, that represent an hot issue in a world more and more devoted to the energy conservation. Moreover, electron device degradation phenomena were investigated, that although not directly accounted for, represent a key issue in microwave power amplifier design.

In particular, the first chapter of this thesis provides an overview of commonly adopted design methodologies for microwave power amplifier, analyzing the advantages and the critical aspects of such approaches. Moreover, nonlinear device modeling issues oriented to microwave power amplifier design have been dealt with.

In the second chapter, an innovative design technique is presented. It is based on experimental electron device nonlinear characterization, carried out by means of a low-frequency large signal measurement setup, in conjunction with the modeling of high-frequency nonlinear dynamic phenomena. Several design examples have been carried out by exploiting the proposed approach that confirm the effectiveness of the design technique.

In the third chapter, the proposed design methodology has been applied to high-efficiency power amplifier classes of operations, that need to control the device terminations not only at the fundamental frequency, but also at harmonics. Two high-efficiency power amplifiers have been

realized by adopting such a technique, demonstrating performance in terms of output power and efficiency comparable with the state of the art.

Finally, in chapter four an important power amplifier design aspect has been dealt with, related to degradation and performance limitation of microwave electron devices. Several experimental results have been carried out by exploiting a new measurement setup, oriented to the characterization of degradation phenomena of microwave electron devices.

Prefazione

Negli ultimi anni, la crescente diffusione dei sistemi wireless ha segnato una sorta di "seconda giovinezza" dell'elettronica analogica. Diversamente da quanto accadeva fino a qualche anno fa, le apparecchiature elettroniche che sfruttano sistemi di telecomunicazioni senza fili non sono necessariamente legate a settori di nicchia, come per esempio quelli militari o per applicazioni spaziali: oggigiorno infatti, la maggior parte dei dispositivi elettronici commerciali, dai telefoni cellulari ai tablet PC, integrano al loro interno sistemi wireless che operano a radiofrequenza o a microonde.

Tale contesto ha suscitato un altrettanto crescente interesse scientifico, sia accademico che legato ai settori di ricerca industriali, sui circuiti operanti a radiofrequenza e a microonde ed, in particolare, sugli amplificatori di potenza, che rappresentano l'elemento cardine di un sistema di trasmissione senza fili e ai quali sono richieste prestazioni sempre più stringenti in termini di potenza, efficienza e banda operativa.

L'oggetto di questa tesi di dottorato riguarda appunto la progettazione di amplificatori di potenza operanti a microonde, che, come detto in precedenza, rappresenta uno dei temi di ricerca più attuali e interessanti. In particolare, si sono analizzate diverse tecniche di progettazione presenti in letteratura, evidenziandone i vantaggi e gli aspetti più critici, arrivando all'introduzione di una nuova metodologia di progetto che supera le limitazioni delle tecniche di progetto più comuni. Tale metodologia è basata su misure sperimentali a bassa frequenza effettuate sfruttando un sistema di misura innovativo e a basso costo, garantendo comunque, grazie all'impiego di una adeguata descrizione degli effetti reattivi, lo stesso livello di accuratezza ottenibile con costosi sistemi di misura operanti a microonde, come dimostrato dai diversi risultati sperimentali proposti.

Particolare enfasi è stata dedicata al progetto di amplificatori di potenza ad alta efficienza, argomento di particolare interesse scientifico in virtù della crescente sensibilità relativa alle tematiche legate al risparmio energetico. Inoltre, è stato approfondito il problema del degrado delle prestazioni dei dispositivi elettronici che, sebbene non sia direttamente preso in considerazione dai progettisti di amplificatori di potenza, rappresenta un tema centrale nella progettazione di tali circuiti.

Nello specifico, nel corso del primo capitolo verranno analizzate approfonditamente le tecniche di progettazione di amplificatori di potenza presenti in letteratura, affrontando anche tematiche di modellistica di dispositivi elettronici per applicazioni a microonde.

Nel secondo capitolo, verrà presentata una metodologia di progetto innovativa, basata sulla caratterizzazione sperimentale di dispositivi elettronici in congiunzione con il modeling degli effetti non lineari dinamici degli stessi. Diversi risultati sperimentali verranno forniti a dimostrazione dell'efficacia della tecnica di progettazione proposta.

Nel terzo capitolo, la metodologia di progetto sviluppata verrà applicata alle classi di funzionamento ad alta efficienza, che prevedono il controllo delle terminazioni dell'amplificatore non solo alla frequenza fondamentale, ma anche alle sue armoniche. Inoltre, verranno descritti nel dettaglio il progetto e la realizzazione di due amplificatori di potenza ad alta efficienza operanti a microonde, progettati adottando la tecnica proposta, che hanno dimostrato prestazioni in termini di potenza ed efficienza in linea con lo stato dell'arte.

In conclusione, nel quarto capitolo si analizzeranno i fenomeni di degrado e le limitazioni delle prestazioni che coinvolgono i dispositivi elettronici orientati alla progettazione di amplificatori di potenza per applicazioni a microonde. Anche in questo caso, la trattazione sarà corredata da diverse evidenze sperimentali, ottenute sfruttando un sistema di misura sviluppato all'uopo.

Chapter 1

Microwave power amplifier design techniques

Introduction

During the last decades, microwave circuits have found a growing diffusion due to the increasing number of electronic systems, from commercial devices (e.g., smartphone, personal computer) going to strategic applications (e.g., radar, satellite), that exploit wireless transmitting systems operating at microwave frequencies.

In this scenario, microwave power amplifiers play a crucial role since they represent the key component of a transmitting chain: as a matter of fact, overall performance of the entire transmitting system strongly depends on the performance of such a kind of circuit.

To date, the great advantages introduced by solid state technology, in terms of costs, size of the circuit and so on, have progressively replaced the vacuum tube domain in microwave power amplifier development: as a consequence, increasing interest of both academic and industrial research community has been focused on more- or less-conventional solid state power amplifier (SSPA) design methodologies, based on both mature (e.g., GaAs) or emerging (e.g., GaN) technologies, in order to meet the severe requirements of the modern wireless transmitting systems.

In this chapter, commonly adopted design strategies for microwave SSPAs will be treated, pointing out the advantages and the critical aspects of such methodologies, that are usually based on both experimental characterization of the electron device (e.g., high-frequency load-pull measurements) and iterative harmonic balance analysis, performed by exploiting computer aided design (CAD) simulators.

Moreover, nonlinear modeling of electron devices oriented to microwave application will be briefly discussed, focusing on the issues related to the design of microwave power amplifiers.

1.1 Load-Pull design approach

One of the crucial design facet of a microwave high power amplifier is to find out the correct input and output terminations that ensure adequate performance. Such a task is made highly hard due to the nonlinear behavior of the active electron devices, that represent the keystone of power amplifier operation under large signal conditions.

A typical and widely used approach in order to characterize the nonlinear behavior of an active electron device and consequently adopted for design of a high power amplifier, is represented by load/source-pull measurements [1-5]. The great advantage of adopting such a technique is represented by the capability of testing the electron device under actual large signal operating conditions: fixed the bias condition, the load/source-pull technique, in fact, consists in varying source and load impedances of a device under test (DUT), while simultaneously measuring the DUT performance at different input driving stimuli. Thus, measurement data collected by exploiting the load/source-pull technique, can be directly used in order to obtain information about the optimal source and load impedances for a specific electron device class of operation.

Load pull measurement systems can be classified in two main categories, depending on the technique adopted for the impedance synthesis [6]: *passive* and *active* load pull setups.

In traditional passive load pull systems, in order to synthesize the required source and load impedances, mechanical or electrical tuners (that consist of passive networks) are exploited. On the other hand, in the active systems, the required terminations are set by adopting a couple of phase- and amplitude- controlled RF signal generators.

Fig. 1.1 shows a block diagram of a passive load-pull measurement system:

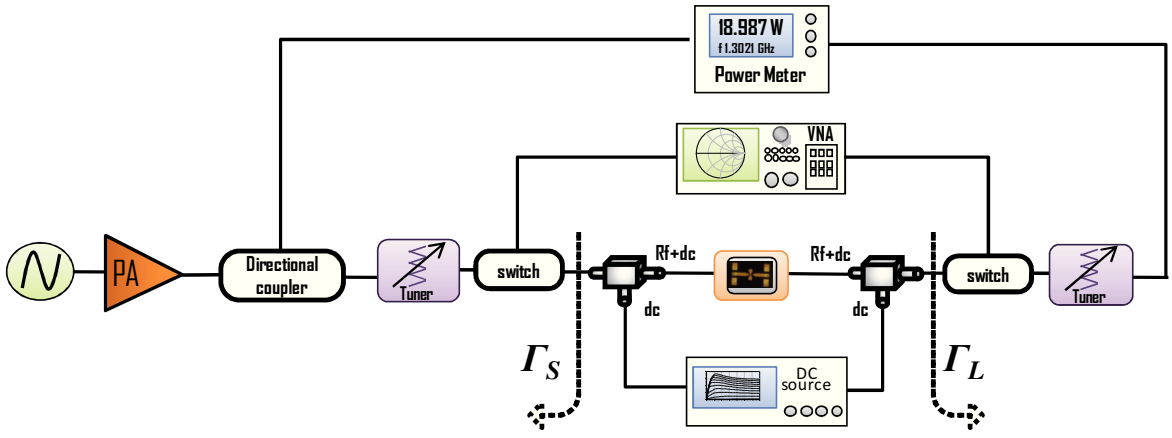

Fig. 1.1 Typical configuration of Load/source-pull passive measurement system

The input signal is monitored by a directional coupler and measured by a power meter. The input tuner is exploited in order to optimize the input match assuring the maximum power delivery to the device. The reflection coefficient Γ_S, that is the actual source impedance, can be set to any desired value within a certain region of the Smith chart, depending on the frequency of operation besides the system capabilities. At the output port another tuner allows to set Γ_L: as well as Γ_S, load reflection coefficient Γ_L can be set within a limited portion of the Smith chart. The second channel of the power meter is exploited in order to measure the output power delivered by the DUT, whereas the bias is supplied by a DC source through a couple of bias tees.

Passive load pull systems need a power- and frequency-calibration before performing measurements. The calibration of the setup is carried out through a VNA: all the setup portions have to be characterized in terms of two ports S-parameters in order to properly evaluate impedance and power levels at the DUT planes. The power level is calibrated by a power meter measurement with the DUT replaced by a thru connection.

After calibration, a standard de-embedding technique can be used to calculate the correct quantities. Load-pull measurements are exploited in order to trace power contours on the Smith chart, which represents a very powerful tool that provides information on the best performance achievable by the device. A constant performance parameter (i.e. power, PAE, etc.) can be displayed as a curve of corresponding measured impedances on the Smith chart.

An example of contours obtained by measurements carried out at different frequencies through a passive load pull measurement system [3] is shown in fig. 1.2:

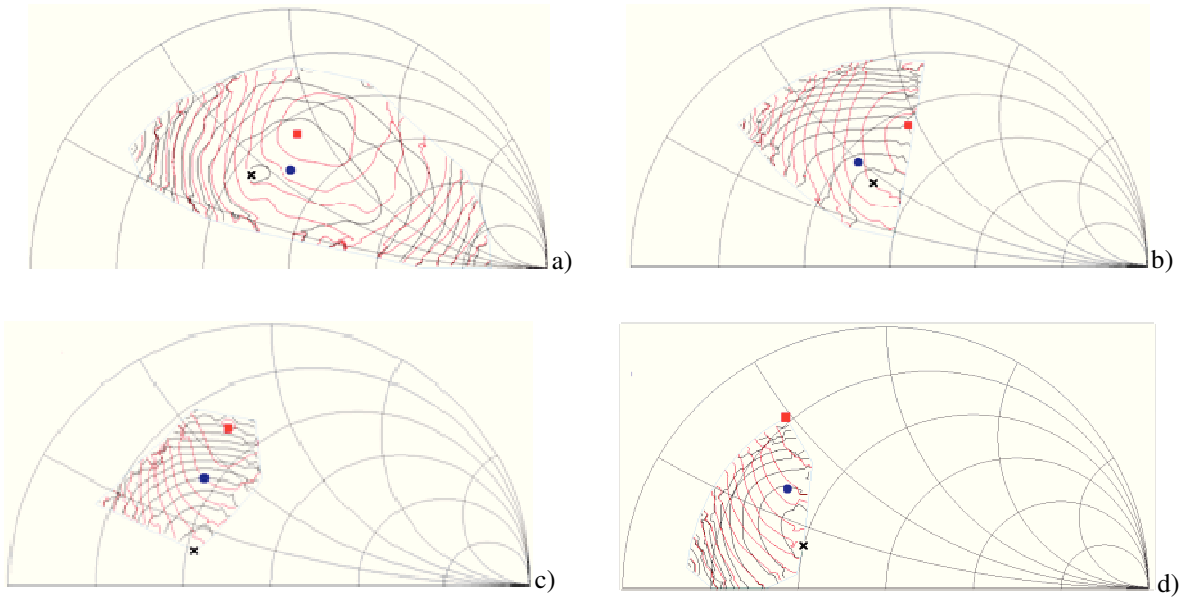

Fig. 1.2. Output-power (black) and efficiency (red) contours measured by means of a 4–26 GHz load-pull setup (at 2.5 dB gain compression) at 4 GHz a), 5 GHz b), 6 GHz c), and 7 GHz d) fundamental frequency. Best output power (cross) and best PAE (square) terminations.

Fig 1.3 shows a diagram of an active load/source-pull system. A large amplitude signal is provided by the RF signal generator and is divided into two signals that drive each port of the DUT. The two variable attenuators and the phase shifter control the power levels and the relative phase of the two incident waves at the input and output ports. Before the signal reaches the network analyzer bidirectional couplers, switches and filters work on lowering the power level of the signal itself to avoid damage of the instrumentation. Isolators are used to protect sensitive components from the high power levels. As well as for the passive load-pull, calibration is also needed for the active one.

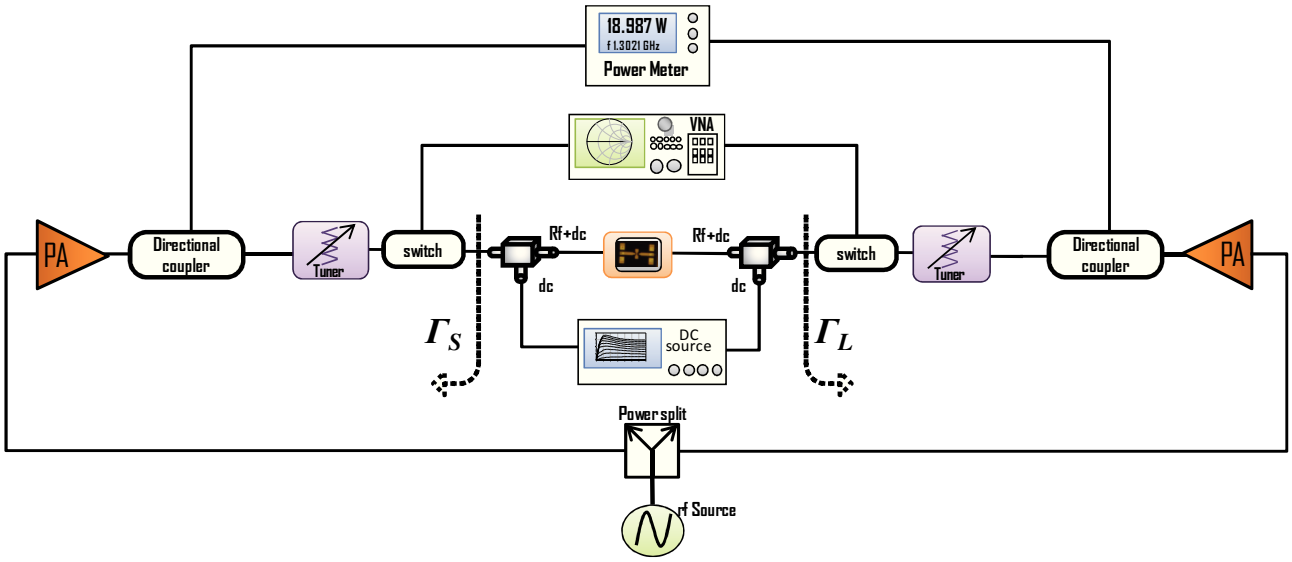

Fig. 1.3 Typical configuration of Active load/source- pull passive measurement system

Another classification regarding load/source-pull setups can be made on the basis of the nature of the measured quantities, i.e. whether information of device figures of merit are acquired through a *scalar* or *vectorial* techniques. Typical scalar systems, as the previously described setups, are generally based on the acquisition of the magnitude of input and output power trough a power meter (or in alternative through a spectrum analyzer). On the other hand, vectorial systems are based on the acquisition of both magnitude and phase of the electrical quantities of interest; consequently, time domain waveforms referred to the DUT terminals can be measured exploiting such a kind of setups and, for this reason, they are generally called *time-domain load-pull systems.*

The time-domain load-pull approach combines the advantages to characterize the DUT under actual large-signal operation together with the knowledge of time-domain current and voltage waveforms at the device ports, enabling to perform waveform engineering technique [7] for microwave power amplifier design.

In order to obtain time-domain waveforms, two different approaches can be followed: sampler-based or mixer-based methodology [8]. A sampler-based measurement instrument uses samplers to perform the down conversion of the high-frequency signals to the IF spectrum and is hence based on the harmonic sampling principle. The large-signal network analyzer (LSNA) is an example of a sampler-based measurement instrument [9-11]. On the other hand, a mixer-based measurement instrument uses the heterodyne principle, which exploits mixers to downconvert the RF signals to the IF spectrum. This principle can be found in the nonlinear vector network analyzer (NVNA) [12], [13]. Recently, a third approach has been developed [14], that exploits an high performance oscilloscope in order to directly acquire time-domain electrical waveforms at microwave frequencies.

Although load-pull systems represent one of the most common aid in power amplifier design, they exhibit some critical aspects. Dealing with load-pull passive architectures, they suffer from the inability in synthesizing the full range of DUT terminations, in particular when very low impedances are needed for on-wafer devices having a large periphery. On the other hand, although active systems overcome such a limitation by adopting active load synthesis, they may become critical from the stability point of view [15].

Moreover, both architectures are frequency and power limited and their cost dramatically increases when high operating power and frequencies are required or when harmonic termination control is needed (e.g., high efficiency power amplifier design).

Finally, when performing load-pull measurements exploiting both scalar or vectorial setups, no information is given about the intrinsic device load-line: loading conditions which show similar microwave performance, in fact, can correspond to very different load-lines at the intrinsic device. This is a vital aspect, for example, for safe operation since reliability conditions are defined at the intrinsic DUT ports [16] as the passive access structures to the active area do not have any major impact on reliability.

1.2 Iterative Harmonic balance analysis approach

CAD simulations represent another diffused paradigm for microwave power amplifier design. Since such a kind of circuit is usually designed in order to work under nonlinear periodic regime, generally harmonic-balance simulators are adopted. The harmonic balance represents the main analysis technique exploited to solve nonlinear microwave circuits in steady-state conditions.

The original Harmonic-balance algorithm [17-20], applied to the solution of nonlinear electronic circuits, combines both time- and frequency-domain approaches, taking the benefits related to the respective representations. More precisely, the initial nonlinear circuit to solve, that is described by nonlinear equations inferred by combining the Kirchhoff laws and the constitutional relationship of each element of the circuit, is split in two subnetworks: in the first one, that is treated exploiting a time-domain technique, all nonlinear elements are gathered; on the other hand, a frequency domain approach is selected for the second network, that contains the linear portion of the circuit. The two subnetworks are connected through ports, whose number depends on the number of the nonlinear elements. With the aim of *balancing* the two subnetworks, the electrical variables at these ports are represented by their Fourier description and the results of the analysis of both subcircuits are combined minimizing the balancing errors at each harmonic component. With the advent of MMIC circuits which exploit a relatively large number of active devices, Harmonic-balance equations are more conveniently defined on a circuit-node basis.

Harmonic-balance algorithm is implemented in almost all commercial microwave CAD simulators, providing a powerful tool for power amplifier design: as a matter of fact, iterative harmonic-balance analysis could overcome the need for expensive load-pull measurement setups since load-pull contours could be traced using simulation results only.

However, iterative harmonic-balance design approach relies on availability of an electron device nonlinear model. Generally, electron device models oriented to microwave CAD applications are the so called empirical models, that represent the best solution for CAD simulations of a nonlinear circuit.

The identification of an empirical model is based on measurements carried out on the fabricated device. Moreover, they may include some knowledge of the physical structure of the device and they are usually referred as equivalent-circuit models, or they may be a powerful and flexible extrapolating/interpolating scheme, and referred as black-box models.

One of the most important limitations of harmonic-balance design approaches is strictly related on the accuracy of the electron device model adopted. In practice, the identification of a global and accurate model of an electron device oriented to microwave power amplifier design is a very hard task, due to the strong nonlinearities involved in the device behavior. As a matter of fact, electron device models, available for example from the foundries, provide accurate nonlinear performance predictions in a relatively narrow neighborhood of given bias and load conditions [21]. As a consequence, a designer is usually forced in considering a mix of design approaches, based on both large-signal experimental characterization of the electron device and iterative harmonic balance analyses.

1.3 Nonlinear modeling for microwave power amplifier design

Commonly adopted active devices for microwave power amplifier are represented by high electron mobility transistors (HEMTs) [22], that are field effect devices particularly suited for such an application due to their superior performance in terms of power, noise and maximum operating frequency. HEMTs for microwave applications are generally based on III-V compounds, as gallium arsenide (GaAs), that represents a mature technology and for many years the main resource in high-frequency applications, or gallium nitride (GaN), an emerging technology that is the strong candidate for high-power high-efficiency power amplifiers due to its higher breakdown voltage and operative temperature.

A simplified model topology of a HEMT device and, in general, of a field effect transistor (FET) is proposed in Fig. 1.4.

The linear extrinsic parasitic network in Fig. 1.4 describes the access passive structure to the device active area and accounts for metallization and dielectric losses as well as for associated inductive and capacitive effects. Its correct modeling is a fundamental issue to obtain accurate model predictions. Parasitic elements can be characterized by exploiting conventional lumped descriptions [23-24], which can be identified by only using small-signal measurements, or, alternatively, by adopting electro-magnetic simulations of the device layout [25-26].

As clearly shown in Fig. 1.4, the "intrinsic device" can be divided into two parts, which can be considered strictly in parallel: a "capacitive core" describing the nonlinear dynamic phenomena, and a "resistive core" accounting for the dc and low-frequency (LF) I/V device characteristics. The latter one differ from the dc response due to surface state densities, deep-level traps and thermal phenomena.

The ED resistive core modeling is extremely complex, not only because a number of important nonlinear phenomena must be considered (e.g., breakdown, forward conduction of the gate-source diode, knee of the I\V curves, etc..) but also due to the non negligible presence of dispersive effects [27-31], which, de facto, impose the exploitation of nonlinear dynamic measurements in order to obtain good prediction capabilities.

In order to probe further this issue we must consider that the drain and gate currents at the intrinsic ED ports, above the cut-off of LF dispersive effects (i.e., some hundreds of kilohertz) but at frequencies low enough to neglect the reactive effects related to the capacitive core, can be expressed as follows:

$$i_g(t) = h\left(\underline{v}(t), P_0, \theta_{case}\right)$$
$$i_d(t) = f\left(\underline{v}(t), \underline{V}_0, P_0, \theta_{case}\right) \quad (1)$$

In (1), h and f are two algebraic (i.e., memory-less) functions, $\underline{v}$ is the vector of the intrinsic voltages, $\underline{V_0}$ its average value, $\underline{P_0}$ the average dissipated power, and, lastly, Θ_{case} is the device case temperature.

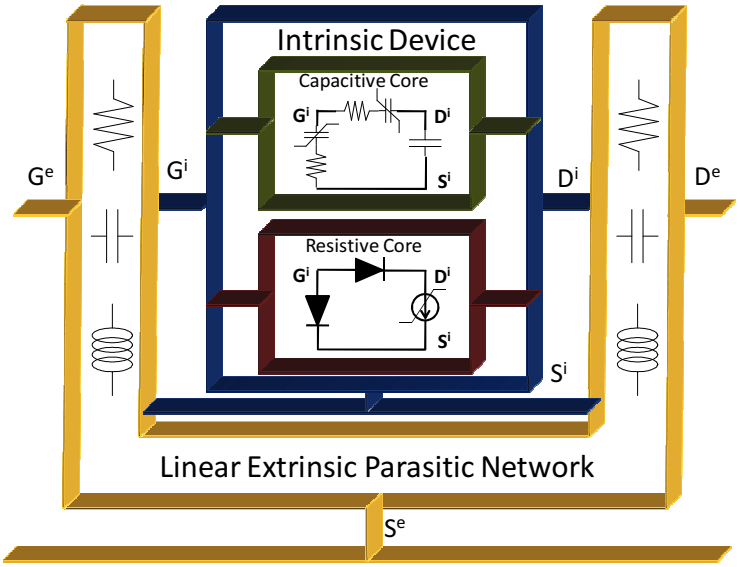

Fig. 1.4: Nonlinear equivalent circuit for an FET Electron Device.

The dependence on $\underline{V_0}$ accounts for the influence of traps and surface state densities [27-31], while $\underline{P_0}$ and Θ_{case} determine, through the thermal resistance, the device I\V characteristic dependence on the junction temperature.

Identification of (1), in particular the drain current equation, is quite a prohibitive task mostly due to the complex dependence on its large number of controlling variables. Moreover, traps and thermal effects cannot be separately dealt with, both because the time constants of those phenomena are not always different and also since the device thermal state influences the trapping state [28]. Thus identification of (1) necessarily requires the introduction of suitable approximations to make the problem affordable.

As far as the capacitive core is concerned, dispersive phenomena due to traps and thermal behavior represent second order effects (whose evidence has rarely been dealt with in the literature

[22]) regularly neglected in electron device models oriented to power amplifier design [22], [32-35]. A π model of capacitors is often adopted for the capacitive core description, nevertheless better prediction capabilities can be obtained at higher frequencies by introducing gate-source and gate-drain RC series, as shown in Fig.1.4, to describe nonquasi-static effects which accounts for a finite device memory time [22], [32-33]. Other nonquasi-static phenomena can be described in terms of trans-capacitances or delay times.

Provided a careful de-embedding of the parasitic network is carried out, small-signal, bias/frequency-dependent S-parameter measurements are usually sufficient to accurately determine the voltage-dependent capacitive-core parameters. These ones can be "fitted" trough suitable analytical expressions, or directly stored into look-up tables [34-37] to build a nonlinear dynamic model. Even problems related to charge conservation, although dealt with in the literature, do not seem to represent a major problem once suitable expedients are adopted [38-40].

Dealing with the resistive core behavior, a number of modeling approaches have been proposed in the literature [27-31] both based on look-up tables or analytical expressions. Some of them introduce assumptions which enable the models to be identified on the basis of bias-dependent dc and ac small-signal differential measurements carried out above the cut-off of low-frequency dispersion. However, in practice, model accuracy is commonly improved by exploiting in the identification phase, besides ac and dc measurements, also large-signal dynamic measurements as, for instance, pulsed I\V characteristics [41-42].

Despite the use of quite expensive, special-purpose pulsed I\V setup's, the identification of an accurate, global model for the resistive core still remains a very complex and hard task and this justifies why foundry models often properly work in a limited number of given quiescent bias conditions: typically, a limited set of pulsed I\V measurements is fitted. Such a kind of approach inevitably leads to local models which cannot provide accurate information outside the range of the few quiescent bias conditions considered. This clearly represents a strong limitation in power amplifier design based on harmonic-balance analysis.

Conclusion

In this first chapter, a panoramic view of commonly adopted design methodologies for microwave power amplifiers has been provided, putting in evidence both advantages and limitations in adopting the described approaches. Particular attention has been paid to design techniques based on the experimental characterization of the ED through large-signal measurement setups and on the

harmonic-balance analysis. Moreover, an overview of ED nonlinear modeling issues oriented to microwave power amplifier design has been given.

In the next chapter, an innovative design technique will be described, that overcomes the limitations of the methodologies described in this chapter, combining the main advantages related to each technique.

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Chapter 2

A new approach to microwave power amplifier design

Introduction

In the previous chapter, an overview of commonly adopted design methodologies for microwave power amplifier has been presented. High-frequency large-signal setups have been dealt with. Although they represent the most common aid for power amplifier design since electron devices are characterized under actual operating conditions, however they are frequency and power limited, and their cost dramatically increases when high operating power and/or frequencies are required. On the other hand, it was pointed out that the availability of an accurate model could overcome the need for experimental measurements (e.g. load-pull measurements) by using simulation results only: unfortunately, the identification of a global and accurate electron device model is a very hard task due to its nonlinear behavior.

In this chapter, a nonlinear measurement system based on low-frequency multi-harmonic excitation will be presented, that allows to characterize the electron device behavior under large signal operation. Such a setup enables given source/load terminations at fundamental and harmonic frequencies to be easily synthesized and results particularly suited to investigate low-frequency dispersion phenomena (i.e., long-term memory effects) affecting microwave devices. To this end, several experimental results based on GaN devices will be discussed.

In this chapter, an original approach to power amplifier design will be also introduced, which overcomes the major limitations of commonly adopted design methodologies discussed in the previous chapter. Such a technique is mainly based on low-frequency nonlinear experimental device characterization, carried out by exploiting the mentioned large signal setup, and shows the same level of accuracy provided by high-frequency large-signal measurements. In order to demonstrate

the effectiveness of the proposed design technique, several power amplifier examples will be proposed and the design and realization of a wideband hybrid high-power amplifier, based on a 20-mm GaN power bar, will be deeply investigated.

2.1 A low-frequency large-signal measurement setup

The architecture of the proposed large-signal low-frequency measurement system is shown in Fig. 2.1. In particular, the function generator has two 50-ohm channels that can independently provide arbitrary waveforms in the frequency range [1 mHz - 120 MHz]. To overcome the power limitation of the function generator, a 30-W power amplifier is cascaded to the channel devoted to the device output port excitation. Two wideband (10 kHz - 400 MHz) dual directional couplers monitor the DUT incident and reflected waves which are acquired by means of a four channel digital oscilloscope (4 GSa/s). A high resolution (4 μV; 20 fA) and accurate (V: 0.05%, I: 0.2%) DC source provides the bias for the DUT. To ensure DC and RF path isolation, two wideband (200 kHz - 12 GHz) bias-tees are used.

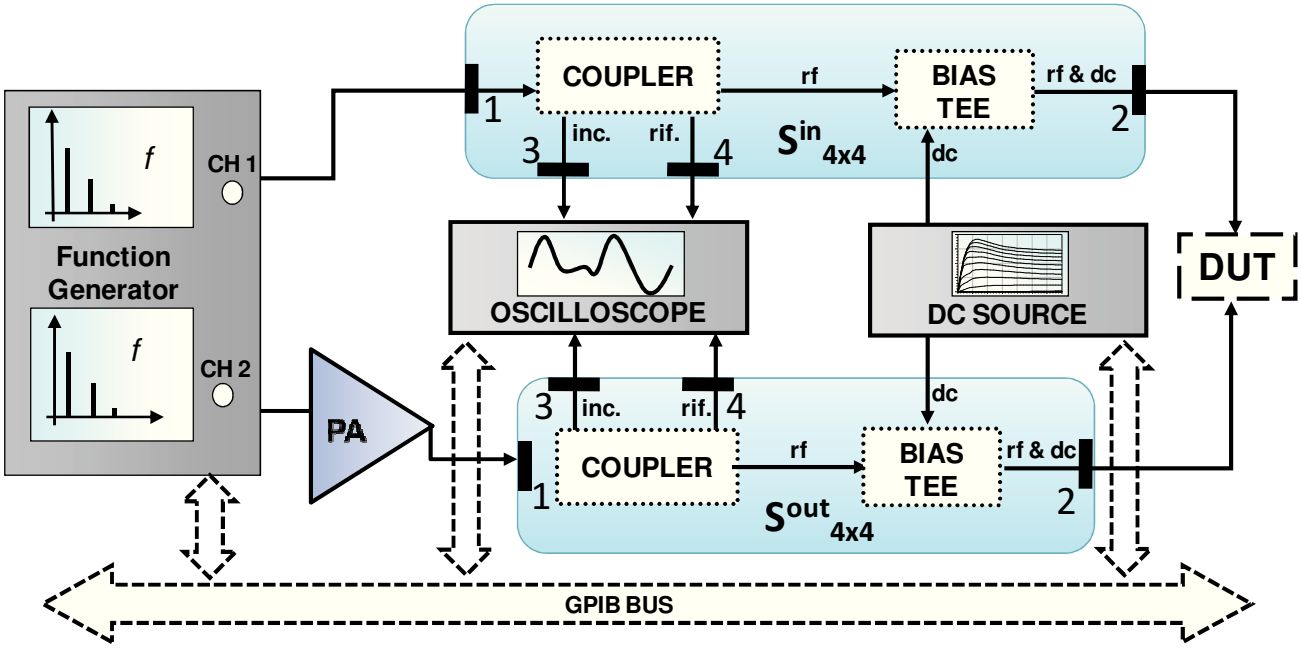


Fig. 2.1: Block diagram of the proposed measurement system.

In order to characterize only the device resistive core, that accounts for DC and low frequency I/V device behavior, it is necessary to operate at frequencies where the dynamic effects associated to charge storage variations and/or finite transit times can be neglected. Moreover, it is of primary

interest to characterize device response above the cut-off of low-frequency dispersion (this is why pulsed setups exploit very short pulse duration). To this end, a 2 MHz fundamental frequency has been found adequate for the considered electron devices. The validity of such a choice has been verified on the basis of S-parameter measurements carried out, in the frequency range [300 kHz – 98 MHz], by exploiting a low-frequency VNA. More precisely, Fig. 2.2 shows the measured output conductance, for a 0.25-µm GaN HEMT device having a periphery of 400 µm, under two different bias conditions corresponding respectively to class-A and AB operation. In the same figure also the output conductance DC values are reported to highlight that frequency variations in the range [2 MHz – 98 MHz] are negligible. This confirms that a 2 MHz frequency is sufficient to operate above the cut-off of low-frequency dispersion coherently with the large number of papers (e.g., [1]) devoted to microwave device characterization where pulsed measurements with pulse width of 500 ns or longer have been adopted.

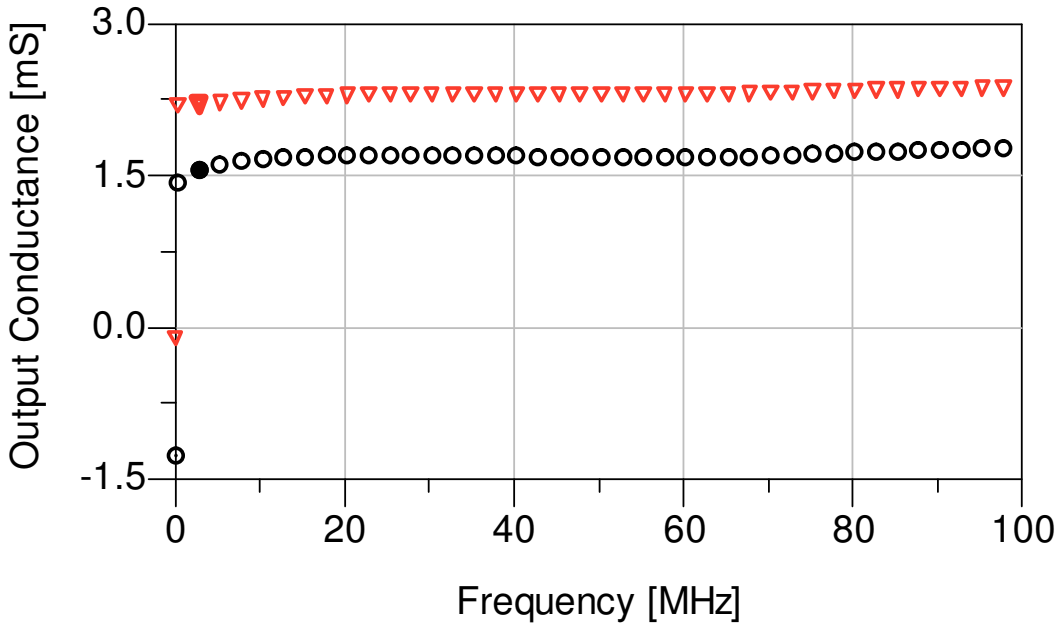


Fig. 2.1: 400-µm GaN HEMT output conductance versus frequency for two different bias conditions: V_{g0} = -3 V, V_{d0} = 20 V (triangles), and V_{g0} = -2 V, V_{d0} = 25 V (circles). The filled symbols represent the output conductance value at 2 MHz.

In the selected frequency range, all the measurement setup components satisfy linear non-distortion conditions. This greatly simplifies the setup calibration procedure which practically consists in the experimental characterization of the two 4-port networks (S_{in}^{4x4} and S_{out}^{4x4}) shown in Fig. 2.1. The characterization can be carried out by adopting the same procedure that has been fully detailed in [2] or, alternatively, by simply exploiting a low-frequency VNA.

The measurement setup has been automated via an IEEE488 standard interface by means of a commercial instrument automation software. The graphical user interface (Fig. 2.2) of the control software enables measurements to be carried out in an automated way: the user can define the dc parameters, in terms of a bias grid (voltage or current) and related compliances, in accordance with the device safe operating area. The two channels of the signal generator, which sets the incident signals applied to the device ports, are controlled in an independent way: for each one, the user can define the fundamental frequency component and the number of harmonics. For maximum level of flexibility, the user can arbitrarily define amplitude and phase for each spectral component.

Fig. 2.2: Graphical user interface of the control software.

2.1.1 Investigation of low-frequency dispersion by exploiting the proposed setup

The proposed measurement setup can be effectively used for in-depth investigation of the complex mechanisms related to low-frequency dispersion. For example, the low-frequency measurements shown in Fig. 2.3, carried out on a 0.7x800 μm^2 GaN HEMT, highlight the current collapse dependence on the average value of the gate voltage V_{g0}. The crosses in the enlarged view within the inset correspond to the same values of the instantaneous voltages (v_g = 0 V, v_d = 5.4 V); if low-frequency dispersion were not present, the same instantaneous current value (corresponding

to the dc one) should be measured. Instead, it is well evident that as the quiescent gate voltage V_{g0} moves into the off state region the instantaneous drain current goes down.

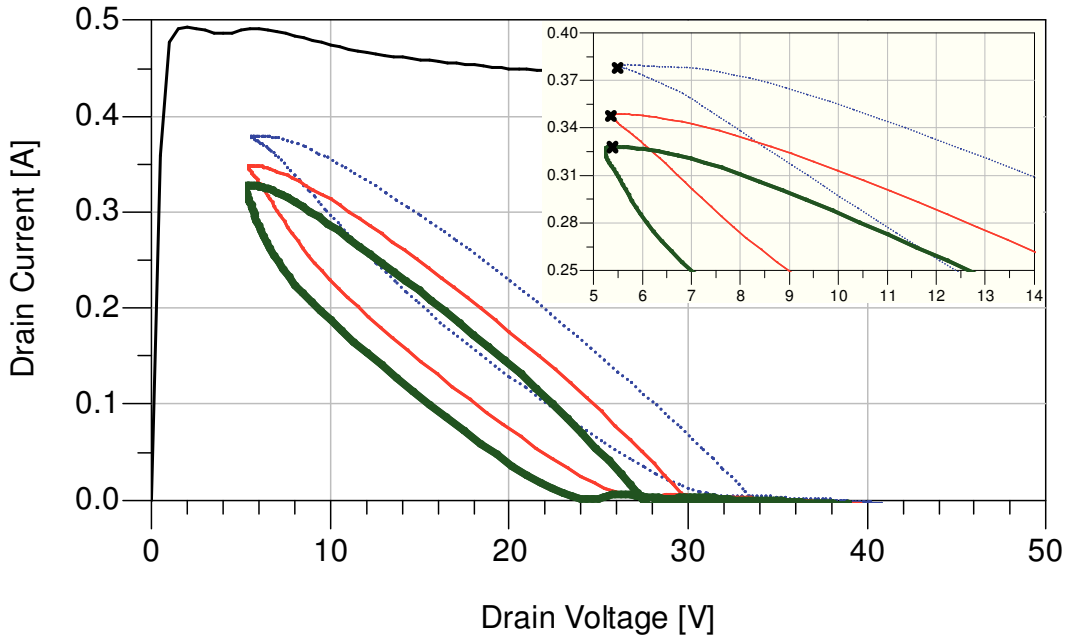


Fig. 2.3: Measurements performed by exploiting the new large-signal measurement system on a 800-µm GaN HEMT device, quiescent condition V_{d0} = 25 V and V_{g0} = -3 V (dotted line), V_{g0} = -4 V (continuous thin line), V_{g0} = -5 V (continuous thick line). The measured load lines are superimposed to dc characteristics at V_{g0} = 0 V. The crosses in the enlarged view within the inset correspond to the same instantaneous voltage pair (v_g = 0 V, v_d = 5.4 V).

Moreover, also the knee walkout [3], [4] can be simply characterized. In Fig. 2.4 different measurement sets are reported to characterize such a phenomenon; measurements were carried out with different drain voltage quiescent conditions and setting the amplitude of the input incident signals in order to dynamically reach the value v_g = 0 V. It is well evident how the knee region is subject to a shift as the average value of the drain voltage increases.

Finally, more complex device behavior can be investigated, which can be particularly useful for discussing and defining assumptions typically adopted in the framework of nonlinear modeling. To this end a 0.25-µm GaN HEMT device having a periphery of 150 µm, biased under class-A operation (V_{g0} = - 2 V, V_{d0} = 25 V), was considered. In particular, the device was excited with very different waveform shapes, under the constraint of dynamically reaching the zero volt gate voltage value. The incident signals applied to the DUT input port are shown in terms of their spectral components (Table 1), and corresponding time-domain voltage waveforms (Fig. 2.5a).

The phase of the incident signals applied at the DUT output port have been set to achieve a 180° displacement with respect to the input signal (such a choice corresponds to a resistive-like load

line), whereas the corresponding amplitudes were properly chosen to dynamically hit the device knee region.

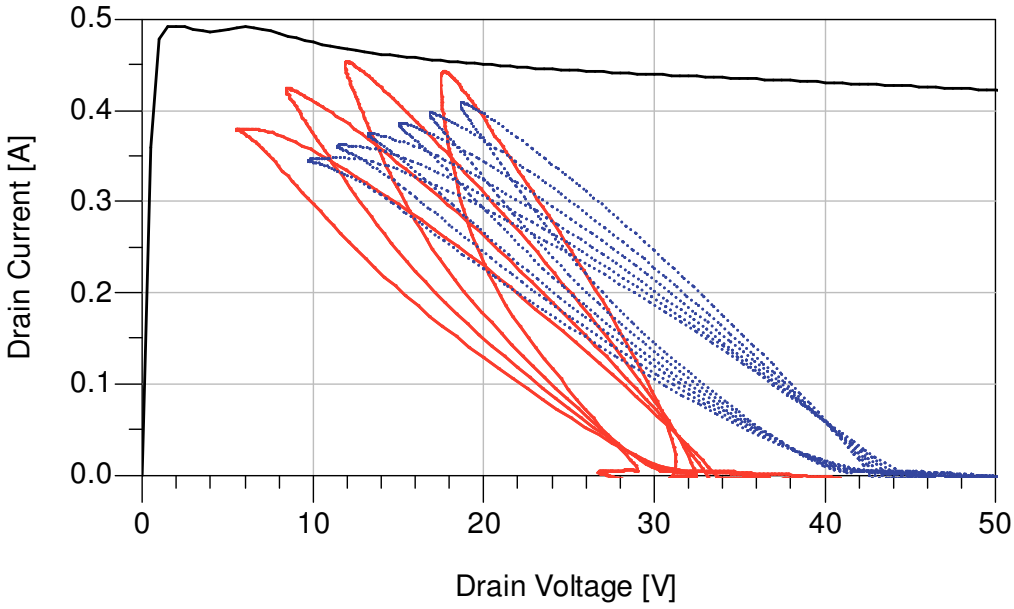
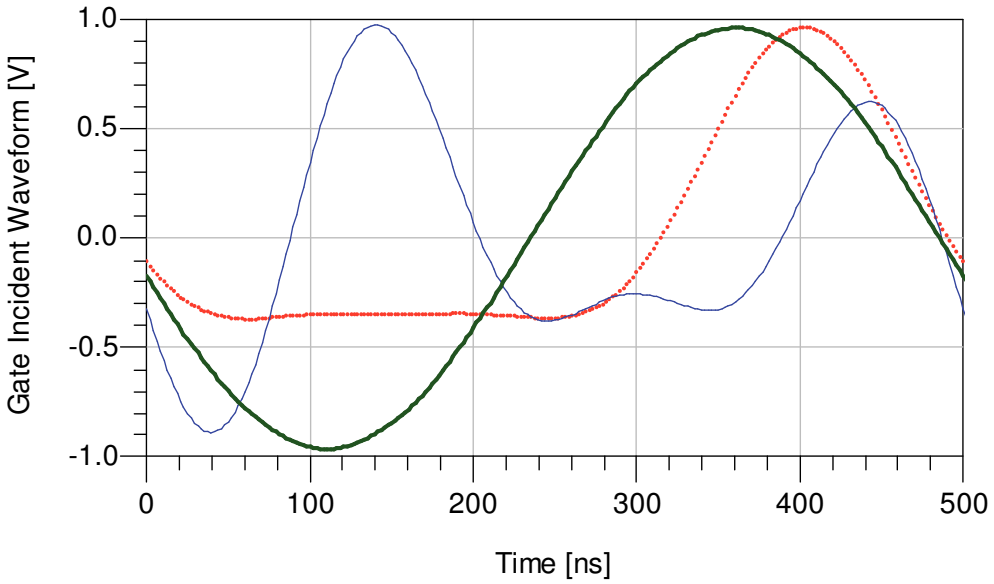


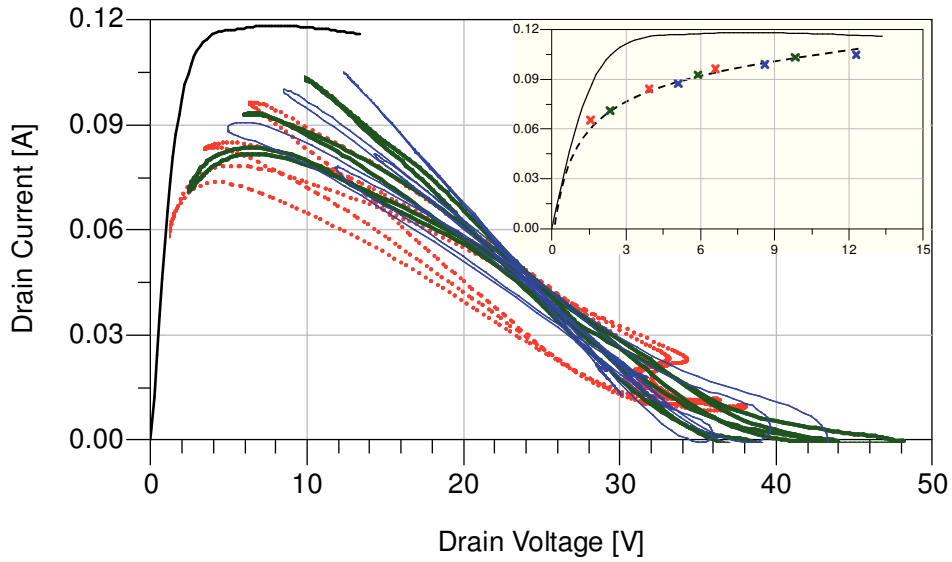
Fig. 2.4: Measurements performed by exploiting the new large-signal measurement system on a 800-µm GaN HEMT device, quiescent condition V_{g0} = -3 V and V_{d0} = 25 V (continuous lines), V_{d0} = 35 V (dotted lines). Amplitude of the gate incident signal phasor A_g = 1.5 V. Relative phase between gate and drain incident signal phasors $\Delta\varphi$ = 180 °. Different load lines are obtained by varying the amplitude of the output incident signal phasor. Measurements are superimposed to dc characteristics at V_{g0} = 0 V.

Sine	*Half-sine*	*Composite*	*Frequency*
1\0°	0.58\70°	0.14\-91°	2 MHz
0	0.31\140°	0.58\127°	4 MHz
0	0.08\-150°	0.38\86°	6 MHz

Table 1: Magnitude and phase of the incident signals applied to the DUT input port



a)



b)

Fig. 2.5: Measurements performed on a 150-µm GaN HEMT by exploiting the proposed large-signal measurement system, quiescent condition (V_{g0} = -2 V, V_{d0} = 25 V). a) Time-domain voltage waveforms at the device gate port. b) Measured load lines. Three load lines are shown for the same gate voltage condition (thin, thick and dotted lines) by varying the amplitude of the output incident signal phasors. Also the dc characteristic for V_{g0} = 0 V is shown

The corresponding load-lines, evidencing the knee walk-out, are shown in Fig. 2.5b. The crosses in the enlarged view within the inset correspond, for the different load lines, to dynamic points having the same value of the instantaneous gate voltage (v_g = 0 V): it is evident that these points trace a unique dynamic characteristic. This confirms the empirical results presented in [7] and the theoretical assumption adopted in [5], [6]: when no important deviations influence the device thermal state (this is true under class-A due to the low-efficiency operation involved), the trapping

state can be assumed univocally defined by the average values of the voltages applied at the device ports and no dependence is observed on the voltage waveforms.

The provided results could be indirectly obtained also by means of high-frequency time-domain measurement systems [4], [7-15]. Nevertheless two reasons make the proposed characterization technique preferable when electron device low-frequency dispersion is dealt with. The first one is that parasitic and reactive effects, under high-frequency operation, tend to hide the response of the intrinsic "algebraic" part of the device (i.e., the resistive core), and the second one is the simplicity and definitely low cost of the proposed measurement technique.

2.1.2 Large-signal measurements for high-efficiency operation

The described setup can be exploited in order to operate as a low-frequency multi-harmonic active load-pull system: by controlling gate and drain incident signals and their relative phase, at the fundamental frequency and its harmonics, different load terminations can be arbitrary synthesized for given bias conditions. Thus, by exploiting waveform engineering approach, optimal I/V load-line satisfying the theoretical requirements associated to a selected amplifier class of operation can be experimentally searched for.

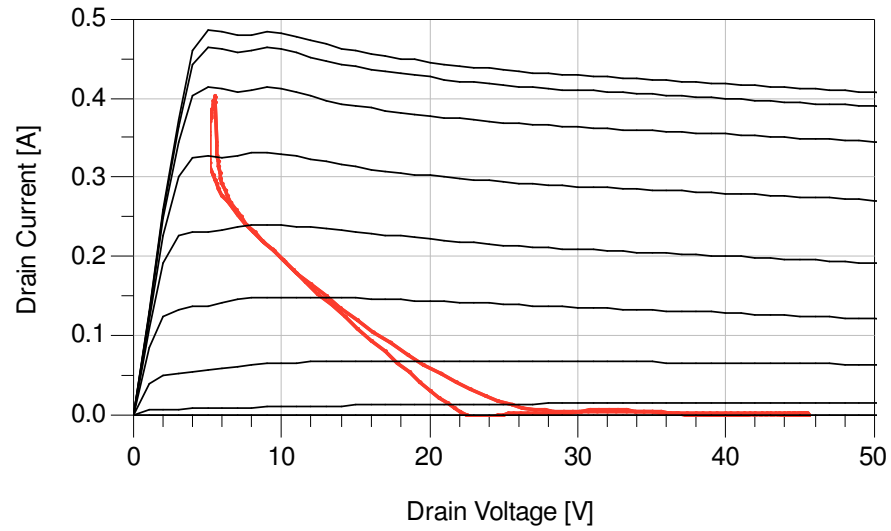
To highlight such capabilities of the described setup, large-signal measurements, oriented to high-efficiency power amplifier design [7], [16-17], were carried out on a 0.7x800 μm^2 GaN HEMT. The bias condition was V_{g0} = -4 V and V_{d0} = 25 V (class B operation), whereas the incident signals applied at the DUT ports are summarized in Table 2 in terms of their spectral components.

Gate Incident Signal Phasors	*Frequency*	*Drain Incident Signal Phasors*
2\85°	2 MHz	6.2\-107°
0	4 MHz	2.3\152°
0	6 MHz	1.3\-110°

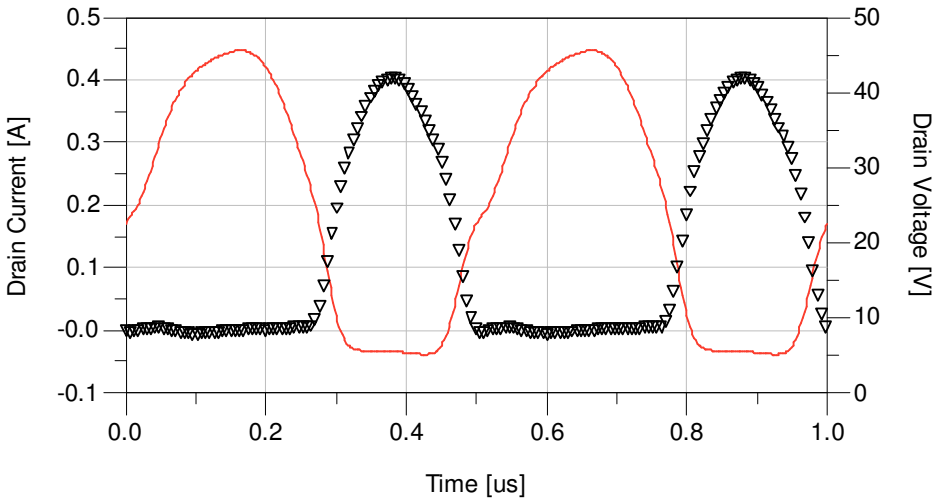
Table 2: Magnitude and phase of the RF signals applied to the DUT

Fig. 2.6a shows the dynamic load line corresponding to the described measurement condition. It is evident that a typical high-efficiency operation is obtainable by simply controlling the amplitude and phase of the fundamental, second and third harmonic components of the incident signal at the

drain terminal of the DUT. In this particular case study, an output power of 2.2 W was measured, corresponding to a drain efficiency of 74 %.



a)



b)

Fig. 2.6: Measurements performed by exploiting the proposed large-signal measurement system on a 800-µm GaN HEMT device, quiescent condition (V_{g0} = -4 V, V_{d0} = 25 V). a) The measured load line is superimposed to dc characteristics (-4 V ≤ V_{g0} ≤ 0 V, step 0.5 V). b) Time-domain voltage (continuous line) and current (triangles) waveforms at the device drain terminal, corresponding to the synthesized high-efficiency operation.

At a few megahertz, the input port of a FET behaves as an open circuit until the off-state of the gate-source diode is preserved. This greatly simplifies the control of the gate incident signal. In the present case, a 4-V amplitude of the gate input voltage is imposed, that leads to a peak-value equal to zero volt. In Fig. 2.6a the device DC characteristics (-4 V ≤ V_{g0} ≤ 0 V) are shown: it is well evident that, due to the current collapse [3], the load-line is not able to dynamically reach the drain-

current values corresponding to the dc characteristic at V_{g0} = 0 V. Moreover an important knee walkout [3], [4] is present. It is evident how the proposed setup effectively characterizes the limits of the given technology.

Time-domain waveforms at the drain port of the electron device are shown in Fig. 2.6b. The dynamic current looks like an half-wave rectified sine-wave, which is different from zero where the drain voltage is minimum, according with high-efficiency power amplifier operation modes [16], [17]. In this context, the capability of synthesizing a given load-line and get information on suitable drain and gate terminations for the device resistive core, can be exploited not only for I/V modeling under realistic operation but also for amplifier design approaches, like the one that will be proposed in the next section.

It is of interest to investigate some commonly accepted assumptions related to power amplifier design. CAD-based amplifier design techniques are based on the accurate knowledge of the device intrinsic resistive core. A clear example is provided by the Cripps' load-line theory [16] which identifies the optimum device operation by analyzing the device dc characteristics and defining the optimum loading condition as the resistance that maximizes voltage and current excursions. As a matter of fact, all amplifier design techniques, from class-A to high efficiency (e.g., class F), are de facto based on the definition of the optimum waveforms of the electrical quantities at the device intrinsic current source, i.e. the device resistive core. However, due to traps and thermal effects [5-6], the transistor resistive core shows under dynamic operation a behavior which is very different with respect to the static one. The proposed setup has the unique capability of directly and exhaustively characterizing such a behavior.

As a case study we investigate the behavior of a 0.25x400 μm^2 GaN HEMT under high-efficiency operation. In particular, Fig. 2.7 shows three different load lines providing the different performance levels reported in Table 3. Also in this case the impact of low-frequency dispersion on the device performance is well evident. The device is not able to dynamically reach the DC characteristic at V_{g0} = 1 V and the I/V knee under dynamic operation is well far from the dc one. Both these phenomena, by limiting the drain current and voltage excursions, reduce the deliverable output power with respect to the one predictable on the basis of the dc characteristics.

By observing the load lines in Fig. 2.7, at a first glance it is well evident which is the best one. Efficiency and power are the worst ones for the thick load line since it involves the highest dissipation path and minimizes the drain current excursion. Similar considerations indicate that the thin load line is the best one. Such a simplicity in stating the best operating condition has to be regarded as peculiar to the proposed setup, since a similar information cannot be drawn by observing extrinsic load lines carried out at microwave frequencies.

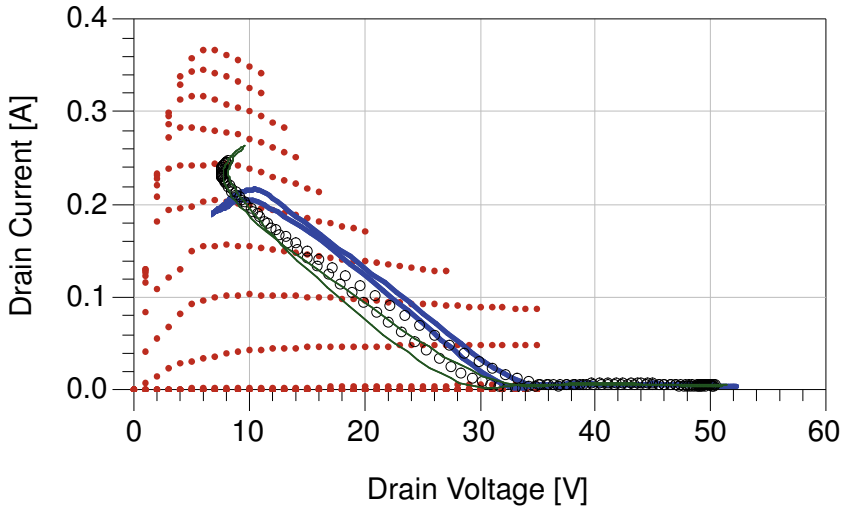


Fig. 2.7: Different load lines synthesized by exploiting the proposed large-signal measurement system on a 400-µm GaN HEMT device, quiescent condition (V_{g0} = -4 V, V_{d0} = 30 V). Amplitude of the gate incident signal fundamental phasor A_g = 2.5 V. Relative phase between gate and drain incident signal fundamental phasors $\Delta\varphi$ = 180 °. The measured load lines are superimposed to dc characteristics (-6 V ≤ V_{g0} ≤ 1 V, step 0.5 V).

Load Line	*Output Power*	*Efficiency*
Thick	1.25 W	54 %
Circles	1.64 W	60 %
Thin	1.72 W	61 %

Table 3: Performance related to the different load lines shown in Fig. 2.7

Theoretical considerations can be also carried out by observing the intrinsic drain voltage waveforms corresponding to the considered load lines; they are shown in Fig. 2.8 with their harmonic components. Fig. 2.8a refers to the thick load line, in this case only the fundamental tones of the input and output incident signals have been controlled. This is evident by looking at the second and third harmonics which assume very low amplitudes. Fig. 2.8b refers to the circles load-line, in this case the amplitude and phase of the third harmonic of the output incident signal have been manipulated also. It is evident the contribution of the third-harmonic, which, being out-of-phase with respect to the fundamental one, raises the amplifier performance according to class-F operation [17]. Nevertheless, class-F operation requires also a short loading condition at the second harmonic, this condition can be simply obtained by manipulating also the second harmonic of the output incident signal. The result is shown in Fig.2.8c, where the amplitude of the second harmonic has been halved.

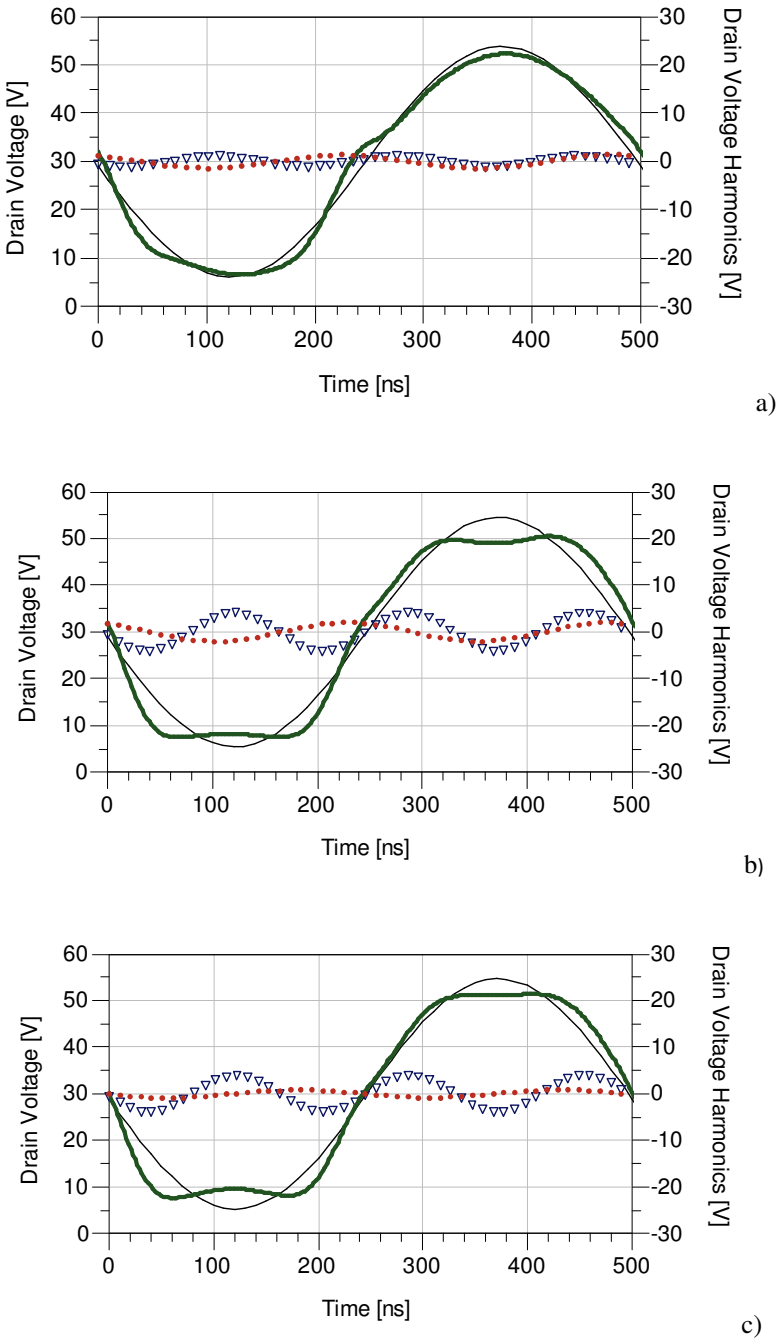


Fig. 2.8: Measurements performed by exploiting the proposed large-signal measurement system on a 400-µm GaN HEMT device, quiescent condition (V_{g0} = -4 V, V_{d0} = 30 V). Time-domain voltage waveform (bold line) and its harmonic components (fundamental - fine line, second harmonic – dots, and third harmonic - triangles) corresponding to the three load lines reported in Fig. 5. a) thick line, b) circles, c) thin line.

In Table 4, the load impedances synthesized for the different load lines are reported. The impedances at the 2nd and 3rd harmonics differ from 50 Ω although, for the thick load line, only the fundamental phasor of the incident signals has been exploited. This can be explained by considering that the values in Table 4 refer to the DUT planes and account for the non idealities of the measurement setup (e.g., 30-W power amplifier output impedance, attenuation and delay provided

by the signal paths). By looking at the impedance values in Table 4, it is evident how the impedances synthesized for the thin load-line are the nearest ones to the ideal class-F amplifier behavior (i.e., a short circuit at the second harmonic and an open circuit at the third harmonic).

Load Line	*Fundamental*	*2nd Harmonic*	*3rd Harmonic*
Thick	219 – i*19 Ω	36 + i*13 Ω	47 + i*20 Ω
Circles	182 – i*11 Ω	37 + i*13 Ω	349 – i*47 Ω
Thin	177 – i*10 Ω	1 + i*15 Ω	481 – i*94 Ω

Table 4: Synthesized load terminations for the different load lines shown in Fig. 2.7

Measurements carried out by adopting the proposed setup, besides representing a valid tool for the design of power amplifiers, may result extremely useful in the identification phase of nonlinear electron device. As a matter of fact, the operating conditions exploited in the identification phase are privileged in terms of the accuracy that the model can guarantee. As a consequence, nonlinear models extracted by adopting measurements under actual device operations unquestionably offer an higher level of accuracy.

2.2 The proposed design approach

The design methodology here discussed finds its motivations in electron device nonlinear modeling theory. For the sake of clarity, electron device nonlinear modeling issues, already discussed in the previous chapter, are here briefly recalled.

As shown in Fig. 2.9, in the equivalent circuit representation of a transistor, three parts can be discerned: the linear extrinsic parasitic network, that describes the access passive structure to the device active area; the capacitive core, that is responsible of electron device nonlinear dynamic effects and the resistive core, that accounts for LF I/V device behavior. These cores, representing the intrinsic device (i.e., the active area), can be considered electrically in parallel.

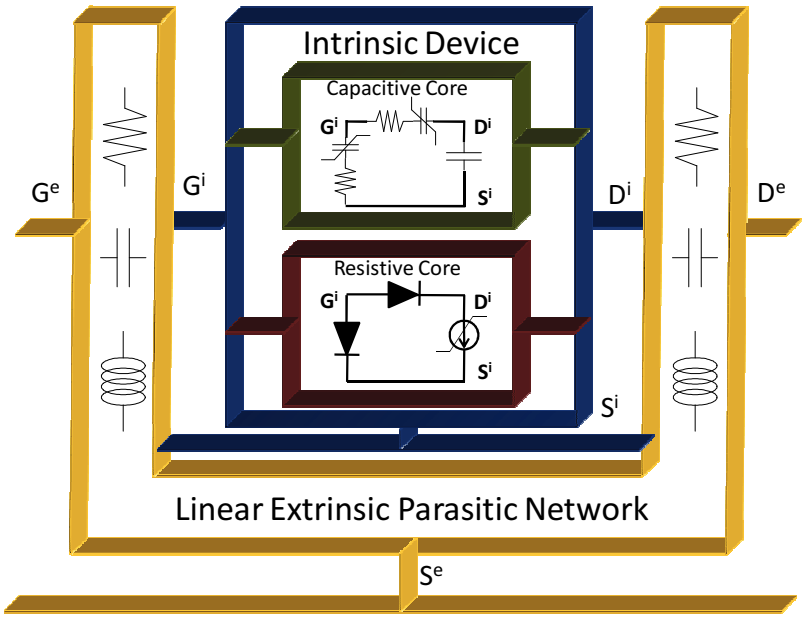


Fig. 2.9: Nonlinear equivalent circuit for an FET Electron Device.

The aim of the design methodology is to overcome the accuracy limitations due to the complex modeling of the ED resistive core, by using a direct experimental characterization of the LF I/V load-line. To this end, the low-frequency (i.e. 2 MHz) setup described in the previous section is exploited in order to achieve active load synthesis capabilities in the framework of power amplifier design. As said, in fact, at the frequencies of few megahertz, the FET representation in Fig. 2.9 is strongly simplified since the parasitic network can be represented by means of parasitic resistances (accounting for metallization and channel access losses), while the reactive elements can be completely neglected. Therefore, the low-frequency load-line synthesized at the external terminals is practically coincident[1] with the load-line imposed at the resistive core of the intrinsic electron device. Since the associated electrical regime uniquely identifies [16-18] the electron device delivered power and efficiency, the described setup provides an easy way to carry out the choice of the load-line which defines given power amplifier performance. It should be pointed out that the proposed approach enables the designer to easily choose for optimal power amplifier operation modes by experimentally monitoring and engineering the waveforms at the electron device intrinsic resistive core. Moreover, reliability issues related to high-field operations [19-21], which must be considered at the intrinsic device drain-gate terminals [22], can be directly controlled.

In order to explain how the low-frequency load-line measured at the extrinsic electron device ports can be used for power amplifier design, it is convenient to express intrinsic and extrinsic voltages and currents in terms of their practically finite number *M* of spectral components:

[1] For safe of accuracy, a simple de-embedding of only resistive parasitic elements is necessary to obtain the load-line imposed at the intrinsic resistive core.

$$x(t)=\sum_{k=-M}^{M} X(k\omega)e^{jk\omega t} \tag{1}$$

By considering for the parasitic network in Fig. 2.9 any possible topology (based on lumped or distributed elements), intrinsic and extrinsic electrical variables are conveniently related by the following equations in the frequency domain:

$$\begin{bmatrix} V_{gs}^{i}(k\omega) \\ V_{ds}^{i}(k\omega) \\ I_{g}^{i}(k\omega) \\ I_{d}^{i}(k\omega) \end{bmatrix} = \underline{H}(k\omega) \begin{bmatrix} V_{gs}^{e}(k\omega) \\ V_{ds}^{e}(k\omega) \\ I_{g}^{e}(k\omega) \\ I_{d}^{e}(k\omega) \end{bmatrix},\ k=-M,..,M \tag{2}$$

where $\underline{H}(\omega)$ is a suitable hybrid-matrix description of the linear extrinsic parasitic network.

At microwave frequencies the harmonic components of the "global" intrinsic currents are composed of the sum of the conduction[2] and displacement currents denoted with the superscripts R and C, respectively:

$$\begin{bmatrix} I_{g}^{i}(k\omega_{RF}) \\ I_{d}^{i}(k\omega_{RF}) \end{bmatrix} = \begin{bmatrix} I_{g}^{i,R}(k\omega_{RF})+I_{g}^{i,C}(k\omega_{RF}) \\ I_{d}^{i,R}(k\omega_{RF})+I_{d}^{i,C}(k\omega_{RF}) \end{bmatrix},\ k=-M,..,M \tag{3}$$

When considering the low-frequency load-line characterization carried out with sinusoidal excitations at the fundamental frequency $\omega=\omega_{LF}$ and its harmonics, the displacement current can be totally neglected. Moreover, $\underline{H}(\omega)$ practically becomes a real and frequency-independent matrix (which, when considering the most common case of lumped parasitic description, reduces to the series parasitic resistors). In such a case, (2) enables to directly compute, starting from the knowledge of the low-frequency harmonic components of the extrinsic voltages and currents, the intrinsic electrical variables (and, as consequence, the intrinsic load-line) at the electron device resistive core: $V_{gs}^{i}(k\omega_{LF})$, $V_{ds}^{i}(k\omega_{LF})$, $I_{g}^{i,R}(k\omega_{LF})$, $I_{d}^{i,R}(k\omega_{LF})$.

[2] Due to the frequency-independence of the conduction current its harmonic RF-components simply coincide with the LF ones, that is $I_{x}^{i,R}(k\omega_{RF})=I_{x}^{i,R}(k\omega_{LF})$.

In order to exploit the low-frequency load-line characterization for microwave power amplifier design, the extrinsic device load and source conditions must be computed, which enables the electrical regime corresponding to the chosen intrinsic load-line to be imposed at the design frequency. To this end, the displacement currents related to the electron device capacitive core must be evaluated according to the following, explicit equations:

$$\begin{bmatrix} i_g^{i,C}(t) \\ i_d^{i,C}(t) \end{bmatrix} = \begin{bmatrix} \sum_{k=-M}^{M} I_g^{i,C}(k\omega_{RF}) e^{jk\omega_{RF}t} \\ \sum_{k=-M}^{M} I_d^{i,C}(k\omega_{RF}) e^{jk\omega_{RF}t} \end{bmatrix} = \sum_{k=-M}^{M} jk\omega_{RF} \underline{C}\left(v_{gs}^i(t), v_{ds}^i(t)\right) \begin{bmatrix} V_{gs}^i(k\omega_{LF}) e^{jk\omega_{RF}t} \\ V_{ds}^i(k\omega_{LF}) e^{jk\omega_{RF}t} \end{bmatrix}, \quad (4)$$

ω_{RF} being the fundamental operating frequency of the power amplifier with

$$\begin{aligned} v_{gs}^i(t) &= \sum_{k=-M}^{M} V_{gs}^i(k\omega_{LF}) e^{jk\omega_{RF}t} \\ v_{ds}^i(t) &= \sum_{k=-M}^{M} V_{ds}^i(k\omega_{LF}) e^{jk\omega_{RF}t}. \end{aligned} \quad (5)$$

As previously said, the capacitance matrix[3] $\underline{C}$ in (3) can be identified on the basis of frequency- and bias-dependent S-parameter measurements. Alternatively, the capacitive core of a suitable, already available, nonlinear model can be used.

It must be outlined that when high-frequency nonquasi-static effects are not negligible, the displacement currents cannot be explicitly evaluated in terms of a capacitance matrix only as in (4), but nonlinear circuit analysis is required. To this end any frequency- or time-domain available CAD environment can be easily adopted.

Once the harmonic components of the "global" intrinsic currents have been evaluated by (3), the extrinsic electrical variables which define the load and source extrinsic regime can be computed by:

$$\begin{bmatrix} V_{gs}^e(k\omega_{RF}) \\ V_{ds}^e(k\omega_{RF}) \\ I_g^e(k\omega_{RF}) \\ I_d^e(k\omega_{RF}) \end{bmatrix} = \underline{H}^{-1}(k\omega_{RF}) \begin{bmatrix} V_{gs}^i(k\omega_{RF}) \\ V_{ds}^i(k\omega_{RF}) \\ I_g^i(k\omega_{RF}) \\ I_d^i(k\omega_{RF}) \end{bmatrix}, \; k = -M,..,M \quad (6)$$

[3] Please note that the difference existing, given a bias condition, among the imaginary parts of the admittance parameters Y_{12} and Y_{21} (typically modeled by a transcapacitance) can be accounted for by (4) without any approximation.

and finally the load impedance at the fundamental and harmonic frequencies can be obtained:

$$Z_L\left(k\omega_{RF}\right) = -\frac{V_{ds}^{e}\left(k\omega_{RF}\right)}{I_{d}^{e}\left(k\omega_{RF}\right)}. \tag{7}$$

In addition, also the input device "large-signal impedance" can be easily computed:

$$Z_{IN}\left(k\omega_{RF}\right) = \frac{V_{gs}^{e}\left(k\omega_{RF}\right)}{I_{g}^{e}\left(k\omega_{RF}\right)}. \tag{8}$$

which, for instance, can be used to synthesize the optimum source impedance (i.e., Z_s = conj(Z_{IN})) which provides a matching condition under large-signal operation. It should be outlined that this information is not obtainable through scalar load-pull systems [23-25], but only by adopting a time-domain load-pull measurement setup [26-28].

To summarize, the proposed approach, which is based on low-frequency, large-signal measurements and bias/frequency-dependent small-signal measurements performed in the frequency range of interest for the considered design, is fully able to provide the same kind of information obtainable by means of expensive nonlinear measurement setups operating at microwave frequencies. The only assumption is that a negligible uncertainty can be achieved in the description of the intrinsic electron device capacitive core whose accuracy ultimately defines the frequency limitations. As will be demonstrated in the following sections, by adopting very different experimental examples, such an hypothesis is more than reasonable from a practical point of view.

The flowchart reported in Fig. 2.10 describes the fundamental steps of the proposed design techniques.

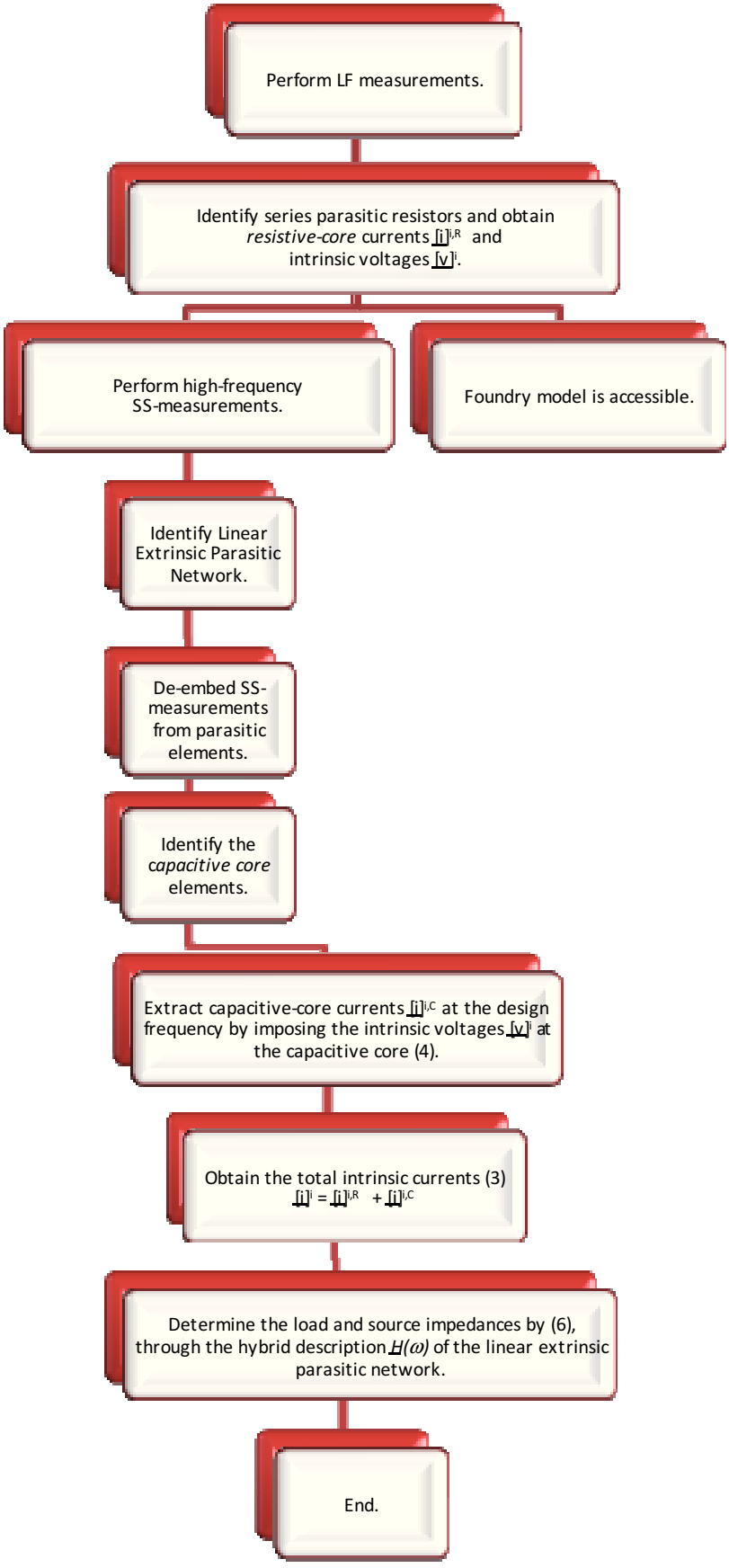


Fig. 2.10: Flowchart describing the proposed design technique.

2.2.1 Class-A power amplifier design example

In this section, a class-A power amplifier example, operating at the central frequency of 4 GHz, is discussed. The electron device adopted for the present case of study is a C-band 0.7 x 800 μm^2 GaN HEMT, whose foundry specifications are reported in Table 5.

Quantity	*Value*
Breakdown Voltage	80 V
Pinch-off Voltage	-3.5 V
Idss	700 mA/mm
Saturated Output Power	4 W/mm

Table 5: 0.7-µm GaN HEMT technology specifications

Accordingly with the design methodology described in the previous section, a preliminary low frequency characterization of the device intrinsic resistive core has been carried out: exploiting the previously mentioned active load-pull setup, the device was biased under class-A condition (V_{g0} = -2 V, V_{d0} = 25 V) and different load-lines were obtained by imposing a constant amplitude of the gate incident signal and sweeping the amplitude of the drain incident signal. More precisely, the amplitude of the gate incident signal was fixed at 1 V with the aim of satisfying the constraints of linear operation. Such low-frequency measurements are shown in Fig. 2.11, whereas the main experimental data for the correct choice of the intrinsic device load-line are listed in Table 6: the loading condition was chosen to meet output power and efficiency requirements, under the constraints of keeping the maximum drain-gate voltage below 42 V. As a matter of fact, the "intrinsic", low-frequency load impedance (Z_l = 109.5 + i•1.3 Ω) satisfies all the design constraints.

Z_l [Ω]	*Power [W]*	*Efficiency [%]*	V_{dg}^{max} [V]
5.4 + i·5.4	0.064	1.3	28.7
29.7 + i·4.3	0.330	7.1	31.6
55.6 + i·2.7	0.585	12.7	35.3
62.5 + i·2.2	0.634	13.9	36.2
76.7 + i·1.1	0.736	16.5	37.9
92.4 + i·0.1	0.812	18.5	39.7
109.5 + i·1.3	0.881	20.5	41.4

Table 6: Power, efficiency and maximum drain-voltage values obtained under lf operation as a function of the synthesized load impedances.

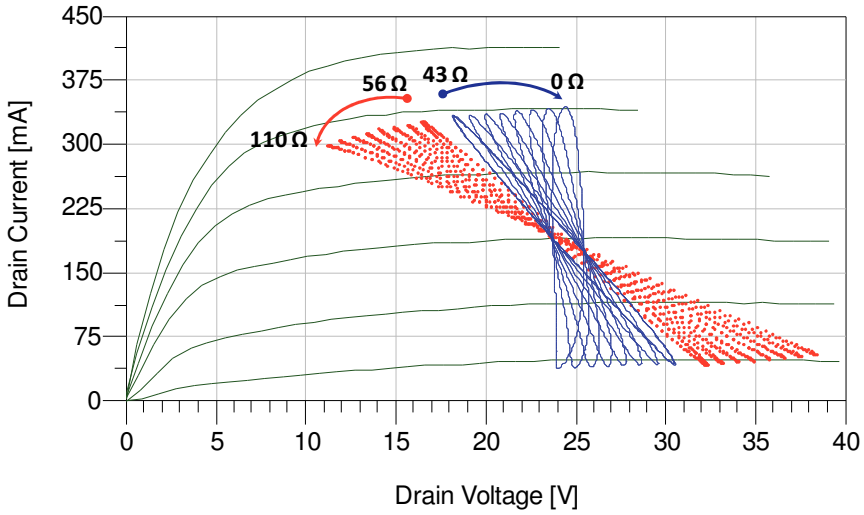
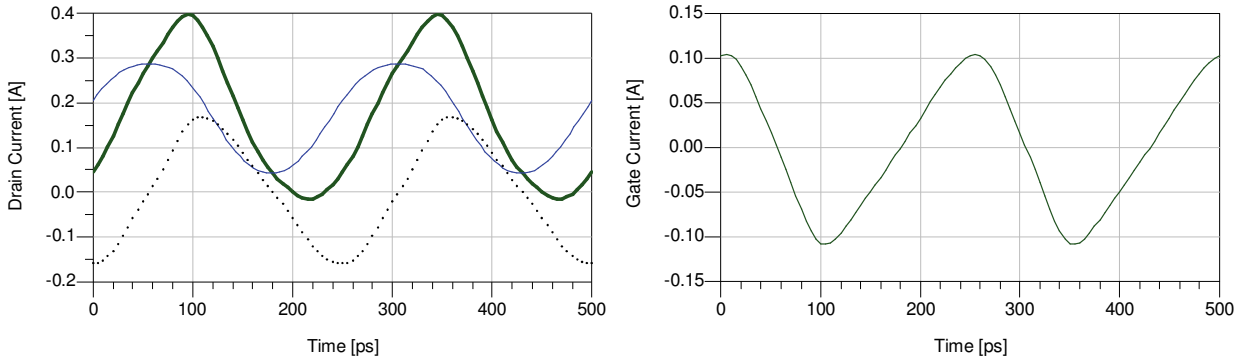


Fig. 2.10: Measurements performed, by exploiting the LF measurement system, on an 800-µm GaN HEMT device biased at (V_{g0} = -2 V , V_{d0} = 25 V). Amplitude of the gate incident signal (A_g = 1 V), amplitude of the drain incident signal (1 V ≤ A_d ≤ 8 V), relative phase ($\Delta\varphi$ = 0° continuous lines, $\Delta\varphi$ = 180° dotted lines). Load-lines are superimposed to pulsed characteristics (-3 V ≤ V_g ≤ -0.5 V) carried out from the considered quiescent bias condition.

Successively, S-parameter measurements were performed in a wide range of bias conditions (- 4 V < V_{g0} < 0 V, 0 V < V_{d0} < 40 V) in the frequency range 40 MHz – 40 GHz. Such measurements were exploited (together with a suitable linear extrinsic parasitic network description) for the modeling of the capacitive-core behavior, as previously discussed. The gate and drain currents, corresponding to the selected amplifier operation, are shown in Fig. 2.11. It is well evident the large contribution deriving from the capacitive core.



a) b)

Fig. 2.11 a) Drain current at the intrinsic device $I_{DS}^{i}(\omega_{RF})$ (green thick solid line) and its two portions: the capacitive one (dots) and the resistive one (blue thin solid line). b) Total gate current at the intrinsic device $I_{GS}^{i}(\omega_{RF})$.

Finally, the synthesized load and source impedances (in this case the latter has been chosen equal to the conjugate of the large-signal device input impedance) were computed at the design frequency according to (7) and (8) (see Table 7).

Source Impedance	*Frequency*	*Load Impedance*
3.41 + i·10.21 Ω	4 GHz	42.42 + i·54.22 Ω
	8 GHz	16.28 - i·12.18 Ω
	12 GHz	14.55 + i·25.79 Ω

Table 7: Synthesized Source and Load Impedances for the 800-µm GaN HEMT.

As a validation of the proposed technique, the predicted results have been compared in Fig. 2.12 with load-pull measurement data carried out by imposing the source and drain impedances reported in Table 7. The excellent agreement, in terms of output power, average drain current, PAE and gain compression, gives a clear idea of the accuracy level achievable by adopting the proposed approach and definitely confirms its effectiveness for power amplifier design.

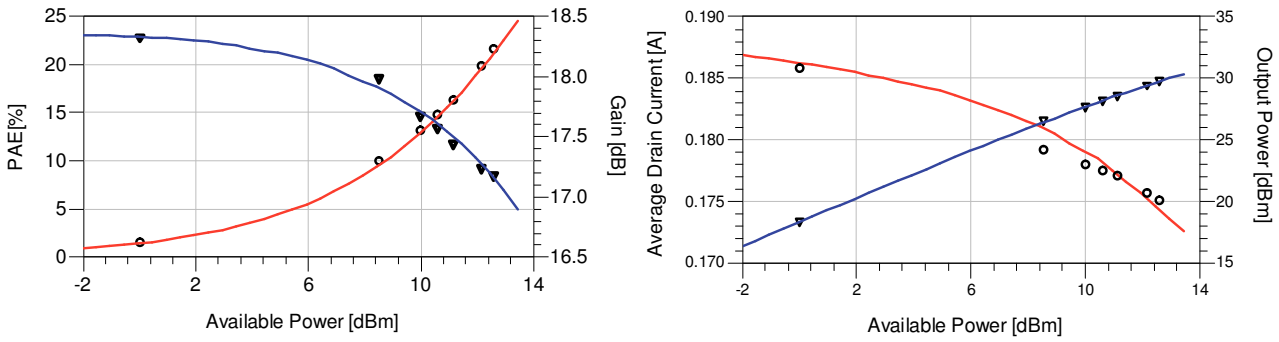


Fig. 2.12 Load-pull measurements (continuous line) versus predictions (symbols) at the fundamental design frequency (4 GHz). (a) Power added efficiency (circles) and transducer power gain (triangles) - (b) Average drain current(circles) and Output power (triangles).

2.2.2 Wideband Class-AB power amplifier design example

The electron device used for the power amplifier design is a C–band 0.25 x 1250 µm^2 GaN on SiC HEMT [29] whose main electrical characteristics are summarized in Table 8.

Quantity	*Value*
Breakdown Voltage	< -70 V
Pinch-off Voltage	-4 V
Idss	1.25 A
Saturated Output Power	> 38 dBm

Table 8: 0.25 x 1250-µm^2 GaN on SiC HEMT device characteristic

The discrete device was placed on a brass carrier and bonded to the microstrip access structures (see Fig. 2.13) in order to easily carry out measurements by exploiting GSG-probes. TRL calibration standards were available to set the measurement reference planes to the bonding wire sections.

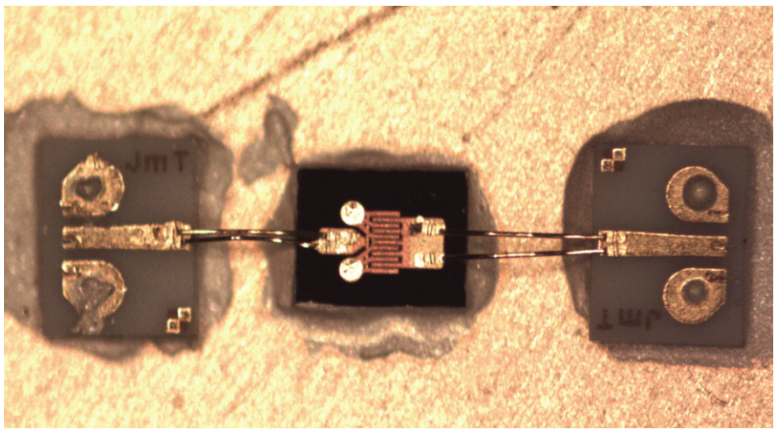


Fig. 2.13: Discrete C–band 0.25 x 1250 µm^2 GaN on SiC HEMT. The device is bonded to the microstrip access structures.

For high-efficiency operation mode, a class-AB bias condition has been chosen (V_{g0} = -3.4 V, V_{d0} = 32 V, I_{d0} = 120 mA). With the aim of satisfying reliability constraints, low-frequency load-pull measurements shown in Fig 2.14 were carried out not exceeding the zero–volt boundary for the maximum gate voltage and keeping the maximum drain voltage lower than 65 V, well below the device breakdown voltage.

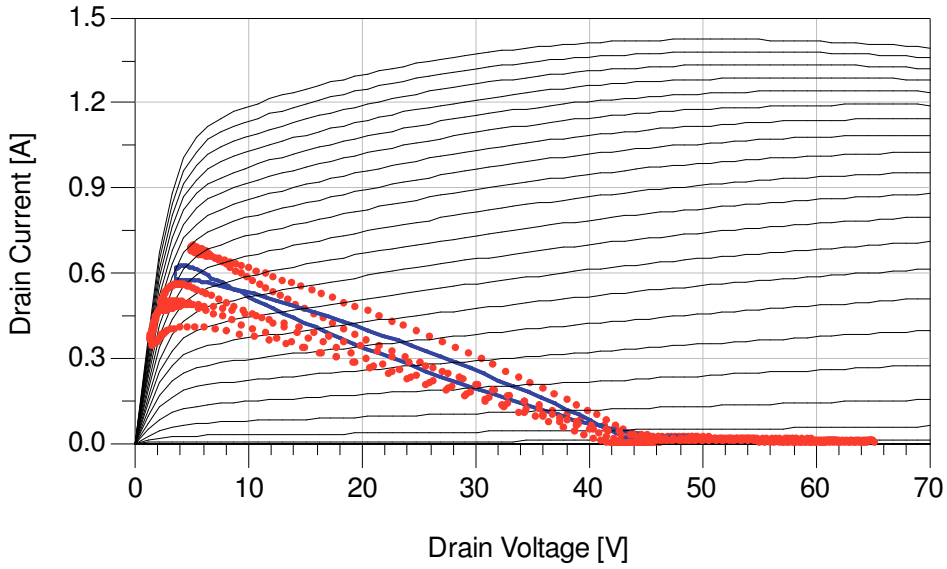


Fig. 2.14: Measurements performed by exploiting an low-frequency load-pull setup on a discrete 1.25 mm GaN on SiC HEMT device biased at (V_{g0} = -3.4 V, V_{d0} = 32 V, I_{d0} = 120 mA). Measured LF intrinsic load-lines and the chosen one (solid line) are superimposed to simulated DC characteristics (-5 V < V_{g0} < 1 V step 0.25 V).

The main experimental data for the correct choice of the intrinsic device load-line are listed in Table 9. As a matter of fact, the low-frequency "intrinsic" load impedance (Z_l = 85.8 – i * 0.9 Ω) satisfies all the given design constraints, providing a good trade-off between maximum output power and efficiency. In particular, an output power of 37.21 dBm and a 69 % of drain efficiency were measured.

Z_l [Ω]	*Output power [dBm]*	*Efficiency [%]*	*V_{ds}^{max} [V]*
70.5 + i * 0.3	37.04	62	53.7
85.8 – i * 0.9	37.21	69	61.6
108.1 – i * 8.2	36.81	75	60.8
139.7 – i*18.1	36.27	79	64.0

Table 9: Power, efficiency and maximum drain-voltage values obtained under low-frequency operation as a function of the synthesized load impedances

Accordingly to the proposed design technique, the foundry model (EE_FET3 [9]) was exploited both for the capacitive core and for the extrinsic parasitic network behavior. A slight modification

of the parasitic network had to be done to take into account the extra parasitic effects of the bonding wires.

The load and source impedances (in this case the latter has been chosen equal to the conjugate of the large-signal device input impedance) were eventually computed for a wide band (4 – 7 GHz) of design frequencies (see Table 10).

Source Impedance	*Frequency*	*Load Impedance*
2.2 + i * 8.5	4 GHz	37.1 + i * 33.5
2.2 + i * 2.8	5 GHz	28.2 + i * 29.1
2.2 – i * 1.7	6 GHz	21.8 + i * 24.0
2.2 – i * 5.6	7 GHz	17.2 + i * 18.8

Table 10: Synthesized load and source terminations for the device as a function of the frequency

In order to demonstrate the validity of predicted results, load-pull measurements were carried out by means of a 4–26 GHz load-pull setup. As a matter of fact, the synthesized load impedances ensure predicted output power greater than 37.2 dBm with efficiency greater than 60 % in the entire design frequency range. As shown in Fig. 2.15 for the considered frequency range, the load impedances synthesized by adopting the proposed design technique represent a good trade-off between the best–output-power and best–efficiency impedances measured by the load-pull setup. Moreover, as reported in Table 10, the output power and efficiency goals predicted by the proposed approach have been confirmed by load-pull measurements.

Frequency	*Output power [dBm]*	*Efficiency [%]*
4 GHz	37.5	62.8
5 GHz	37.4	64
6 GHz	37.2	64.8
7 GHz	37.4	71.9

Table 10: Power, efficiency and maximum drain-voltage values obtained under low-frequency operation as a function of the synthesized load impedances

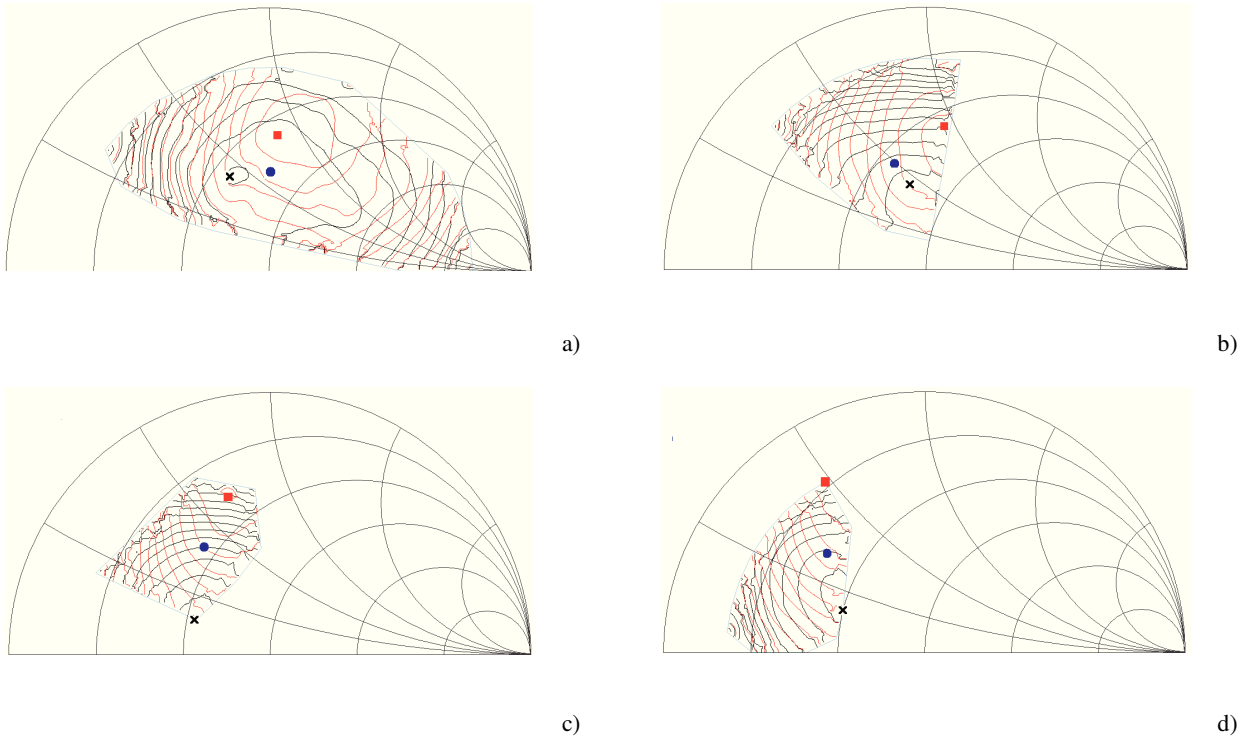


Fig. 2.15: Output-power (black) and efficiency (red) contours measured by means of a 4–26 GHz load-pull setup (at 2.5 dB gain compression) at 4 GHz a), 5 GHz b), 6 GHz c), and 7 GHz d) fundamental frequency. Best output power (cross) and best PAE (square) terminations are compared with the load impedances predicted through the new design procedure (circle).

Finally, the obtained results were evaluated also by considering the information reported in the foundry data-sheet [9]. The foundry optimum power load impedance measured at 3.5 GHz is provided in terms of a parallel RC intrinsic output network. The data-sheet output network (with the addition of the output parasitic effect) has been frequency scaled to compute the external terminals optimum load impedance in the 4 to 7 GHz frequency range. As shown in Fig. 2.16, at 4 GHz the load impedance predicted by our design technique is practically coincident with the one deduced through the foundry data-sheet, while for frequencies greater than 4 GHz, frequency re–scaled foundry load impedances follow a different sub-optimal trajectory which is not coherent with the required performance. As a consequence, such a kind of approach is only suitable for a narrowband design but not adequate for wideband designs which would require a broadband time-consuming device characterization.

On the contrary, the optimal load impedances predicted in the 4 to 7 GHz range through the proposed design procedure, are in excellent agreement with the required PA performance.

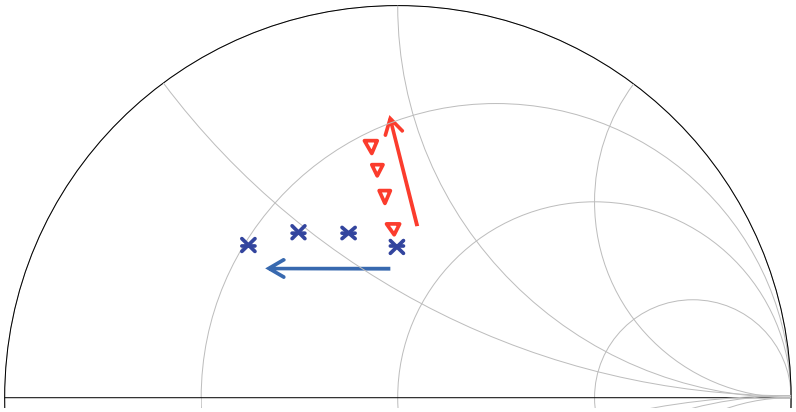


Fig. 2.16: Broadband load impedance termination trajectory evaluated at 4, 5, 6, 7 GHz: data-sheet frequency–scaled terminations (triangles) and load impedances predicted through the new design procedure (stars).

2.3 Power amplifier design accounting for input large-signal matching

As previously said, one of the crucial aspects in power amplifier design is to find out the correct input and output terminations that ensure adequate performance. In this context, the output matching network (OMN) of a power amplifier is generally designed in order to reach optimal performance under large-signal operations, whereas, when dealing with pre-driver or driver amplification stages, input matching network (IMN) design is often based on small-signal measured- or simulated- data, in order to optimize both small-signal gain and input return loss [16-17]. As a matter of fact, input power levels of the first stages in the amplification line-up are definitely lower than the output ones, thus justifying the described design paradigm. On the contrary, in the final amplification stage the input power levels become significantly high: as a consequence, IMN design based on small-signal operation could be inappropriate, since the small-signal optimal impedance is not necessarily related to the optimal one under large-signal operation. In any case, the large-signal matching condition does not coincide with the small-signal one.

On the other hand, when dealing with broadband power amplifier design, OMN has to be synthesized in order to guarantee, over the whole bandwidth, the same I/V load-line trajectory at the electron device intrinsic current generator plane, that, as well known, is the main actor in defining the power amplifier output performance in terms of delivered power and efficiency. As well as for the OMN, the design of the IMN must be carried out in order to guarantee the optimum condition (i.e., the conjugate of the large-signal input impedance of the electron device) over a large range of frequencies.

The design methodology discussed in this chapter satisfy such design requirements: by exploiting the proposed approach, in fact, time-domain electrical waveforms, in terms of large-signal voltages and currents referred to electron device ports, can be monitored. Such information enables to easily compute the optimal source termination as the conjugate of the electron device input large-signal impedance and allows to evaluate broadband output termination that maintain the same I/V load-line referred to the current generator plane, guaranteeing adequate performance over the entire bandwidth.

In the next section, a broadband class-AB power amplifier design is proposed, based on a 20-mm GaN power bar. In particular, broadband terminations for both IMN and OMN optimized for large-signal operation have been synthesized, ensuring adequate performance over a wide range of frequencies. More precisely, as far as IMN is concerned, a conjugate matching condition has been reached under large-signal operation over the whole design bandwidth.

The provided experimental results demonstrate unequivocally the great advantages of adopting a large-signal input matching condition, with respect to design approaches based on small-signal operation.

2.3.1 Power amplifier design and realization

By exploiting the previously described active time-domain load-pull system, a preliminary low-frequency large-signal characterization has been carried out on a 2-mm ED, representative of a 20-mm power bar composed of ten elementary cells electrically in parallel. The main electrical characteristics of the selected ED are summarized in Table 11.

Quantity	*Value*
Breakdown Voltage	100 V
Pinch-off Voltage	-1.5 V
Idss	250 mA/mm
Saturated Output Power	5 W/mm

Table 5: 0.5-µm GaN HEMT technology specifications

The selected dynamic load-line referred to the current generator plane is shown in Fig. 2.17: as a matter of fact, such load-line provides an output power of 38.1 dBm with a drain efficiency of 63.8 %. The elementary cell is biased under deep class-AB condition (V_{DS} = *40 V,* I_{DS} = *57 mA*).

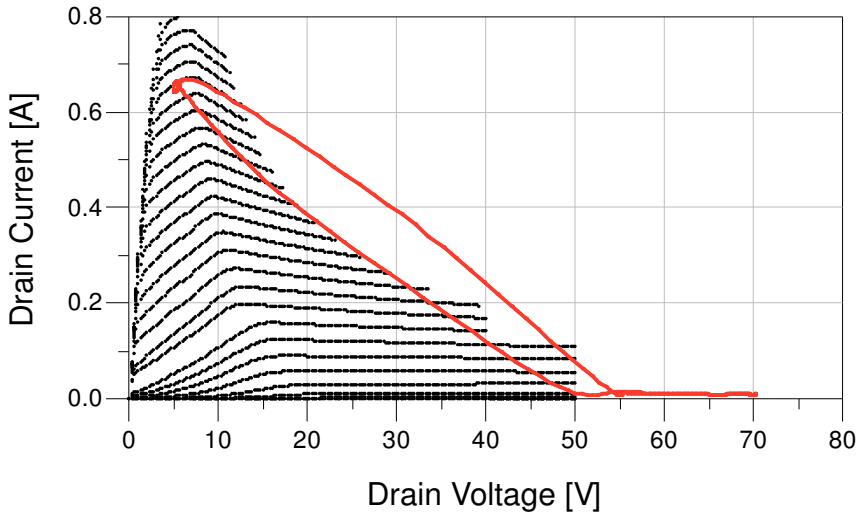


Fig. 2.17: Measurements performed on a 2-mm GaN HEMT device biased at (V_{d0} = 40 V, I_{d0} 57 mA). The load line is superimposed to the measured DC characteristics (-2 V ≤ V_{gs} ≤ 1 V, step 0.1 V).

Successively, accordingly with the adopted design approach, the capacitive core model (based on S-parameter measurement) has been iteratively exploited over the design band of 400 MHz centered at 1.2 GHz, in order to find out input and output broadband terminations corresponding to the selected low-frequency load line. In particular, the source termination was chosen in order to guarantee in the whole design bandwidth, a conjugate matching with respect to the large-signal input electron device impedance: such a condition allows the maximum power transfer under large-signal operations

Table 11 reports the synthesized source and load terminations, at the center frequency (i.e., 1.2 GHz) and at the extremes of the selected band related to the 2-mm elementary cell.

Source Impedance [Ω]	*Frequency [GHz]*	*Load Impedance [Ω]*
0.1 + j 32.0	1 GHz	73.0 + j 41.2
0.3 + j 26.4	1.2 GHz	66.7 + j 44.5
0.5 + j 22.4	1.4 GHz	60.6 + j 46.7

Table 11: Synthesized source and load impedances in the considered frequency range

The GaN HPA has been designed by synthesizing, on a high frequency laminate, an OMN which provides the chosen load impedances (Table 11) to each single 2-mm cell of the power bar. A picture of the realized amplifier is shown in Fig. 2.18. The high load impedance required by the

GaN devices allows for impedance transformation through a simple microstrip step-impedance structure together with open- and short-circuit stubs. IMN transformation has been obtained by means of a step-impedance transmission line in conjunction with two radial open-circuit stubs. Furthermore, a combined series-shunt RC stabilizing network, implemented by means of SMD resistors and ceramic capacitors, makes the device unconditionally stable from DC to the cut-off frequency. The power bar has been connected to both IMN and OMN boards by means of gold bonding wires.

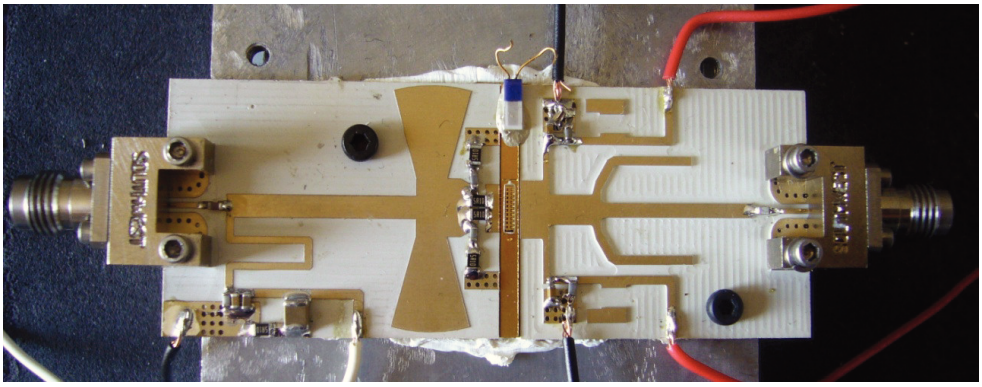


Fig. 2.18: Realized GaN hybrid HPA

Performance of the realized HPA has been evaluated by exploiting a large-signal measurement setup: as shown in Fig. 2.19, the HPA, driven with a constant available power of 38 dBm over the whole bandwidth, delivers an average saturated output power of 48.5 dBm over the frequency range of 1 – 1.4 GHz, with a power variation lower than 1 dB.

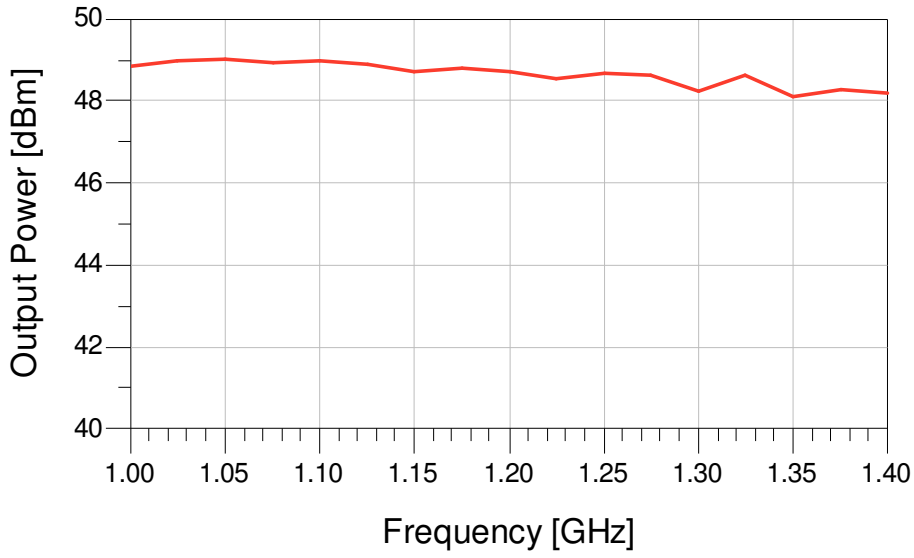


Fig. 2.19: Saturated output power of the realized HPA across the bandwidth 1 – 1.4 GHz..

Such a measurement condition corresponds to 3.5 dB of compression with respect to the measured linear gain of 14 dB. Moreover, measured power added efficiency (PAE), shown in Fig.2.20 is greater than 55 % in the whole design bandwidth, with a peak value of 65.2 % measured at 1.05 GHz. As a matter of fact, measured performance of the designed HPA are perfectly in agreement with the time-domain load-pull predictions, performed on the elementary cell representative of the power bar. In order to guarantee the same load-line at the current generator plane over the entire bandwidth, the three load impedances in Table 10 have been equally weighted in the IMN and OMN optimization. As a consequence, it is not surprising to have a slight better behavior at the lower bound of the bandwidth.

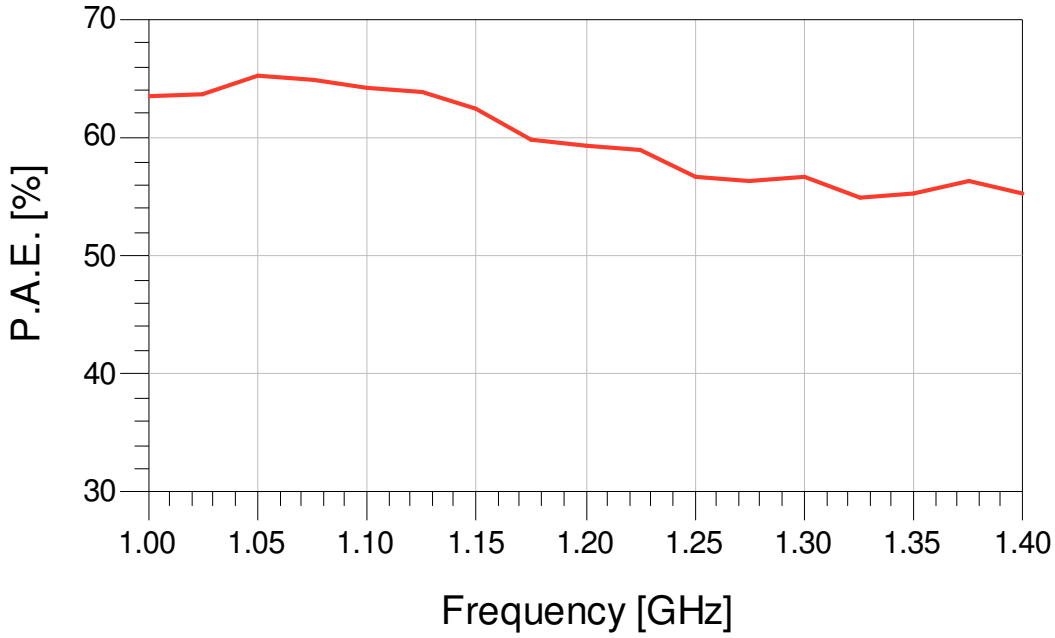


Fig. 2.20: PAE of the realized HPA across the bandwidth 1 – 1.4 GHz.

With the aim of demonstrating the great advantage introduced by exploiting large-signal input matching, the output power performance has been evaluated by driving the HPA with an available power of 19 dBm, corresponding to a small-signal driving condition. As clearly shown in Fig. 2.21, under such a back-off operating mode, measured output power shows 5 dB of variation over the whole HPA bandwidth. Moreover, the frequency trend of the measured output over the design bandwidth presents a monotonic slump from the lower to the upper bound. Such experimental evidences confirms unequivocally that optimal small-signal input termination is not related to the optimal large-signal impedance, which is the one of interest for HPA design.

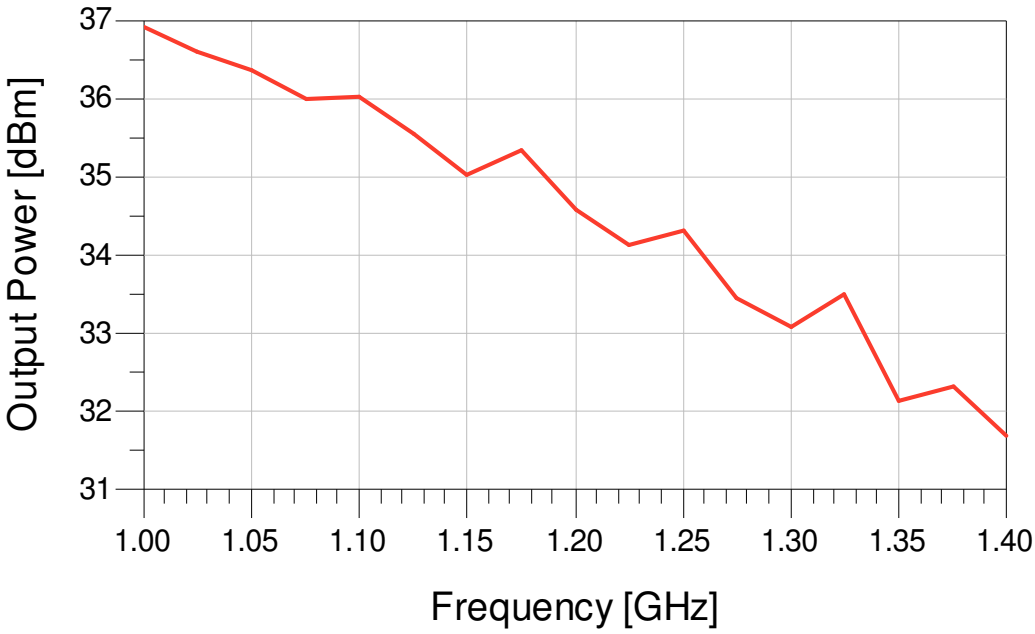


Fig. 2.21: Output power of the realized HPA measured in back-off condition across the bandwidth 1 -1.4 GHz.

Conclusion

In this chapter, an innovative power amplifier design methodology has been presented, based on low-frequency experimental characterization of the electron device nonlinear behavior in conjunction with a model based description of both nonlinear dynamic effects and parasitic phenomena. The technique enables the same level of accuracy provided by high-frequency large signal setups, exploiting a low-frequency active load-pull system, that allows to perform waveform engineering technique at the current generator plane of the electron device. Moreover, such setup has been exploited in order to deeply investigate low-frequency dispersion phenomena affecting microwave devices based on GaN technology.

Several power amplifier design examples have been provided, and a hybrid wideband high-power amplifier has been successfully realized, that confirms the effectiveness of the proposed technique.

In the next chapter, the proposed approach will be applied to high-efficiency classes of operations, that require the correct synthesis of power amplifier terminations not only at fundamental frequency, but also at its harmonics.

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Chapter 3

High-efficiency power amplifier design

Introduction

GaN technology has de facto established new trends in microwave systems and, in particular, in power amplifier (PA) design due to its promising performance. High power density capability of GaN transistors, in fact, has encouraged PA designers to be less concerned with output power restrictions, focusing their attention on more challenging design aspects.

In a world that is becoming more and more conscious about the need to ensure a sustainable energy future for wireless transmissions, increasing the efficiency of a microwave PA represents one of the most crucial design challenges. High-efficiency PAs, in fact, are the key components of the so called "green" microwave transmitting systems due to their intrinsic low power consumption, that enables a significant reduction of operating costs and an easier thermal management of the entire system.

In this scenario, high-efficiency PA operating classes have become a strategic topic, increasingly attracting the interest of both academic and industrial research community. In particular, designers tend to exploit harmonically-tuned (e.g., class F [1-4]) and switching (e.g. class E [5]) PA classes of operation since they exhibit better performance in terms of efficiency rather than traditional high-efficiency PA modes (e.g., class B [1-3]).

Accordingly with the theoretical formulation of harmonically-tuned PA classes, such as class F, short- and open-circuit harmonic terminations have to be synthesized at the device current generator plane, in order to obtain the required squared-up voltage and half-rectified current waveforms, which lead to the high-efficiency operation.

On the other hand, when dealing with class-E PAs, load matching networks have to be synthesized in order to satisfy the minimal overlapping condition of current and voltage waveforms at the current generator plane, forcing the ED to behave as a switch: this condition is a fundamental issue for dissipated power minimization.

In this chapter, the design approach described in the previous chapter is extended to predict fundamental and harmonic terminations that ensure adequate performance, in terms of output power and efficiency, for high-efficiency PA operating classes. To this aim, two high-efficiency class-F and class-E PAs have been successfully designed exploiting the mentioned technique.

3.1 Design scenario for class-F and class-E power amplifiers

The fundamental issue that is common to all high-efficiency PA operating modes, is to ensure that time-domain electrical variables, i.e., voltage and current waveforms, satisfy the minimal overlapping condition, to reduce the PA power consumption during its actual operation. It is worth noticing that such a kind of condition has to be imposed to the electron device (ED) intrinsic resistive core [6] (i.e., to the ED current generator plane), that is responsible for ED output power delivery and efficiency. In particular, waveforms at the ED intrinsic resistive-core are substantially different from the extrinsic ones due to important parasitic and nonlinear dynamic phenomena. These non-idealities are not negligible when the device operates in a proper frequency range (i.e., close to the maximum frequency of operation where the device still shows adequate performance).

Ideal class-F operating mode, for instance, ensures no overlapping between voltage and current time-domain waveforms referred to the ED current generator plane, leading to a theoretical efficiency of 100% [1-4]. Such a condition should be reached by engineering the waveforms in order to obtain a squared-up voltage waveform, that contains only fundamental and odd higher harmonic components, and a half-rectified current waveform, as shown in Fig.3.1.

From a frequency-domain point of view, class-F operating mode is obtained by imposing to the ED intrinsic resistive core ideal short- and open-circuit terminations at even and odd harmonic frequencies, respectively, whereas optimal load has to be synthesized at the fundamental frequency [1-4]. However, when dealing with practical class-F PA design, generally only fundamental, second and third harmonic terminations can be successfully synthesized [7-12]. As a consequence, the maximum achievable efficiency is reduced with respect to its theoretical value. In the case of class-F operating mode, efficiency is limited to 90.7% [2] that, however, still remains an utopian value, especially at microwaves.

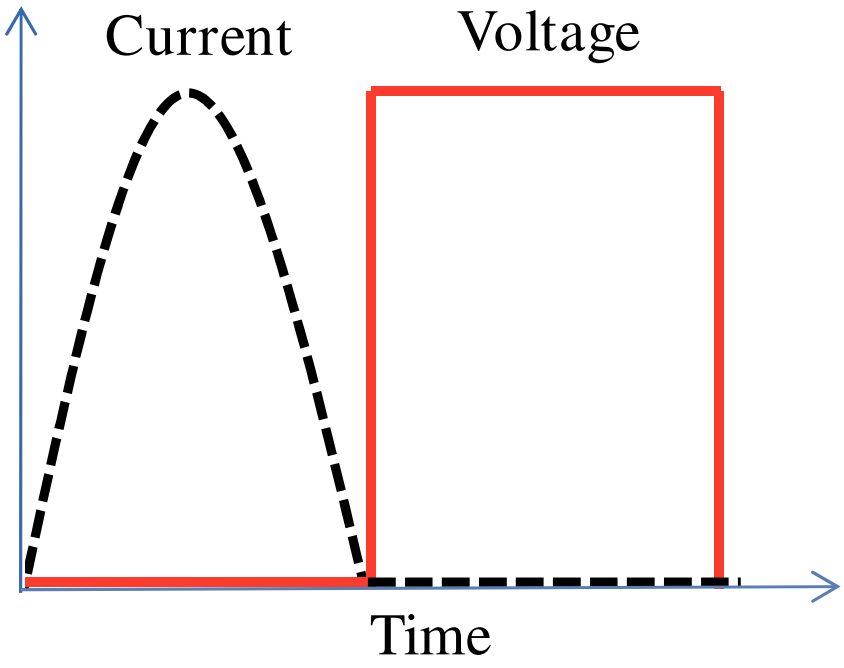


Fig. 3.1: Ideal current and voltage time domain waveforms corresponding to class-F operating mode.

Class-E operating mode belongs to switching classes of operation: in a class-E PA, in fact, the transistor is forced to behave as a switch in order to prevent simultaneous high level of voltage and current at the ED intrinsic resistive core.

As clearly shown in Fig. 3.2, typical class-E time domain voltage and current waveforms, referred to the ED resistive core, satisfy no-overlapping condition due to the switch behavior of the ED, leading such a kind of PA to achieve an ideal efficiency of 100% [5].

However, as for class-F, in practical class-E PA design the ideal value of 100% of efficiency significantly drops due to the ED switching delay together with parasitic losses.

Another peculiar aspect of class-E operation mode is related to high peak drain voltage, that typically reaches three time the bias voltage [2]: the inspection of ED intrinsic resistive core time domain waveforms become absolutely necessary for the correct choice of the drain bias voltage in order to keep the transistor far from possible disruptive damage.

In any case, one of the most effective approaches in order maximize the efficiency of a PA is represented by the waveform engineering technique applied at the ED current generator plane: the direct control of time domain voltage and current waveforms, in fact, allows to guarantee the minimal overlapping condition, that is necessary in order to enhance the efficiency of the PA.

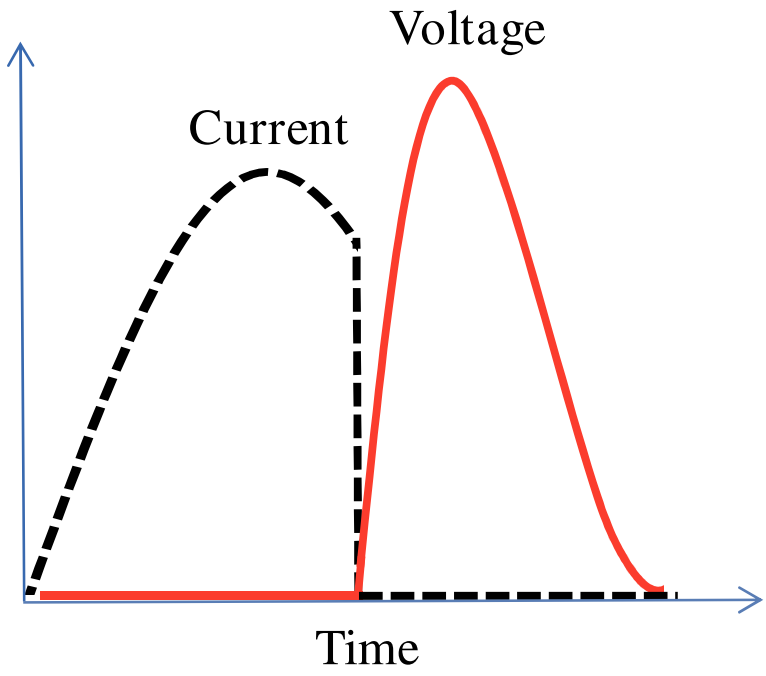


Fig. 3.2: Ideal current and voltage time domain waveforms corresponding to class-E operating mode.

3.2 Class-F power amplifier design

In this Section, a wideband class-F PA design carried out by exploiting the design approach described in chapter 2, is presented. The PA was based on a discrete 0.25 x 1250 μm^2 GaN on SiC HEMT, whose main foundry specifications are summarized in Table 1.

Quantity	*Value*
Breakdown Voltage	> 70 V
Pinch-off Voltage	-4 V
Idss	1 A/mm
Saturated Output Power	5 W/mm

Table 1: 0.25-µm GaN HEMT technology specifications

The GaN HEMT was biased under class-B condition (V_{g0} = -4 V, V_{d0} = 32 V, I_{d0} = 0 A) and, accordingly with the proposed approach, a low-frequency characterization of the device intrinsic resistive core was carried out. To this end, by exploiting the harmonic active load pull setup described in the previous chapter, appropriate incident gate and drain signals have been imposed to

the HEMT, at the fundamental frequency of 2 MHz and its harmonics, in order to find out a high-efficiency class-F load line.

In Table 2 the obtained low-frequency drain impedances are reported, while Fig. 3.3 shows the trajectory of the load line synthesized at the ED intrinsic resistive core, corresponding to a measured output power of 37.3 dBm with a drain efficiency of 78.8 %. In Fig. 3.3, the measured load line is compared to the one obtained by exploiting the foundry model (simulated output power of 38.4 dBm with a drain efficiency of 90 %). It is well evident the poor prediction capability, which is essentially due to the fact that foundry models are usually identified for class-A or AB operation. As said, thermal and trapping phenomena make very difficult the identification of a global and accurate model for the current generator [13-14].

Frequency [MHz]	*Load impedance [Ω]*
2	104.8 + j 5.9
4	0.7 – j 0.9
6	718.0 + j 1.2

Table 2: Measured low frequency drain impedances

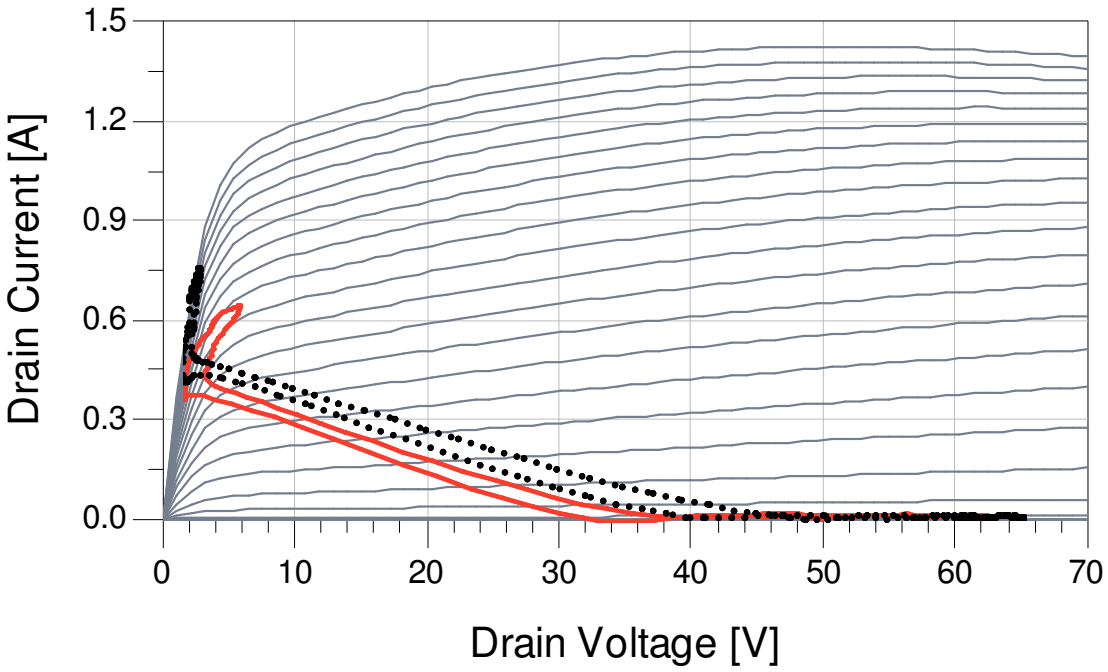


Fig. 3.3: Measurement (continuous line) and simulation (dotted line) under class-F operation performed on a 1.25-mm GaN HEMT device biased at (V_{d0} = 32 V, I_{d0} = 0 A). The load-lines are superimposed to simulated DC characteristics (-4 V ≤ V_{gs} ≤ 1 V, step 0.25 V).

As a matter of fact, as reported in Table 2, the second harmonic impedance results in a short-circuit condition whereas a high-impedance third harmonic termination has been obtained, both referred to the ED current generator plane. The experimentally synthesized impedances perfectly match with class-F theoretical formulation [1-4].

Fig. 3.4 shows the measured low-frequency time-domain voltage and current waveforms referred to the current generator plane: it is well evident that such electrical variables satisfy the minimal-overlapping condition imposed by class-F operation mode.

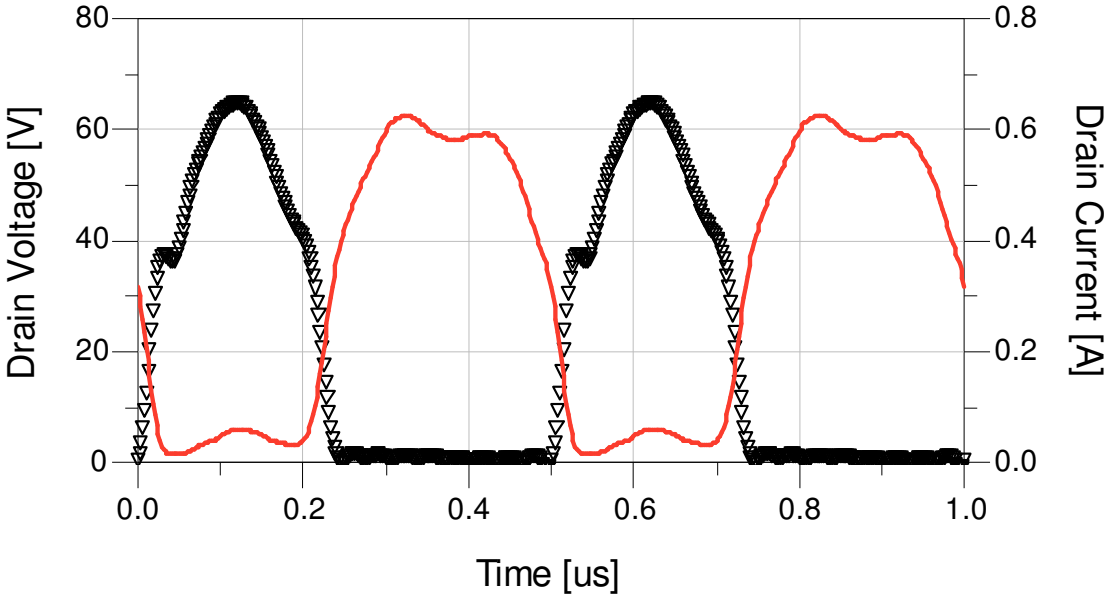


Fig. 3.4: Low-frequency time-domain voltage (continuous line) and current (triangles) waveforms at the device current generator plane, corresponding to the synthesized class-F operating mode.

Successively, according with the proposed design methodology, the obtained low-frequency electrical variables were iteratively applied to the capacitive-core and parasitic network descriptions, in order to obtain the frequency behavior of the terminations corresponding to the selected class-F operating mode. More precisely, the foundry model (EE_FET3 [15]) has been exploited for both the capacitive-core and the linear extrinsic parasitic network behavior.

Fig. 3.5 shows the trajectories of the fundamental, second and third harmonic input (a) and output (b) impedances, that have been computed in the frequency range of 2.3-2.5 GHz. Table 3 reports the synthesized terminations at the center frequency and at the extremes of the selected band. In particular, the source impedance has been chosen equal to the conjugate of the large-signal ED input impedance, over the whole bandwidth.

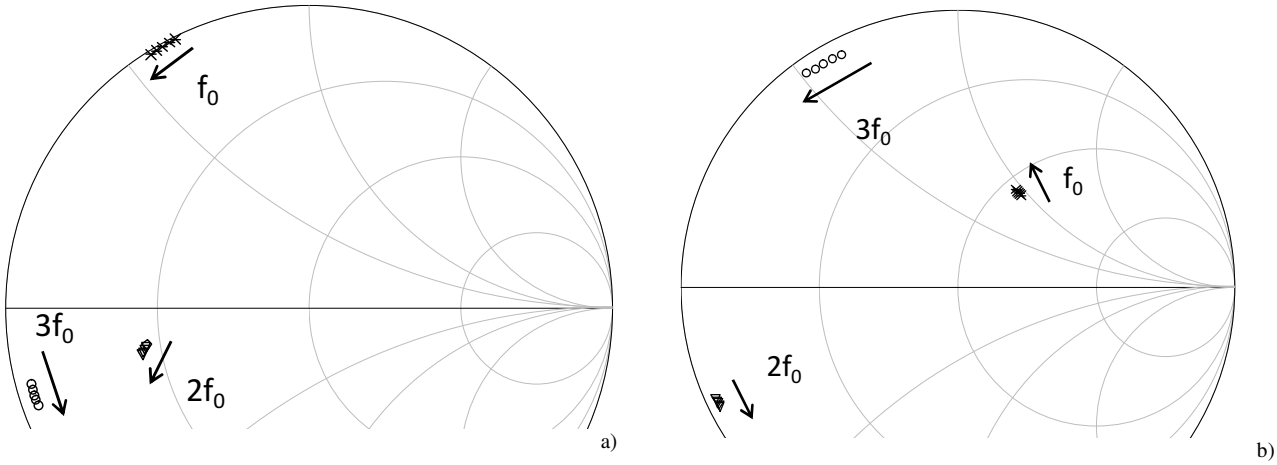


Fig. 3.5 Broadband source (a) and load (b) impedances evaluated in the frequency range 2.3 – 2.5 GHz: fundamental (stars), second (triangles) and third (circles) harmonic termination trajectories (4 GHz). (a) Power added efficiency (circles) and transducer power gain (triangles) - (b) Average drain current(circles) and Output power (triangles).

Source impedance [Ω]	*Frequency [GHz]*	*Load impedance [Ω]*
0.3 + j 31.0	2.3	59.7 + j 47.0
14.8 – j 5.1	4.6	1.0 – j 11.0
1.3 – j 6.7	6.9	2.2 + j 30.8
0.4 + j 29.3	2.4	57.7 + j 47.1
14.3 – j 5.8	4.8	1.0 – j 11.4
1.3 – j 7.7	7.2	2.0 + j 28.2
0.4 + j 27.7	2.5	55.7 + j 47.0
13.9 – j 6.5	5.0	1.0 – j 11.9
1.3 – j 8.7	7.5	1.8 + j 25.8

Table 3: Synthesized input and output terminations in the considered frequency range

In Table 4 extrinsic and intrinsic resistive-core load terminations are compared at the central frequency of 2.4 GHz. It must be outlined that information on the intrinsic resistive core impedance values is not directly deducible from the extrinsic data. As an example, the obtained third harmonic high impedance condition at the intrinsic device, typical of class-F operating mode, is not easily evincible from its extrinsic value. This is the reason why large-signal measurements carried out at the design frequency cannot give useful information at the current generator plane, unless a rigorous nonlinear de-embedding procedure is adopted [16].

Intrinsic resistive core load impedance [Ω]	*Frequency [GHz]*	*Extrinsic load impedance [Ω]*
104.8 + j 5.9	2.4	57.7 + j 47.1
0.7 – j 0.9	4.8	1.0 – j 11.4
718.0 + j 1.2	7.2	2.0 + j 28.2

Table 4: Comparison between selected intrinsic resistive core load impedance and extrinsic one as a function of frequency

Moreover, as clearly shown in Fig. 3.5, by observing extrinsic voltage and current time-domain waveforms at the design frequency of 2.4 GHz, it is very difficult to assert that the GaN HEMT is working in class-F operation mode, whereas this is well evident by looking to the same electrical variables referred to the current generator plane (Fig. 3.4).

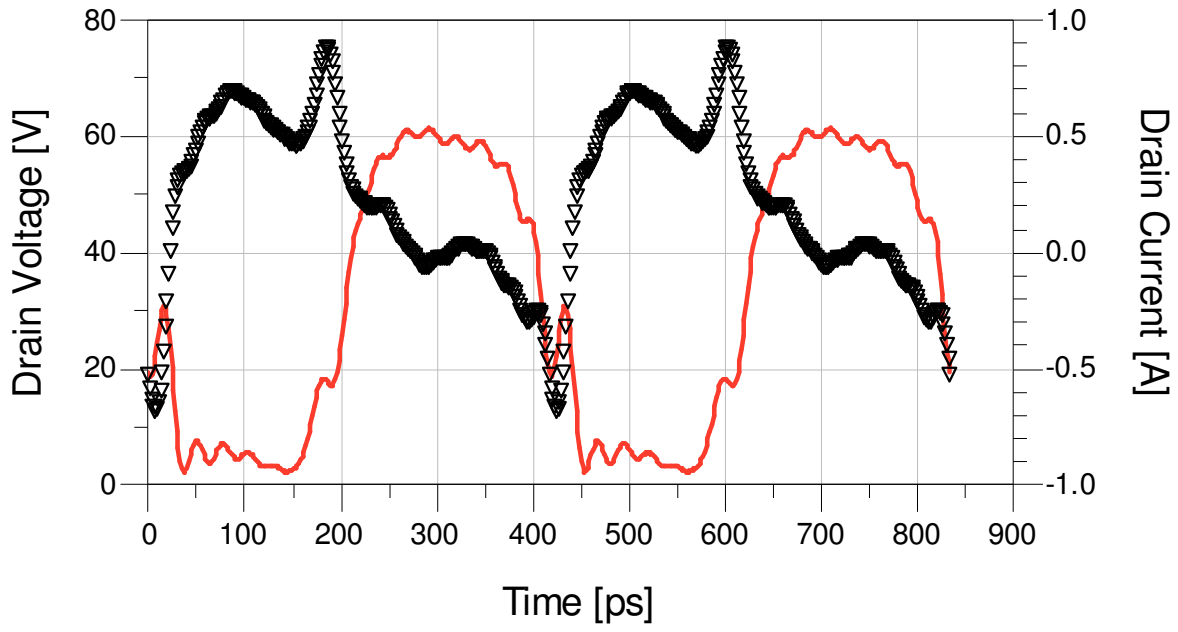


Fig. 3.5: Extrinsic time-domain voltage (continuous line) and current (triangles) waveforms at the device drain terminal, at the design frequency of 2.4 GHz..

The designed GaN class-F PA was manufactured on a high frequency laminate. A photograph of the realized class-F PA is shown in Fig. 3.6.

Fundamental and harmonic target impedances have been synthesized in the frequency range of 2.3 – 2.5 GHz by means of simple topologies for both the input (IMN) and output matching network (OMN), which are shown in Fig. 3.7. It must be observed that, once the trajectories over the frequency of fundamental and harmonic impedances have been computed exploiting the

proposed approach, an arbitrarily large bandwidth could be in theory obtained by increasing the topological complexity of the IMN and OMN. It must be outlined that few design techniques for broadband harmonically-tuned amplifiers are present in the literature, thus confirming the complexity of this topic.

Dealing with the IMN, the impedance transformation from 50 ohm has been obtained by means of step-impedance structures together with an open circuit stub. Two short-circuit stubs, having both electrical length of $\lambda/4$ at $2f_0$ and f_0, have been added in order to match second and third harmonic impedances (Fig. 3.7a).

The OMN has been implemented by means of open- and short-circuit stubs in conjunction with step-impedance transmission lines. Second and third harmonic matching has been obtained by exploiting two short-circuit stubs having both electrical length close to $\lambda/4$ at $2f_0$ and $3f_0$ (Fig. 3.7b).

Ceramic capacitors have been used in order to separate RF and DC signals for both IMN and OMN.

Finally, the ED has been connected to both the IMN and OMN boards by means of gold bonding wires.

Performance of the realized class-F PA has been evaluated by exploiting a high-frequency large-signal measurement setup, that has been properly calibrated for ensuring accurate measurements at the device planes.

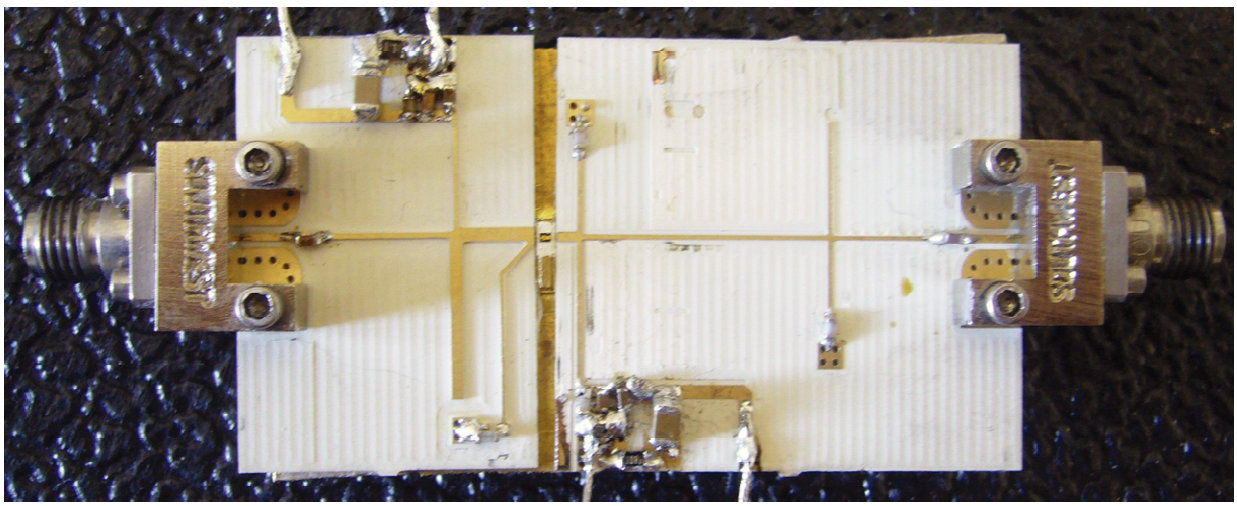


Fig. 3.6: Realized GaN class-F hybrid power amplifier

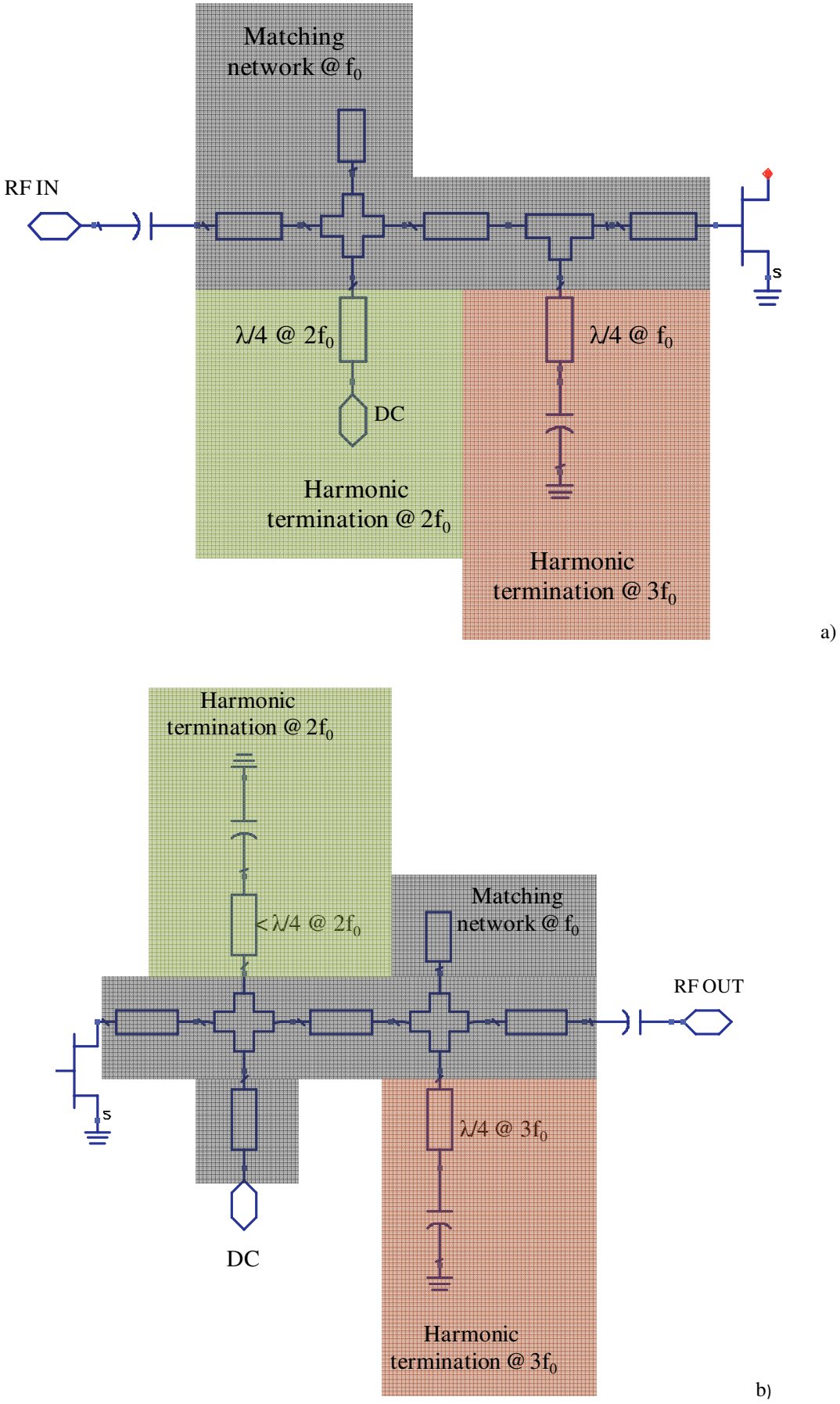


Fig. 3.7: Input (a) and output (b) matching network topologies of class-F PA..

As shown in Fig. 3.8, the realized class-F PA delivers an output power greater than 36 dBm with a drain efficiency greater than 55% over the frequency range of 2.3 – 2.5 GHz, with a maximum of 36.9 dBm and 74% at 2.45 GHz.

Moreover, if the PA bandwidth is considered in the frequency range 2.375 – 2.475 GHz, measured efficiency is always greater than 70%, while output power is never lower than 36.9 dBm.

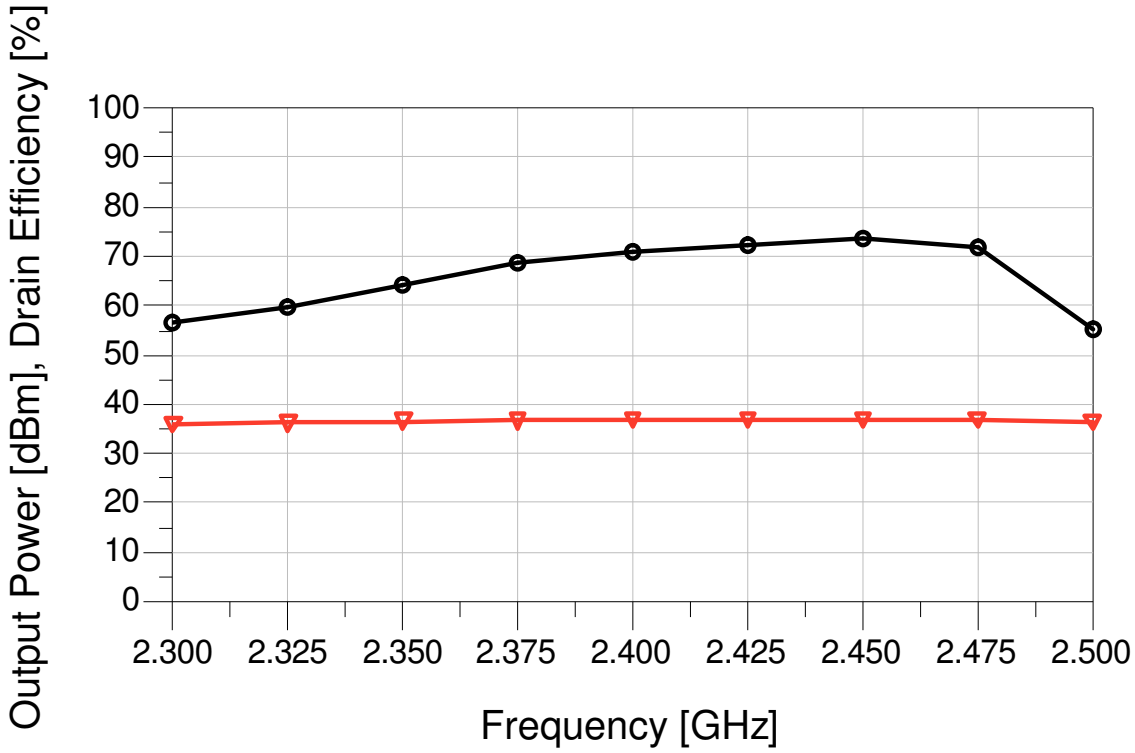


Fig. 3.8: Measured output power (triangles) and drain efficiency (circles) of the realized PA across the bandwidth 2.3 – 2-5 GHz.

With the aim of comparing the experimental performance of the PA with the predicted one, that are referred to the ED ports, both measured output power and drain efficiency were de-embedded from the losses of the OMN. Fig 3.9 shows the performance of the PA referred to the ED plane. As a matter of fact, an output power greater than 36.4 dBm with a drain efficiency greater than 61% were registered over the frequency range of 2.3 – 2.5 GHz. The peak value of the output power and drain efficiency were, in this case, 37.4 dBm and 84% respectively. Besides, in a smaller range of frequencies (2.375 -2.475 GHz), efficiency is always greater than 80% and output power is never smaller than 37.3 dBm.

Experimental performance at the ED reference plane are in very good agreement with the predicted ones (37.3 dBm and 79 %), based on the low-frequency load line characterization.

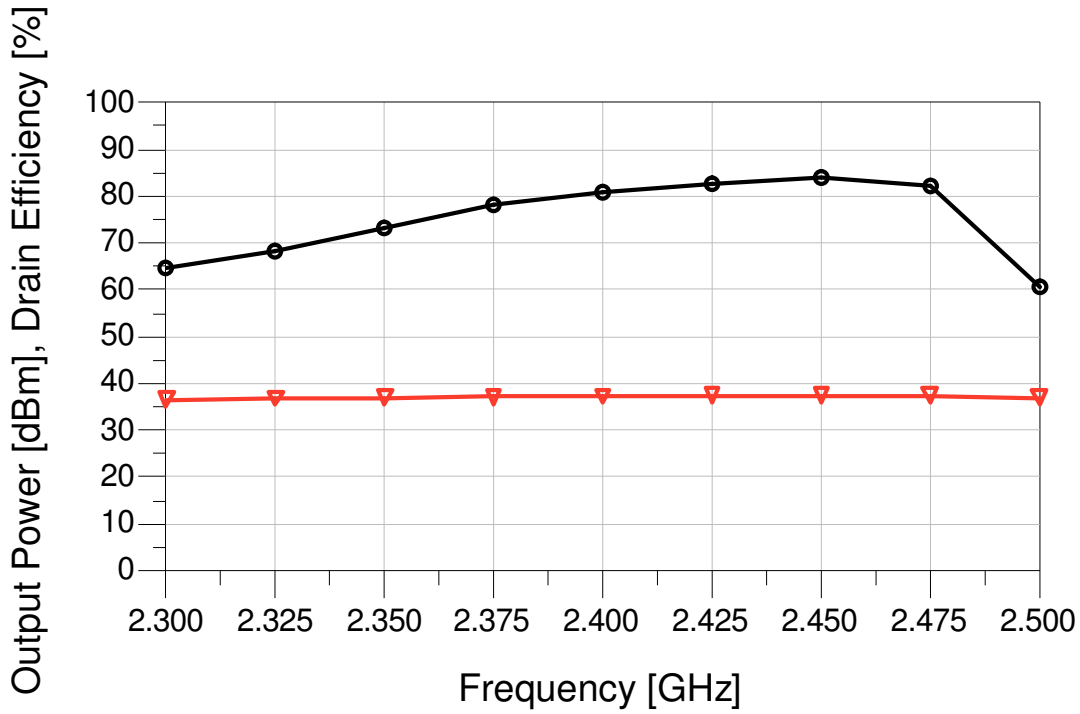


Fig. 3.8: Measured output power (triangles) and drain efficiency (circles) of the realized PA, referred to ED plane, across the bandwidth 2.3 – 2-5 GHz.

Finally, Fig 3.9a shows the output power and drain efficiency sweeps at 2.45 GHz (frequency where the best performance are reached) referred to the amplifier ports, whereas in Fig 3.9b the same data are shown at the ED plane.

It should be pointed out that excellent performance of high-efficiency PAs in terms of bandwidth is typically reached by considering large variations of the output power (the state of the art can be found in [17]). However, the designed PA has shown a relatively constant output power over the whole bandwidth. Moreover, the obtained output power, compared with the periphery of the adopted GaN device, is very close to the limit achievable by exploiting the selected technology (i.e., 5 W/mm).

It is worth noticing that the PA performance in terms of output power and efficiency, over the whole bandwidth, represents a very attractive result since it has been obtained exploiting very simple topologies of both input and output matching networks.

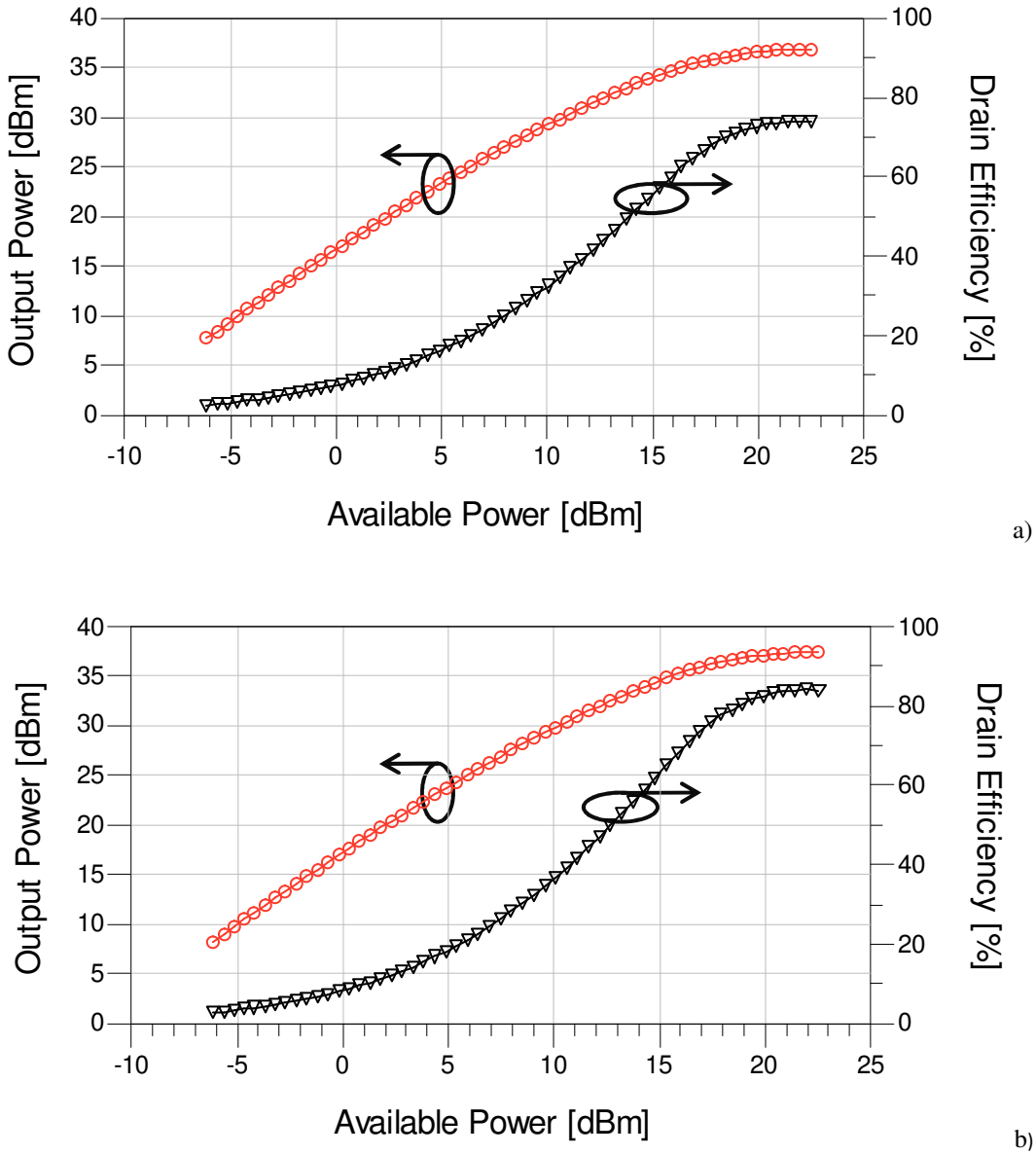


Fig. 3.9: Measured performance of the realized class-F PA: a) output power (circles) and drain efficiency (triangles) of the PA; b) output power (circles) and drain efficiency (triangles) referred to the electron device plane

3.3 Class-E power amplifier design

Class-E PA design has been carried out by exploiting a discrete 0.25 x 1250 μm^2 GaN on SiC HEMT device, that is the same ED used for the class-F PA design described in the previous section and whose main foundry specifications are summarized in Table 1.

According with the design methodology described in chapter 2, a low-frequency (i.e., 2 MHz) characterization of the ED resistive core was carried out by exploiting the measurement setup previously mentioned. To this end, the discrete 0.25 x 1250 μm^2 GaN on SiC HEMT was initially biased under class-B condition (V_{d0} = 21 V, I_{d0} = 0 A). More precisely, the drain bias voltage was

chosen in order to not exceed breakdown limitation of the selected technology under RF operation (see Table 1).

Successively, appropriate low-frequency drain and gate incident signals, at fundamental and harmonic frequencies, were imposed to the electron device in order to synthesize a class-E-shaped load-line. Table 5 summarizes the obtained low-frequency drain impedances, whereas Fig. 3.10 reports the trajectory of the synthesized load-line. It is worth noticing, that the dynamic drain voltage was kept lower than 60 V, well below the device breakdown limit. As a matter of fact, an output power of 33.7 dBm with a drain efficiency of 81.1 % were measured on the elementary cell.

Frequency [MHz]	*Load impedance [Ω]*
2	104.1 - j 92.0
4	1.2 + j 103.2
6	299.8 + j 181.3

Table 5: Obtained low frequency drain impedances

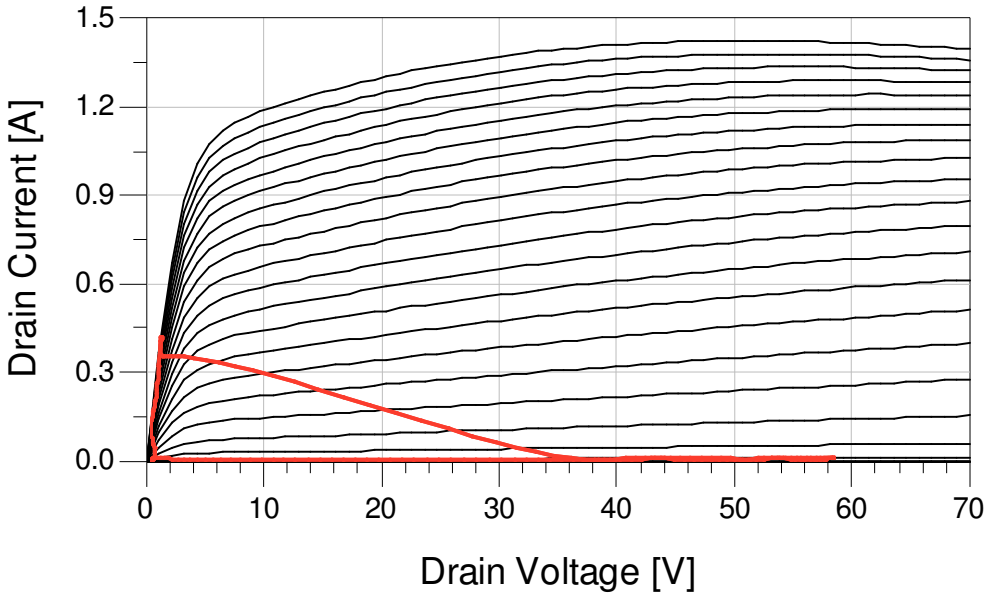


Fig. 3.10: Measurements performed by exploiting the LF load-pull setup on a 1.25-mm GaN HEMT device biased at (V_{d0} = 21 V, I_{d0} = 0 A). The measured load-line is superimposed to simulated DC characteristics (-4 V ≤ V_{gs} ≤ 1 V, step 0.25 V).

Fig. 3.11 shows the intrinsic time-domain voltage and current waveforms: it is well evident that the selected operating mode is typical of a Class-E PA and satisfies the minimal-overlapping condition imposed by switching mode PAs.

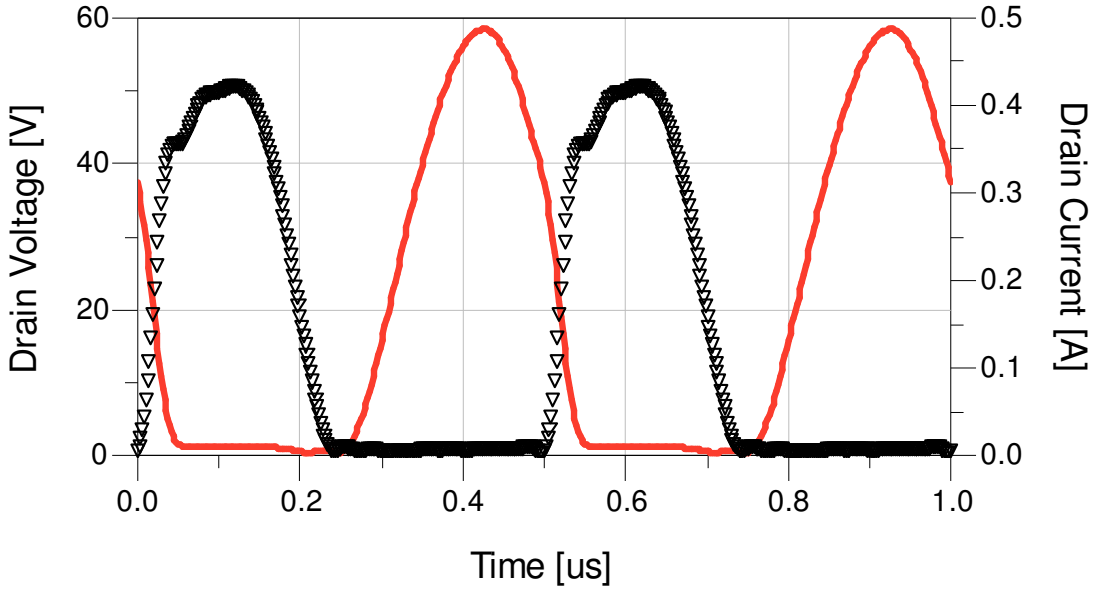


Fig. 3.11: LF time-domain voltage (continuous line) and current (triangles) waveforms at the elementary cell current generator plane, corresponding to the synthesized class-E operation mode.

In order to find out load and input impedances at the design frequency of 1.2 GHz, the design methodology outlined in chapter 2 has been applied. More precisely, a foundry-model-based (EE_FET3 [15]) description for both the elementary cell capacitances and parasitic elements has been adopted in order to compute the extrinsic device voltage and currents shown in Fig. 3.12: it is worth noticing that, by observing extrinsic electrical variables, it is practically impossible to deduce the switch-behavior typical of Class-E operating mode which is instead well evident at the current generator plane (see Fig. 3.11).

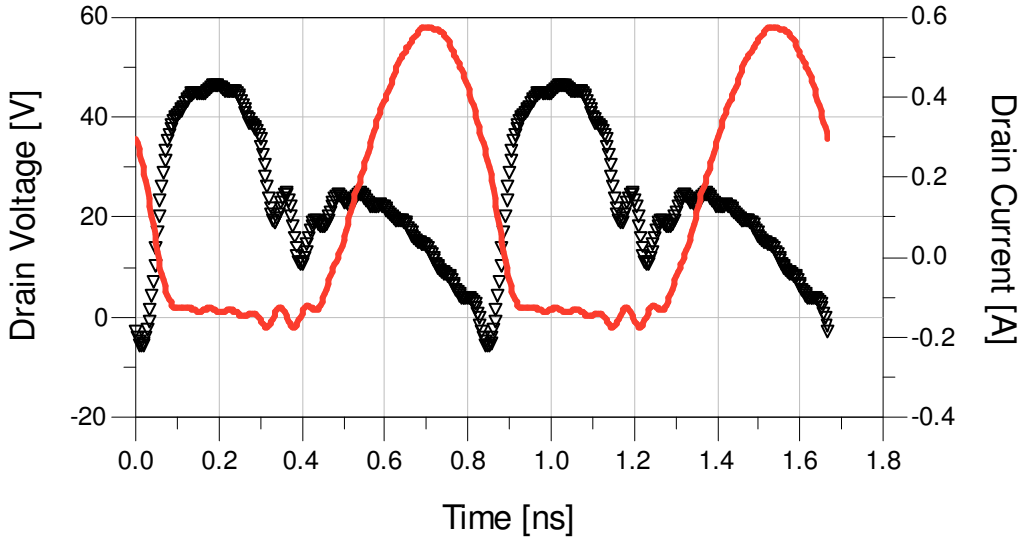


Fig. 3.12: Extrinsic time-domain voltage (continuous line) and current (triangles) waveforms at the device drain terminal, at the design frequency of 1.2 GHz.

Table 6 summarizes the computed source and load terminations at the fundamental frequency (f_0) of 1.2 GHz and related harmonics, that have been scaled for the power bar starting from the obtained elementary cell impedances. In particular, the source termination was chosen equal to the conjugate of the power bar input large signal impedance.

Source impedance [Ω]	*Frequency [GHz]*	*Load impedance [Ω]*
16.7 + j 72.9	1.2	175.5 - j 31.2
15.6 – j 2.3	2.4	1.0 + j 54.5
1.8 – j 5.1	3.6	11.5 + j 55.3

Table 6: Computed source and load impedances.

The class-E GaN power amplifier has been designed by synthesizing, on a high frequency laminate, suitable input and output networks which provide the chosen source and load impedances (Table 6) to the discrete 1.25-mm ED. A picture of the realized amplifier is shown in Fig. 3.13.

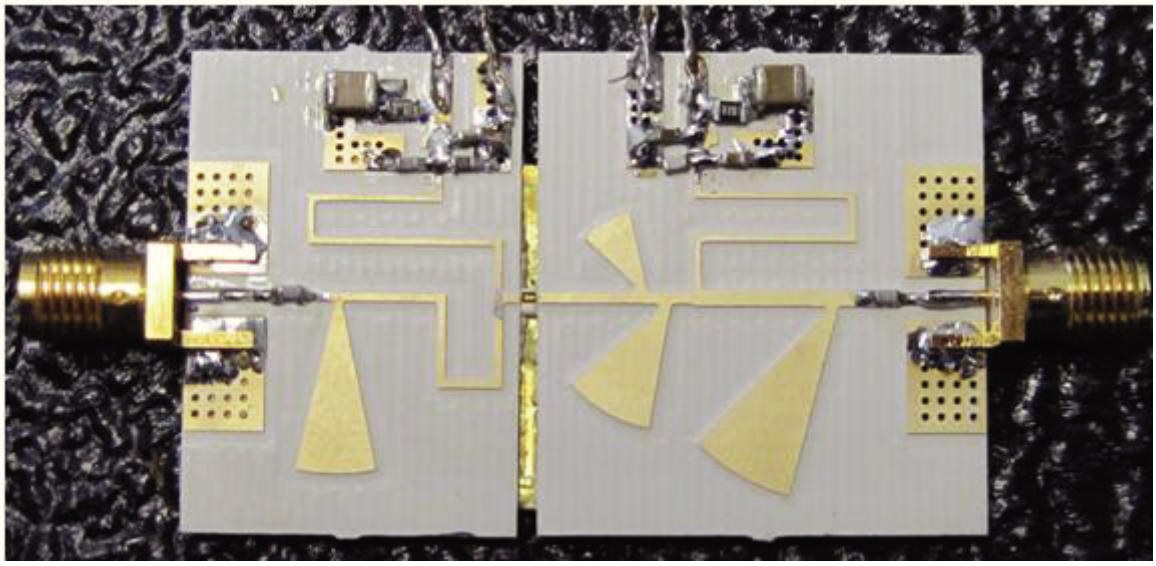


Fig. 3.13: Realized GaN class-E hybrid power amplifier

Impedance transformations related to both input and output matching network, have been implemented by means of radial stubs in conjunction with step-impedance structures, which guarantee the predicted terminations at the ED plane. The topologies of the input matching network (IMN) and output matching network (OMN) are shown in Fig. 3.14.

In particular, the input matching network has been designed in order to synthesize the predicted impedance only at the fundamental frequency, whereas for the output matching network, two radial

stubs having electrical length of λ/4 at $2f_0$ and $3f_0$ respectively have been added close to the drain of the ED (see Fig. 3.14b) in order to match the second and third harmonic impedances.

Decoupling ceramic capacitors have been chosen for both the matching networks in order to separate RF and DC signals. Moreover, gate and drain bias networks have been realized employing high impedance λ/4 microstrip lines with shunted SMD chip capacitors. Finally, the ED was connected to the input and output matching networks by means of gold bonding wires.

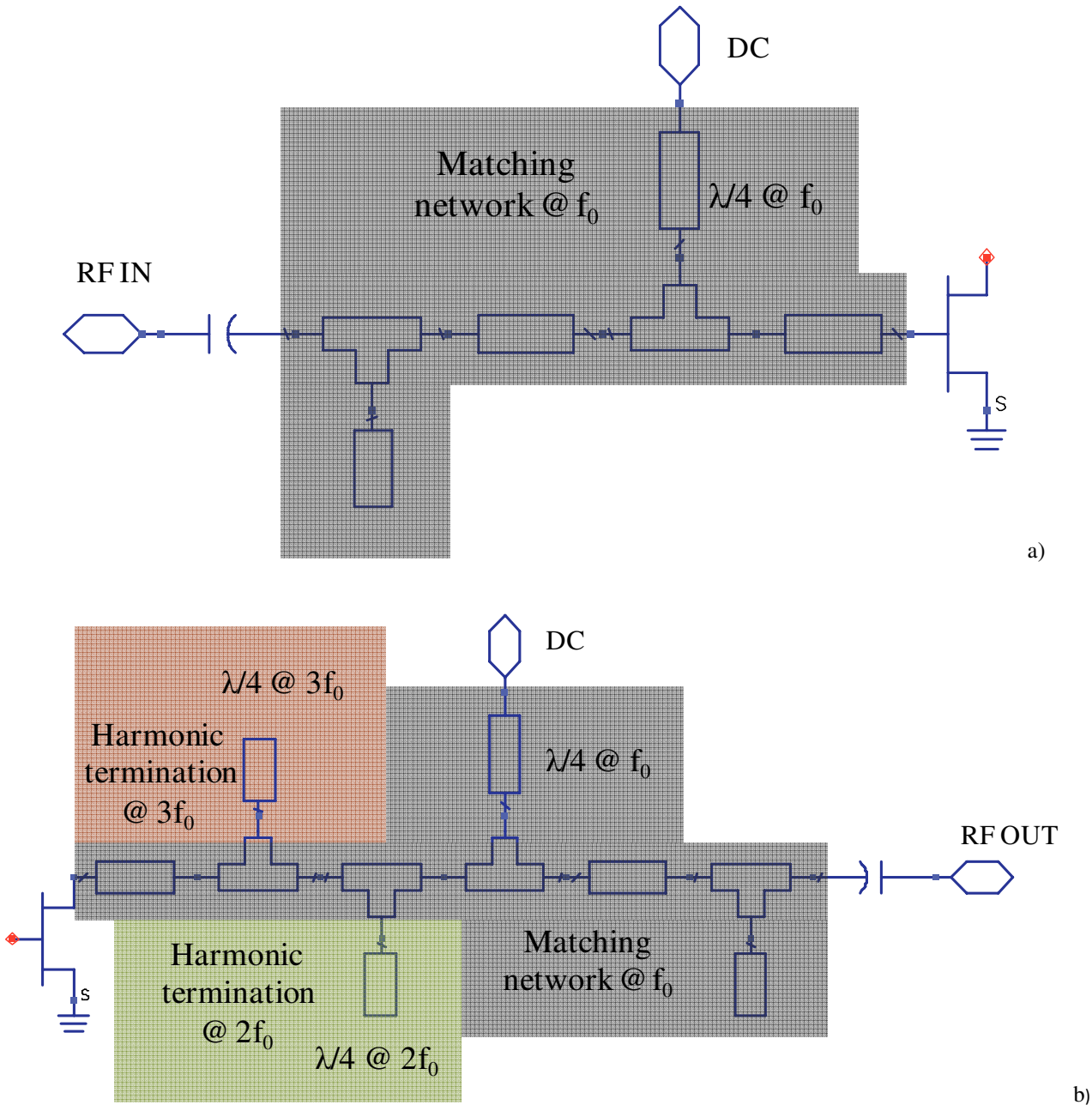
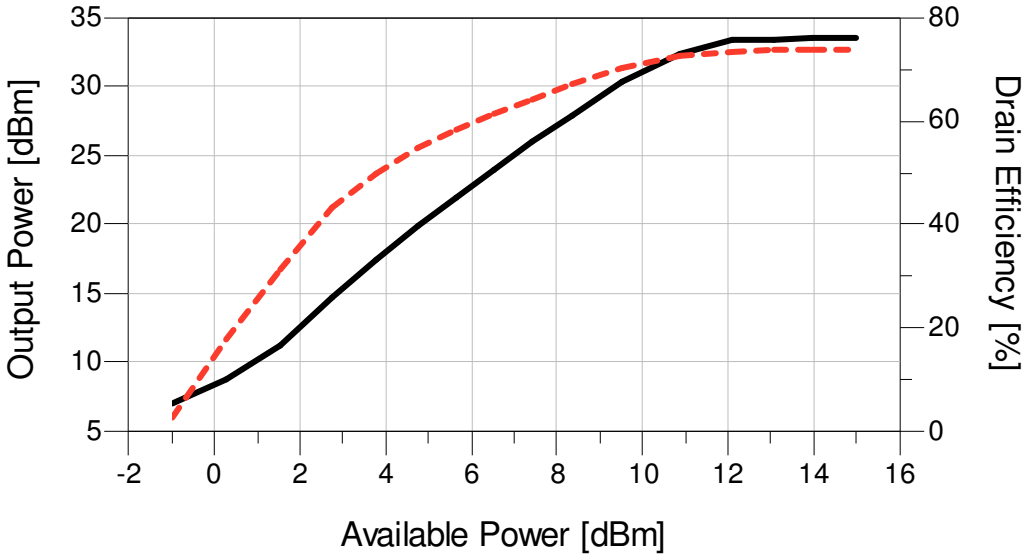
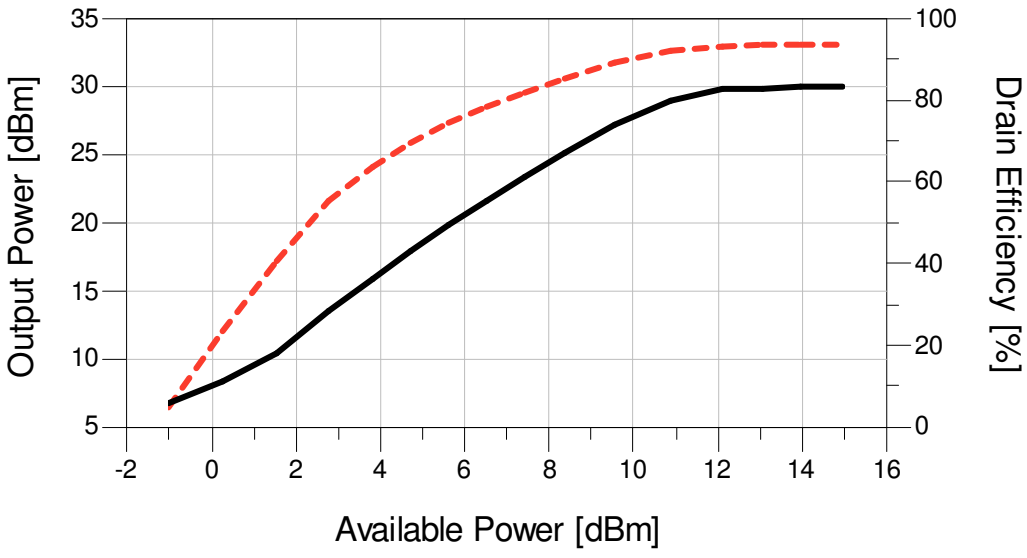


Fig. 3.14: Input (a) and output (b) matching network topologies of class-E PA.

Fig. 3.15 (a) shows the main performance of the realized PA: as a matter of fact, an output power of 32.7 dBm with a drain efficiency of 76 % were measured. Moreover, Fig. 3.15 (b) shows the performance of the amplifier referred to the device plane: as confirmed by Table 7, output power and drain efficiency at this plane are in excellent agreement with the performance predicted by the low-frequency characterization.



a)



b)

Fig. 3.15: Measured performance of the hybrid class-E PA: a) output power (dashed line) and drain efficiency (solid line) of the PA; b) output power (dashed line) and drain efficiency (solid line) referred to the electron device plane.

Predicted	*Quantity*	*Measured*
33.7 dBm	Output Power	33.4 dBm
81.1 %	Drain Efficiency	83 %

Table 7:Comparison between device performance predicted by the proposed technique and measurement data.

Conclusion

In this chapter, the design of two high-efficiency class-F and class-E PAs has been carried out by adopting the innovative design approach described in chapter 3 in order to find out the correct terminations not only at fundamental frequency, but also at harmonics. Both the realized PAs had shown adequate performance in terms of output power and efficiency, that are perfectly in agreement with the predictions carried out by applying the waveform engineering technique at low frequency, ensuring the same level of accuracy of expensive high frequency nonlinear setups.

In the next chapter, another important PA design aspect will be dealt with, related to degradation and performance limitation of microwave electron devices. Several experimental results will be presented and a new measurement setup, oriented to the characterization of degradation phenomena of microwave electron devices, will be introduced.

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Chapter 4

Degradation phenomena of electron devices in microwave power amplifier design

Introduction

Electron device degradation, although not directly accounted for, represents a key issue in microwave power amplifier design. This is especially true when the particular applications involved (e.g., satellite, military, consumer) do not allow or strongly discourage any kind of maintenance. As a matter of fact, in order to account for device degradation in circuit design, a suitable electron device model is needed which is able to predict the performance degradation as a function of the actual electrical regime involved in the device operation. Such a kind of model is not available in literature.

In this chapter, an innovative measurement setup, oriented to the characterization of degradation and performance limitation of microwave field effect transistor (FET) devices will be proposed. Quantitative results will be provided for device-degradation indicators which correlate DC and RF stress experiments, carried out on GaAs FET electron devices by exploiting the proposed measurement system. These results can be considered an important step toward the definition of a nonlinear model accounting for device degradation.

Moreover, an empirical study of the performance limitation of GaN devices will be dealt with. Measurements has been performed on three devices provided by three different foundries will be presented, in order to assess the generality of the investigated phenomena that limit the achievable performance of the transistors.

4.1 The innovative measurement system

The architecture of the proposed measurement setup is shown in Fig. 4.1:

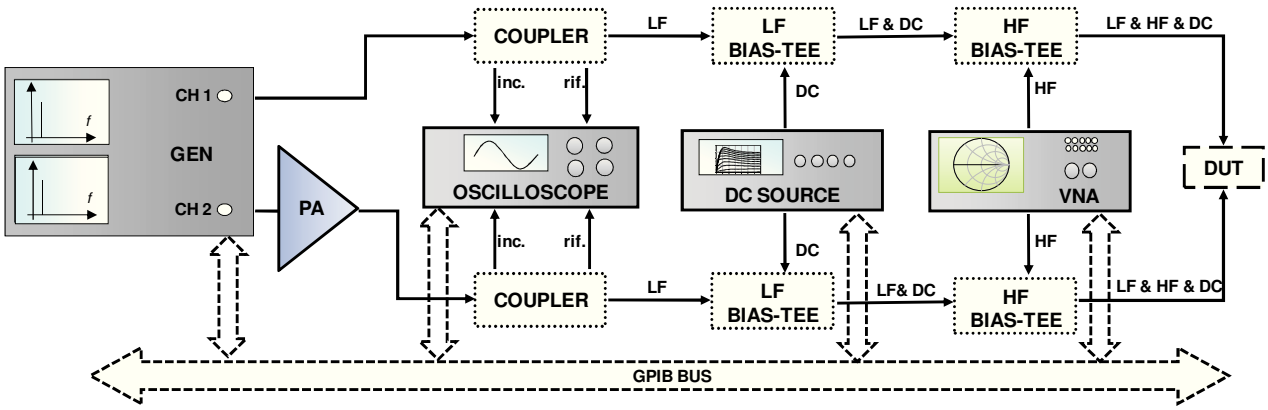


Fig. 4.1: Block diagram of the proposed measurement system.

This setup allows to perform transistor characterization and stress measurements on the device under static or dynamic conditions. In particular, it features a full dual-source excitation system that allows to automatically synthesize any loading condition of interest. Moreover, with the aim of investigating the degradation impact at the design frequency, the capability of measuring S-parameters at microwave frequencies has been added. In order to characterize the device under both high- and low-frequency excitations, as shown in Fig. 4.1, two couples of bias-tees are used: the low-frequency (LF) bias-tees (200 kHz – 12 GHz) are used to perform large-signal measurements at a few megahertz, under realistic nonlinear operation, whereas through the high-frequency (HF) bias-tees (1 GHz – 26.5 GHz) the device linear response at microwave frequencies can be monitored, even during the stress procedure. It should be pointed out that the HF bias-tees have been chosen in order to guarantee that both DC and low frequency (i.e., few megahertz) signals flow unaltered through the DC path of the HF bias-tees. The proposed setup requires a double calibration: the first one, as described in [1], is related to LF measurements; in addition, a standard on-wafer calibration for microwave S-parameter measurements [2] is adopted.

Exploiting the proposed measurement system, several stress procedure can be defined. Under static operation the device can be stressed by applying: I) constant currents; II) constant voltages; III) constant current at one port and constant voltage at the other. Since FETs are typically voltage-controlled, the all-current option is the least interesting. On the other hand, the other two choices present some valuable aspects: option II is the natural way to control the device, while with option III one can impose the gate current, which defines the carrier flow through the gate, and the drain voltage, which sets the electric field applied to the carriers.

Moreover, under nonlinear dynamic operation, the stress modes can be set in order to synthesize realistic operating conditions (i.e., voltage bias and plausible load line) as well as some degree of stress acceleration.

The setup has been fully automated to collect all the data of interest during the stress experiments.

4.2 Analysis of the gate current as a suitable indicator for GaAs FET degradation

Nonlinear modeling of electron devices represents one of the fundamental topics of microwave literature [3-5]. A nonlinear model allows simulating the device behavior under the actual operating conditions (i.e., nonlinear dynamic operation) that are defined by the specific circuit considered (e.g., amplifier, mixer, oscillator). However, when electron devices are subject to degradation [3], [6-7] during their operating life, this inevitably leads to a degradation of circuit performance. As a consequence, device and circuit performance during operating life may become increasingly different from the one predicted by the nonlinear model identified on the basis of measurements carried out on the "fresh" (i.e., not stressed) device.

As a matter of fact, microwave FET device degradation has been extensively studied under static device operation [6-7], which is extremely different from the actual device operation. The reasons for such a choice are multiple: a) DC experiments are simpler and allow for easier identification of accelerated stressing conditions, thus avoiding the complexity of large-signal high-frequency measurement setups [8]; b) also from the standpoint of numerical simulation and modeling in general, nonlinear dynamic operation is quite unpractical both for complexity and simulation time.

On the other hand, RF lifetesting has been extensively used to project mean time-to-failure (MTTF) data under more realistic conditions, but the combination of temperature acceleration, DC bias, and compression-level power results in a very complex situation to interpret and the conclusions that one can draw based on these tests typically do not go much beyond the extrapolated MTTF.

A nonlinear model for microwave design allowing to predict device (and, as a consequence, circuit) degradation does not exist in the literature. The following study of degradation indicators under actual device operation, represents an important first step toward the definition of a nonlinear model accounting for degradation issues.

4.2.1 Theoretical overview

The present considerations are related to FETs for microwave power amplifiers. Under dynamic conditions, whichever is the chosen class of operation, the region of the device characteristics characterized by high drain-source voltage and low drain current is inevitably touched by the I/V load line. Biasing the device, either statically or dynamically, in this high-field region often leads to observing degradation modes like DC current and transconductance collapse, and RF output power and gain degradation. These degradation modes are always accompanied (and typically preceded) by the breakdown walkout phenomenon [1], [7], which is a very sensitive indicator of the presence of hot-carrier-induced changes in the device.

A degradation model should be able to provide accurate predictions of device performance degradation on the basis of preliminary data acquired by nonlinear model extraction performed on fresh devices and suitable stress experiments. These preliminary data describe the device initial state and must contain suitable indicators that can be efficiently adopted to monitor degradation.

When stress analysis is carried out under DC operation, the gate current is commonly accepted as a stress indicator (e.g., [6]). In order to maintain compatibility with the large amount of information available in the literature, a first reasonable guess is that of preserving the gate current as a stress indicator also under high-frequency nonlinear dynamic operation. Nevertheless, which component of the gate current should be considered is an open question. In fact, the gate current can be divided in two terms:

$$i_g = i_{gr} + i_{gc}, \tag{1}$$

where i_{gc} represents the capacitive contribution and i_{gr} the resistive one. More precisely, i_{gr} can be expressed as:

$$i_{gr} = I_g^0 + i_{gr}^s, \tag{2}$$

where I_g^0 is the average value, whereas i_{gr}^s is the signal component. The capacitive contribution will be neglected in this work coherently with the common approach in reliability studies based on DC stress [6-7]. In this scenario, eq. (2) indicates two possible degradation indicators: the average value (I_g^0), which measures the average flow of carriers through the gate, and its peak value i_{gr}^p , which is connected with the peak value of the electric field applied at the gate-drain junction.

4.2.2 Experimental results and considerations

As a first step, a constant-gate-current stress has been applied to 0.35 µm GaAs PHEMTs having a gate periphery of 1.5 mm, maintaining a constant drain voltage. Fig. 4.2 shows the gate voltage walkout. It is evident that after 130 h the device has not reached a "stable" asymptotic condition.

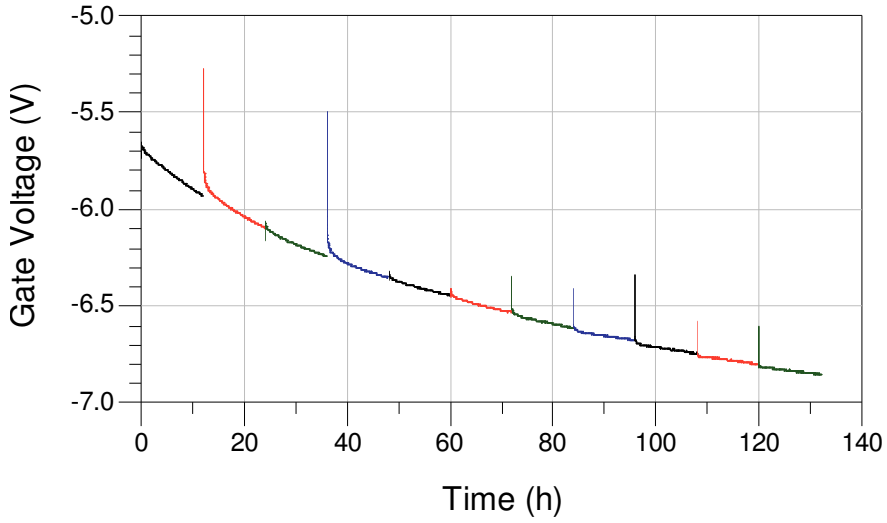
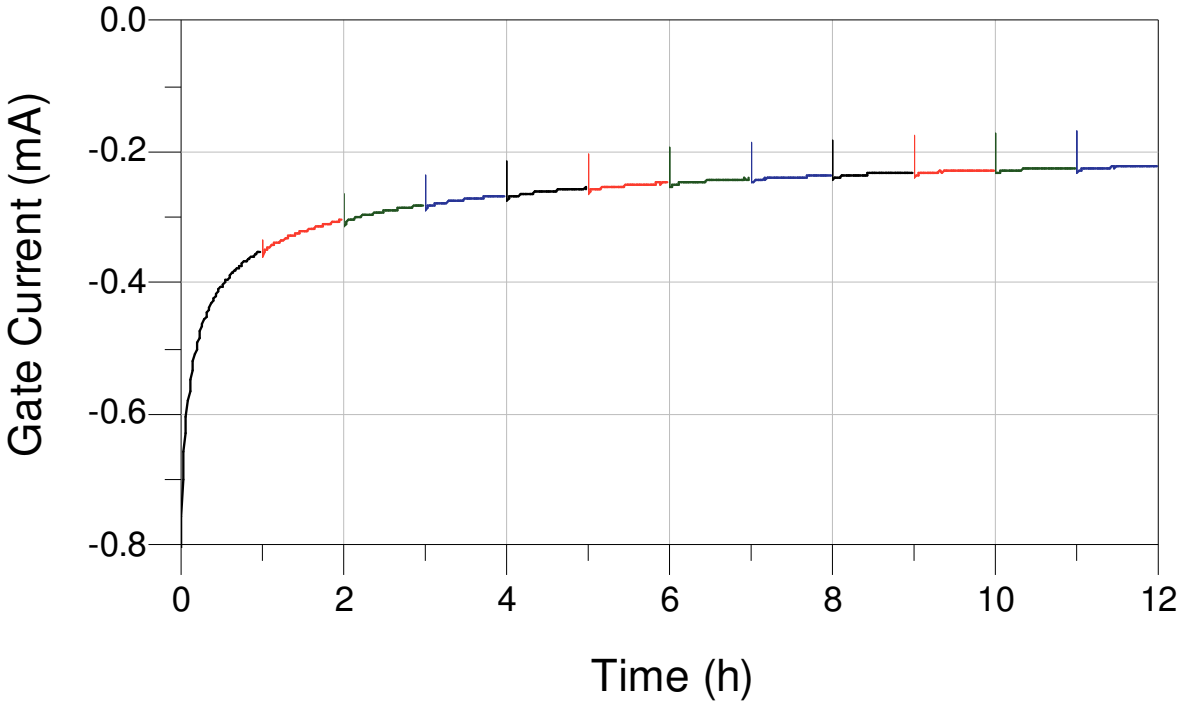


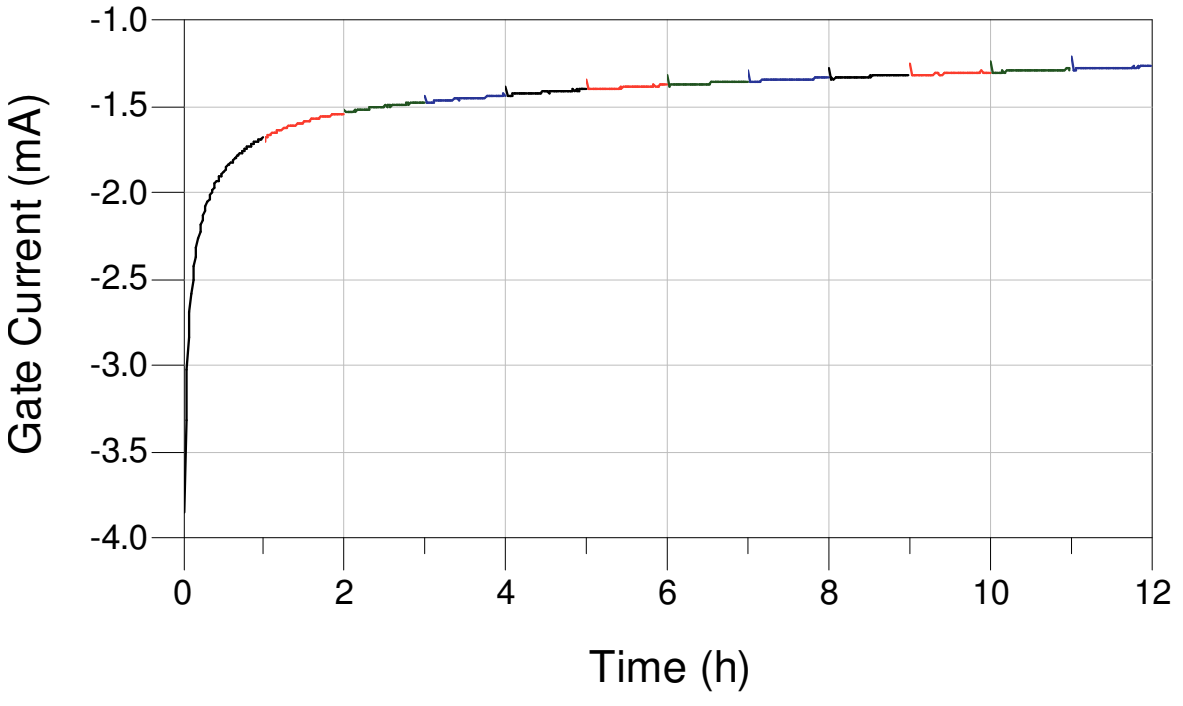
Fig. 4.2: Gate voltage walkout under DC stress (I_g^0 = - 0.7 mA/mm, V_d^0 = 18 V). The stress is interrupted every 12 hours and resumed after device characterization.

On the contrary, the device quickly reaches an asymptotic condition by applying constant voltages at the device ports. As an example, Fig. 4.3 shows the gate current walkout obtained by setting gate and drain voltages such that the initial value of the gate current is (a) - 0.8 mA (- 0.53 mA/mm) and (b) -3.9 mA (-2.6 mA/mm). After 12 hours the device has practically reached its asymptotic condition.

Fig. 4.4 shows an example of dynamic stressing: the peak gate voltage is controlled so that its maximum value is 0 V, thus preventing forward gate conduction, whereas the maximum drain-source voltage is kept below 25 V in order to avoid device breakdown. The frequency is 2 MHz.



a)



b)

Fig. 4.3: Gate current walkout under DC stress. (a) V_g^0 = - 2 V, V_d^0 = 17.5 V; (b) V_g^0 = - 2 V, V_d^0 = 23.5 V. The stress is interrupted every hour and resumed after device characterization.

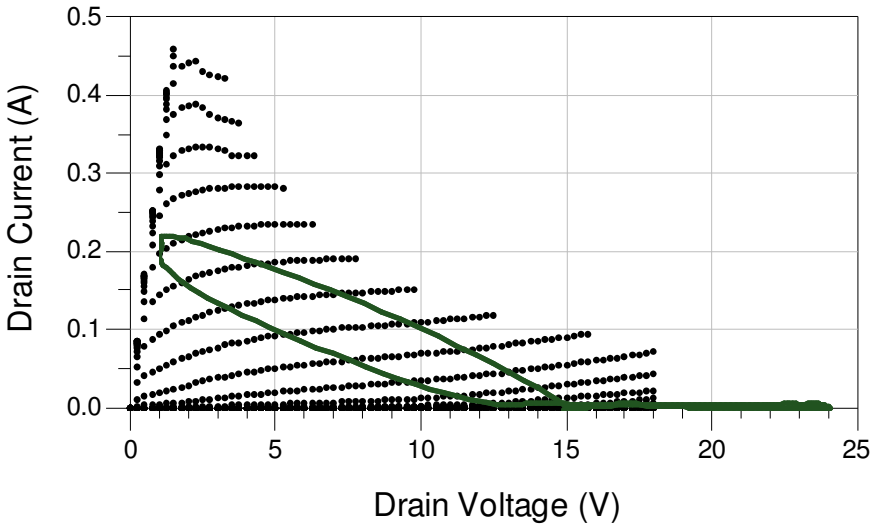


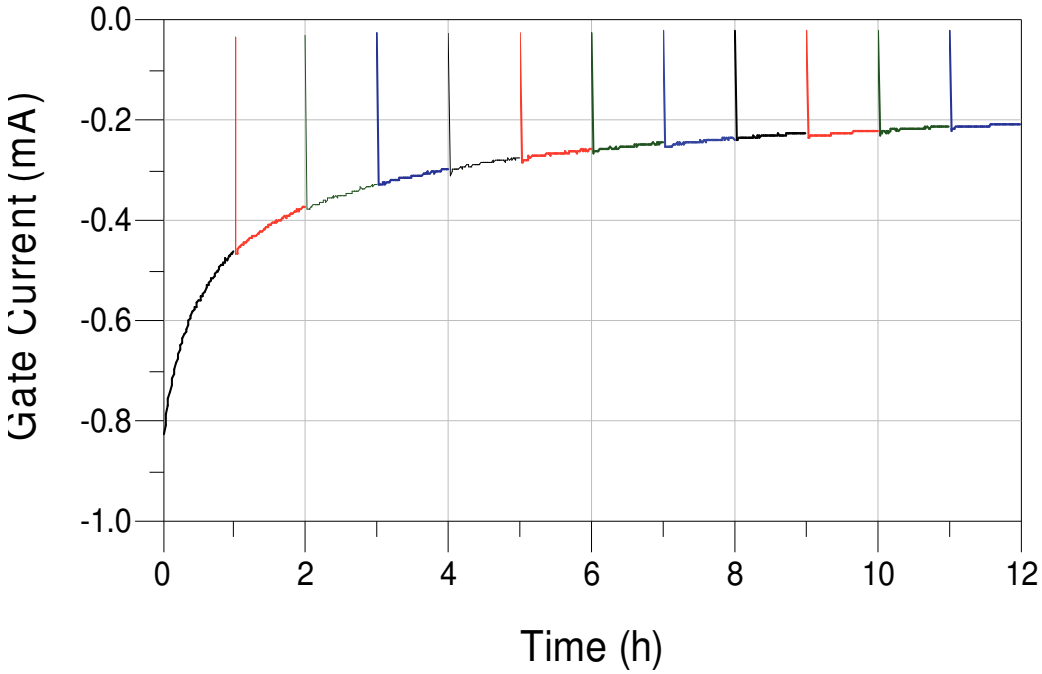
Fig. 4.4: Load line for the 2 MHz dynamic stress condition (V_g^0 = -2 V, V_d^0 = 13.5 V). The load line is superimposed to DC characteristics (-2 V ≤ V_g ≤ 0 V, step 0.1 V).

As clearly shown in Fig. 4.5, during nonlinear dynamic operation both the average and peak values of the gate current are subject to time-drift. In particular, Fig. 4.5b shows the time domain waveforms acquired at the beginning and at the end of the 12-hour dynamic stress. The negative peak in the waveforms corresponds to the transit through the high-field region of the load line shown in Fig. 4.4.

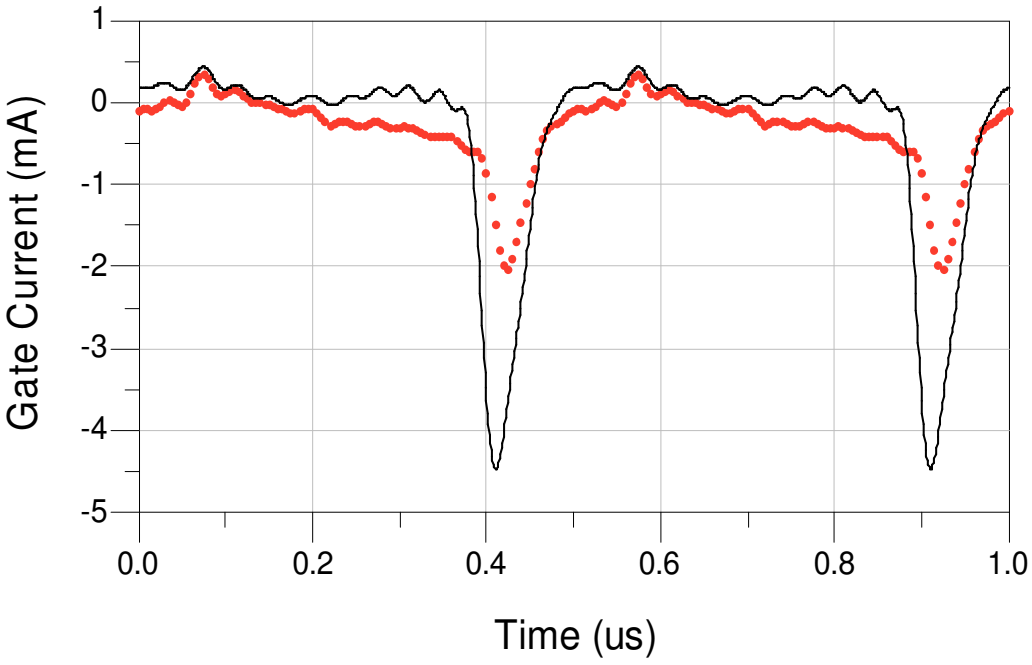
The observation of the different examples given in the previous section prompts some interesting considerations. The dynamic stress has been carried out starting from an initial state that gives I_g^0 = - 0.8 mA (- 0.53 mA/mm) and i_{gr}^p = - 4.45 mA (- 2.97 mA/mm). These two quantities are very similar to the starting values of the gate current for the DC stress experiments shown in Fig. 4.3.

The average gate current I_g^0 appears to tend, under dynamic operation (Fig. 4.5a), to the same asymptotic value of the DC stress (Fig. 4.3a). On the contrary, the static stress of Fig. 4.3b, with a gate current equal to the initial peak value i_{gr}^p of the dynamic experiment, reaches a very different asymptotic value, and one that cannot be correlated with the dynamic stress.

The previous considerations do not only apply to the gate current: in general, dynamically-stressed devices reach the same overall asymptotic condition of DC-stressed ones, provided that the initial value of the gate current of the DC stress is equal to the initial value of I_g^0 under dynamic stress. This clearly identifies the average value of the gate current as the sought-for degradation indicator under dynamic operation.



a)



b)

Fig. 4.5: Gate current walkout under the dynamic stress condition of Fig. 4. (a) Average gate current. (b) Instantaneous gate current waveform for the fresh (solid line) and stressed (dots) device.

In order to prove this statement more conclusively, further measurements have been carried out under static and dynamic operations. Fig. 4.6 shows the static gate current characteristics at constant gate voltage for the fresh device and for the devices after the 12-hour stress experiments described above.

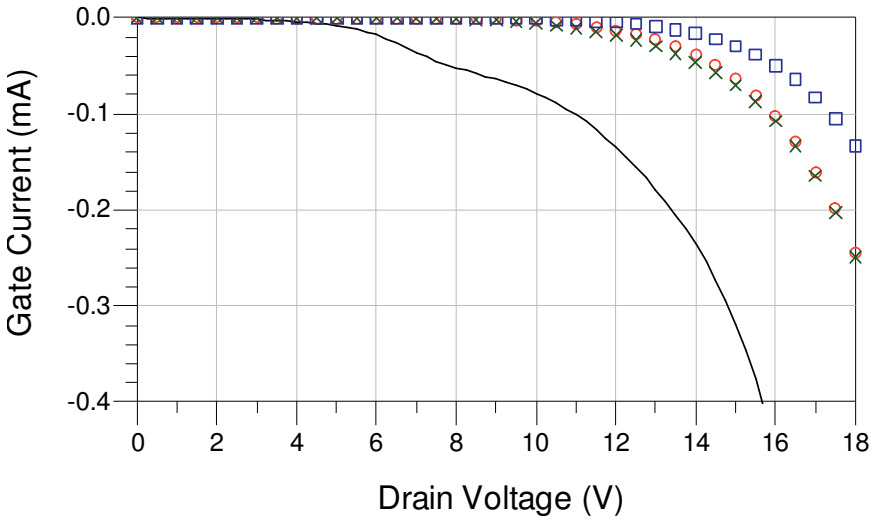


Fig. 4.6: Static gate current characteristics at V_g^0 = - 2 V. The fresh device (solid line) is compared with stressed devices: dynamic (circles) and DC stress (crosses) with initial value of the gate current of - 0.8 mA, and DC stress with initial value of the gate current of - 3.9 mA (squares).

The two devices stressed under dynamic or DC operation with the same gate current initial value (- 0.8 mA) reach exactly the same asymptotic condition, which is clearly different from the one reached by the DC-stressed device with the larger initial value of the gate current (- 3.9 mA).

As visible in Figs. 4.3 and 4.5a, stress cycles were stopped at 1 h intervals to assess device performance degradation. In particular, the devices were driven under class-A operation (V_g^0 = - 0.6 V, V_d^0 = 8 V), and 180° out-of-phase incident signals, of 0.3 V and 2 V amplitude respectively, were applied at the gate and drain ports. Significant output power decrease (Fig. 4.7) was observed only in the device stressed at higher gate current, whereas the other two devices did not show significant output power slump.

As widely documented in the reliability literature (e.g., [9]), power drift, unlike power slump, can be recovered. In order to investigate this aspect, we carried out two subsequent stress experiments, lasting 18 and 84 hours respectively, on a 0.35 µm GaAs PHEMT device with 1.8 mm gate periphery. The PHEMT was left to recover for 12 hours between the two stress cycles. The bias condition (V_g^0 = - 2 V, V_d^0 = 13.5 V) and the amplitude of the signals applied at the device ports were chosen so that: I_g^0 = - 0.9 mA (- 0.5 mA/mm), i_{gr}^p = - 4.5 mA (- 2.5 mA/mm). The results are shown in Fig. 4.8. It clearly appears that during the 12-hour stop the device totally recovers its power performance. Moreover, it should be pointed out that after 18 hours into the second stress, the device approximately reaches the same output power shown at the end of the first 18-hours stress.

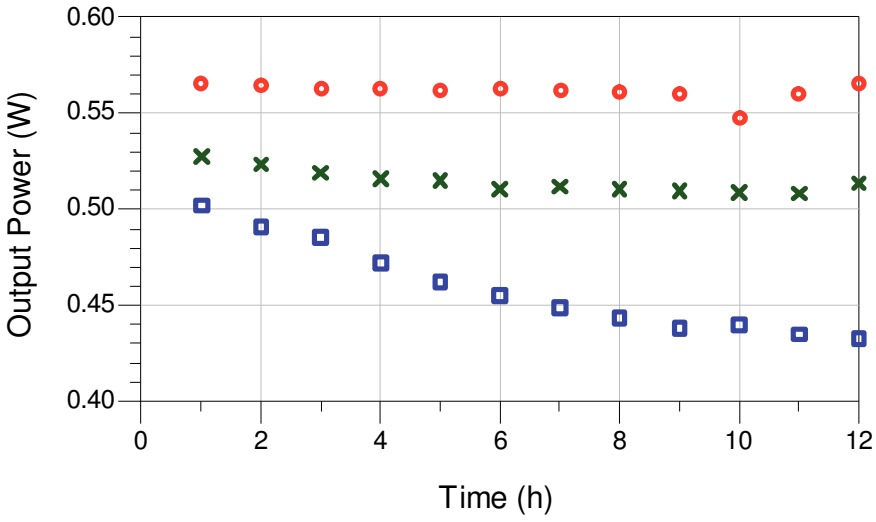


Fig. 4.7: Class-A (V_g^0 = - 0.6 V, V_d^0 = 8 V) output power degradation: dynamic (circles) and DC stress (crosses) with initial value of the gate current of - 0.8 mA, and DC stress with initial value of the gate current of - 3.9 mA (squares).

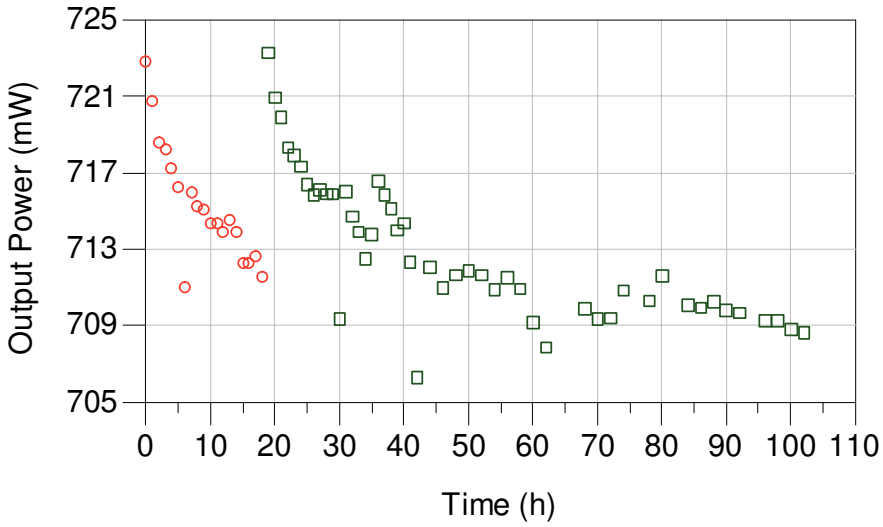


Fig. 4.8: Class-A (V_g^0 = - 0.6 V, V_d^0 = 8 V) output power degradation: the 18-hour stress (circles) and the 84-hour stress (squares) are carried out in sequence under the same initial dynamic condition (I_g^0 = - 0.9 mA, i_{gr}^p = - 4.5 mA).

In order to give an exhaustive insight of degradation phenomena that can be investigated by means of the proposed characterization technique, it is worth noticing that similar stress conditions can give rise to different degradation phenomena when different technologies are investigated. Two subsequent 12-hour stress experiments were carried out on two 0.25 µm GaAs PHEMT devices with 900 µm gate periphery. The first PHEMT was left to recover for 72 hours between the two stress cycles, while the second one was left to recover for 6 hours. The bias condition (V_g^0 = - 1.2 V, V_d^0 = 8 V) and the amplitude of the signals applied at the device ports were chosen in order to

have I_g^0 = - 0.7 mA (-0.8 mA/mm) for the first device, and I_g^0 = - 1.1 mA (-1.2 mA/mm) for the second one. Fig. 4.9 shows the trend of the average values of the gate current under the stressing procedures.

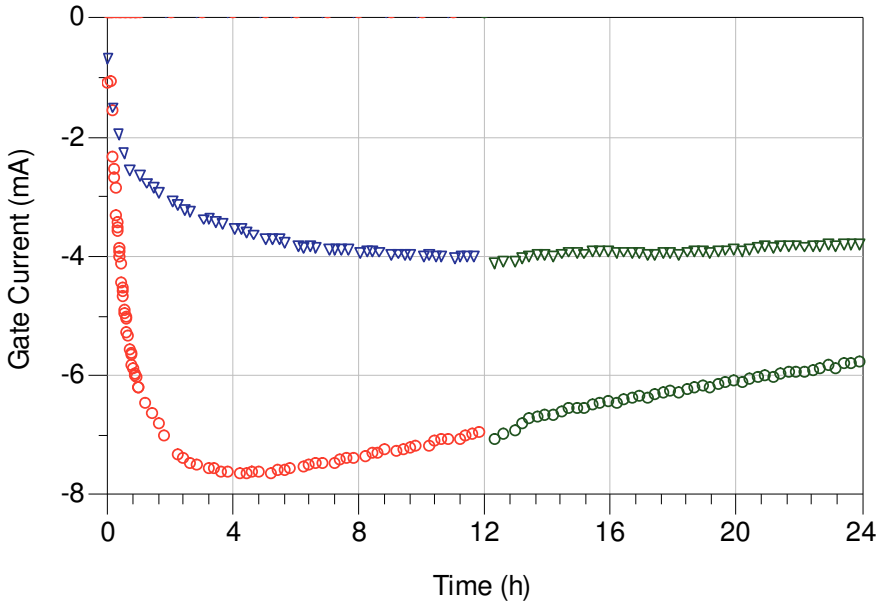


Fig. 4.9: Gate current drift under dynamic stress conditions: (V_g^0 = -1.2 V, V_d^0 = 8 V), I_g^0 = - 0.7 mA (triangles) and I_g^0 = - 1.1 mA (circles).

At a first glance it appears evident that the magnitude of the gate current increases during the stress, that is an opposite behavior with respect to the previous documented stress experiments. It is also evident that no recovery mechanism is present, since, in both cases, the gate current restarts from the same value assumed at the end of the first 12-hour stress. Such a consideration is also confirmed by the monotonic output power collapse observed in Fig. 4.10 under class-A operation.

In particular, also in this case, the stress cycles were stopped at regular intervals to assess device performance degradation. The devices were driven under class-A operation (V_g^0 = - 0.6 V, V_d^0 = 8 V), and 180° out-of-phase incident signals, of 0.3 V and 0.5 V amplitude respectively, were applied at the gate and drain ports. A simple explanation for the observed power slump can be deduced by comparing in Fig. 4.11 the static drain current characteristics at constant gate voltage for the fresh device and for the devices after the 24-hour stresses.

It is evident that, in both cases, an important current collapse [10] occurs which can be related to trap creation induced by the forced stress conditions [11].

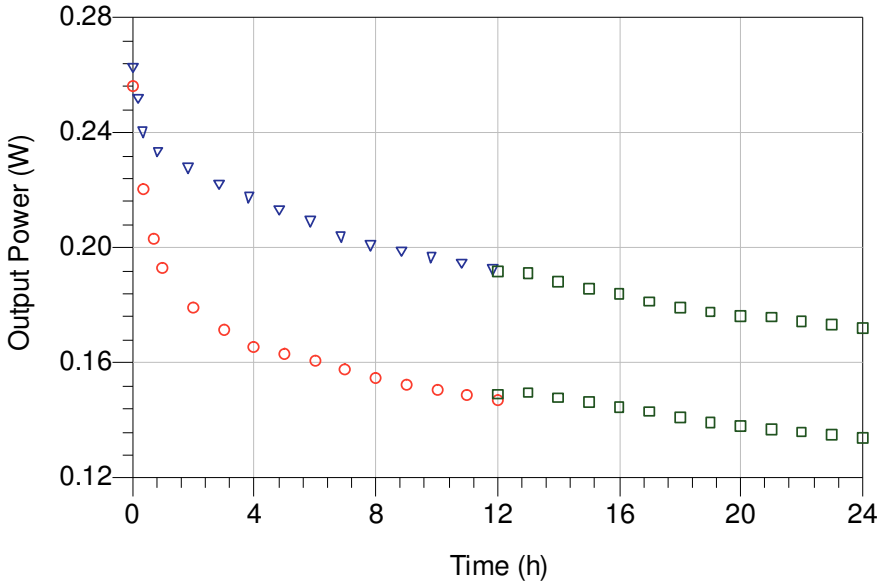


Fig. 4.10: Class-A (V_g^0 = - 0.6 V, V_d^0 = 8 V) output power degradation. Initial values of the gate current of: I_g^0 = - 0.7 mA (triangles) and I_g^0 = - 1.1 mA (circles).

As a matter of fact, also in the present case, the average value of the gate current appears a valuable indicator for quantifying device degradation under dynamic operation, that is: increasing values (in magnitude) of the average gate current unquestionably corresponds to more severe device performance drop.

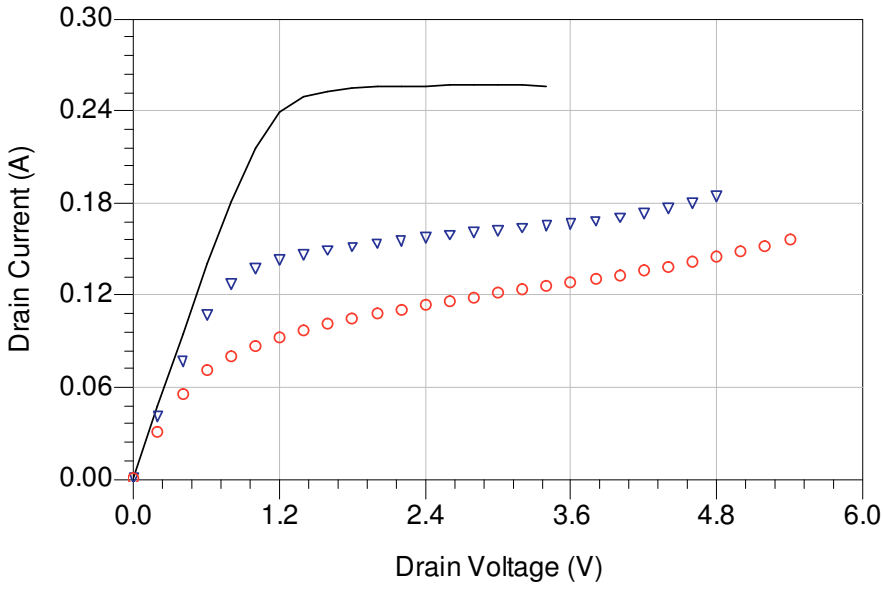
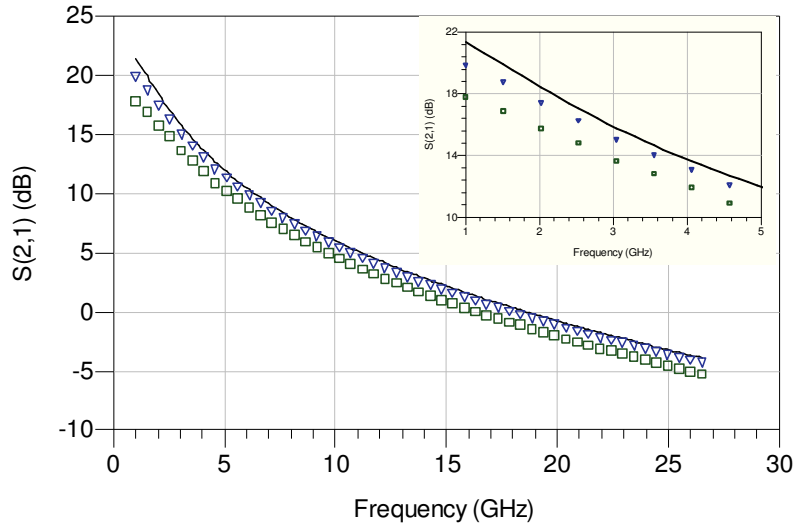
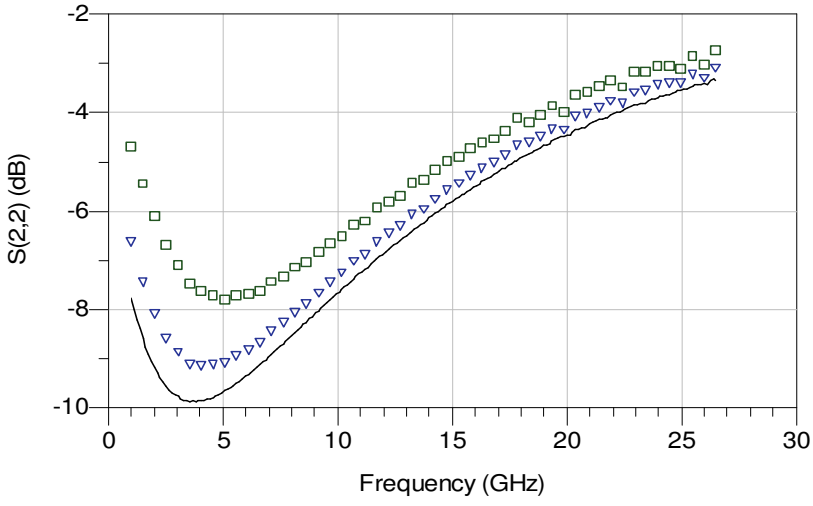


Fig. 4.11 Static drain current characteristics at V_g^0 = 0 V. The fresh device (solid line) is compared with stressed devices with initial values of the gate current of: I_g^0 = - 0.7 mA (triangles) and I_g^0 = - 1.1 mA (circles).

A monotonic degradation of the device performance is also assessable at microwave frequencies by observing the S-parameter time dependence. Fig. 4.12 shows, for the device stressed starting from an initial value of the average gate current I_g^0 = - 1.1 mA, the magnitude of S(2,1) and S(2,2) parameters under class-AB operation (V_g^0 = - 0.9 V, V_d^0 = 8 V). It is worth noticing that the main variations are observable at low frequencies, which clearly indicates that the device degradation is essentially related to low-frequency dispersion (i.e., trapping phenomena),or, in other words, to the device resistive core [12].



a)



b)

Fig. 4.12: Small-signal parameter degradation at microwave frequencies. Class-AB bias condition (V_g^0 = - 0.9 V, V_d^0 = 8 V), initial values of the gate current during the stress procedure I_g^0 = - 1.1 mA. The fresh device (solid line) is compared with stressed device characteristics after 12-hour stress (triangles) and 24-hour stress (squares). a) S(2,1) parameter. b) S(2,2) parameter.

4.3 Empirical study of performance degradation of X-band GaN HEMTs

High-power capability of GaN technology has been largely demonstrated [13] in the lowest range of microwave frequencies (i.e., L-,S-, and C-band). On the other hand, it is very difficult to guarantee similar results at higher frequencies. As an example, in X-band operation, a power density of 4 W/mm appears to be a challenging target, when high reliable MMICs have to be designed (e.g., [14]).

The presence of traps and thermal effects [15-16] undoubtedly affects the maximum performance achievable by a selected technology, nevertheless these phenomena are not peculiar to high-frequency operation. As a matter of fact, when the operating frequency increases, the main limitation derives from short channel effects [17] that, causing high levels of sub-threshold currents (i.e., poor pinch-off [15]), define the maximum drain bias voltage compatible with safe device operation. The device pinch-off behavior can be strongly improved by refining the technological process [17], nevertheless, at the present time, X-band GaN devices are usually limited to 30 V drain bias voltage. It is worth noticing that, differently from other phenomena occurring in GaN devices under high-field operation (e.g., piezoelectric effects [18]), short-channel effects have not been strictly related to device degradation and failure. As a consequence, it is possible to empirically investigate these phenomena, under different operations, without incurring in device permanent modifications.

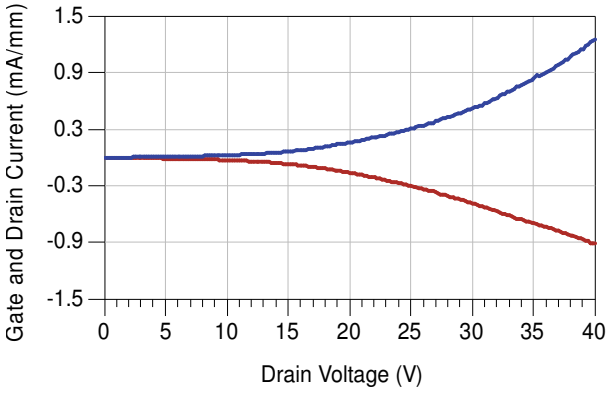
Exploiting the measurement system described in section 4.1, an extensive characterization has been carried out, under both static and dynamic operation, of some phenomena that limit the performance achievable by X-band GaN HEMTs. Transistors provided by three different foundries have been considered in order to assess the generality of the investigated phenomena.

In order to analyze some phenomena which limit the performance achievable by X-band GaN HEMTs, we have analyzed three devices provided by different foundries. In particular, the considered devices have the same channel length (i.e., 0.25 μm), the same finger width (i.e., 100 μm), comparable peripheries (0.8 mm, 1.2 mm, and 1 mm, respectively), and drain bias voltage limited to 30 V. In the following the three technologies will be labeled as “A”, ”B”, and “C”.

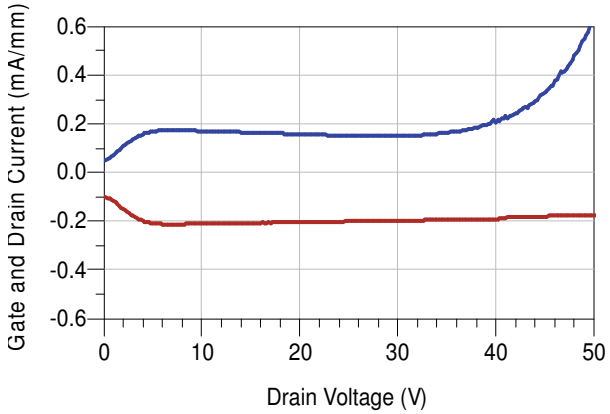
4.3.1 DC characterization

The simplest technique to investigate the maximum operating voltage for a given technology is the static characterization. In Fig. 4.13 the DC measurements carried out on the investigated devices

are shown. In particular, the gate voltage has been set for operation under pinched-off condition, whereas the drain voltage has been swept. It is evident that, under high-voltage operation, all the devices show a more pronounced drain current increment compared to the gate current. This phenomenon has been largely documented in literature (e.g., [19]) and poses a limit to the maximum drain voltage bias since it ultimately leads to a dramatic efficiency slump in power amplification.



a)



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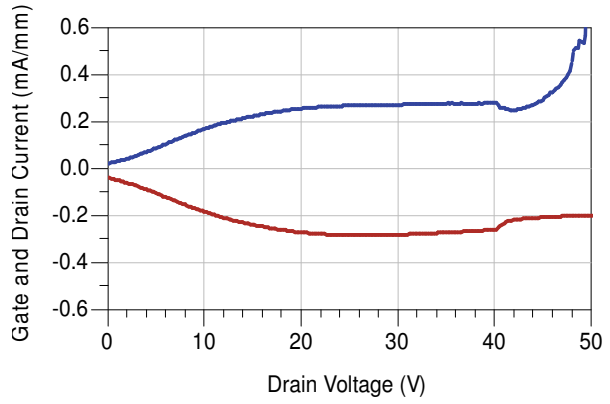


c)

Fig. 4.13: Static gate (negative) and drain (positive) currents measured under pinched-off condition on device "A" (a), "B" (b), and "C" (c). V_d^0-step 0.2 V.

With the aim of quantifying the robustness of the different devices with respect to this phenomenon, the current deviation (CD) between the drain and gate currents can be defined as:

$$CD(V_g, V_d)\Big|_{V_g=V_g^0} = \frac{I_d(V_g, V_d) - \left|I_g(V_g, V_d)\right|}{\left|I_g(V_g, V_d)\right|}\Bigg|_{V_g=V_g^0}, \quad (1)$$

where V_g^0 represents the fixed gate voltage at which DC measurements are carried out. Tab. 1 reports the drain voltage values $V_d^{20\%}$ where the drain current exceeds the gate current of 20 percent (i.e., CD = 0.2). Such a figure of merit would indicate the device "C" as the most suitable for operation under high values of the drain bias voltage, nevertheless it is also useful to analyze the CD derivative. The latter represents a rough evaluation of the evolution of the CD at the higher voltages which are reached under nonlinear dynamic operation. To this purpose the derivative of the CD, evaluated at $V_d^{20\%}$, is also reported in Tab. 1. It is well evident that for such a figure of merit the device "C" represents the worst case as the drain current dramatically increases at $V_d^{20\%}$.

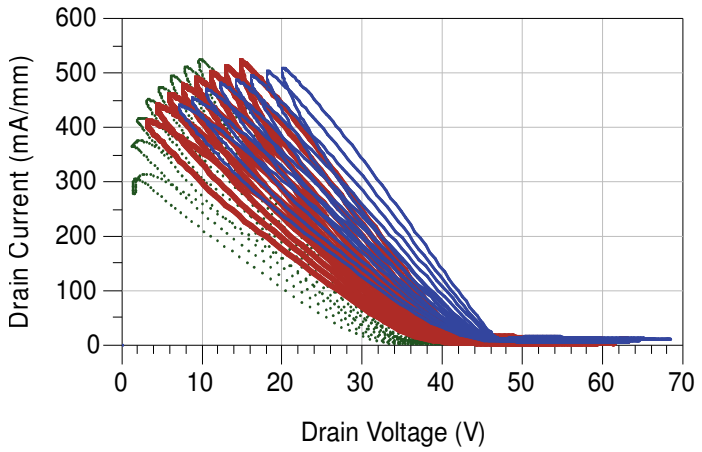
Device	$\mathbf{V_d^{20\%}}$ *[V]*	*d(CD) [%/V]*
A	35	6.9
B	41	7.8
C	43	8.6

Table 1: Figures of merit of device robustness to sub-threshold effects under DC operation

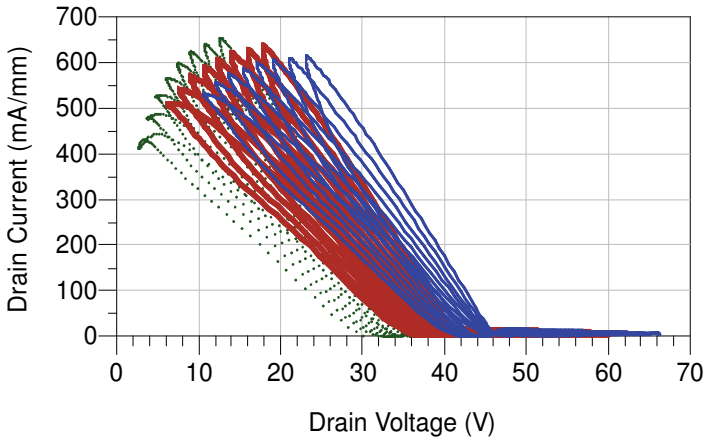
4.3.2 Low-frequency large-signal characterization

With the aim of investigating the impact of sub-threshold effects under nonlinear dynamic operation, the previously mentioned setup can be conveniently adopted as a low-frequency time-domain active load-pull measurement system [20], operating at the fundamental frequency of 2 MHz. In particular, measurements carried out on the selected devices are shown in Fig. 4.14. The gate bias voltage has been fixed at the threshold voltage (V_g^{Th}, class B operation), whereas the drain bias voltage has been swept for assessing the device behavior under very-high field operation. The amplitude of the gate incident voltage has been set in order to dynamically reach the instantaneous gate voltage value of 0 V, whereas the amplitude of the drain incident voltage has been swept for synthesizing different loading conditions. By observing the load line behavior in the low-voltage high-current region, it is evident that all the investigated technologies clearly show a knee walkout

[15-16] that monotonically increases by increasing the drain bias voltage. Such a phenomenon, by limiting the drain voltage excursion, limits the power capability deliverable by a given technology. Nevertheless, moving from the minimum to the maximum drain bias voltage considered, all the devices show an important output power increment (about 20 percent).



a)



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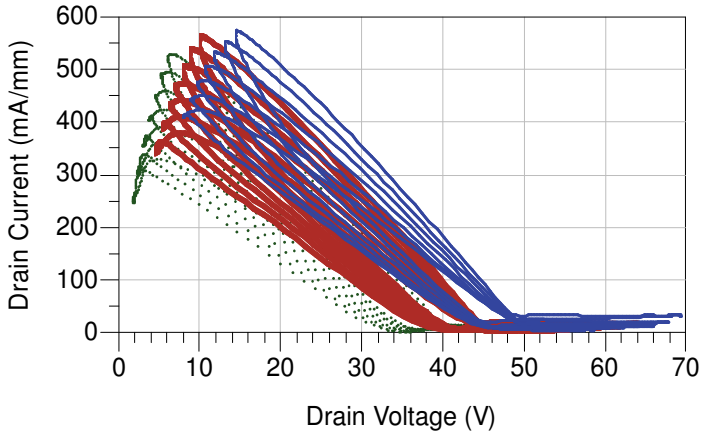


c)

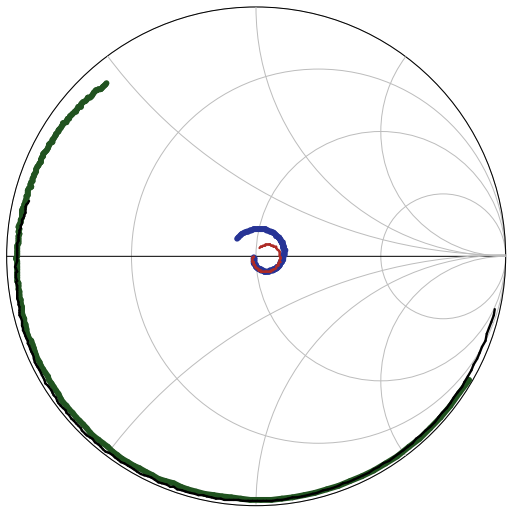
Fig. 4.14: Nonlinear measurements carried out on device "A" a), on device "B" b)and on device "C" c) at 2 MHz. $V_g^0 = V_g^{Th}$, V_d^0 = 30 V (dotted line), 35 V (bold line), and 40 V (thin line)

This clearly demonstrates how the knee walkout does not represent the most critical non-ideality, at least for the drain bias voltages considered. As a matter of fact, the non-ideality which mostly limits the maximum drain bias voltage is represented by the sub-threshold conduction [15-20]. From Fig. 4.14, by observing the load-line behavior in the high-voltage low-current region, it is well evident that the worst case is represented by the device "C". In order to quantify this aspect, the maximum drain current values exhibited by the devices in the sub-threshold region are calculated. For the three devices A, B, and C such a value was found to be 10 mA, 5 mA, and 32 mA, respectively. It is not surprising that the device "B", showing the best compromise for the two figures of merit considered under DC operation (see Table I), exhibits the best behavior under nonlinear operation.

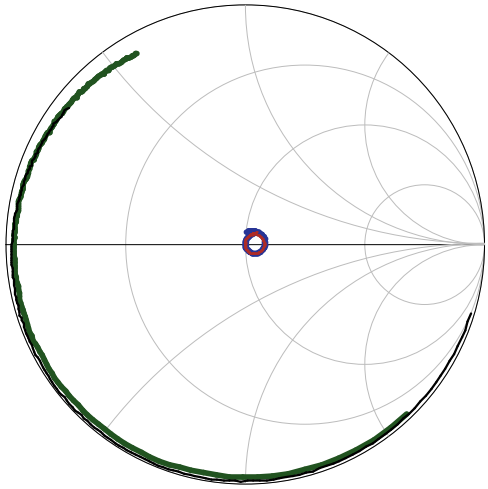
4.3.3 Small-signal characterization

Interesting information can be also deduced by observing the device small-signal behavior under high-frequency operation. In order to put in evidence the impact of sub-threshold effects, the gate bias voltage has been set to the sub-threshold value adopted for the device DC characterization (Fig. 4.13), while the drain voltage has been set at $V_d^{20\%}$. Fig. 4.15 shows S-parameter measurements, carried out under the selected operation.

The discrepancy between S_{12} and S_{21}, which should be identical under sub-threshold, operation, can be adopted as figure of merit. It appears evident that, at microwave frequencies, the device "B" shows the best performance, and differences with device "A" can be clearly appreciated. Also in this context, the device "C" exhibits very poor performance.



a)



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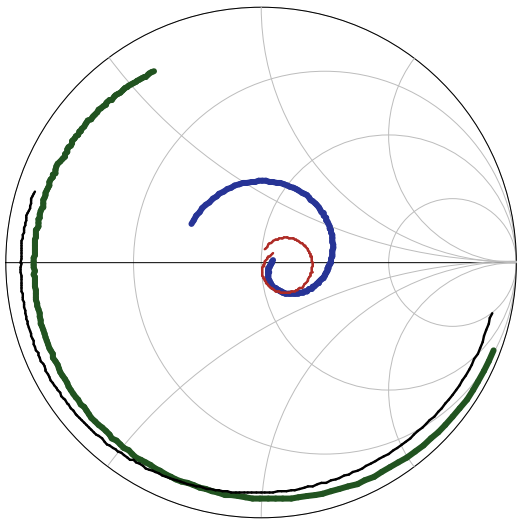

c)

Fig. 4.15: S-parameter measurements under pinched-off condition. S(1,1) (bold line), S(1,2) (thin line), S(2,1) (bold line), S(2,2) (thin line). Device "A" (a), "B" (b), and "C" (c). $V_d^0 = V_d^{20\%}$, 1 GHz ≤ freq ≤ 26.5 GHz, step 127 MHz.

Conclusion

In this chapter, an innovative measurement setup for characterizing electron device degradation has been introduced. Exploiting such setup, a first quantitative link between stress experiments carried out on GaAs HEMTs for PA design under static and dynamic operation has been found, that represents a very promising initial result in view of the possible use of DC stress data to develop degradation nonlinear dynamic models.

Moreover the proposed measurement system has been exploited in order to investigate some phenomena that limit the performance achievable by actual GaN technologies devoted to X-band PA design.

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General conclusion

In this thesis, the results of three years of research activity focused on microwave power amplifier design have been described. Commonly adopted design approaches have been treated, putting in evidence both advantages and limitations in adopting such methodologies; moreover, an innovative design technique has been presented, which overcomes the major limitations of the discussed design methodologies. Such a technique is mainly based on low-frequency nonlinear experimental electron device characterization, carried out by exploiting a new large-signal setup based on low-cost instrumentation, jointly with a suitable model-based or measurement-based description of reactive effects. The proposed approach shows the same level of accuracy provided by high-frequency large-signal measurements.

Particular emphasis has been devoted to high-efficiency microwave power amplifier design and to this end several design examples, representing the state of the art, have been carried out by exploiting the proposed approach.

Finally, an important power amplifier design aspect has been dealt with, related to degradation and performance limitation of microwave electron devices. Several experimental results have been carried out by exploiting a new measurement setup oriented to the characterization of degradation phenomena in microwave electron devices.

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