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CICLO XXVII

COORDINATORE Prof. Trillo Stefano

CHARACTERIZATION AND MODELING OF III-V TRANSISTORS FOR MICROWAVE CIRCUIT DESIGN

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Models: no-one believes them, except the person who made them.

Measurements: everyone believes them, except the person who made them.

Prof. B. Munk

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PREFACE

New mobile communication technologies have given a boost to innovations in electronic for telecommunications and microwave electronics. It's clear that the increasing request for mobile data availability, as proved by the growth of 69% of mobile data traffic in 2014, poses great challenges to industries and researchers in this field.

From this point of view a rapid diffusion of wireless mobile broadband network data standards, like LTE/4G, should be seen, which requests a state-of-the-art transceiver (i.e., transmitter/receiver) electronics. It will be mandatory to use higher frequencies, with wider bandwidth and excellent efficiency, to improve battery duration of mobile phones and reduce the energy consumption of the network infrastructures (i.e. base stations).

Moreover, the microwave electronics is ubiquitous in satellite systems. As an example the GPS-GLONASS systems, developed respectively by United-States and Russian Federation for geo-spatial positioning, now are commonly used as navigation support for planes, ships, trains, automobiles, and even people.

Other interesting applications are the earth-observation satellites, like the Italian system COSMO-SkyMed: a constellation of four satellites developed for the observation of the entire planet. These systems are able to produce a detailed image of the earth surface exploiting a microwave synthetic aperture radar, with the possibility to observe an area even by night or with bad weather conditions. Clearly these features are impossible for traditional optical systems.

Even if a lot of electronic applications are focused on the system architecture, in microwave electronics the single transistor still plays a key role. Indeed, the number of transistors in high-frequency circuits is low and wide areas are occupied by numerous passive elements, required to optimize the system performance. There is a lot of interest in finding the optimum transistor operating condition for the application of interest, because the high-frequency electron-device technologies are relatively young and often still in development, so the transistor performance is generally poor.

As a matter of fact, transistor characterization plays a very important role: various measurement systems, developed for this purpose, have been proposed in literature, with different approaches and application fields.

Moreover, a meticulous characterization of the transistor is the basis for the identification of accurate models. These models, allowing to predict the transistor response under very different operating conditions, represent a fundamental tool for microwave circuit designers.

This thesis will resume three years of research in microwave electronics, where I have collaborated in research activities on transistor characterization and modelling oriented to microwave amplifier design. As various kinds of amplifiers (i.e., low-noise amplifier, power amplifier) have been developed, various characterization techniques have been exploited.

In the first chapter, after a presentation of the most common large-signal characterization systems, a low-frequency large-signal characterization setup, oriented to transistor low-frequency dispersion analysis and power amplifier design, will be described as well as the development of the control algorithm of the measurement system and its application to the design of a Gallium-Nitride class-F power-amplifier, operating at 2.4 GHz with 5.5 W of output power and 81% efficiency. Another application of the proposed setup for fast-trap characterization in III-V devices is then reported. Successively, an extension of the setup to very low frequencies will be presented.

In the second chapter, small-signal characterization techniques will be dealt with, focusing on noise measurement systems and their applications. After a brief introduction on the most relevant small-signal measurement system (i.e., the vector network analyzer), an innovative formulation will be introduced which is useful to analyze the small-signal response of Gallium-Arsenide and Gallium-Nitride transistors at very low frequencies. Successively, the application of neural network to model the low-frequency small signal response of a Gallium-Arsenide HEMT will be investigated.

The third and last chapter will deal with the EM-based characterization of Gallium-Nitride transistor parasitic structures and its usage, combined with small-signal and noise measurements, for developing a transistor model oriented to low-noise amplifiers design. In particular, the design of a three stages low-noise amplifier with more than 20 dB of gain and less than 1.8 dB of noise figure operating in Ku-band will be described.

PREFAZIONE

I nuovi sistemi di comunicazione mobile hanno dato una forte spinta all'innovazione dell'elettronica delle telecomunicazione e delle microonde. Infatti è chiaro che la crescente richiesta di accessibilità alla rete da dispositivi mobili, come provato dall'aumento del 69% del traffico dati da reti mobili nel 2014, impone grandi sfide alle industrie ed ai ricercatori che operano in questo settore.

Da questa prospettiva dovrebbe essere vista la rapida diffusione dei nuovi standard di comunicazione mobile wireless a larga banda, come LTE/4G, che richiedono una circuiteria di trasmissione/ricezione allo stato dell'arte. In particolare sarà sempre richiesto l'utilizzo di frequenze più elevate, con associate larghezze di banda maggiori, e livelli di efficienza molto alti, in modo da prolungare la durata delle batterie nei telefoni cellulari e ridurre i consumi energetici delle infrastrutture di rete (i.e., stazioni radio base).

In aggiunta l'elettronica delle microonde è onnipresente in ambito satellitare. Un esempio sono i sistemi GPS-GLONASS, sviluppati rispettivamente da Stati Uniti e dalla Federazione Russa come sistemi di posizionamento globale, oggi largamente utilizzati come supporto alla navigazione di aerei, navi, treni, automobili e anche persone.

Altre interessanti applicazioni sono i satelliti per l'osservazione terrestre, come il sistema italiano COSMO-SkyMed: una costellazione di quattro satelliti sviluppata per l'osservazione di tutto il pianeta. Questi sistemi sono in grado di riprodurre una immagine dettagliata della superficie terrestre grazie all'utilizzo di radar ad apertura sintetica, con la possibilità di osservare un'area anche di notte o con condizioni meteo sfavorevoli, cosa impossibile con i sistemi ottici tradizionali.

Anche se in molte branche dell'elettronica l'attenzione si è spostata verso l'architettura del sistema, nell'elettronica delle microonde il transistore gioca ancora un ruolo chiave. A conferma di ciò il numero di transistori nei circuiti operanti ad alta frequenza è generalmente ridotto e ampie aree del circuito sono occupate da elementi passivi, richiesti per ottimizzare le performance del sistema. Il grande interesse nel trovare le condizioni di lavoro ottimali di un transistor operante ad alta frequenza è legato al fatto che tali dispositivi sono realizzati con tecnologie nuove e spesso ancora in sviluppo, per cui è necessario sfruttare al meglio le loro ridotte prestazioni.

Per questi motivi è fondamentale caratterizzare in maniera accurata il transistor e sono stati proposti in letteratura vari sistemi di misura sviluppati per questo scopo, con differenti approcci e campi di applicazione.

È chiaro inoltre che la caratterizzazione accurata di un transistor, nelle sue diverse condizioni di funzionamento, è alla base dell'estrazione di modelli che consentano di predirne in modo accurato la risposta. Tali modelli rappresentano uno strumento essenziale per la progettazione a mi-

croonde, permettendo al progettista di avere un perfetto accordo tra le simulazioni CAD ed il circuito, o il sistema, da realizzare.

Questa tesi riassume tre anni di ricerca nell'elettronica delle microonde, dove ho collaborato ad attività di ricerca sul modeling e sulla caratterizzazione di dispositivi elettronici orientati al progetto di amplificatori a microonde. Poiché sono stati realizzati vari tipi di amplificatori (i.e., amplificatori a basso rumore, amplificatori di potenza), si è fatto uso di diversi sistemi di caratterizzazione, che sono stati oggetto del presente lavoro di tesi.

Nel primo capitolo, dopo una breve introduzione sulle tecniche di caratterizzazione a grande segnale, sarà descritto un sistema di caratterizzazione a bassa frequenza e grande segnale, orientato all'analisi della dispersione a bassa frequenza di transistori e al progetto di amplificatori di potenza. A seguire è riportato lo sviluppo dell'algoritmo di controllo del sistema di misura e la sua applicazione al progetto di un amplificatore di potenza in classe F in Nitruro di Gallio, operante a 2.4 GHz con 5.5 W di potenza d'uscita e 81% di efficienza. In seguito è riportata un'altra applicazione del setup: la caratterizzazione dei fenomeni di intrappolamento in dispositivi III-V. Il capitolo termina descrivendo l'estensione del sistema di misura a frequenze più basse.

Il secondo capitolo tratterà delle tecniche di caratterizzazione a piccolo segnale e si concentrerà sulle misure di rumore e sulla misura degli effetti dispersivi in bassa frequenza. Dopo una breve introduzione sul principale sistema di misura a piccolo segnale (i.e., l'analizzatore di reti vettoriale), sarà introdotta una formulazione innovativa utile ad analizzare la risposta a piccolo segnale di transistori in Nitruro di Gallio e Arseniuro di Gallio a bassissima frequenza. Successivamente verrà esaminata la possibilità di utilizzare delle reti neurali per modellare la risposta a bassa frequenza di un HEMT in Arseniuro di Gallio.

Il terzo e ultimo capitolo tratterà della caratterizzazione elettromagnetica delle strutture di accesso di un transistore in Nitruro di Gallio e il suo utilizzo, combinato con misure di rumore, per sviluppare un modello di transistori orientato alla progettazione di amplificatori a basso rumore. In particolare sarà descritto il progetto di un amplificatore a basso rumore a tre stadi con più di 20 dB di guadagno e meno di 1.8 dB di figura di rumore operante in banda Ku.

1 A LOW-FREQUENCY HARMONIC LOAD-PULL SYSTEM

Linear systems are defined as those which satisfy the principles of superposition and scaling. Specifically, given the two inputs $x_1(t)$ and $x_2(t)$ as well as the respective outputs:

$$y_1(t) = F(x_1(t)) \quad , \tag{1.1}$$

$$y_2(t) = F(x_2(t)) \quad , \tag{2}$$

the response to the excitation:

$$\alpha x_1(t) + \beta x_2(t) \quad , \tag{1.3}$$

must be:

$$\alpha y_1(t) + \beta y_2(t) \quad , \tag{1.4}$$

with α and β scalar constants.

In electronics, whenever possible, systems and circuits are considered as linear, because a non-linear circuit is in a large way more complicated to analyze than a linear one, and the design of non-linear systems is even more ambitious.

One of the first circuits which violates the linear assumption is the power amplifier [1]. The push of telecommunications toward more power-efficient design has moved the power-amplifier design from linear class A power amplifiers, to more efficient class A-B and class B power amplifiers. This introduces, as a drawback, a lot of non-linear phenomena, as, for example, harmonic generation and power saturation.

Moreover non-linearities are ubiquitous. Even passive elements, like resistors, capacitors and inductors, are non-linear when large voltages or currents are applied. Thus, linearity in electronic circuit is just an approximation, and a full understanding of electronic circuits requires non-linearity comprehension.

Various high-frequency large-signal measurement systems have been developed to analyze non-linear systems, in particular the transistor, because it is the source of almost all the non-linearities in microwave circuits.

In the first part of this chapter a brief presentation will be proposed of the two most common non-linear characterization setups: the Non-Linear Vector Network Analyzer (NVNA) and the load- and source-pull characterization system.

These systems surely are able to characterize a device in high-frequency non-linear operation but a low-frequency large-signal setup can give a more clear view of the available performance of a transistor, analyze the dispersive phenomena or rigorously investigate the transistor operating condition. This assumption will be discussed in the second part of this chapter, when a low-frequency large-signal setup will be presented

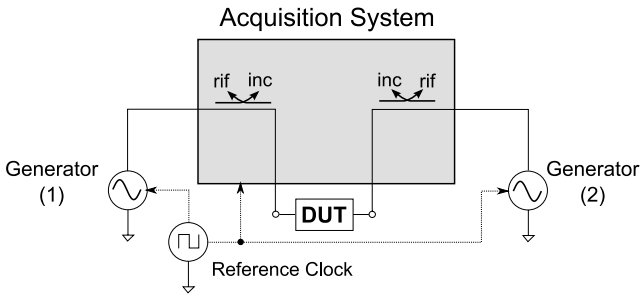

Fig. 1.1 General NVNA setup. DUT input and output ports are excited by two generators. Incident and reflected waves at both ports are acquired by an acquisition system.

with some possible applications, like high-frequency power-amplifier design [2], and fast dispersive effects characterization [3].

In the last part of the chapter, a possible extension to very low frequencies will be reported, useful to analyze the low-frequency dispersive phenomena in their bandwidth of occurrence [4].

1.1 NON LINEAR VECTOR NETWORK ANALYZER

A big issue in non-linear system characterization is the harmonic generation. While the linear system response to an input signal is at the same frequency of the input, generally in non-linear systems a lot of frequency components are generated. This phenomenon is well evident after a brief mathematical analysis.

By considering a sinusoidal input to a non-linear system:

$$x(t) = \cos(\omega_0 t) \quad , \tag{1.5}$$

with the simple non-linear input/output relationship:

$$y(t) = f\big(x(t)\big) = x(t) + x(t)^2 \quad , \tag{1.6}$$

the output can be written as:

$$\begin{aligned} y(t) &= \cos(\omega_0 t) + \cos^2(\omega_0 t) \\ &= \cos(\omega_0 t) + \frac{1}{2} \\ &\quad + \frac{1}{2}\cos(2\omega_0 t) \end{aligned} \quad . \tag{1.7}$$

The output signal has three frequency components, one at the same frequency of the input (i.e., ω_0), one at DC and one at the double of the input frequency (i.e., $2\omega_0$). So the acquisition of all the frequency spectrum is fundamental to carefully characterize the system non-linearities.

In **Fig. 1.1** it is reported a simplified block diagram of a NVNA. The Device Under Test (DUT) input and output ports are excited by two generators, and incident and reflected waves at both the DUT input and output are acquired by an acquisition system. Generators and acquisition system are synchronized by a reference clock, to avoid spectral leakage.

To exhaustively characterize a non-linear device operating at microwave frequencies these requirements are necessary:

A HIGH-FREQUENCY WAVEFORM GENERATOR: generated signals could be sinusoids but also modulated waveforms, in order to evaluate the performance of a device (e.g., an amplifier) in operative-like conditions.

A LARGE BANDWIDTH ACQUISITION SYSTEM, to acquire both the excitation frequency and the harmonics. A 4-channel system is necessary to acquire all the information required to reconstruct the voltages and currents at the DUT ports.

A SYNCHRONIZATION SYSTEM, necessary to the acquisition system and to synchronize the two generators.

A CALIBRATION TECNIQUE, able to de-embed the influence of the acquisition system. Non-linear system calibration is not trivial; for example phase calibration, necessary to correctly reconstruct the relative phases of harmonic components, is very complex. The calibration procedure requires specific instruments, as comb-generators [5].

Clearly the NVNA is a complicated system, and its complete description is not the purpose of this thesis. However, we will report some implementations of the NVNA, in particular the most important part: the acquisition system.

1.1.1 Oscilloscope-based setup

The first developed solution uses a high-speed 4-channel oscilloscope. In this way all the signals are acquired simultaneously in time domain, so harmonic phases in the spectral domain are aligned without extra effort. Oscilloscopes able to acquire high-frequency waveforms can be of two types:

REAL-TIME OSCILLOSCOPES [6], where the samples are acquired directly by the scope at the maximum sampling rate. So the Analog-Digital Converter (ADC) sampling rate must be at least the double of the maximum frequency of the signal, to fulfill Shannon criteria. High-speed ADCs are very expensive and this solution could not be practical or no commercial instrument could be available if the operating frequency is very high. As an example, at the time when this thesis is written, the fastest oscilloscope is the LabMaster 10 Zi by Lecroy, with a maximum sampling rate of 160 Gs/s, and a bandwidth of 65 GHz, for approximatively 200'000 $ [7].

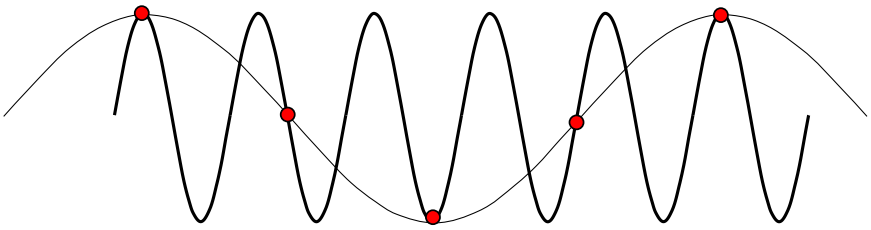

Fig. 1.2 Sinusoidal signal acquired with an equivalent time oscilloscope, samples are marked with red circles.

EQUIVALENT-TIME OSCILLOSCOPES [8], where the samples are acquired each one in a separate period of the signal, as reported in **Fig. 1.2**. Using this technique the sample-rate could be hundreds of time lower than the signal frequency, still maintaining an accurate acquisition of waveform shape. It's clear that the reduction of the ADC speed decreases the complexity and cost of the system but a very accurate control of the trigger point (i.e., the time instant when the sample is acquired) is fundamental. Indeed a small uncertainty of the trigger point, i.e., the timing jitter, can introduce great variations on the acquired sample value, in particular when the signal derivative is higher, thus limiting the system bandwidth.

The calibration of an oscilloscope-based setup is a bit tricky. In addition to the uncertainty associated to the bandwidth limitation of the acquisition path, the time grid of the acquired samples is affected by non-linear distortion thus a complex timebase correction is needed [9].

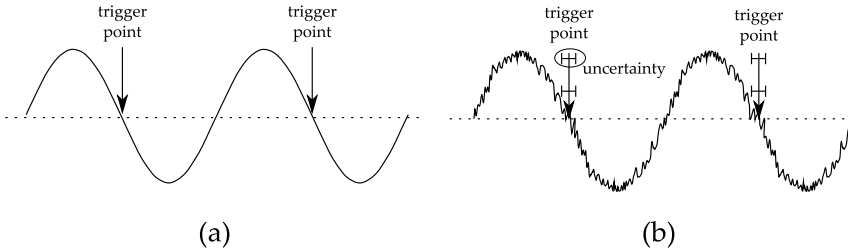

Fig. 1.3 Ideal trigger-point time definition (a) and its uncertainty in case of noisy signals (b).

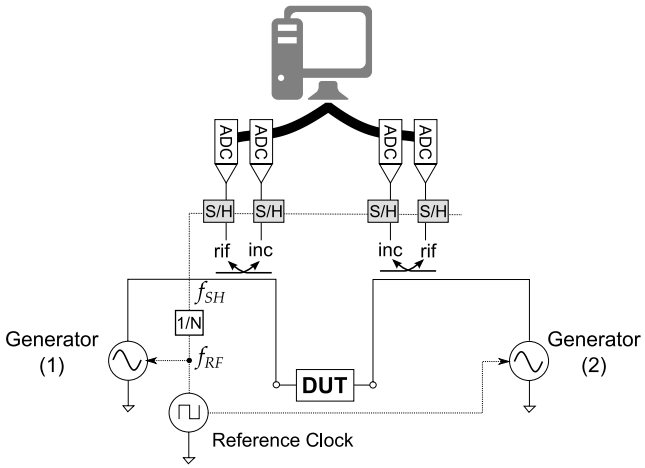

Fig. 1.4 NVNA with a sampler-based receiver system. Incident and reflected waves are sampled with sampling instants based on a reference signal, then are acquired by ADCs and sent to a computer.

1.1.2 Sampler-based setup.

The sampler-based NVNA follows the approach of the equivalent-time oscilloscopes, trying to solve the main problems of it: the trigger timing jitter.

The trigger-point time definition relies on the comparison between two signals, the trigger voltage value and a reference signal, so high uncertainty can be found if noise afflicts these signals. In **Fig. 1.3,** where the ideal case (**Fig. 1.3a)** is compared to a real case (**Fig. 1.3b),** it is evident the trigger-point time uncertainty. Moreover, this problem cannot be prevented because it is not possible to average the noise present in the trigger circuit.

A solution can be a fractional N synthesizer: a device that exploiting the Phase Locked Loop (PLL) technique is able to generate a signal whose frequency is a fraction of the reference signal frequency. Moreover, unlike standard PLLs, the output signal frequency can be selected with very fine granularity.

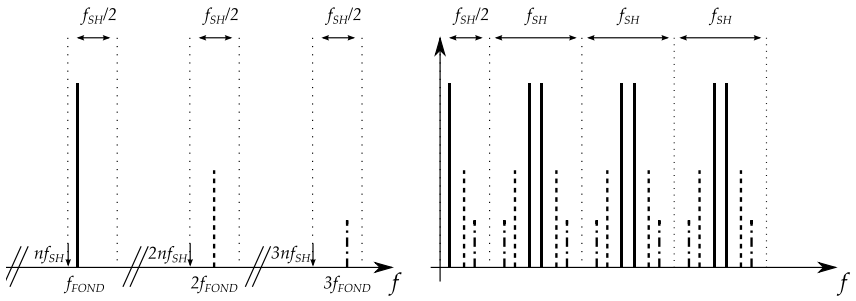

Fig. 1.5 Spectral components at the input (right) and at the output (left) of the sampler. The multitone excitation signal frequency components are folded down to the Nyquist frequency band and, if the sampler reference frequency is selected accurately, the high-frequency signal can be reconstructed.

The system is the one reported in **Fig. 1.4**, four samplers (S/H in the figure) synchronized by the output signal of the fractional N synthesizer (1/N in the figure) take samples of the incident and reflected waveforms, then the samples are converted by the ADCs and acquired (by a PC in the figure).

The spectral components of the output signals of the sampler are the same of the high-frequency signals but folded down in the Nyquist band (i.e., the band between 0 Hz and $f_{SH}/2$) as reported in **Fig. 1.5**, so the ADC could work at the low frequency f_{SH}, decreasing cost and increasing accuracy.

The high-frequency signals can be reconstructed only if the various spectral lines do not overlap when they are folded down to the Nyquist band. Moreover the reconstruction of the high-frequency signals can be very tricky for wideband modulated excitation signals, because the determination of the origin of all the spectral lines in the sampled signal can be challenging [10].

1.1.3 Mixer-Based setup

In all the two approaches presented the acquisition is in time domain. The main advantage is that all the signal spectral components are acquired at the same time. In a mixer based setup instead the acquisition is done in frequency domain, one frequency components at time [11], [12]. This introduces a phase uncertainty: it is not possible to know the phase difference between the harmonic components, as they are not acquired at the same time.

To overcome this problem a synchronizer is needed. This device creates a train of pulse of its excitation signal. This train of pulse is than acquired and used as a reference signal.

The Fourier transformation of a pulse train is:

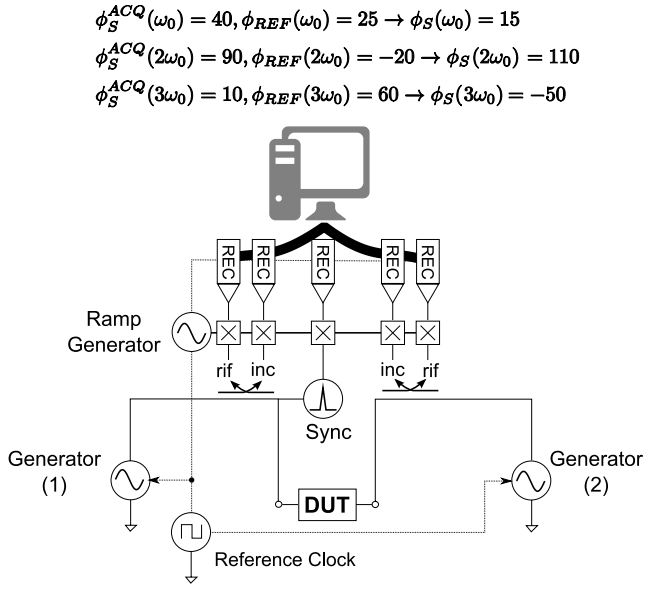

Fig. 1.6 NVNA with a mixer-based receiver system. Incident and reflected waves are mixed with a signal coming from a ramp generator to select one single frequency component. Then it is acquired one frequency at time. Also the signal coming from a sync generator is acquired to reconstruct the phase of the incident and reflected waves, as reported on the top of the figure. With REF it is marked the sync signal, with S the acquired signal before (ACQ) and after phase compensation.

$$\sum_{n=0}^{n=\infty} \delta(t - nT) \xrightarrow{\mathcal{F}} \sum_{n=0}^{n=\infty} e^{j2\pi f nT} \quad , \tag{1.8}$$

so all the harmonic components generated by the synchronizer have the same phase and can be exploited as phase-reference to determine the absolute phase of the acquired waveforms.

The setup of the mixer based NVNA is the ones reported in **Fig. 1.6**, where also the reconstruction of the absolute phase of the spectral components is highlighted.

1.2 LOAD- AND SOURCE-PULL

Source- and load-pull characterization systems are addressed to:

- Setting the source and load terminations of the DUT.
- Measuring the performance of the DUT.

The aim of these systems is to find the input and output terminations (Γ_S and Γ_L) of the DUT that fulfill the performance required. This could be a difficult task because in non-linear devices, unlike in linear ones, it is difficult to predict the optimal operating point on the basis of device models. A solution could be to experimentally find the optimal condition by using load- and source-pull characterization setups.

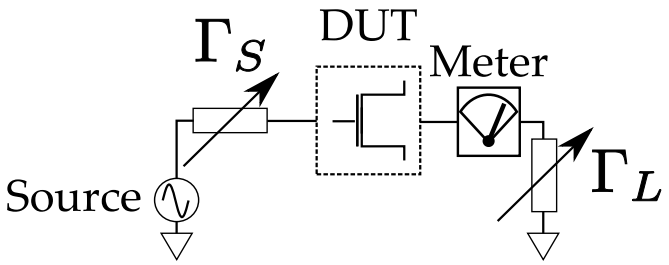

Fig. 1.7 Basic diagram of a load- and source-pull characterization setup. Source and load terminations are controlled while monitoring the performance of the DUT in non-linear operation.

The firsts source- and load-pull systems were developed in the '70 [13], [14], and the modern evolutions of these systems are useful to characterize microwave devices in large-signal operation.

In particular a source- and load-pull can be exploited to:

DEVICE EVALUATION: the performance of the device is measured for few input and output conditions, to evaluate the quality of the production

MATCHING NETWORK DESIGN: various source and load terminations are presented to a device (typically a transistor for the design of an amplifier or an oscillator) operating in non-linear condition to find the source and load impedances that maximize the performance of interest. The input and output matching networks have to be designed in such a way to synthetize the optimal source and load impedances measured.

LARGE-SIGNAL DEVICE MODELLING: load- and source-pull measurements can be used to extract a device model, directly or using additional types of measurements.

DEVICE RELIABILITY: the failure process can be studied as a function of the variation of the Voltage Standing Wave Ratio (VSWR), to identify the failure conditions.

TECHNOLOGY PROCESS DEVELOPMENT: the effects of a variation of a process parameter (e.g., doping level) or device geometry (e.g., field-plate width) can be investigated by using source and load-pull measurements.

The simplest implementation of a source- and load-pull system is reported in **Fig. 1.7**, where an active device is driven by a microwave source and its performance is monitored while its input (source-pull) or its output (load-pull) impedances at the excitation frequency are changed. The data of interest are typically:

- Input and output power (P_{IN} and P_{OUT});

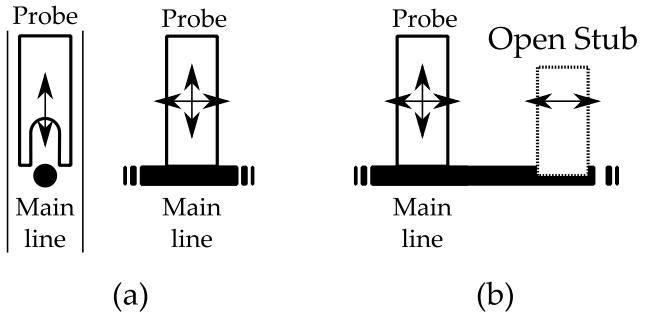

Fig. 1.8 Passive tuner: a conductive probe position is controlled in two directions within a slab line (a). In (b) an open-stub resonator is inserted for harmonic control.

- DC Power (P_{DC});
- Power Gain ($G = P_{OUT}/P_{IN}$) and its compression (i.e., the difference between the small-signal gain and the gain at the given input power);
- Power Added Efficiency ($PAE = {(P_{OUT} - P_{IN})}/{P_{DC}}$) or drain efficiency ($\eta = P_{OUT}/P_{DC}$).

The main difference between the various load- and source-pull setups is the way the input and output DUT termination is controlled. There are three kinds of solution:

PASSIVE TUNERS: where the reflection coefficient is modified using a passive mechanically tunable device.

ACTIVE TECHNIQUES that synthesize the load electronically with a suitable signal injected into the device output port.

HYBRID TECQNIQUES: combinations of the two techniques above.

Moreover, the load- and source-pull systems can control the terminations not only at the fundamental frequency of the excitation signal, but also at the higher-order harmonics. In this case the system is called harmonic load- or source-pull.

In the following, we will discuss in more detail the different implementations of the load-pull techniques; the discussion can be extended also to source-pull systems because the control of the source reflection coefficient is similar to the control of the load reflection one.

1.2.1 Passive Tuners

A passive-tuner basic implementation is reported in **Fig. 1.8a**. It is based on two ground planes with a main line at the center. A conductive probe is inserted at a controllable distance from the main line and at a controllable longitudinal point of the main line. The conductive probe creates

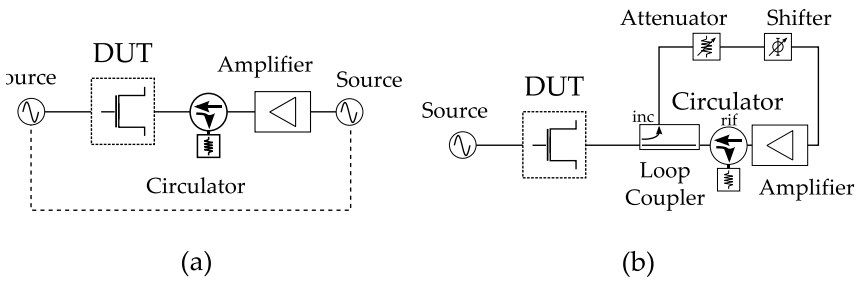

Fig. 1.9 Active load pull setup. In (a) an open-loop setup is presented, in (b) is reported an active-loop load-pull setup.

a discontinuity in the line typical impedance and by controlling the magnitude of this discontinuity (the distance between the main line and the probe) and where this discontinuity is inserted (the longitudinal position of the probe) it is possible to manipulate the reflection coefficient of the tuner.

The position of the probe is often controlled automatically by step motors, allowing a fine tune of the position and a great repeatability [15].

The main problem of a passive tuner is related to its losses; even if ideally this solution is able to reproduce every refection coefficient, the presence of intrinsic losses reduces the maximum magnitude of the reflection coefficient synthesizable. This is a strong limitation because in this way the impedances near to the edge of the Smith chart are not synthesizable.

1.2.2 Active techniques

To reach a higher module of the reflection coefficient, active load-pull systems were introduced. These systems inject a signal at the output of the DUT, and, by controlling accurately its phase and amplitude, a load termination can be synthesize. There are two approaches:

OPEN LOOP TECHNIQUES, where part of the excitation signal is taken from the input, amplified and, with a controlled phase, injected at the output of the DUT as the output incident wave [16]. A block diagram of the system is reported in **Fig. 1.9a**. This kind of solution has some drawback, the load reflection coefficient depends on the ratio between reflected and incident waves, and even if the incident wave is controlled, the reflected wave is a non-predictable function of the excitation signal and the incident wave itself; thus a complex computer control is mandatory to impose the output termination at a desired value. Moreover, it is possible a failure which can damage the DUT, because also negative reflection coefficients can be synthesized.

ACTIVE-LOOP TECNIQUES: as seen in **Fig. 1.9b** a portion of the reflected wave at the output of the DUT is taken by a coupler, controlled in

amplitude and phase, and sent back to the DUT as an incident wave. If all the components are matched to the same reference impedance, the reflection ratio can be controlled by varying the amplification and the phase-shift of the loop. The advantage of these techniques is that the control is simpler than in the open-loop case, because the ratio between incident and reflected waves is controlled directly, avoiding errors and potential failures. So this control is more straightforward and safer, but has some drawback yet, as the potential instability of the loop.

1.2.3 Hybrid Techniques

It is possible to merge the active and passive load-pull techniques, as reported in [17], [18] and [19].

The idea is to help the active load-pull system by inserting a passive tuner, and by using the additional signal only to compensate the losses and increase the maximum reflection coefficient achievable by the system.

1.2.4 Harmonic Load-Pull

It could be of interest to characterize the DUT not only by varying the output impedance at the excitation frequency, but also at its harmonics. This could be necessary for two reasons:

- It is of interest to find an optimal load condition also at the second and the third harmonic. This is the case of a class-F amplifier design, where the output terminations at the second and third harmonics are ideally a short and an open circuit [2].
- For device working under high gain compression or with high VSWR, the output signal could be distorted and have a lot of frequency components. It is necessary to control the terminations at these frequency components, because they strongly affect the performance of the device [20]

Several solutions have been proposed: as an example it is possible to insert more passive tuners, each working at a different frequency, in series or in parallel using a triplexer [17]. The main draw-back of this solution is the high-losses, due to the series of the tuners or the insertion loss of the triplexer, reducing the maximum reflection coefficient synthesizable.

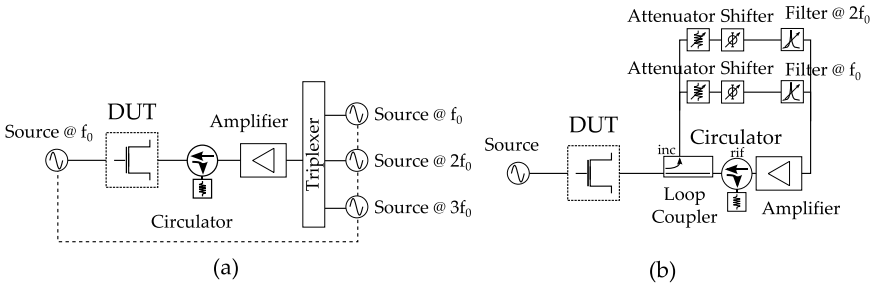

Fig. 1.10 Active harmonic load-pull systems. In (a) it is reported a closed-loop load-pull with the capability to control the load terminations up to the third harmonic. In (b) instead it is presented an active-loop load-pull with a loop for the fundamental load control and a loop for the second harmonic load control.

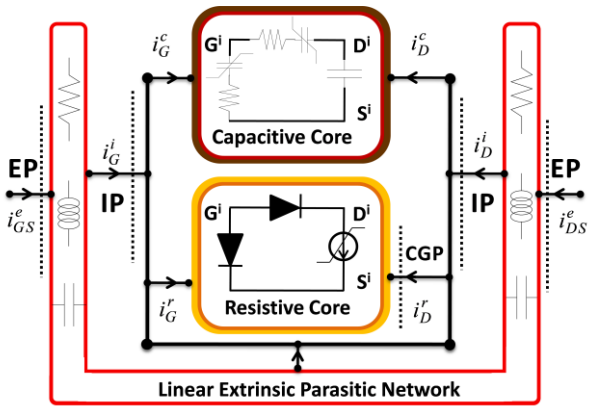

Fig. 1.11 Field Effect Transistor (FET) generic model topology. The linear extrinsic parasitic network, representing the access structures, connects the Extrinsic Plane (EP) of the device with the Intrinsic Plane (IP). The Capacitive Core, representing non-linear dynamic phenomena and the Resistive Core, taking into account the device DC and low-frequency I/V characteristic, are connected in parallel. The most common amplifier-design techniques are defined at the Current Generator Plane (CGP).

Commercial solutions exploit tuners with more than one probe, where all the possible probe positions have to be characterized, or tuners with open-stub quarter-wavelength resonators at the second or third harmonics **(Fig. 1.8b)**. This technique is simpler than the previous one but it allows to set only high-reflective loads.

In open-loop active-systems the harmonic-termination control can be achieved by injecting signals with components also at harmonics, like the setup in **Fig. 1.10a** [21], or in active loop it is possible to add loops for higher frequency components, **Fig. 1.10b**.

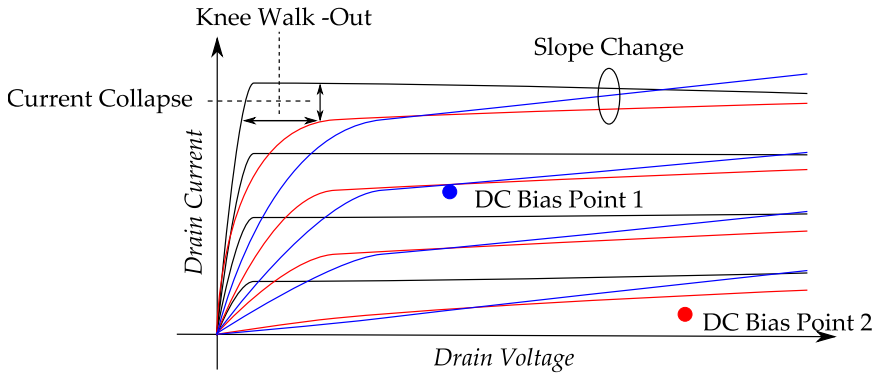

Fig. 1.12 Output I/V characteristic with dispersive phenomena. DC output characteristic (black lines), greatly differs from output characteristics measured dynamically (colored lines) from the marked bias point (e.g., exploiting a pulsed I/V measurement setup). It is evident how the dynamic I/V characteristic is a function of the of the bias-point. Most important dispersion effects are marked in the figure.

1.3 A LOW-FREQUENCY LARGE-SIGNAL CHARACTERIZATION SETUP

Surely the characterization setups previously presented allow to know the device response under actual operating condition at the design frequency, as a function of source and load impedances, but the most diffused design techniques for power amplifiers (e.g., [22], [23], and [24]) are not referred to the device Extrinsic Plane (EP), where the measurements are carried out, but to the Current Generator Plane (CGP).

In **Fig. 1.11** it is reported a general non-linear model of an electron device. It is clear that it is not trivial to achieve the current generator response from the measurements taken at the EP, because even if linear parasitic structures can be de-embedded with minor efforts, the non-linear capacitive-core contribution is very hard to eliminate. This approach has been successfully followed in [25] , [26] but it is useful only to perform a "reverse engineering" of the device operating regime, that is to check which condition at the transistor CGP is set by the terminations at the EP.

A power-amplifier designer needs to do the opposite, to set the operative condition at the CGP of the transistor and found which termination at the EP of the device allows this operative condition. The design could be carried out by using CAD models, but only if they allow the access to the CGP currents and voltages. However, a number of drawbacks must be considered, model inaccuracies first of all. Anyway, models must be extracted, and the transistor current generator has to be characterized.

Unfortunately it is not possible to exploit the DC characteristics of the transistor of interest, indeed the measured DC current generator response

is different than the one at RF. This is essentially due to the presence of dispersive phenomena.

These phenomena, known as low-frequency dispersion, strongly affect the electron device current generator response, as seen in **Fig. 1.12**. These effects are mainly due to defects in the device (e.g., impurities, vacancies) and self-heating effects [27], so innovative technologies are more afflicted by this, because the construction process of the transistor are not fully optimized and a lot of defects could be present in the device structures. This is the case of Gallium-Arsenide (GaAs) and Gallium-Nitride (GaN) heterojunction electron devices. These field effect transistors can manage higher power densities at higher frequencies than silicon electron devices [28], because the device structure is designed to create the channel in a non-doped region, where electron mobility is very high [29], so they are of common use in microwave electronics.

The solution is to perform the characterization at a frequency where the reactive effects of the device access structures are still negligible, but higher than the cut-off frequency of the low-frequency dispersion effects. As demonstrated in literature, a measurement frequency of few megahertz generally fulfils these requirements [30].

Settled the working frequency, the design of the characterization system can be discussed:

BASIC STRUCTURE: an NVNA-like structure has been used, because it grants great flexibility and the access at all the variables of interest.

ACQUISITION SYSTEM: as the working frequency is low there is no need of down-conversion. A commercial medium-performance ADC is able to accurate digitize the signal directly at the excitation frequency, so a 4 channel real-time oscilloscope is exploited to acquire the reflected and incident waves at the input and output port of the DUT.

LOAD TERMINATION CONTROL: the load can be controlled both with passive and active techniques. Conventional tuners are not usable at these frequencies, because the length of the internal transmission line would be tens of meters, so a simple resistor, or a controlled switched resistor matrix, could be connected to the output of the DUT. This solution is very simple and also allows to characterize high-power transistors (above tens of watt) with a low-cost setup [31] but it is not possible to have a fine control of the load termination. Moreover, the resulting system has not the capability to impose the harmonic terminations.

To overcome these problems an active load-control technique can be applied. To reduce the components needed, an open loop technique has been applied, with some differences: the triplexer is unnecessary, because at low-frequency an arbitrary function generator is not expensive and can impose at its output a signal with all the harmonic components needed; also the circulator is not present be-

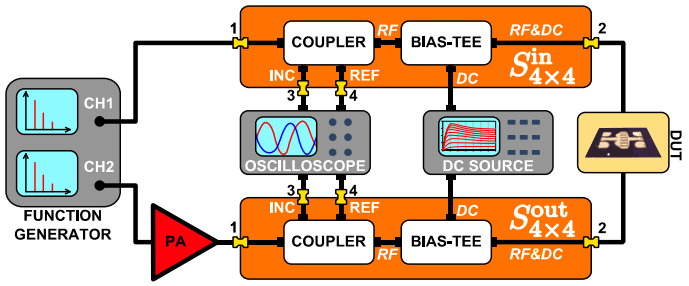

Fig. 1.13 Large-Signal low-Frequency harmonic load-pull setup. The basic structure is similar to an oscilloscope-based NVNA with a 2-channels function generator as a source. All the instruments are controlled by a software running on a PC.

cause it is not practical at low frequency (for the same reason of the tuner). So the amplifier must have the capability to work with very high VSWR (i.e., its output termination is always negative).

CALIBRATION: it has been found that at such a low frequency a simple characterization procedure can take the place of a rigorous calibration, moreover the oscilloscope acquisition channels can be treated as ideal [30]. This is a great advantage: complex non-linear calibrations are not needed, thus the measurements can be carried out with good accuracy with only the compensation of the passive structures, whose effects are simply measurable (e.g., by a Vector Network Analyzer (VNA)).

The system previously described is represented in **Fig. 1.13**. In particular, a dual-channels arbitrary-function source can independently provide arbitrary waveforms in the frequency range [1 mHz–120 MHz]. A 30-W power amplifier (PA) is cascaded to the device output port excitation; this PA can operate with strongly mismatched loads and was selected in order to allow the characterization of device up to some watt of output power (even if the maximum output power is 30 W the mismatch reduces the effective power transfer). Two wideband (10 kHz–400 MHz) dual directional couplers monitor the DUT incident and reflected waves, which are acquired by means of a four-channel digital oscilloscope (4 GSa/s). A high-resolution (4 uV; 20 fA) and accurate (V: 0.05%, I: 0.2%) DC source provides the bias for the device-under-test (DUT). To ensure DC and RF path isolation, two wideband (200 kHz–12 GHz) bias-tees are used in the selected frequency range. In **Fig. 1.13** the two 4-port passive networks that must be characterized in order to get the all the needed information at the device plane are marked with the labels S_{4x4}^{OUT} and S_{4x4}^{IN}.

In the following part of this section the control algorithm of the setup is presented. Successively, an application of this setup for power amplifier design is proposed, then the setup is exploited for fast-trap characterization on transistor of various technologies.

$$\Gamma = \frac{a_2}{b_2} = \frac{a_2}{f_?(\ldots, a_2)}$$

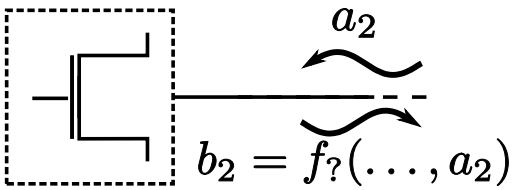

Fig. 1.14 Incident and reflected waves at the DUT output.

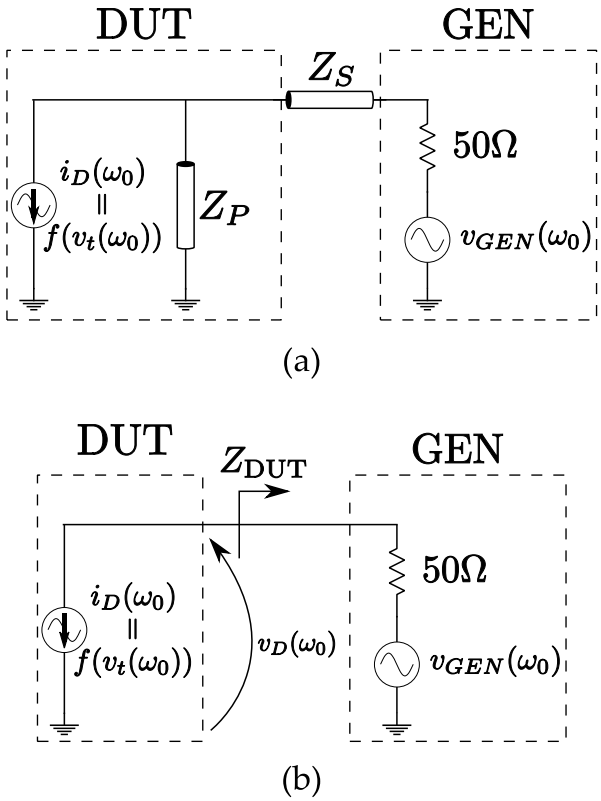

Fig. 1.15 Model of the output section of the setup (a) and its approximation (b) used for the algorithm formulation.

1.3.1 Multi-harmonic load-termination control algorithm.

As said before the load-termination control is carried out with an open-loop technique. This approach requires fewer components (i.e., no variable attenuator, phase-shifter, loop coupler) than the active loop solution, but the control algorithm is more critical. This is because, as represented in **Fig. 1.14**, the system has the ability to control only the incident wave at the output of the DUT and not the reflected wave. Due to this problem it's not possible to know "a priori" which is the incident wave to apply at the out-

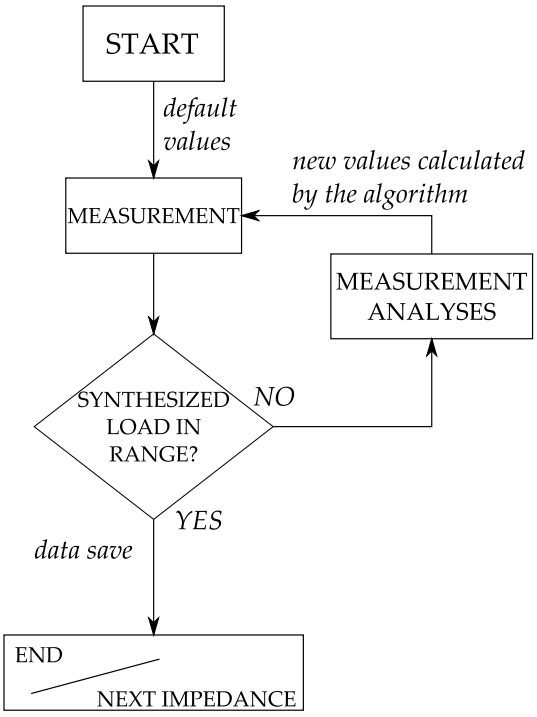

Fig. 1.16 Algorithm that exploiting one of the formulation described synthesizes an output load at a desired frequency. "Values" stand for the amplitude and phase to apply at the signal-generator outputs.

put in order to synthesize the desired impedance. As a consequence, the solution must be found with an iterative algorithm.

Several solutions have been explored and two algorithms have been implemented.

A model of the output section of a transistor connected to the characterization setup is reported in **Fig. 1.15a**. In a first-order approximation the impedance Z_P is negligible, because in most of the operative conditions it is largely bigger than the synthesized impedance. Also Z_S, representing the cable series-impedance can be neglected, as widely lower than the generator input impedance (i.e., the reference impedance 50 Ω). These assumptions simplify the output section of the device, as seen in **Fig. 1.15b**, and lead to the first algorithm which is based on the following formulation:

$$\begin{aligned} & Z_{DUT}(\omega_0) = \frac{v_D(\omega_0)}{i_D(\omega_0)} = \frac{v_{GEN}(\omega_0)}{i_D(\omega_0)} + 50\ \Omega \rightarrow \\ & \rightarrow v_{GEN}(\omega_0) = (Z_{DUT}(\omega_0) - 50\ \Omega) \cdot i_D(\omega_0) \end{aligned} \quad , \qquad (1.9)$$

Thus, known the output current of the device $i_D(\omega_0)$, it is possible to find the desired impedance $Z_{DUT}(\omega_0)$ at the desired frequency ω_0 by setting the generator voltage $v_{GEN}(\omega_0)$.

Naturally this approximation is too strong to be used to find directly the desired impedance, but it can be exploited in an algorithm, that itera-

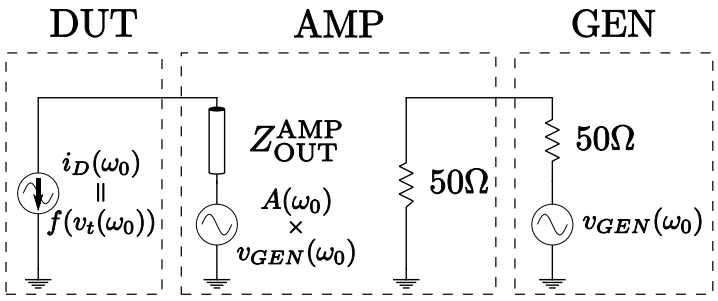

Fig. 1.17 Simplified model of the output section of the measurement setup with the power amplifier.

tively employs the above formula. As reported in the flux-diagram in **Fig. 1.16** the algorithm starts by applying a default excitation signal, then calculates the generator excitation voltage from the current measured in the previous iteration. It has been empirically found that this algorithm has good convergence properties in the practical cases of interest.

If a power-amplifier is needed at the drain section of the DUT, its effect must be taken into account. To this end, the amplifier is modeled as shown in **Fig. 1.17**, where the output impedance Z_{OUT}^{AMP} is supposed constant and known, whereas the amplification A^{AMP}, complex number, is measured at every iteration as the ratio between the incident wave imposed at the generator and the incident wave at the output of the amplifier. So it is still possible to exploit the formulation (**1.9**) even in this case, with small differences:

$$\begin{aligned} Z_{DUT}(\omega_0) &= \frac{v_D(\omega_0)}{i_D(\omega_0)} \\ &= \frac{A(\omega_0)\cdot v_{GEN}(\omega_0)}{i_D(\omega_0)} + Z_{OUT}^{AMP}(\omega_0) \rightarrow \\ \rightarrow\ v_{GEN}(\omega_0) &= (Z_{DUT}(\omega_0) \\ &\quad - Z_{OUT}^{AMP}(\omega_0)) \cdot i_D(\omega_0)/A(\omega_0) \end{aligned} \quad . \qquad (1.10)$$

If a high-impedance (i.e., an open) has to be synthesized the impedance Z_P in **Fig. 1.15a** is not negligible and the formulations in (**1.9**) and (**1.10**) are no more valid. In this case another algorithm can be applied: if the device output termination module is an open circuit/high impedance no/negligible current flows, so it can be concluded that:

$$\begin{aligned} v_D(\omega_0) \simeq v_{GEN}(\omega_0) \rightarrow\ & v_{GEN}(\omega_0) \\ & = v_D(\omega_0) \end{aligned} \quad , \qquad (1.11)$$

because the voltage drop on the 50 Ω resistance or the Z_{OUT}^{AMP} is negligible. Like in the previous case this formulation is used in an iterative algorithm where at each step equation (**1.11**) is imposed until the desired impedance has been found.

In both of the presented algorithms, to improve the convergence, a step-limitation is used. So the maximum distance between two steps (i.e., $|v_{GEN}(k) - v_{GEN}(k-1)|$) is limited.

These algorithms can be exploited to control simultaneously up to three harmonic terminations by simply running three instances of the algorithm together, each one working on a specific frequency.

A characterization-setup control program has been developed. This program controls the instrumentation in **Fig. 1.13** and implements the algorithms previously described, giving the possibility to control the output terminations at the fundamental frequency and at the second and third harmonics (i.e., 2 MHz, 4 MHz, 6 MHz).

In the following section the described setup will be exploited to design a high-efficiency microwave power amplifier.

TABLE I
0.25-μm GAN HEMT TECHNOLOGY SPECIFICATIONS

Quantity	*Value*
Breakdown Voltage	70 V
Pinch-off Voltage	-4 V
I_{Dss}	1 A/mm
Saturated Output Power	5 W/mm

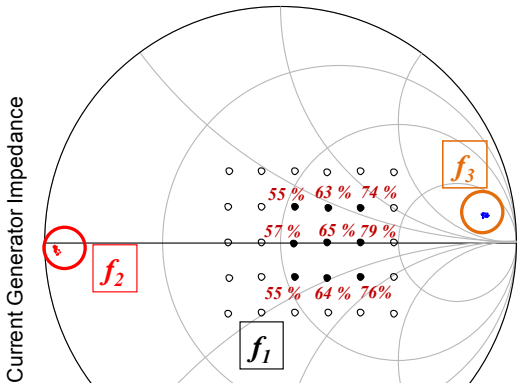

Fig. 1.18 Grid of impedances measured at the fundamental frequency of 2 MHz (circles) for a 1.25-mm periphery 0.25-μm GaN HEMT biased at V_{D0} = 32 V, I_{D0} = 10 mA. Impedances corresponding to an output power level of at least 5 W (filled circles) and corresponding efficiency values.

1.3.2 Class-F PA design

The class-F PA design here presented is based on a discrete 1.25-mm periphery 0.25-μm GaN on SiC HEMT, whose main foundry specifications are summarized in **Table I**.

The GaN HEMT was biased under class-AB condition (V_{G0} = -3.9 V, V_{D0} = 32 V, I_{D0} = 10 mA) and a LF load-pull characterization of the device intrinsic resistive core was carried out. To this end, by exploiting the harmonic active load-pull setup in **Fig. 1.13**, the 2-MHz impedances shown in **Fig. 1.18** were synthesized. For each of the thirty impedances synthesized at the fundamental frequency, the second harmonic impedance was settled to be a short circuit and the third one to be a high-impedance termination. All the experimentally synthesized impedances perfectly match with class-F theoretical formulation [23], [24] and [32].

Once the LF characterization phase was concluded, all information in terms of output power, drain efficiency, maximum gate-drain voltage, etc., was available and LF load-pull contours were drawn to evaluate the device performance. The design target was to obtain as maximum power as

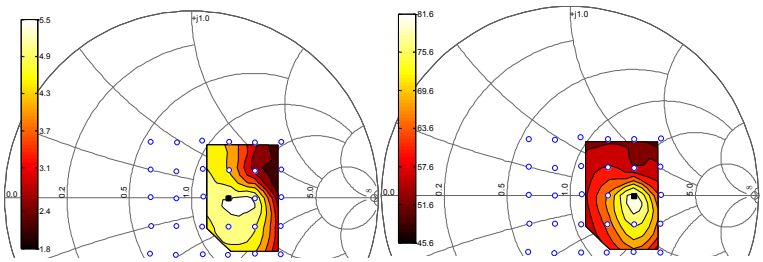

Fig. 1.19 Constant output power (left) and efficiency (right) contours at constant minimum gate-drain voltage V_{GD} = -69 V. Measurements carried out at 2 MHz for a 1.25-mm periphery 0.25-µm GaN HEMT biased at V_{D0} = 32 V, I_{D0} = 10 mA.

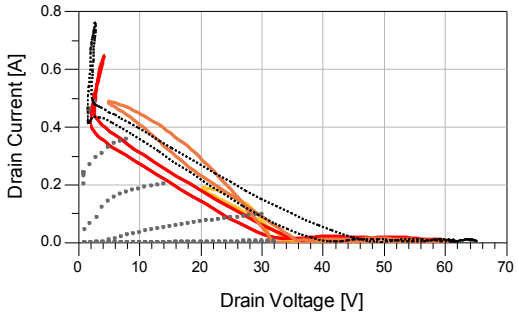

Fig. 1.20 LF measurements (solid line) for the load impedance Z_L = 103 - j*0.4 Ω as a function of increasing input power under class-F operation performed on a 1.25-mm periphery 0.25-µm GaN biased at V_{D0} = 32 V, I_{D0} = 10 mA. The load-lines are superimposed to DC characteristics (V_{GS} swept from -5 V to 0 V step 0.5 V).

possible for the selected device (1.25-mm periphery) with the maximum efficiency achievable: 5 W (~37 dBm) has been considered a reasonable target for the output power. Efficiency values for the selected output power level are shown in **Fig. 1.18**.

It should be pointed out that only nine impedances get the target. The reason is essentially related to reliability constraints since, for the remaining impedances, the compliances related to the maximum gate-source or gate-drain voltage are reached. In order to clarify this important aspect, **Fig. 1.19** shows the output power and efficiency contours for the fixed, maximum V_{GD} value of 69 V (value close to the breakdown voltage in **Table I**). In the left of **Fig. 1.19** it can be noticed that the maximum 5.5 W output power, corresponding to a 68.4 % drain efficiency, is achieved at $Z_P^{l,CGP} \simeq 75\ \Omega$, whereas from the right of **Fig. 1.19** the optimal efficiency condition (81.6 %) is found at $Z_E^{l,CGP} \simeq 103\ \Omega$ which corresponds to 5.4 W output power. Since the target is to maximize the efficiency obtaining as much power as possible, $Z_E^{l,CGP}$ has been chosen for the design phase.

The optimum impedances are 103-j0.4 Ω for the fundamental, 0.3+j0.1 Ω for the second harmonic and 344+j515 Ω for the third harmonic. As can be seen, short and open circuits are synthesized at the second and third harmonic, respectively.

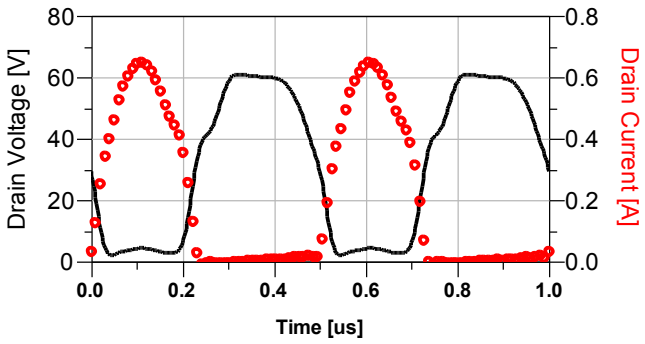

Fig. 1.21 LF time-domain voltage (solid line) and current (symbols) waveforms at the device CGP for the highest value of input power, corresponding to the synthesized class-F operating mode (loading condition of **Table II**) performed on a 1.25-mm periphery 0.25-μm GaN HEMT biased at V_{D0} = 32 V, I_{D0} = 10 mA.

Fig. 1.20 shows the trajectories of the load-line synthesized at the ED intrinsic resistive core as a function of the input power sweep. The measured load-line for the highest value of input power was compared with the one obtained by exploiting the foundry model which predicts 6.9 W output power with a drain efficiency of 90 % (dotted line in **Fig. 1.20**). It is well evident the poor predictive capability of the foundry model which is, usually, tailored for class-A or AB design. As previously said, thermal and trapping phenomena make the identification of a global and accurate model for the current generator [33], [34] very difficult. **Fig. 1.21** shows the measured LF time-domain voltage and current waveforms referred to the CGP: it is well evident that such electrical variables satisfy the minimal-overlapping condition imposed by class-F operation.

The obtained LF electrical variables corresponding to each termination were elaborated in order to obtain the termination at the EP at the design frequency of 2.4 GHz for the selected class-F operating mode.

Referring to **Fig. 1.11**, the previous characterization has gathered (neglecting the parasitic network resistive elements, anyway easily de-embeddable) the vectors of the *resistive-core currents* $[i(k\,\omega_{LF})]^r$:

$$[i(k\,\omega_{LF})]^r = [i_G(k\omega_{LF})^r \quad i_D(k\omega_{LF})^r] \quad , \tag{1.12}$$

(where k represents the harmonic index) and the associated vector $[v(\omega_{LF})]^r$ of the *resistive-core voltages*:

$$[v(k\,\omega_{LF})]^r = [v_{GS}(k\omega_{LF})^r \quad v_{DS}(k\omega_{LF})^r] \quad . \tag{1.13}$$

It is worth noticing that the resistive-core contribution is actually frequency independent. As a consequence:

$$[v(k\omega_{LF})]^r = [v(k\omega_{RF})]^r; [i(k\omega_{LF})]^r = [i(k\omega_{RF})]^r \quad . \tag{1.14}$$

As resistive and capacitive core are connected in parallel, the resistive core voltage vector and the *capacitive-core voltage* vector are equal to the *intrinsic voltage* vector:

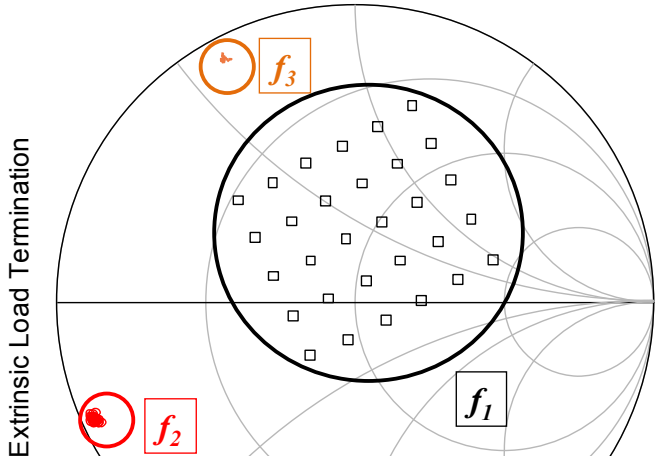

Fig. 1.22 Grid of impedances at the fundamental frequency of 2.4 GHz obtained from the measurement grid in **Fig. 1.18** for a 1.25-mm periphery 0.25-μm GaN HEMT. For each impedance synthesized at the fundamental frequency f_1 (square), the second harmonic f_2 (circles) and the third one (f_3) (dots) are shown.

$$[v(k\,\omega_{RF})]^c = [v(k\,\omega_{RF})]^r = [v(k\omega_{RF})]^i \quad . \tag{1.15}$$

Exploiting the foundry model (EE_FET3 [35], the vector $[v(k\omega_{RF})]^i$ of the intrinsic voltages can be applied to the capacitive-part description in order to achieve the device *capacitive-core currents* $[i(k\,\omega_{RF})]^c$.

The vector $[i(k\,\omega_{RF})]^i$ of the total intrinsic currents (*resistive-core currents* plus *capacitive-core currents*) can now be simply calculated by:

$$[i(k\,\omega_{RF})]^i = [i(k\,\omega_{RF})]^r + [i(k\,\omega_{RF})]^c \quad , \tag{1.16}$$

and, since all the electrical variables at the intrinsic device are known, the extrinsic electrical variables $[v(k\omega_{RF})]^e$ and $[i(k\,\omega_{RF})]^e$ can be obtained by exploiting the 4-port parasitic network description $\underline{H}(\omega)$, also derived from the foundry model:

$$\begin{Bmatrix} [v(k\omega_{RF})]^e \\ [i(k\,\omega_{RF})]^e \end{Bmatrix} = \underline{H}(k\omega_{RF}) \times \begin{Bmatrix} [v(k\omega_{RF})]^i \\ [i(k\,\omega_{RF})]^i \end{Bmatrix} \quad . \tag{1.17}$$

Once the extrinsic electrical variables are known, the load impedance (similar considerations can be done for the source impedance) at the fundamental and harmonic frequencies can be obtained:

$$Z_l(k\omega_{RF}) = -\frac{V_{DS}^e(k\omega_{RF})}{I_{DS}^e(k\omega_{RF})} \quad . \tag{1.18}$$

Fig. 1.22 shows the grid of impedances at the fundamental frequency of 2.4 GHz, resulting from the computation of the LF grid reported in **Fig. 1.18**. It is evident how much different second and third harmonic values are with respect to short and open circuit synthesized at the CGP.

At this point all the information in terms of output power, efficiency, PAE, gain etc. is available at the design frequency of 2.4 GHz and can be conveniently exploited to find the optimal impedance.

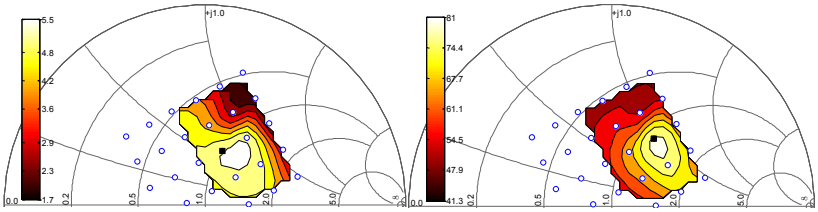

Fig. 1.23 Constant power contours (left) and constant efficiency contours (right) for the minimum gate-drain voltage V_{GD} = -69 V, both obtained at 2.4 GHz for a 1.25-mm periphery 0.25-μm GaN HEMT biased at V_{D0} = 32 V, I_{D0} = 10 mA.

TABLE II
COMPARISON BETWEEN SELECTED CURRENT GENERATOR LOAD IMPEDANCE AND EXTRINSIC ONE AS A FUNCTION OF FREQUENCY

CGP load impedance [Ω]	*Frequency [GHz]*	*Extrinsic load impedance [Ω]*
103 - j 0.4	2.4	57 + j 45.4
0.3 + j 0.1	4.8	1.4 – j 11
344 + j 515	7.2	2.3 + j 29.7

As shown for the CGP measurements (f_1 = 2 MHz), **Fig. 1.23** reports output power and drain efficiency contours for the fixed V_{GD} value of 69 V at the design frequency of 2.4 GHz. In the left of **Fig. 1.23**, a maximum output power of 5.5 W and a corresponding 68 % drain efficiency are achieved at $Z_P^{l,EP}$ = 50.6+j*29.9 Ω, whereas from the right of **Fig. 1.23** the optimal efficiency condition is found at $Z_E^{l,EP}$ =57 + j*45.4 Ω which corresponds to 81 % drain efficiency and 5.4 W output power. It is evident that the impedance providing the best efficiency for this application is represented by the value $Z_E^{l,EP}$ which will be synthesized with the PA output matching network (OMN). It should be pointed out that the optimal impedance $Z_E^{l,EP}$ found at the design frequency is the $Z_E^{l,CGP}$ after elaboration from "intrinsic" to "extrinsic" (section II). The procedure is applied to the whole impedance grid in order to draw contours at 2.4 GHz.

Table II shows the optimum extrinsic load terminations at the frequency of 2.4 GHz compared to the CGP terminations. It must be outlined that information on the CGP impedance values is not directly deducible from the extrinsic data. As an example, the obtained third harmonic high impedance condition at the intrinsic device, typical of class-F operating mode, is not easily evincible from its extrinsic value. This is the reason why large-signal measurements carried out at the design frequency cannot give useful information at the CGP, unless a rigorous nonlinear de-embedding procedure is adopted [25], [26].

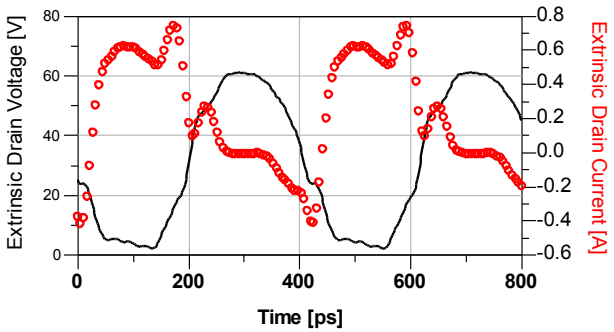

Fig. 1.24 Extrinsic time-domain voltage (continuous line) and current (circles) waveforms at the device drain extrinsic terminal for the highest value of input power, at the design frequency of 2.4 GHz (loading condition of **Table III**) obtained for a 1.25-mm periphery 0.25-μm GaN HEMT HEMT biased at V_{D0} = 32 V, I_{D0} = 10 mA.

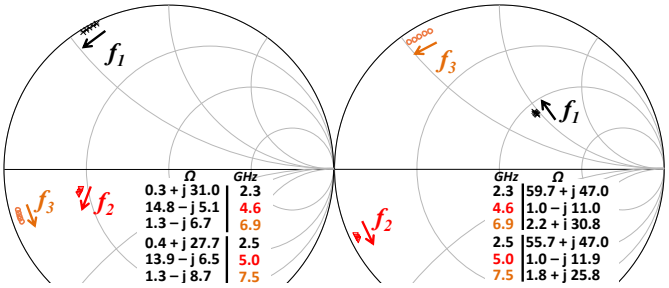

Fig. 1.25 Source (left) and load (right) impedances evaluated in the frequency range 2.3 – 2.5 GHz: fundamental (stars), second (triangles) and third (circles) harmonic termination trajectories for a 1.25-mm periphery 0.25-μm GaN HEMT biased at V_{D0} = 32 V, I_{D0} = 10 mA.

Moreover, as clearly shown in **Fig. 1.24**, by observing extrinsic voltage and current time-domain waveforms at the design frequency of 2.4 GHz, it is very difficult to assert that the GaN HEMT is working in class-F operation, whereas this is well evident by looking at the same electrical variables referred to the CGP (**Fig. 1.21**).

Successively the electrical variables corresponding to the optimum loading condition at the CGP have been computed in the frequency range 2.3-2.5 GHz. **Fig. 1.25** shows the trajectories of the fundamental, second and third harmonic input (a) and output (b) impedances in this frequency range. **Fig. 1.25** also shows the terminations to be synthesized at the extremes of the considered bandwidth corresponding to fundamental frequencies of 2.3 GHz and 2.5 GHz. In particular, the source impedance has been chosen equal to the conjugate of the large-signal ED input impedance, over the whole bandwidth.

The designed GaN class-F PA was manufactured on a HF laminate. Fundamental and harmonic target impedances have been synthesized in

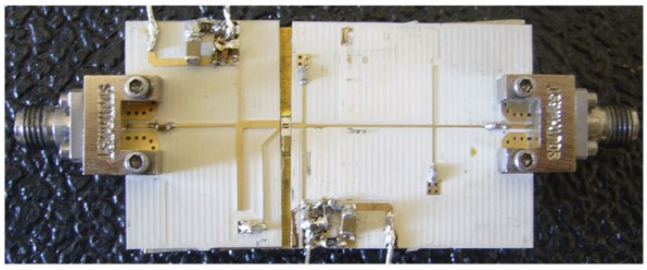

Fig. 1.26 Realized GaN class-F hybrid power amplifier.

the frequency range 2.3 – 2.5 GHz by means of simple topologies for both the input (IMN) and output matching network (OMN). It must be observed that, once the trajectories over the frequency of fundamental and harmonic impedances have been computed by exploiting the proposed approach, an arbitrarily large bandwidth could be obtained in theory by increasing the topological complexity of the IMN and OMN. Nevertheless, since the aim of this work is to demonstrate the effectiveness of the proposed technique, we privileged the use of simple topologies for the IMN and OMN.

A photograph of the realized class-F PA is shown in **Fig. 1.26**. The PA delivers an output power greater than 36 dBm (~ 4 W) with a drain efficiency greater than 55% over the frequency range of 2.3 – 2.5 GHz, with a maximum of 36.9 dBm and 74% at 2.45 GHz. Moreover, if the PA bandwidth is considered in the frequency range 2.375 – 2.475 GHz, the measured efficiency is always greater than 70%, while the output power is never lower than 36.9 dBm.

With the aim of comparing the experimental performance of the PA with the predicted ones, which are referred to the ED ports, both measured output power and drain efficiency were de-embedded from the losses of the OMN. Fig. 1.27 shows the comparison between the performance of the PA with and without considering the matching networks.

As a matter of fact, an output power greater than 36.4 dBm with a drain efficiency greater than 61% were registered over the frequency range 2.3 – 2.5 GHz. The peak value of the output power and drain efficiency were, in this case, 37.4 dBm and 84% respectively. Besides, in a smaller range of frequencies (2.375 -2.475 GHz), efficiency is always greater than 80% and output power is never smaller than 37.3 dBm (5.4 W). Experimental performance at the ED reference plane are in very good agreement with the predicted ones (37.3 dBm and 81 %), based on the LF load-line characterization.

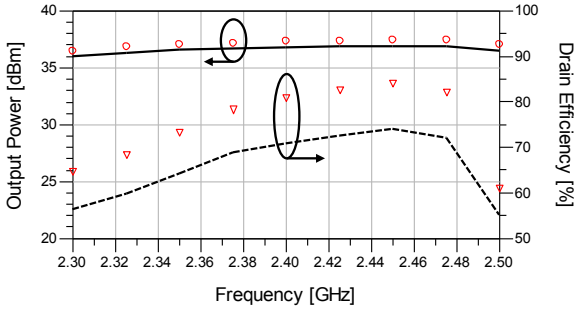

Fig. 1.27 Measured output power and drain efficiency of the realized PA across the bandwidth 2.3 – 2-5 GHz at the PA plane (bold and dotted lines respectively) and ED plane (circles and triangles respectively).

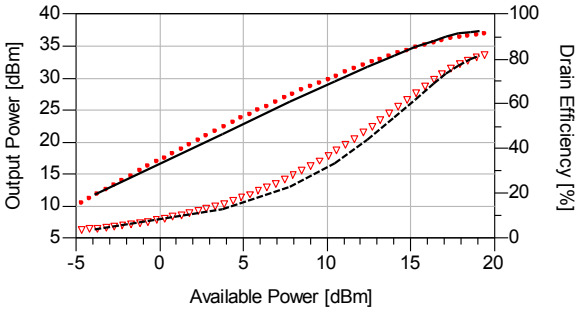

Fig. 1.28 Measured output power and drain efficiency of the realized class-F PA at the ED plane (dots and circles respectively) compared to the one predicted by the proposed technique (solid line and dashed line respectively).

Finally, Fig. 1.28 shows the comparison between measured and predicted output power and drain efficiency sweeps at 2.45 GHz, frequency where the impedance values reported in Fig. 1.25 have been more accurately synthesized since the best performance is reached. The excellent agreement between data definitely confirms the validity of the proposed load-pull technique.

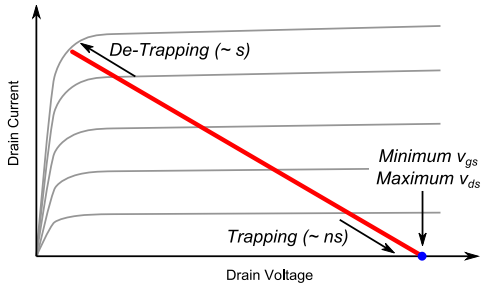

Fig. 1.29 Qualitative example of a load line with the indication of trapping and de-trapping phenomena.

1.3.3 Characterization of Charge-Trapping Effects in GaN FETs

In GaN devices asymmetries existing between capture and release time constants have been largely discussed. In particular, the capture process seems very fast (e.g., nanoseconds [36], [34]), whereas electrons are released with time constants even in the order of several seconds, well beyond the period of the typical signals which excite the device [34], [37].

Pulsed measurements [38], are the typical approach to characterize fast-trapping phenomena whose main consequence is the reduction of the maximum drain current achievable under RF operation and a variation of the slope of the dynamic I/V characteristics in the saturation region with respect to the DC ones.

The minimum and maximum values of the intrinsic gate and drain voltage waveforms (i.e., v_{gs} and v_{ds}, that are dynamically reached under actual operating conditions), determine the intensity of the fast-trapping phenomena [36], [34]. Therefore, to characterize the actual device I/V characteristics through pulsed measurements, they must be performed not only by fixing the selected bias condition, but also accounting for the v_{gs} and v_{ds} peak values the device will experience under its optimum operation. In other words, this approach requires the knowledge of the operating condition the device will operate under, which is clearly not known *a priori*. Moreover, under pulsed-bias operation the device thermal state is different from the one corresponding to device realistic operation in typical microwave circuits (e.g., power amplifiers). Nevertheless, pulsed setups represent a valid approach for low-frequency dispersion characterization [39]. As an alternative, the effects of fast-trapping phenomena can be accurately characterized by exploiting the setup reported in **Fig. 1.13**.

In **Fig. 1.29**, a qualitative example of a load line measurable with the LF setup is shown. As the load line reaches the pinch-off region, gate and drain voltages approach their minimum and maximum value respectively, inducing the fast-trapping process. The de-trapping process should occur as the DUT dynamic operation turns from this condition.

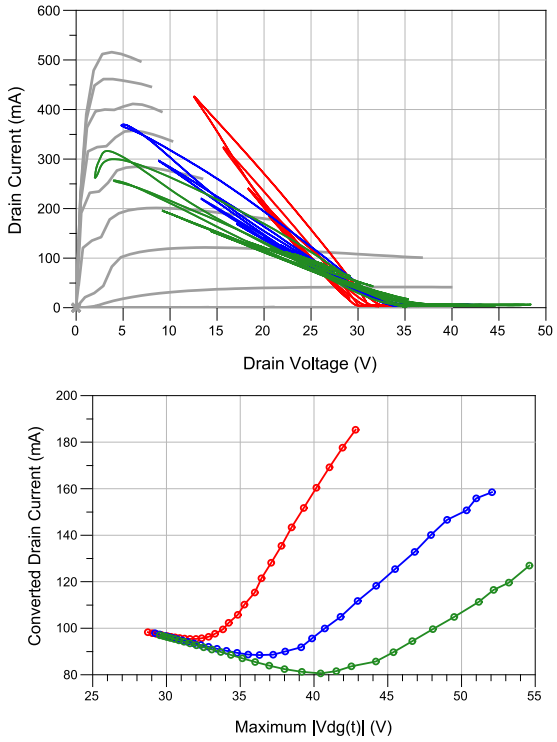

Fig. 1.30 Load lines (upper) and DC drain current (lower) as a function of the maximum magnitude of the gate-drain voltage measured on the Triquint 0.35 × 600 μm² GaN HEMT for a load impedance of 50 Ω (red), 100 Ω (blue) and 150 Ω (green). It's well evident the current drop for low-input power due to trapping effects. The bias point is V_{D0} = 25 V, I_{D0} = 100 mA.

However, due to the long-time constants of this phenomenon if compared with the period of the exciting signals (i.e., 500 ns), electrons cannot break free before the device reaches the pinch-off region once again in the following period. In this way, the effects of both slow- and fast-trapping phenomena [36] are gathered by the LF measurements in the same operating condition occurring at RF.

The upper part of **Fig. 1.30** reports some terminations synthesized at the output of a Triquint 0.35×600 μm² GaN HEMT at the frequency of 2 MHz for a load impedance of 50 Ω, 100 Ω and 150 Ω at various input-power values. The average drain current, (i.e., I_{D0}) as a function of the magnitude of the minimum intrinsic gate-drain voltage dynamically reached for each load line (i.e., $|v_{GD}^{MIN}|$ to take into account both the minimum value of v_{GS} and the maximum one of v_{DS}) is depicted in the lower part of **Fig. 1.30**.

It is evident its initial drop for lower input power levels, where the load lines have not yet reached either the linear region or the pinch-off region of the I/V characteristics. This is considered one of the most important evidences of fast-trapping phenomena [34] and, as here shown, it can be easily captured by the LF measurement system. It is remarkable that, despite each measurement refers to a very different operating condi-

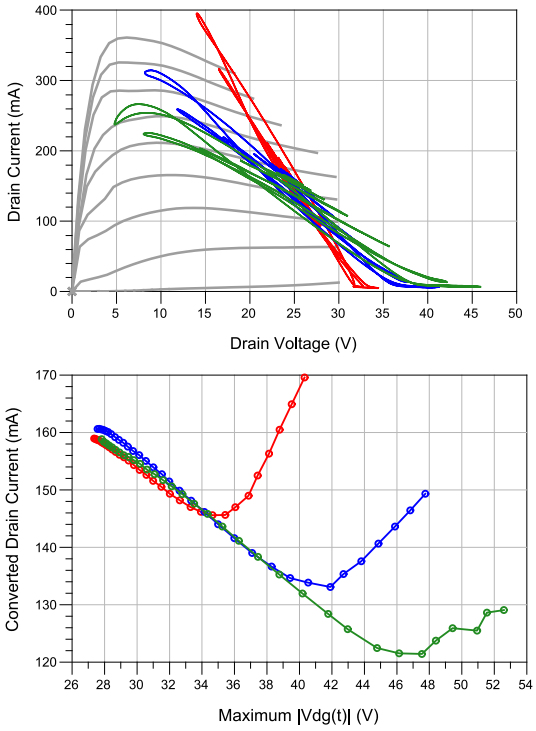

Fig. 1.31 Load lines (upper) and DC drain current (lower) as a function of maximum magnitude of the gate-drain voltage measured on the Selex ES 0.5 × 1000 μm² GaN HEMT for a load impedance of 50 Ω (red), 100 Ω (blue) and 150 Ω (green). It's well evident the current drop for low-input power due to trapping effects. The bias point is V_{D0} = 25 V, I_{D0} = 160 mA.

tion, the initial current-drop shape of each curve is perfectly superimposed to the others. In this part of the plot, the influence of the variation of the device thermal state is still very limited, since the measured efficiency remains below 10%.

The trend of the curves reported in **Fig. 1.30** is consistent with the conventional interpretation of the fast-trapping phenomena, according to which charge trapping produces a back-gating effect [40], [41] that becomes evident in the reduction of I_{D0} even under a small-signal regime. In fact, we can interpret the reduction of the current as if the bias-point of the device (i.e., V_{G0}) were dynamically changed during the power sweep, in accordance with the minimum value of the gate-drain voltage. From **Fig. 1.30**, it is also evident, especially for higher impedances, a saturation mechanism. For instance, for the 150-Ω load, I_{D0} decreases up to $|v_{GD}^{MIN}|$ = 37 V and remains approximately constant between this value and $|v_{GD}^{MIN}|$ = 42 V. It has to be noticed that in this voltage range the load lines have not yet reached the pinch-off region, which determines the typical conversion of I_{D0} in a power sweep measurement.

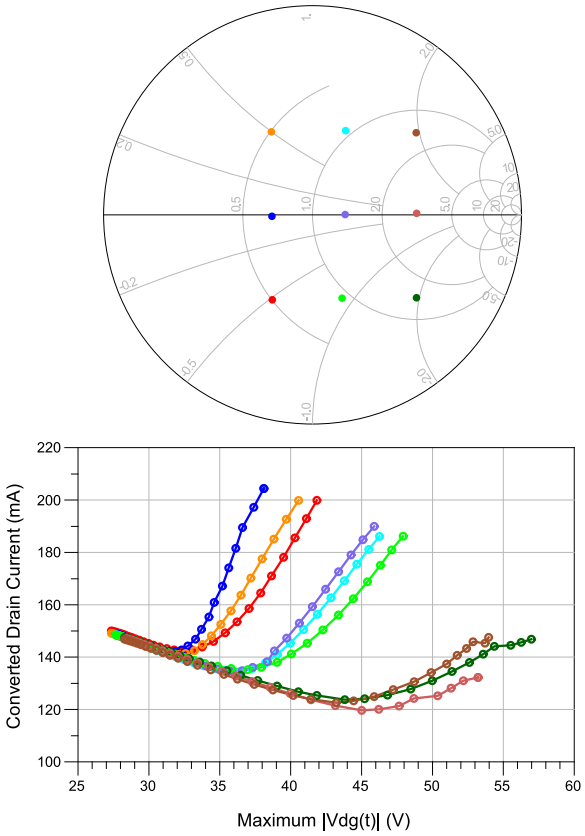

Fig. 1.32 DC drain current (lower) as a function of maximum magnitude of the gate-drain voltage measured on the 0.25 × 600 μm² GaN HEMT by UMS for various load terminations (upper). It's well evident the current drop for low-input power due to trapping effects. The bias point is V_{D0} = 25 V, I_{D0} = 150 mA.

To have a rough evaluation of the manufacturing process it could be of interest to perform these measurements on transistors from different manufacturers. As these effects are due to defects in the transistor structure, a technology with a reduced number of defects should present a reduced drop of I_{D0}.

Fig. 1.31 reports the same measurements in **Fig. 1.30** but carried on a 0.5×1000 μm² GaN HEMT by Selex ES.

For $|v_{GD}^{MIN}|$ = 40 V the device by Triquint presents a current drop of 20 mA, the 20% of the initial DC current, on the other hand for the same $|v_{GD}^{MIN}|$ the device by Selex ES has a current drop of 30 mA, more or less the 19% of initial DC current. So even if the current drop seems more evident for the Selex ES transistor, in percentage the magnitude of the phenomenon is comparable.

A similar analysis was performed on a 0.25×600 μm² GaN HEMT by UMS; this technology is the most recent one of those considered in this study. Nine load terminations were synthesized, reported in the upper part in **Fig. 1.32**. The DC drain current is reported in the lower part in **Fig. 1.32**. The trend is similar to the one measured for the two previous devic-

es, but the current drop is lower at $|v_{GD}^{MIN}| = 40$ V, about 20 mA, that is the 13% of the initial small-signal current, thus the 0.25 technology by UMS has fewer defects in the transistor structures than the other two technologies considered.

In conclusion, with the setup described in this chapter, fast trapping phenomena in III-V transistors can be also analyzed. These phenomena, besides affecting transistor performance, can be used to evaluate the technology process. It is worth noticing that the technology in which a fewer number of defects was found is also the latest.

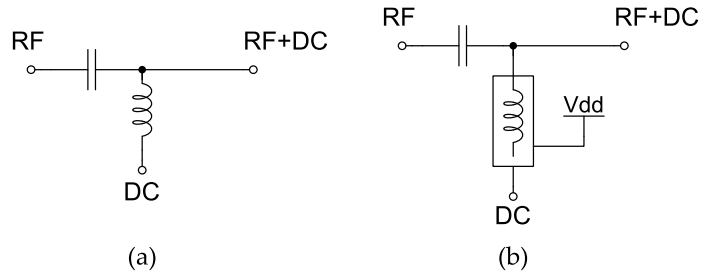

Fig. 1.33 Classic bias tee (a) and proposed "active" bias tee (b) block diagram.

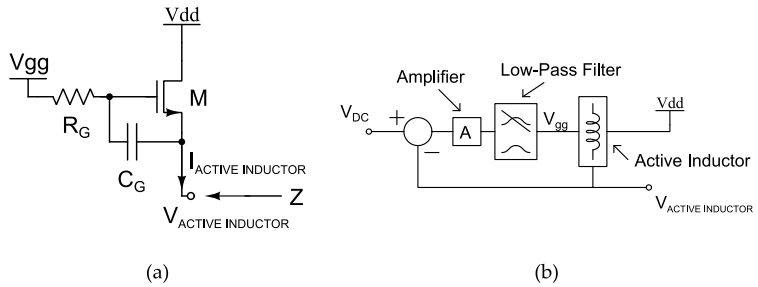

Fig. 1.34 Generic circuit diagram of an active inductor (a) and feedback network block diagram (b).

1.4 EXTENSION OF THE LF SETUP TO VERY LOW FREQUENCIES

In the previous section a fast-trapping effects characterization using the proposed setup has been presented. Nevertheless, also very low-frequency dispersive phenomena characterization is of interest. As an example, in radar and telecommunication applications long-term memory effects afflict PA performance, resulting for example in asymmetry in intermodulation sidebands, or collapse of the DC drain current in pulsed bias radar operation [42]. Part of these effects can be related to the transistor thermal and trapping states. As a consequence, there is a great interest by the microwave community on the characterization of this kind of phenomena, in order to build models for the accurate prediction of device behavior [27]. Unfortunately, assembling a suitable measurement setup for the identification of these models is very complicated, in fact great efforts have been spent by the microwave researcher community for developing setups able to characterize transistors at very low frequencies. The major problem is coupling and decoupling signals and bias. Commercial bias-tees bands have a lower frequency of tens of kilohertz; instead, to correctly measure low-frequency dispersive phenomena a bias-tee capable to operate at tens of hertz is needed. Various solutions have been proposed based on a resistive approach [42] or active inductor [43].

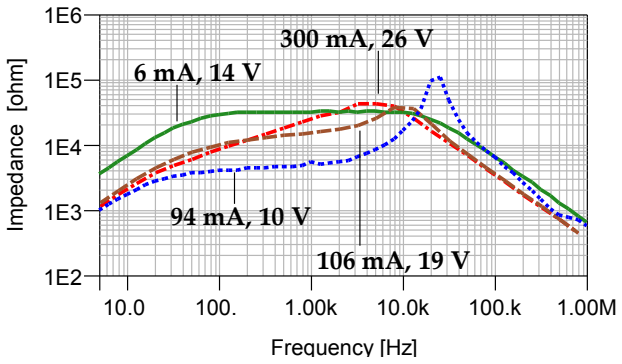

Fig. 1.35 Active inductor impedance magnitude versus frequency for different bias conditions of the transistor in **Fig. 1.34a**.

A novel bias tee design will be presented here which is based on an active inductor. In particular, the circuit operation is described and the performance is verified by extensive empirical characterization. Different experimental examples under small- and large-signal operation are also reported in order to demonstrate the suitability of the proposed bias-tee in actual application contexts.

1.4.1 Active Bias Tee

The schematic of a classic bias tee is shown in **Fig. 1.33a**. In order to decrease its cutoff frequency one must use very large and high-quality inductors. At very low frequencies the inductance value must be so high that it is unpractical and, moreover, there are no commercially available components with adequate quality. To avoid this problem we propose an active bias tee (ABT), represented in **Fig. 1.33b**, which uses an active inductor.

An active inductor can be obtained by using an FET device with a high-pass-feedback network between gate and source as shown in the circuit diagram in **Fig. 1.34a**. By means of a simple small-signal analysis the active inductor impedance can be derived, which shows an equivalent inductance given by:

$$L_{EQ} = \frac{R_G C_G}{g_m - g_{DS}} \quad . \tag{1.19}$$

To increase the active inductor performance, two approaches can be followed. The first one is to increase the order of the high-pass-feedback network (a pi-shape feedback circuit is used). The second one is to select a suitable transistor to have low trans-conductance and low output conductance, in order to increase the equivalent inductance, as shown in equation (**1.19**).

TABLE III
ACTIVE BIAS TEE SPECIFICATIONS

Name	Value
Impedance	50 Ω
Lower Frequency	5 Hz
Upper Frequency	400 kHz
Insertion Loss	< 0.10 dB
Return Loss	> 20 dB
Max DC output Voltage	40 V
Max DC output Current	1 A
Max transistor DC Power	10 W
Supply Voltage	7 – 60 V
DC Blocking Capacitance	3 mF

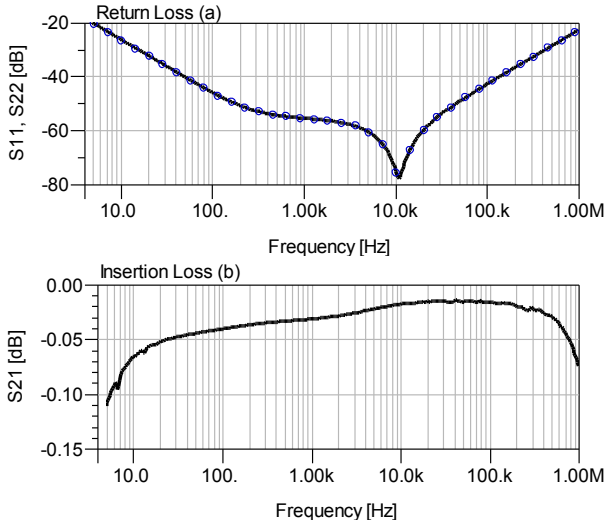

Fig. 1.36 Return (a) and insertion losses (b), continuous line for S_{11}, circles for S_{22}, of the proposed active bias tee for an output current of 138 mA and an output voltage of 20 V (Supply voltage 35 V).

Unfortunately, these two conditions cannot be simultaneously achieved by using a single transistor: thus a suitable transistor cascade is required. Both of these approaches are exploited.

The FET gate voltage is used to control the output voltage of the active inductor; in particular it is necessary to settle the average value of the output voltage. This can be obtained by using a feedback circuit with a low-pass filter as represented in **Fig. 1.34b**.

A dedicated measurement setup was realized for testing the performance of the active inductor. In particular, a Vector Network Analyzer (VNA) port was connected to the active inductor through a capacitor bank while a power resistor acts as load. The calibration plane was placed just after the capacitor bank. Additionally, a system to protect the VNA during the capacitor charge and discharge was properly designed. The power re-

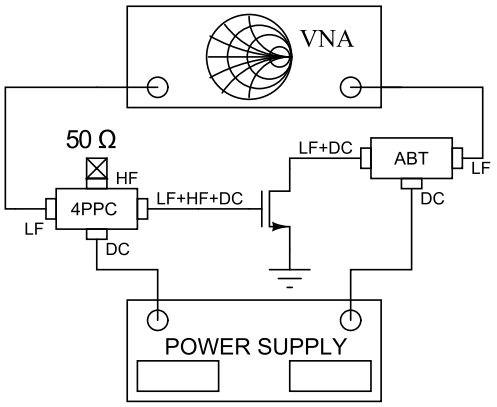

Fig. 1.37 Measurement setup for small signal analysis.

sistor was characterized and subsequently de-embedded to obtain the impedance of the active inductor in various operating conditions.

The impedance magnitude of the active inductor is shown in **Fig. 1.35**. As expected, the inductor, due to its active nature, shows impedance values depending on the bias condition of the transistor in **Fig. 1.34a**. As shown in **Fig. 1.35** the inductor impedance is greater than 1 kΩ (our design specification) between 5 Hz and 400 kHz, even in the worst case. Please note that 5 Hz is the lowest measurable frequency of the VNA.

According to **Fig. 1.33b** we realized the active inductor and a capacitive bank using different capacitors in order to increase the bandwidth of the system. The insertion and return losses of the designed ABT are shown in **Fig. 1.36** while **Table III** reports a summary of its characteristics.

A big issue is related to system calibration. As shown in **Fig. 1.35,** the impedance of the active inductor is a function of its operating condition. We adopted an error correction procedure based on the knowledge of the active inductor behavior. In particular, the active inductor is preliminarily characterized in terms of S-parameters and considering the selected operation, so that its contribution can be properly de-embedded.

With the aim of validating the performance of the designed ABT, several transistors were characterized. More precisely, output characteristics were measured by placing the ABT at the output of the device under test.

Small- and large-signal drain side measurements were carried out on a 12x80x0.25-μm² GaAs pHEMT and the pulsed bias response was evaluated on a 8x75x0.25-μm² GaN HEMT.

The small-signal measurement setup for performing low-frequency characterization must be designed to have a good behavior even at higher frequencies. In fact, a poor high frequency termination may result in possibly harmful oscillations of the DUT. To this end, a four-port passive circuit (4PPC) has been designed and placed on the gate side to guarantee transistor stability. In particular, it is composed of a bias-tee, for properly coupling bias (DC) and low-frequency (LF) signals, and a high-pass filter terminated with a wideband 50 Ω (HF-port) providing a dissipative termination up to gigahertz frequencies. The measurement setup is shown in **Fig. 1.37**.

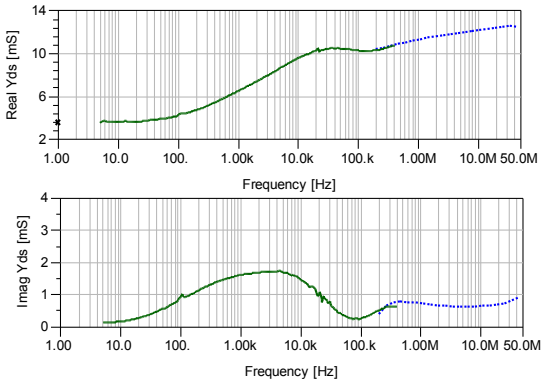

Fig. 1.38 Measured real (upper) and imaginary (lower) parts of Y_{DS} of the GaAs device versus frequency (logarithmic) for V_{GS0} = - 0.2 V, V_{DS0} = 2.5 V, I_{D0} = 210 mA with the extremely low-frequency ABT (continuous) and the commercial medium frequency (dotted) bias tee, respectively. The 'x' point has been derived from DC I/V characteristics.

The measurements were carried out in two frequency ranges: namely extremely low-frequency with the proposed ABT and medium frequency with a commercial bias tee.

The measured output admittance Y_{DS} of the GaAs transistor is reported in **Fig. 1.38**. The real and imaginary parts show important changes in the selected frequency range. These phenomena are essentially caused by dispersive effects of the transistor, in particular deep-level traps.

The Y_{DS} measurement shows a good agreement between the analysis carried out with the ABT and the one with the commercial bias tee in the overlapping frequency range. Also the Y_{DS} DC value, calculated as the slope of DC curves around the bias point considered, is in excellent agreement. This result confirms the good performance of the realized ABT in small-signal operation.

The large-signal characterization was performed in the same bias point where the small-signal experiment was carried out. In particular, constant V_{GS} dynamic drain current versus drain voltage curves were traced at different frequencies (5 Hz – 400 kHz). Output voltage and current were acquired with oscilloscope probes directly at the output port of the DUT. At low-frequency the curves should coincide with the DC output characteristic, while deviating at higher frequencies. This measurement was performed also at megahertz frequencies with the large-signal low-frequency setup in [44].

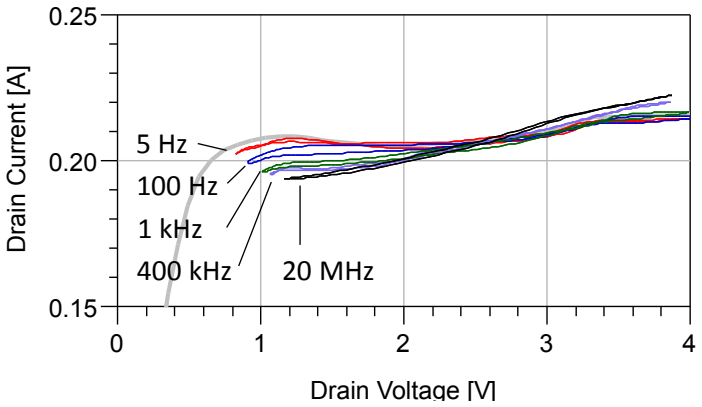

Fig. 1.39 Constant V_{GS} (-0.2 V) dynamic $I_D - V_{DS}$ curves at various frequencies for the GaAs device. DC output characteristic at V_{GS0}=-0.2 V is superimposed to the curves.

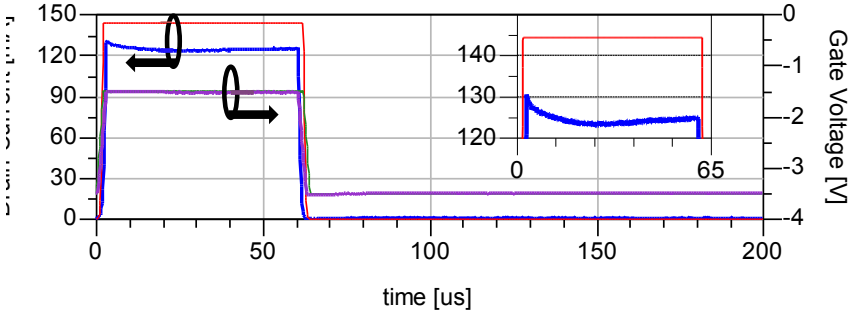

Fig. 1.40 Response to a typical radar pulse (Frequency = 5 kHz, T_{ON} = 60 μs) of the GaN device. Model predictions using DC data only (thin line) are compared with measurements (thick line).

The measured characteristics are reported in **Fig. 1.39**. The lower frequency curves almost coincide with the DC characteristic, whereas at higher frequencies we see a clear variation of the slope, in agreement with **Fig. 1.38**.

Power amplifiers in radar systems often use pulsed bias technique to reduce power consumption and heating. A typical radar bias pulsed waveform has harmonic components which lie in the band of low-frequency dispersion. As a consequence, the response of the active device cannot be deduced by its DC characteristics.

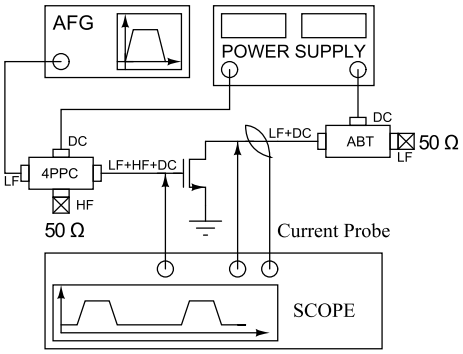

Fig. 1.41 Measurement setup for pulsed bias response.

The proposed ABT, having a very low cutoff frequency, allows to measure accurately the response of the device. In **Fig. 1.40**, the response of a 8x75x0.25-μm² GaN HEMT to a pulse excitation (T_{ON} = 60 μs, duty cycle 30 %) is reported. In the same figure simulated data are also shown, which are obtained by exploiting a model based on the DC device characteristics. It is well evident that the DC characteristics are not able to accurately describe the device slow dynamics under actual operation. The measurement setup is reported in **Fig. 1.41**.

In conclusion a 5 Hz - 400 kHz ABT has been designed and realized, and its specifications and performance have been discussed in detail. In order to assess the suitability of the proposed approach under operating conditions of interest for the microwave community, the ABT was exploited to carry out accurate small- and large-signal measurements on GaAs and GaN devices. It is well evident that the proposed bias tee allows to reach a clear-cut insight in low-frequency dispersive phenomena affecting microwave transistors.

1.5 CONCLUSION

In the first part of this chapter the two most common non-linear characterization techniques have been presented: the Non Linear Vector Network Analyzer (NVNA) and Load- and source-pull characterization systems. These systems are very useful in a lot of application but, as discussed in the chapter, are not able to characterize properly an electron device at the CGP, where the most common design techniques are referred. To overcome this problem, a low-frequency large-signal setup with harmonic load-termination control ability has been presented. This setup is useful not only for power amplifier design, as confirmed by the reported Class-F PA design example, but also for dispersive phenomena characterization. In the last part of the chapter a possible extension of the setup to lower frequencies has been discussed. In conclusion the proposed characterization setup is a valid instrument for power amplifier design and for electron device dispersive phenomena characterization.

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2 LINEAR CHARACTERIZATION SETUP

A linear network, described as a black-box with unknown internal content, can be fully characterized by means of quantities measured at the network ports (i.e., the network terminals). Once these parameters have been determined, the steady-state behavior of the network can be predicted with any exciting conditions within the characterization frequency range and provided that suitable interpolation techniques are adopted.

In low-frequency applications, Z- and Y-parameters are typically used. As a matter of fact, these parameters are the most intuitive because directly relate voltages and currents at the network ports:

$$\underline{V} = \underline{\underline{Z}} \cdot \underline{I} \longrightarrow \begin{bmatrix} V_1 \\ V_2 \end{bmatrix} = \begin{bmatrix} Z_{11} & Z_{12} \\ Z_{21} & Z_{22} \end{bmatrix} \cdot \begin{bmatrix} I_1 \\ I_2 \end{bmatrix} \quad , \tag{2.1}$$

$$\underline{I} = \underline{\underline{Y}} \cdot \underline{V} \longrightarrow \begin{bmatrix} I_1 \\ I_2 \end{bmatrix} = \begin{bmatrix} Y_{11} & Y_{12} \\ Y_{21} & Y_{22} \end{bmatrix} \cdot \begin{bmatrix} V_1 \\ V_2 \end{bmatrix} \quad , \tag{2.2}$$

where the subscripts "1" and "2" stand for port 1 and port 2.

These parameters can be measured by applying suitable conditions at the network ports, as an example:

$$Z_{12} = \left.\frac{V_1}{I_2}\right|_{I_1 = 0} \quad , \tag{2.3}$$

$$Y_{11} = \left.\frac{I_1}{V_1}\right|_{V_2 = 0} \quad . \tag{2.4}$$

Thus the parameter Z_{12} can be measured as the ratio between the voltage at port 1 and the current at port 2 when there is no current at port 1, so an open is connected to port 1. Similar considerations can be made also for Y_{22} where a short is connected to port 1.

At higher frequencies these parameters are no more practical because its direct measure is often not possible: a high-reflective termination (as open or short circuit) at the input or output of an active microwave device leads very often to instability, triggering oscillations that invalidate the measurements and could be also harmful for the device under test (DUT). Moreover the broadband short and open terminations are often not practical, because at high-frequencies the parasitic effects seriously afflict high-reflective loads.

To overcome these problems the Scattering Parameters (S-Parameters) have been introduces by Kurokawa [1]. These parameters are not the ratios between voltages and currents but the ones between the normalized incident waves and reflected waves:

$$a_i = \alpha \sqrt{\Re(Z_0)}\, \frac{V_i + I_i Z_0}{2 Z_0} \quad , \tag{2.5}$$

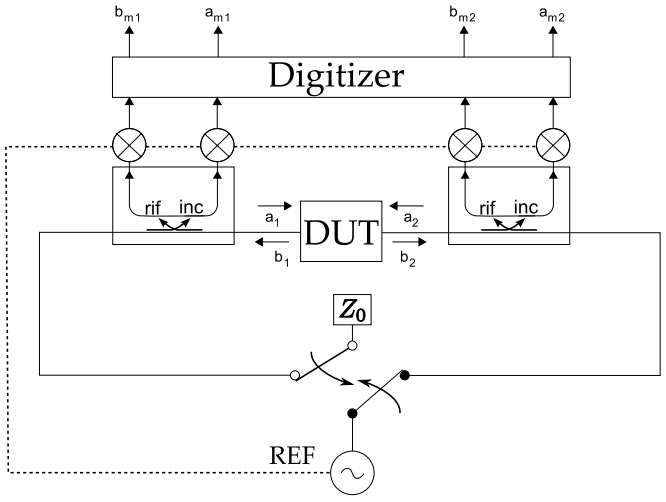

Fig. 2.1 Block diagram of a 2-port VNA, the signal source excites the DUT whereas its incident and reflected waveforms are acquired.

$$b_i = \alpha\sqrt{\Re(Z_0)}\,\frac{V_i + I_i Z_0}{2\,Z_0} \quad , \tag{2.6}$$

where V_i and I_i are the voltage and the current at the port "i", α is an arbitrary constant and Z_0 a complex reference impedance (usually 50 Ω).

The linear equations now describing the two-port network are:

$$\underline{b} = \underline{\underline{S}} \cdot \underline{a} \longrightarrow \begin{bmatrix} b_1 \\ b_2 \end{bmatrix} = \begin{bmatrix} S_{11} & S_{12} \\ S_{21} & S_{22} \end{bmatrix} \cdot \begin{bmatrix} a_1 \\ a_2 \end{bmatrix} \quad , \tag{2.7}$$

so the S-parameter of order "i","j" is defined as:

$$S_{ij} = \left.\frac{b_j}{a_i}\right|_{a_j=0} \quad . \tag{2.8}$$

To measure the S-parameters it is necessary to connect to the port j of the DUT a load with impedance Z_0, to eliminate the components a_j. If the reference impedance is selected as a dissipative load, like 50 Ω, the instability is avoided in almost all cases and accurate measurements can be carried out.

It is worth of notice that one time the S-parameters are measured, the other parameters (Z-parameters, Y-parameters, ABCD-parameters …) can be obtained using the formulations reported in [2].

In the first part of this chapter it will be described the instrument exploited to measure the S-parameters: the Vector Network Analyzer (VNA). Successively, how trapping effects afflict the small-signal parameters will be discussed. In particular, the characterization of the transistor output conductance, which is of particular importance in amplifier design, will be detailed. In the last part of the chapter the possibility of using a neural-network model to predict small-signal low-frequency parameters will be discussed.

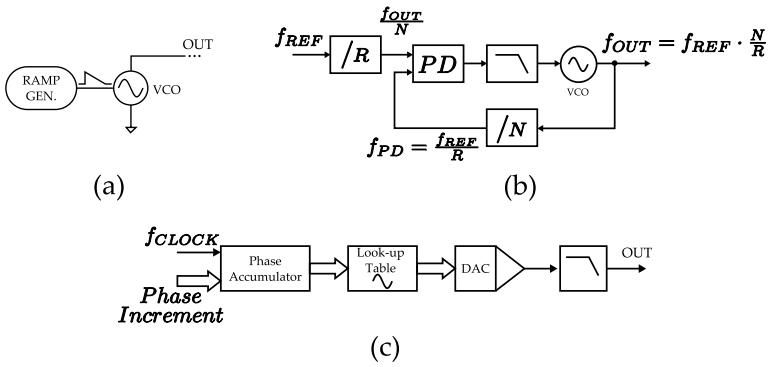

Fig. 2.2 Signal Sources. In (a) is reported a sweeper based sources, in (b) is presented a frequency synthesizer exploiting PLL technique. At last in (c) is drawn a block diagram of a DDS.

2.1 VECTOR NETWORK ANALYZER

The VNA is the instrument used to measure the S-parameters of a network.

The first VNA was introduces during the '50 [3], and was composed by racks full of instruments and with narrow frequency range. Successively, it evolved in the modern VNAs, compact and broadband. Nowadays, an example of a state of the art VNA is the N5251A by Keysight technologies; it is able to perform measurements up to 110 GHz and 1.1 THz with external millimeter probe extensions [4].

A basic diagram of a VNA is reported in **Fig. 2.1**. The main components are:

SIGNAL SOURCES, one or more, the signal frequency has to be controllable, and the signal purity must be adequate for the measurement; if a single source is shared between more ports, one or more switches must be used.

DIRECTIONAL COUPLERS, one for each port, they pick up a portion of the incident and reflected waves at the DUT ports.

RECEIVERS, they acquire the incident and reflected waves feed by the coupler; usually the acquisition is performed al low frequency, so they often incorporate a down-conversion system.

A CALIBRATION TECNIQUE: measuring a phase shift of 1° on a DUT S_{11} connected to the VNA by a 1 m Teflon cable is like to weigh 300 gr of ham with a one-ton plate scale [5]. It is clear that some form of correction is necessary to have an acceptable measurement quality.

The main components of the VNA will be here discussed in more detail.

2.1.1 *Signal Sources*

The sources integrated in a VNA must have two main capabilities:

- to accurately control the output frequency
- to control the output power.

For the first requirement three solutions can be found:

SWEEPER-BASED SOURCES, a block diagram, of a simple sweeper is reported in **Fig. 2.2a**. It's a very simple circuit, with quite fast settling time (i.e., the time needed to pass from one frequency to another) and reduced spectral impurities. However, the synchronization of the source with the acquisition circuitry is difficult thus leading to potential frequency errors. Due to this reason they are not used anymore in modern VNAs.

SYNTHESIZER-BASED SOURCE, like reported in **Fig. 2.2b**. A Phase Locked Loop (PLL) technique is used to achieve high spectral purity using an high-quality, low-frequency, crystal reference oscillator. This oscillator can be shared with the acquisition part, to synchronize all the VNA subsystems. PLL design is very complex [6], and far beyond this thesis subject, but some general considerations can be made. Historically Yttrium Iron Garnet (YIG) oscillators have been commonly used in high frequency synthesizer. This type of oscillator has a low phase noise but it is a bit slow. In broadband VNAs the settling time is very important, so the varactor-based Voltage Controlled Oscillators (VCOs) are exploited. These oscillators are more rapid in frequency changes, but the phase noise is worse than the one in YIG oscillators. A fine frequency tuning capability can be achieved with Fractional-N structures, allowing a below-Hz resolution.

DDS-BASED SOURCE, at the current time, Direct Digital Synthesis (DDS, in **Fig. 2.2c**) is not common in VNA sources, because the maximum frequency reachable by these systems (i.e., few GHz) are very lower than the previous solutions. Nevertheless this gap has been shrinking as DDS technology grows, allowing very simple signal generation, with very fine frequency tuning at the cost of a bit more spurious components.

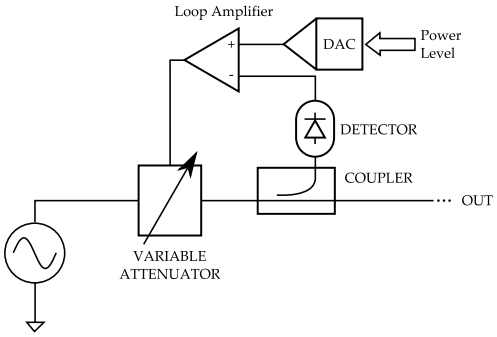

Fig. 2.3 Variable power control in a signal source

Output power control is necessary in a VNA, because different DUTs need different input powers, and in many measurements (e.g., Intermodulation Distortion, Gain Compression) a power sweep is needed.

The power level control is made, according to **Fig. 2.3**, by detecting the source output power, exploiting a coupler and a detector, comparing the source output power with a reference level, then using the comparator output to feed a variable attenuator, thus closing a negative feedback loop.

If a single source feeds more than one port, a switch is needed. Two switch technology solutions have been found:

PIN DIODES [7]. These diodes have a very thick intrinsic layer between heavily doped p and n regions. This solution leads to a very small reverse-bias capacitance, thus increases the isolation when the diode is in the interdiction region. One drawback is that the carrier recombination is quite high, so when a low-frequency signal is applied some distortion can be found.

COLD FET [8]. It is a FET where the bias condition guarantees low thermal dissipation and the signal passes from drain to source. Considering for example a depletion mode transistor, if the gate voltage is low enough no electron is available in the channel, providing isolation between drain and source. However if the gate voltage is near the ground potential only a low parasitic resistance is present between drain and gate.

A commercial switch can use one or one combination of the two technologies described above, and several diodes (and/or transistors) in shunt (shorting the signal to ground) or series (interrupting the signal path) configuration.

2.1.2 Directional Couplers

A directional coupler is a device that collects a portion of the energy of the incident and the reflected waves that are flowing through it, influencing the system where is connected the less possible. It is a 4-port network

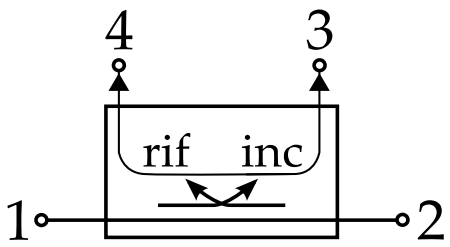

Fig. 2.4 Bidirectional coupler, main (1-2) and coupled (3-4) lines are reported.

and its diagram is reported in **Fig. 2.4**. The S-parameter matrix of a coupler, assuming that the network is passive and reciprocal, is:

$$S = \begin{bmatrix} S_{11} = \rho_{main} & S_{12} = l_{main} & S_{31} = c_f & S_{14} = i_f \\ S_{21} = l_{main} & S_{22} = \rho_{main} & S_{23} = i_f & S_{24} = c_f \\ S_{31} = c_f & S_{32} = i_f & S_{33} = \rho_{coupl} & S_{34} = l_{coupl} \\ S_{41} = i_f & S_{32} = c_f & S_{43} = l_{coupl} & S_{44} = \rho_{coupl} \end{bmatrix} , \quad (2.9)$$

where:

THE MAIN- AND COUPLED- LINE RETURN LOSS, ρ_{main} and ρ_{coupl} are to be minimized (i.e., ideally they have to be zero) to not influence the signal path and to provide an adequate termination to the DUT and to the receivers.

THE MAIN- AND COUPLED- LINE INSERTION LOSS, l_{main} and l_{coupl} must also be minimized (i.e., ideally they have to be zero) to reduce the losses and to make the coupler transparent to the DUT.

THE ISOLATION FACTOR, i_f has to be small, in order to make the coupler work properly. If the isolation factor is zero, then the reflected waves at the coupled port (i.e., b_3 and b_4) are proportional to the incident waves at the main port (i.e., a_1 and a_2) respectively through the coupling coefficient c_f.

THE COUPLING FACTOR, c_f relates the incidents waves at the main ports to the reflected waves at the coupled ports. Ideally (i.e., $i_f \simeq 0$ and very small losses) we have:

$$b_3 = c_f \cdot a_1 \simeq c_f \cdot b_2 \quad , \quad (2.10)$$

$$b_4 = c_f \cdot a_2 \simeq c_f \cdot b_1 \quad , \quad (2.11)$$

A well designed directional coupler is transparent to the signal path ($a_1 \simeq b_2$,$a_2 \simeq b_1$) and collects a portion of the wave flowing through it. Coupling factors usually are in the order of -10 dB~-20 dB.

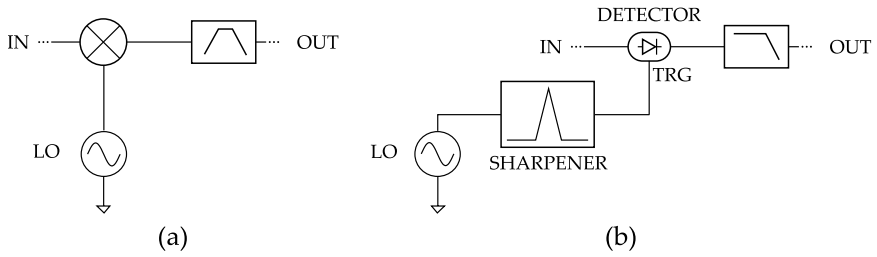

Fig. 2.5 Acquisition systems. In (a) is reporter a mixer based approach, while in (b) a sampler is presented

DIRECTIVITY, i_f/c_f (some formulations take into account also the losses), quantifies how the coupler is able to separate incident and reflected waves.

Another important directional coupler parameter is the bandwidth: to maintain a good directivity across a very large bandwidth (e.g., 10 MHz to 110 GHz) is not trivial, and very complex coupler architectures are often required.

2.1.3 Receivers

Signal acquisition is often performed at low-frequency, to increase accuracy and decrease costs. So the first part of the receiving system is a down converter. Two approaches can be followed:

MIXER BASED, where the signal to be acquired and a reference signal generated by a Local Oscillator (LO) are fed to a mixer, according to **Fig. 2.5a**. The mixer combines the two signals, generating new frequency components:

$$f_{out} = n \cdot f_{in} \pm m \cdot f_{lo} \quad n, m \in \mathbb{N} \quad . \tag{2.12}$$

Then one of these frequency components, called Intermediate Frequency (IF), is selected by a filter, usually the one at $f_{IF} = f_{in} - f_{lo}$.

SAMPLER BASED, where the signal to be acquired is sampled according to the LO frequency. The LO output is sharpened, in order to form a train of pulses, and exploited to synchronize a sampler (e.g., sampling diodes) that captures a time sample of the signal to be acquired. A diagram of the system is reported in **Fig. 2.5b**. The resulting signal (s_{out}) is a multiplication of the signal to be acquired (s_{in}) by a pulse train:

$$\begin{aligned} s_{out}(t) &= s_{in}(t) \cdot \sum_k \delta(t - kT) \\ &= \sum_k s_{in}(t - kT) \end{aligned} \quad , \tag{2.13}$$

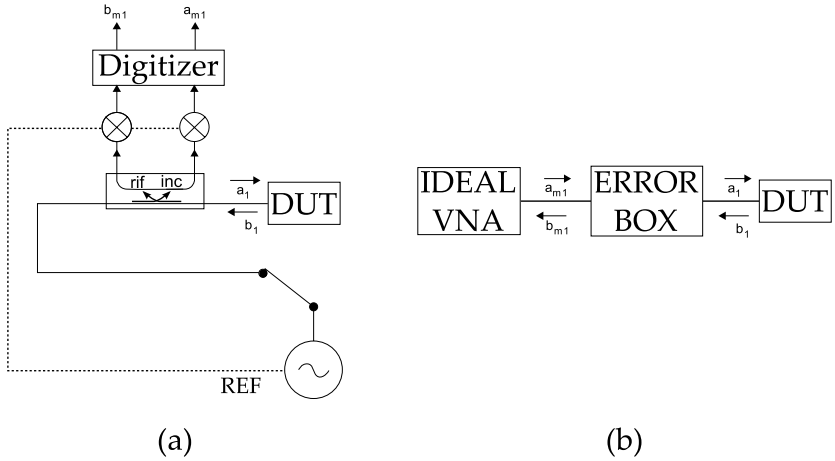

Fig. 2.6 One-port VNA block diagram (a) and the error box approach representation(b).

where k is a natural number and T the period of the LO signal. In the frequency domain the output signal (s_{out}) is the input signal (s_{in}) repeated and folded down in the Nyquist band (i.e., $1/2T$). So the lower frequency component (at IF) is selected and acquired by a filter.

Another design choice is the possibility to use one LO to feed all the four acquisition channels (one for each incident and reflected wave at the two ports) or use one LO for each acquisition channel. The first solution can introduce some leakage between the channels, thus decreasing the channel-to-channel isolation, but the latter is very expensive.

The signal at the IF can be acquired by using an Analog-Digital Converter (ADC); the speed of the ADC depends on the IF selected, an higher IF leads to less self-conversion noise problems [9] but requires a more complex ADC.

Also it is necessary to filter the signal, reducing noise, and to eliminate aliases and other know interferers; this can be done with analog filters or digitally after the ADC.

2.1.4 Calibration Technique

Compensating VNA measurements is crucial. Considering the one-port VNA in **Fig. 2.6a**, it is necessary to reconstruct the DUT-quantities starting from the acquired ones.

The aim is to relate the measured incident and reflected waves (a_m and b_m) with the incident and reflected wave (a_1 and b_1) at the DUT section. If all the acquisition system is considered linear, a simple error model can be developed:

$$\begin{bmatrix} b_1 \\ a_1 \end{bmatrix} = \begin{bmatrix} d_{11} & d_{12} \\ d_{21} & d_{22} \end{bmatrix} \cdot \begin{bmatrix} a_{m1} \\ b_{m1} \end{bmatrix} = \underline{\underline{D}} \cdot \begin{bmatrix} a_{m1} \\ b_{m1} \end{bmatrix} \quad . \tag{2.14}$$

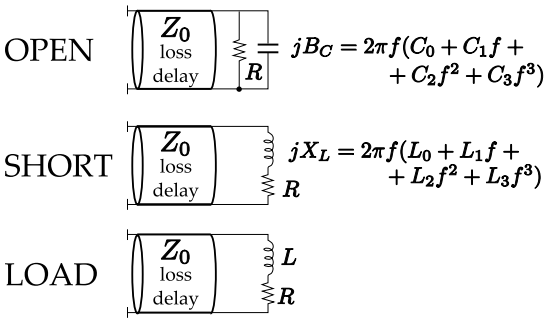

Fig. 2.7 Open, Short, and Load models commonly implemented in VNAs firmware.

The error matrix $\underline{\underline{D}}$ can be expressed as the S-parameter matrix of a fictitious network connected between an ideal VNA and the DUT (the error box in **Fig. 2.6b**):

$$\begin{bmatrix} b_{m1} \\ a_1 \end{bmatrix} = \begin{bmatrix} e_{11} & e_{12} \\ e_{21} & e_{22} \end{bmatrix} \cdot \begin{bmatrix} a_{m1} \\ b_1 \end{bmatrix} = \underline{\underline{E}} \cdot \begin{bmatrix} a_{m1} \\ b_1 \end{bmatrix} \quad . \tag{2.15}$$

So a measured reflection coefficient (Γ_m) is related to the DUT reflection coefficient (Γ) by [5]:

$$\Gamma_{\mathrm{m}} = \frac{b_{m1}}{a_{m1}} = \frac{e_{11} - (e_{11}e_{22} - e_{12}e_{21})\Gamma}{1 - e_{22}\Gamma} = \frac{e_{11} - \Delta\Gamma}{1 - e_{22}\Gamma} \quad , \tag{2.16}$$

$$\Gamma = \frac{b_1}{a_1} = \frac{\Gamma_m - e_{11}}{e_{22}\Gamma_m - \Delta} \quad . \tag{2.17}$$

Thus, to achieve the DUT reflection coefficient (Γ) three correction terms are needed: e_{11}, e_{22} and Δ. It is possible to obtain these terms by measuring three different known reflection coefficients (Γ_s^i). In particular, three different calibration standards, previously characterized in a very accurate way, are exploited.

Rewriting equation (**2.17**) as:

$$e_{11} + e_{22}\Gamma\Gamma_m - \Delta\Gamma = \Gamma_m \quad , \tag{2.18}$$

the value of the correction terms can be achieved by exploiting a system of three linear equations:

$$\begin{bmatrix} 1 & \Gamma_s^1\Gamma_m^1 & -\Gamma_s^1 \\ 1 & \Gamma_s^2\Gamma_m^2 & -\Gamma_s^2 \\ 1 & \Gamma_s^3\Gamma_m^3 & -\Gamma_s^3 \end{bmatrix} \begin{bmatrix} e_{11} \\ e_{22} \\ \Delta \end{bmatrix} = \begin{bmatrix} \Gamma_m^1 \\ \Gamma_m^2 \\ \Gamma_m^3 \end{bmatrix} \quad , \tag{2.19}$$

Different standards can be exploited. The older, and most used, one-port calibration technique uses a Short, an Open and a Load [10] and is called SOL.

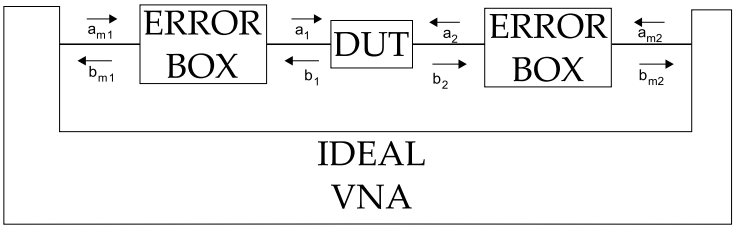

Fig. 2.8 Error Box Approach diagram for a two-port VNA.

Clearly it is impossible to create an ideal standard, in particular the frequency behavior of these devices is not ideal, so it is necessary to develop an electrical model to describe the response of the standards as a function of the frequency. The most common models, already implemented in VNA firmware, are reported in **Fig. 2.7**. Non-ideal frequency dependencies are expressed with simple polynomial expressions and extracted with fitting.

With two-ports VNAs (**Fig. 2.1**) the approach is similar: instead of one error box there are two error boxes (**Fig. 2.8**), one for each port. It is worth noticing that in addition to the linearity assumption, the two VNA measurement ports are considered uncoupled: no internal leakage between port 1 and 2 is taken into account. The error boxes are:

$$\begin{bmatrix} b_{m1} \\ a_1 \end{bmatrix} = \begin{bmatrix} e_{11}^A & e_{12}^A \\ e_{21}^A & e_{22}^A \end{bmatrix} \cdot \begin{bmatrix} a_{m1} \\ b_1 \end{bmatrix} = \underline{\underline{E_A}} \cdot \begin{bmatrix} a_{m1} \\ b_1 \end{bmatrix} \quad , \tag{2.20}$$

$$\begin{bmatrix} b_{m2} \\ a_2 \end{bmatrix} = \begin{bmatrix} e_{11}^B & e_{12}^B \\ e_{21}^B & e_{22}^B \end{bmatrix} \cdot \begin{bmatrix} a_{m2} \\ b_2 \end{bmatrix} = \underline{\underline{E_B}} \cdot \begin{bmatrix} a_{m2} \\ b_2 \end{bmatrix} \quad , \tag{2.21}$$

or in a more convenient cascade matrix representation:

$$\begin{bmatrix} b_{m1} \\ a_{m1} \end{bmatrix} = \begin{bmatrix} t_{11}^A & t_{12}^A \\ t_{21}^A & t_{22}^A \end{bmatrix} \cdot \begin{bmatrix} b_1 \\ a_1 \end{bmatrix} = \underline{\underline{T_A}} \cdot \begin{bmatrix} b_1 \\ a_1 \end{bmatrix} \quad , \tag{2.22}$$

$$\begin{bmatrix} b_{m2} \\ a_{m2} \end{bmatrix} = \begin{bmatrix} a_2 \\ b_2 \end{bmatrix} \cdot \begin{bmatrix} t_{11}^B & t_{12}^B \\ t_{21}^B & t_{22}^B \end{bmatrix} = \underline{\underline{T_B}} \cdot \begin{bmatrix} b_2 \\ a_2 \end{bmatrix} \quad . \tag{2.23}$$

Referring to **Fig. 2.8** the relationship between the measured and DUT quantities is:

$$\begin{aligned} \begin{bmatrix} b_{m1} \\ a_{m1} \end{bmatrix} &= \underline{\underline{T_A}} \cdot \underline{\underline{T_{DUT}}} \cdot \underline{\underline{T_B}}^{-1} \cdot \begin{bmatrix} a_{m2} \\ b_{m2} \end{bmatrix} \\ &= \underline{\underline{T_M}} \cdot \begin{bmatrix} a_{m2} \\ b_{m2} \end{bmatrix} \end{aligned} \quad . \tag{2.24}$$

The matrix $\underline{\underline{T_M}}$ is achieved with two sets of different measurements, where the source is switched between the two ports:

$$\begin{bmatrix} a_{m1}^{s1} & a_{m1}^{s2} \\ b_{m1}^{s1} & b_{m1}^{s2} \end{bmatrix} = \underline{\underline{T_M}} \cdot \begin{bmatrix} a_{m2}^{s1} & a_{m2}^{s2} \\ b_{m2}^{s1} & b_{m2}^{s2} \end{bmatrix} \Rightarrow \underline{\underline{M_1}} = \underline{\underline{T_M}} \cdot \underline{\underline{M_2}} \quad , \tag{2.25}$$

and:

$$\underline{\underline{T_M}} = \underline{\underline{M_1}} \cdot \underline{\underline{M_2}}^{-1} \quad , \tag{2.26}$$

where the quantities with the apex "s1" are measured with the source connected at port 1 and the quantities with the apex "s2" are measured with the source connected at port 2.

The other quantities needed to achieve the DUT parameters ($\underline{\underline{T_{DUT}}}$) are the two error matrices $\underline{\underline{T_A}}$ and $\underline{\underline{T_B}}$,:

$$\underline{\underline{T_{DUT}}} = \underline{\underline{T_A}}^{-1} \cdot \underline{\underline{T_{DUT}}} \cdot \underline{\underline{T_B}} \quad . \tag{2.27}$$

This error model is called eight-terms error model [11].

The techniques exploited for the identification of the two error boxes, like in the one port case, are based on the measurements of already well characterized devices. The most important techniques are:

THRU-REFLECT-LINE (TRL), this technique uses a direct connection between the ports (Thru), a longer connection between the ports (Line) and a reflection standard, that can also be unknown. This technique is very powerful because requires few information about the standards [12] [13]: the only information that must be known about the line is the characteristic impedance, that automatically becomes the reference impedance of the VNA. Moreover, if the thru is ideal (zero length), the reflection standard could be unknown, thus in this case the line reference impedance is the only parameter required to obtain a successful calibration. This makes the TRL calibration very traceable to the mechanical dimension of the line, so all the metrology labs use a set of lines as their primary microwave standards. One of the main drawbacks of the TRL technique is the relative small bandwidth: if the line-resonance phenomenon occurs the calibration fails, so for broad-band calibration a Multiline TRL calibration should be used [14].

LINE REFLECT MATCH (LRM), this technique requires a line and a reflective standard as the TRL but requires a "match" (a load at the reference impedance) instead of the thru. The reference impedance of the VNA is set by the load, and broadband high-performance is achievable if load with good frequency behavior is used.

SHORT OPEN LOAD THRU (SOLT), this is the oldest and the most used technique, because it is very simple and easy to manage, as the required standards are commercially available. However a lot of measurements are needed and all the standards need to be fully characterized.

SHORT OPEN LOAD RECIPROCAL (SOLR), this calibration technique can be used if the two ports are far apart. A fully known thru is difficult to obtain or the ports have a different angles (a bended ideal thru is impossible to obtain at microwave frequencies). To substitute it, a reciprocal (i.e., $S_{12} = S_{21}$) network can be used. The only draw-back

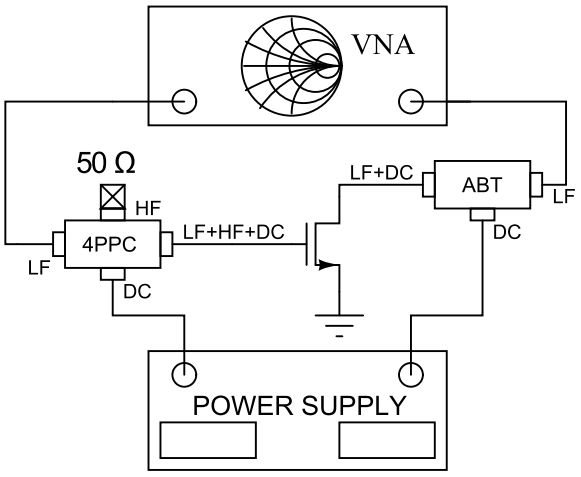

Fig. 2.9 Small-signal low-frequency characterization setup.

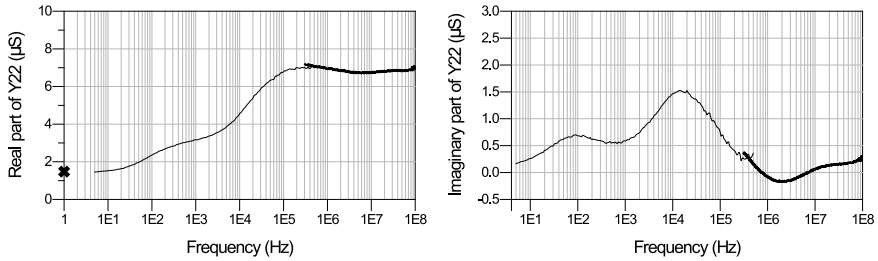

Fig. 2.10 Real (left) and Imaginary (right) part of Y_{22}, measured on a GaN 8x75-µm, biased in $V_{DS} = 20\ V, I_D = 200\ mA$. The frequency band [5 Hz – 400 kHz] (thin lines) was measured exploiting the setup in **Fig. 2.9**, the frequency band [200 KHz – 100 MHz] (thick lines) was measured exploiting a commercial setup.

is that, like in the SOLT technique, all the one-port standards must be perfectly known.

2.2 LOW FREQUENCY DISPERSIVE PHENOMENA CHARACTERIZATION

Using the setup represented in **Fig. 2.9** several Gallium-Arsenide (GaAs) and Gallium-Nitride (GaN) transistors have been characterized: small-signal S-parameter measurements were carried out starting from few hertz up to tens of megahertz. The typical response is reported in **Fig. 2.10** (i.e., the figure represents the real and imaginary parts of the Y_{22} parameter of a GaN transistor, periphery 8x75 µm, biased in $V_D = 20\ V$, $I_D = 200\ mA$). The strange sequence of peaks and valleys are associated to traps [15], but even if several attempts have been made to correlate these phenomena to the device physics [16], a clear explanation has not been found at the time.

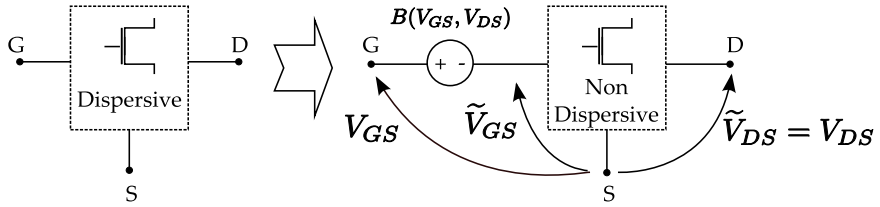

Fig. 2.11 Diagram of the equivalent voltage approach. Dispersive device is seen as a non-dispersive device with an equivalent voltage source in series to the gate port.

In the first part of this section an attempt to find a correlation between trapping phenomena and small-signal parameters low-frequency deviations will be reported. Using the presented formulation, some considerations about the output conductance deviations will be drawn. In the second part of this section an investigation on low-frequency dispersion modelling will be reported.

2.2.1 Trapping Effects in Small-Signal Parameters

In the following analysis we will make two basic assumptions:

SMALL-SIGNAL, the excursion of the exciting signals are so reduced that the behavior of the device is a linear function of the exciting signals.

GATE BACK-GATING, traps modulate the device control voltage (V_{GS} for a FET). A filled trap reduces the effective control voltage, an empty trap does not alter device behavior [17], [18] (the approach could be extended also to V_{DS}, with minimum efforts, if needed).

Let us consider an ideal intrinsic field-effect transistor low-frequency response, where capacitive and inductive phenomena are negligible due to the low frequency operation. A purely algebraic function without any memory effect (f_{ID}) can be assumed between the currents and the voltages:

$$I_D(t_0) = f_{ID}\left(V_{GS}(t_0), V_{DS}(t_0)\right) \quad , \tag{2.28}$$

so the drain current (I_D) at the time t_0 is a nonlinear function of the gate and drain voltages (V_{GS} and V_{DS}) at the time t_0. Due to low-frequency dispersive effects this relationship is not valid, as some memory effects are introduced.

Following the approach reported in [19] the dispersive effects can be described by an equivalent voltage. So equation (**2.28**) becomes:

$$I_D(t_0) = f_{ID}\left(V_{GS}(t_0) + B\left(V_{GS}([0,t_0]), V_{DS}([0,t_0])\right), V_{DS}(t_0)\right) \quad , \tag{2.29}$$

where $B\left(V_{GS}([0,t_0]),V_{DS}([0,t_0])\right)$ is an equivalent voltage, function of the evolution of gate and drain voltages up to t_0. The approach is described in **Fig. 2.11**.

Now we are interested to find the effects of low-frequency dispersion on small signal parameters, in particular:

$$g_m = \left.\frac{\partial I_D}{\partial V_{GS}}\right|_{V_{DS}=V_{DS_0}} \quad , \tag{2.30}$$

and

$$g_{ds} = \left.\frac{\partial I_D}{\partial V_{DS}}\right|_{V_{GS}=V_{GS_0}} \quad . \tag{2.31}$$

So the equivalent drain ($\tilde{V}_{DS}$) and gate ($\tilde{V}_{GS}$) voltages can be defined as:

$$\tilde{V}_{GS}(t) = V_{GS}(t) - B(V_{GS}(t),V_{DS}(t)) \quad , \tag{2.32}$$

$$\tilde{V}_{DS}(t) = V_{DS}(t) \quad , \tag{2.33}$$

and substituting in equation (**2.29**) we obtain:

$$I_D(t_0) = f_{ID}\left(\tilde{V}_{GS}(t),\tilde{V}_{DS}(t)\right) \quad , \tag{2.34}$$

where f_{ID} is still a nonlinear function without memory: the memory is taken into account by the equivalent voltage source B.

Let us now calculate g_m, equation (**2.30**) can be written as:

$$g_m = \frac{\partial I_D}{\partial V_{GS}} = \frac{\partial I_D}{\partial \tilde{V}_{GS}}\frac{\partial \tilde{V}_{GS}}{\partial V_{GS}} + \frac{\partial I_D}{\partial \tilde{V}_{DS}}\frac{\partial \tilde{V}_{DS}}{\partial V_{GS}} \quad , \tag{2.35}$$

where the chain rule [20] has been applied. Now we can analyze each term:

$$\frac{\partial I_D}{\partial \tilde{V}_{GS}}\frac{\partial \tilde{V}_{GS}}{\partial V_{GS}} = g_{m\,ID}\left(1 - \frac{\partial B}{\partial V_{GS}}\right) \quad , \tag{2.36}$$

where $g_{m\,ID}$ (i.e., the high-frequency trans-conductance) is a real number because I_D is a function of $\tilde{V}_{GS}$ without memory.

The other term instead is null:

$$\frac{\partial \tilde{V}_{DS}}{\partial V_{GS}} = 0 \Rightarrow \frac{\partial I_D}{\partial \tilde{V}_{DS}}\frac{\partial \tilde{V}_{DS}}{\partial V_{GS}} = 0 \quad , \tag{2.37}$$

so we can write g_m as:

$$g_m = g_{m\,ID}\left(1 - \frac{\partial B}{\partial V_{GS}}\right) \quad . \tag{2.38}$$

We want to investigate the frequency behavior of this parameter, so we can express g_m as a function of the frequency:

$$g_m = g_{m\,ID}\left(1 - \frac{\partial B}{\partial V_{GS}}\right) \overset{\mathcal{F}}{\Rightarrow} g_m(\omega) = g_{m_{ID}}(1 - b_{ds}(\omega)) \quad , \tag{2.39}$$

where $\mathcal{F}$ stands for the Fourier transform and $b_m(\omega)$ takes into account the low-frequency dispersive effects. It is a complex function of the fre-

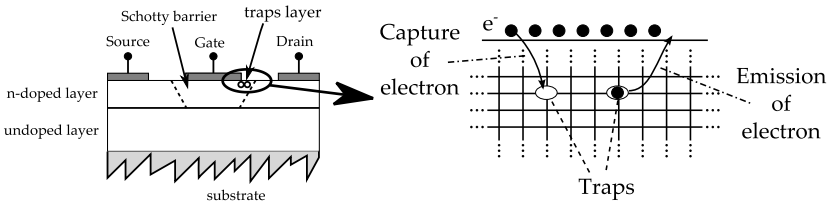

Fig. 2.12 Basic structure of a HEMT (left) and diagram of capture and emission mechanism.

quency of the excitation signal (i.e., the angular frequency ω) because B is a function with memory.

A similar approach can be applied to g_{ds}:

$$g_{ds} = \frac{\partial I_D}{\partial V_{DS}} = \frac{\partial I_D}{\partial \tilde{V}_{GS}} \frac{\partial \tilde{V}_{GS}}{\partial V_{DS}} + \frac{\partial I_D}{\partial \tilde{V}_{DS}} \frac{\partial \tilde{V}_{DS}}{\partial V_{DS}} \quad , \tag{2.40}$$

the first term can be written as:

$$\frac{\partial I_D}{\partial \tilde{V}_{GS}} \frac{\partial \tilde{V}_{GS}}{\partial V_{DS}} = -g_{m_{ID}} \frac{\partial B}{\partial V_{DS}} \overset{\mathcal{F}}{\Rightarrow} -g_{m_{ID}} b_{ds}(\omega) \quad , \tag{2.41}$$

where $b_{DS}(\omega)$ takes into account the low frequency dispersion, and as $b_m(\omega)$ is a function of frequency. The other term is:

$$\frac{\partial I_D}{\partial \tilde{V}_{DS}} \frac{\partial \tilde{V}_{DS}}{\partial V_{DS}} = g_{ds_{ID}} \cdot 1 = g_{ds_{ID}} \overset{\mathcal{F}}{\Rightarrow} g_{ds_{ID}} \quad , \tag{2.42}$$

where $g_{ds_{ID}}$ (i.e., the high-frequency output conductance) is a real number because I_D is a function of $\tilde{V}_{DS}$ without memory.

So in conclusion the small-signal parameters of interest are:

$$g_m = g_{m_{ID}}(1 - b_m(\omega)) \quad , \tag{2.43}$$

$$g_{ds} = g_{ds_{ID}} - g_{m_{ID}} b_{ds}(\omega) \quad , \tag{2.44}$$

where the two terms $b_m(\omega)$ and $b_{ds}(\omega)$ are:

$$b_m(\omega) = \mathcal{F}\left(\frac{\partial B}{\partial V_{GS}}\right) \quad , \tag{2.45}$$

$$b_{ds}(\omega) = \mathcal{F}\left(\frac{\partial B}{\partial V_{DS}}\right) \quad , \tag{2.46}$$

where $\mathcal{F}(x)$ is the Fourier transformation of x.

It is worth noticing that typically for a transistor both $g_{m_{ID}}$ and $g_{ds_{ID}}$ are positive.

We are now interested in finding the frequency behavior of these two parameters. First of all we suppose that the equivalent voltage B is somewhat directly related to the number of occupied traps; now we aim to find how the trap occupation state is modified by the exciting signal frequency.

Let us consider a layer of N traps (**Fig. 2.12**), all with the same characteristic. The function status f_T is the probability that one trap is occupied:

$$f_T = \frac{N_{OCC}}{N} \quad , \tag{2.47}$$

where N_{OCC} is the number of occupied traps. The variations of f_T are proportional to the capture rate (that is inversely proportional to the number of occupied traps) and inversely proportional to the emission rate (that is proportional to the number of traps occupied) [21]:

$$\frac{\partial f_T}{\partial t} = c_{TUN}(1 - f_T) + c(1 - f_T)\frac{n}{N} - e f_T \left(1 - \frac{n}{N}\right) \quad , \tag{2.48}$$

where:

- c_{TUN} is a tunneling capture coefficient;
- c is a capture coefficient;
- e is an emission coefficient;
- n/N is the conduction-band occupation factor.

In the barrier the conduction-band occupation factor is very small [21], so equation (**2.48**) becomes:

$$\frac{\partial f_T}{\partial t} = c_{TUN}(1 - f_T) - e f_T \quad . \tag{2.49}$$

In [21] equation (**2.49**) is exploited to analyze trap response to pulsed waveforms, instead in this thesis we are interested to find the variation of f_T for small perturbations of the voltages V_{DS} and V_{GS}.

Let us assume the two parameters c_{TUN} and e functions without memory of the voltages applied to the transistor [22], [23], [24], and [25]:

$$c_{TUN} = f_{c_{TUN}}(V_{GS}, V_{DS}) \quad , \tag{2.50}$$

$$e = f_e(V_{GS}, V_{DS}) \quad , \tag{2.51}$$

Due to the small-signal hypothesis, these two parameters can be divided in their mean values and perturbations:

$$c_{TUN} \simeq c_{TUN_0}^{GS} V_{GS_0} + \Delta c_{TUN}^{GS} v_{gs} + c_{TUN_0}^{DS} V_{DS_0} + \Delta c_{TUN}^{DS} v_{ds} \quad , \tag{2.52}$$

$$e \simeq e_0^{GS} V_{GS_0} + \Delta e^{GS} v_{gs} + e_0^{DS} V_{DS_0} + \Delta e^{DS} v_{ds} \quad , \tag{2.53}$$

where V_{GS_0} and V_{DS_0} are the mean values of the gate and drain voltages, instead v_{ds} and v_{ds} are their perturbations. $c_{TUN_0}^{GS}$, $c_{TUN_0}^{DS}$, e_0^{GS}, and e_0^{DS} are real coefficients that relate the mean value of the voltages to the mean value of the emission and capture coefficients. Instead Δc_{TUN}^{GS}, Δc_{TUN}^{DS}, Δe^{GS}, and Δe^{DS} are real coefficients that relate the perturbation of the capture and emission coefficient to the perturbation of drain and gate voltages.

Let us focus on the deviation of the transistor output conductance; as reported in equation (**2.31**) V_{GS} is considered constant at its mean value (V_{GS_0}) so the equations (**2.52**) and (**2.53**) become:

$$\begin{aligned} c_{TUN} &\simeq c_{TUN_0}^{GS} V_{GS_0} + c_{TUN_0}^{DS} V_{DS_0} + \Delta c_{TUN}^{DS} v_{ds} \\ &= c_{TUN_0} + \Delta c_{TUN}^{DS} v_{ds} \end{aligned} \quad , \tag{2.54}$$

$$e \simeq e_0^{GS} V_{G S_0} + e_0^{DS} V_{D S_0} + \Delta e^{DS} v_{ds} = e_0 + \Delta e^{DS} v_{ds} \quad . \tag{2.55}$$

where e_0 and c_{TUN_0} represent the mean value of c_{TUN} and e.

So equation (**2.49**) becomes:

$$\frac{\partial f_T}{\partial t} \simeq (c_{TUN\,0} + \Delta c_{TUN}^{DS} v_{ds})(1 - f_T) - (e_0 + \Delta e^{DS} v_{ds}) f_T \quad , \tag{2.56}$$

It is convenient to divide also the state function in its mean value plus the perturbation:

$$f_T = f_{T_0} + \Delta f_T \quad , \tag{2.57}$$

in particular its time derivative can be calculate as:

$$\frac{\partial f_T}{\partial t} = \frac{\partial f_{T_0}}{\partial t} + \frac{\partial \Delta f_T}{\partial t} = j\omega \Delta f_T \quad . \tag{2.58}$$

Indeed, as the excitements signals are time-sinusoids at the frequency ω, also Δf_T is a time-sinusoid at the frequency ω, because the system is considered linear. So equation (**2.56**) becomes:

$$j\omega \Delta f_T \simeq \left(c_{TUN\,0} + \Delta c_{TUN}^{DS} v_{ds}\right)\left[1 - \left(f_{T_0} + \Delta f_T\right)\right] - (e_0 + \Delta e^{DS} v_{ds})\left(f_{T_0} + \Delta f_T\right) \quad , \tag{2.59}$$

The last consideration is that at the equilibrium (i.e., DC) the capture and the emission process must balance:

$$0 = c_{TUN_0}(1 - f_{T_0}) - e_0 f_{T_0} \quad . \tag{2.60}$$

Now it is possible to put together in a system of equations (**2.59**) and (**2.60**). Then, neglecting the second order terms (e.g., $\Delta e^{DS} \cdot \Delta f_T \simeq 0$), we can obtain Δf_T as:

$$\Delta f_T = \frac{1}{\omega_p} \frac{\Delta c_{TUN}(1 - f_{T_0}) - \Delta e f_{T_0}}{1 + j\frac{\omega}{\omega_p}} v_{ds} \quad , \tag{2.61}$$

with:

$$\omega_p = \frac{1}{c_{TUN_0} + e_0} \quad . \tag{2.62}$$

As said previously the equivalent voltage B is directly related to the number of occupied traps, so for small perturbations:

$$B = k f_T = k f_{T_0} + k \Delta f_T \quad , \tag{2.63}$$

where k is a real constant, because the equivalent voltage is assumed to respond immediately to a variation of the numbers of traps. Moreover k is positive, because the occupied traps reduce the effective gate voltage [17].

Considering now $b_{DS}(\omega)$ we have :

$$b_{ds}(\omega) = \frac{\partial B}{\partial V_{DS}} = \frac{\partial (k f_{T_0} + k \Delta f_T)}{\partial (V_{D S_0} + v_{ds})} \cong \frac{(k \Delta f_T)}{v_{ds}} = k \frac{\Delta f_T}{v_{ds}} \quad , \tag{2.64}$$

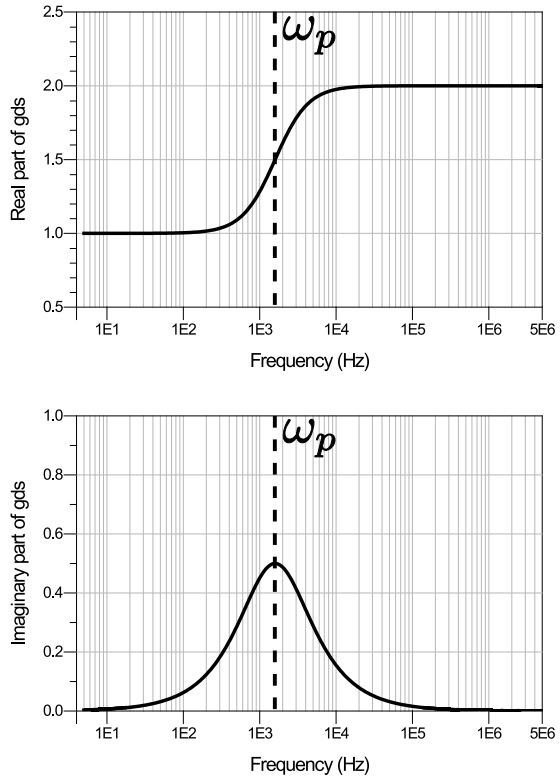

Fig. 2.13 Characteristic behavior of real and imaginary part of g_{ds} calculated using the formulation reported in equation (**2.66**).

where for small perturbations the derivative is approximated by the perturbation terms ratio. Substituting equation (**2.61**) we obtain:

$$b_{ds}(\omega) = k\left(\frac{1}{\omega_p}\frac{\Delta c_{TUN}\left(1-f_{T_0}\right)-\Delta e f_{T_0}}{1+j\frac{\omega}{\omega_p}}\right)v_{ds}/v_{ds} = k\left(\frac{1}{\omega_p}\frac{\Delta c_{TUN}\left(1-f_{T_0}\right)-\Delta e f_{T_0}}{1+j\frac{\omega}{\omega_p}}\right), \tag{2.65}$$

We can now achieve the small-signal output conductance of a dispersive transistor:

$$g_{ds} = g_{ds_{ID}} - g_{m_{ID}} k\left(\frac{1}{\omega_p}\frac{\Delta c_{TUN}\left(1-f_{T_0}\right)-\Delta e f_{T_0}}{1+j\frac{\omega}{\omega_p}}\right), \tag{2.66}$$

$$\omega_p = \frac{1}{c_{TUN_0}+e_0}. \tag{2.67}$$

where k, f_{T_0}, c_{TUN_0}, e_0, $g_{ds_{ID}}$, and $g_{m_{ID}}$ are real positive numbers, while Δc_{TUN}, and Δe are real numbers.

A graphical representation of the relations in equations (**2.66**) and (**2.67**) is reported in **Fig. 2.13**. The peak of the imaginary part and the variation of the real part are very similar to the measured ones reported in **Fig.**

2.10, so the results of the proposed approach reasonably reproduce the behavior of measured data (i.e., the different trapping mechanisms present in the measured data).

The following considerations can also be drawn:

THE MOST USEFUL INFORMATION IS THE PEAK FREQUENCY, (ω_p) because it depends only on two parameters (i.e., c_{TUN_0} and e_0). In particular it is also related to the main value of the state function (i.e., f_{T_0}), that is of great interest, as trapping effects are strongly related to it.

CAPTURE AND EMISSION PROCESS CANNOT BE SIMPLY DIVIDED, like in Transient Current Spectroscopy (TCS) [21] or Deep Level Transient Current Spectroscopy (DTCS) [25], [26]. The most useful experimental information, the peak of the imaginary part, corresponding to ω_p, is related to the sum of the capture and emission coefficients.

PEAK AMPLITUDE HAS A COMPLEX BEHAVIOUR, the peak value of the imaginary part of g_{ds} can be written as:

$$\Im\left(g_{ds}(\omega_p)\right) = \frac{1}{2} g_{m_{ID}} k(\Delta c_{TUN}(1 - f_{T_0}) - \Delta e f_{T_0}) \quad , \tag{2.68}$$

so it depends on a lot of unknown parameters (i.e., k, Δc_{TUN}, f_{T_0}, and Δe), that generally vary as a function of the operating condition (e.g., different bias points).

BOTH POSITIVE AND NEGATIVE BEHAVIORS ARE POSSIBLE, increments in the real part and positive peak of the imaginary part of g_{ds} are possible if b_{ds} is negative; decreases in the real part and negative peak of the imaginary part of g_{ds} are possible if b_{ds} is positive. The sign of b_{ds} is primarily influenced by Δc_{TUN} and Δe ($g_{m_{ID}}$, β and k are positive):

- If $\Delta c_{TUN} > 0$ and $\Delta e < 0$ (drain voltage enhances capture process and inhibits emission) the peak in the imaginary part of g_{ds} is positive. A trap with this behavior is likely to be near the gate structure of the transistor [28].
- If $\Delta c_{TUN} < 0$ and $\Delta e > 0$ (drain voltage enhances emission and inhibits capture process) the peak in the imaginary of g_{ds} is negative. A trap with this behavior is likely to be near the transistor channel [28]
- A mixed case, in which both the capture and the emission coefficients have the same sign, has no empirical evidence to our knowledge.

As an example of a very preliminary validation, these formulations have been exploited to investigate some small-signal low-frequency

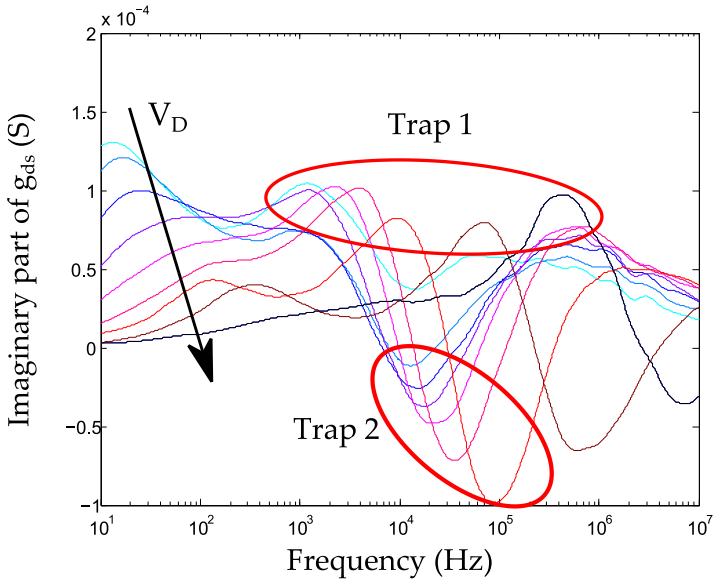

Fig. 2.14 Imaginary parts of g_{ds} measured on a 4x25-μm GaAs pHEMT in the frequency range 5 Hz – 10 MHz. Bias point: $V_G = -0.6\ V$, $V_D = [1\ V - 9\ V]$. Two peak series due to trapping phenomena "trap 1" and "trap 2 " are highlighted.

measurements; a set of output conductance were measured for a Triquint 4x25-μm GaAs pHEMT, biased with a gate voltage of -0.6 V and varying the drain voltage in the range 1 V – 9 V with 1 V step, the frequency band was 5 Hz – 10 MHz.

The measured imaginary part of g_{ds} is reported in **Fig. 2.14**, where two trapping phenomena are highlighted.

The first one "trap 1" has positive peaks, so it could be associated to a trap near the transistor gate, instead the second one "trap 2" has negative peaks, so it could be localized near the transistor channel.

An interesting phenomena, unexplained in literature [15], is the shift toward higher frequency of the peaks as a function of the drain voltage. Previous formulations, empirically obtained through physical simulation analyses [16], predict that the peak frequency should be inversely proportional to the drain voltage, so, at higher drain voltages, and so at higher voltages, the peak frequency should diminish. This is in contrast with the measured behavior, where (except for the first points of trap 1) the peak frequency increases as the drain voltage increases.

Using the formulation previously described this phenomena could be simply explained. Considering the case of a trap near the gate region (trap 1), the peak frequency in equation (**2.67**) can be expressed as a function of the capture coefficient and the state function:

$$\omega_p = \frac{f_{T_0}}{c_{TUN_0}} \quad . \tag{2.69}$$

The capture coefficient c_{TUN_0} can be assumed an increasing function of the drain voltage:

$$V_{DS} \uparrow \xrightarrow{\Delta C_{TUN}>0} c_{TUN_0} \uparrow \quad , \tag{2.70}$$

but also the emission coefficient is dependent on the drain voltage:

$$V_{DS} \uparrow \xrightarrow{\Delta e_0<0} e_0 \downarrow \quad , \tag{2.71}$$

so, the state function (f_{T_0}) is strongly dependent on the drain voltage, because if simultaneously the capture coefficient increases and the emission coefficient decreases, the mean number of occupied traps will grow rapidly.

Similar considerations can be made also for the negative peak cases (trap 2): when $\Delta C_{TUN} < 0$ and $\Delta e_0 > 0$. This time we express the peak frequency in equation (**2.67**) as a function of the emission coefficient and the state function:

$$\omega_p = \frac{1 - f_{T_0}}{e_0} \quad . \tag{2.72}$$

So, if the drain voltage increases the emission coefficient increases ($\Delta e_0 > 0$) and the capture coefficient decreases ($\Delta C_{TUN} < 0$), thus the traps will be emptied quickly: $1 - f_{T_0}$ will greatly increases.

To take into account these phenomena we will consider for the traps near the gate region (first case):

$$c_{TUN_0} \propto e^{V_{DS}} \quad , \tag{2.73}$$

$$f_{T_0} \propto e^{V_{DS}^2} \quad . \tag{2.74}$$

Instead in the second case, for traps near the channel we will consider:

$$e_0 \propto e^{V_{DS}} \quad , \tag{2.75}$$

$$1 - f_{T_0} \propto e^{V_{DS}^2} \quad . \tag{2.76}$$

So, for both the two cases it is possible to fit the peak frequency (ω_p) as a function of the drain voltage with the formulation:

$$w_p = \mathrm{a} \frac{\mathrm{e}^{bV_{ds}^2}}{e^{cV_{ds}}} \quad , \tag{2.77}$$

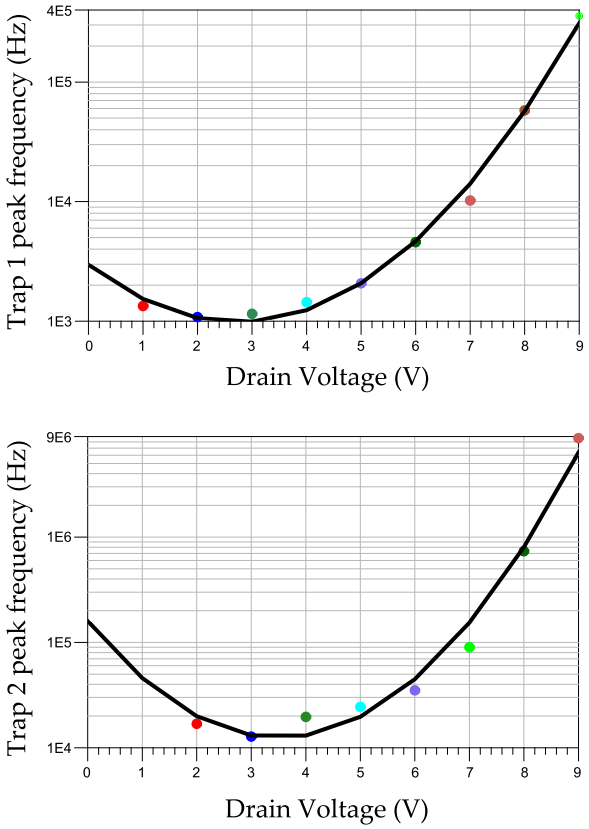

Fig. 2.15 Fitting of peak frequency (ω_p) relative to "trap 1" (upper) and "trap 2"(lower). The measurements (dots) are correctly fitted (solid line) by equation (**2.77**).

In the upper part of **Fig. 2.15** is reported the fitting of the "trap 1" peak frequency as a function of the drain voltage with the fitting parameters:

$$a = 2936, b = 0.15, c = 0.8 \quad . \tag{2.78}$$

The fitting is very good and also the initial decreasing is taken into account. In the lower part of **Fig. 2.15** instead the fitting of "trap 2" with the proposed formulation is reported; this time the model parameters are:

$$a = 1601 \cdot 10^3, b = 0.2, c = 1.45 \quad . \tag{2.79}$$

Also in this case the fitting is good, confirming that the proposed approach seems to be a reasonable way to analyze the low-frequency dispersion of a transistor. It is worth noting that these results are very interesting as it is the first time that this kind of behavior is explained, but it's clear that a more rigorous validation is still needed.

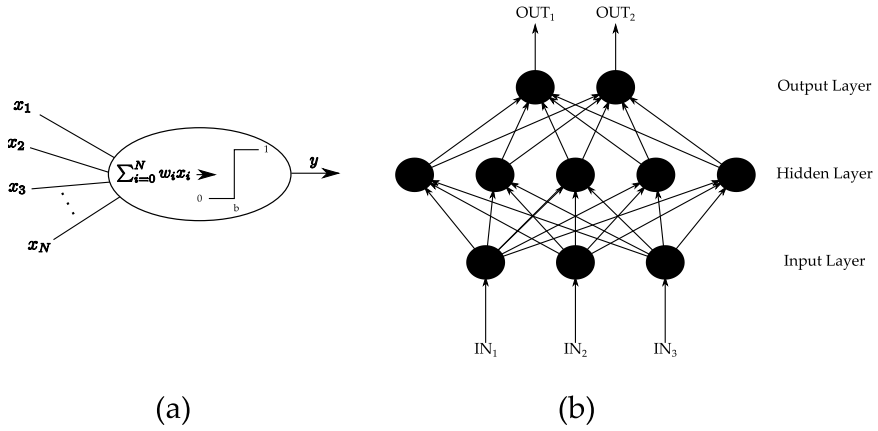

Fig. 2.16 Perceptron basic scheme (a) and MLP ANN (b) diagram, whit 3 inputs, one hidden layer of 5 neurons, and 2 outputs.

2.2.2 *Low-frequency dispersion modelling with artificial neural network.*

As seen in the previous section the behavior of low-frequency small-signal parameters is very complex, a lot of dependencies are involved, and often these dependencies are strongly non-linear.

If a model able to predict this behavior is needed, a possible approach could be the identification of an Artificial Neural Network (ANN). ANNs are computational models structured as a densely interconnected network of simple processing elements (artificial neurons) that mimic the computational properties of the brain (e.g., adaptivity, noise tolerance). In the following, a basic introduction on ANN is reported, a more detailed introduction on neural network theory can been found in [29].

The basic elements of an ANN are:

THE PERCEPTRON: it is the system formed by an artificial neuron and his inputs (**Fig. 2.16a**). The artificial neurons combine the various inputs (x_i) to form the "net" input v:

$$v = \sum_{i=1}^{N} w_i x_i \quad , \tag{2.80}$$

where N is the number of inputs and w_i the weight of the input x_i. The net input is then compared to a threshold:

$$y = \begin{cases} 1, & v > b \\ 0, & otherwise \end{cases} \quad , \tag{2.81}$$

where b is called "bias" and y is the perceptron output. In the network used in the following a soft transition is exploited using the hyperbolic tangent sigmoid transfer function, a good approximation of the hyperbolic tangent but more computationally efficient [30]:

$$v = \sum_{i=1}^{N} w_i x_i + b_i \quad , \tag{2.82}$$

$$y = tansig(\psi) \quad , \tag{2.83}$$

where b_i is the bias relative to the input x_i.

THE STRUCTURE: the ANN identified uses a *MultiLayer Perceptron* (MLP) architecture (**Fig. 2.16b**). It consists of three or more artificial-neuron layers, the first one has a number of neurons equal to the number of inputs, and it is called input layer. The middle layers have an arbitrary number of neurons, each neuron has its inputs connect to all the outputs of the previous layer neurons; these layers are called "hidden" layers. In particular the ANN identified has only a hidden layer.

The last layer is the output layer. It has a number of neurons equal to the number of outputs: the outputs of the neurons are connected to the ANN outputs, and the inputs of each neuron are connected to all the outputs of the previous layer neurons. This kind of network is known to be able to model even strongly non-linear functions, so it has been found suitable for the application of interest.

THE TRAINING ALGORITHM: the identification of the neural network consists in the identification of the weights (w_i) and the biases (b_i) for each neuron. A back-propagation algorithm is suitable for MLP networks. The term back-propagation refers to the way the error between the ANN outputs and the training data is propagated backward to the hidden layer, and finally to the input layer. A detailed description of the backpropagation algorithm is reported in [31]. The Back-Propagation ANNs (BPANNs) are versatile, and can be used for a lot of applications (e.g., modelling, classification, forecasting, data recognition). The main drawback of this algorithm is that the identified network can change as a function of the weights and biases starting values, often small random variables, due to local minima.

The aim of this analysis is to investigate if ANNs can be used for modelling the low-frequency small-signal dispersion. The network architecture selected is a MLP with one hidden layer, the optimization algorithm is a Levenberg–Marquardt back-propagation algorithm [32]. The training data are a set of small-signal low-frequency measurements on a Triquint 4x25-μm GaAs pHEMT biased with a gate voltage of 0.6 V and varying the drain voltage in the range 1 V – 9 V with 1 V step in the frequency band 5 Hz – 10 MHz. The network was trained in the range 5 Hz – 1 MHz, because the most important variations are present in this frequency range.

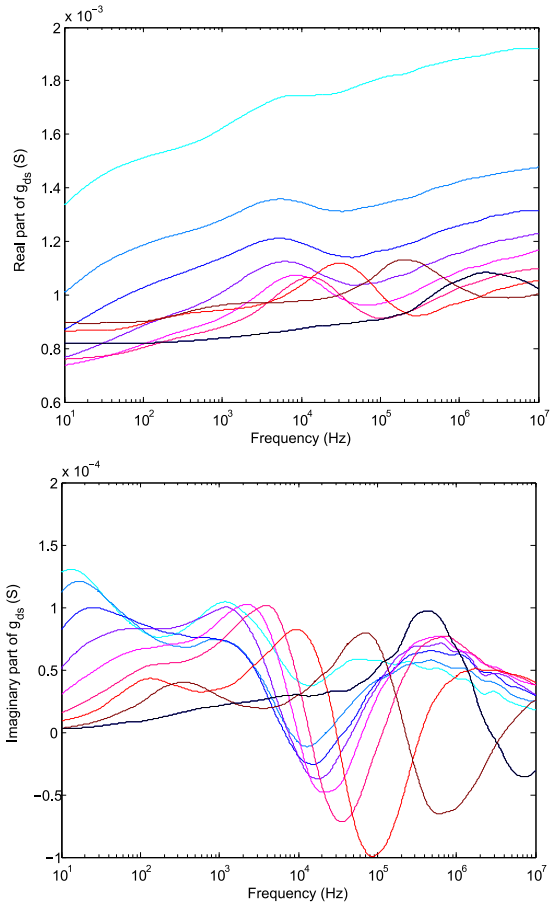

Fig. 2.17 Real (upper) and imaginary (lower) parts of g_{ds} measured on a 4x25-μm GaAs pHEMT in the frequency range 5 Hz – 10 MHz. Bias point $V_G = -0.6\ V$, $V_D = [1\ V - 9\ V]$.

In particular, it is considered the real and imaginary part of Y_{22}, reported in **Fig. 2.17**. The inputs of the network are the frequency and the bias drain voltages, the outputs are the real and imaginary part of Y_{22} of the considered transistor.

The only ANN variable of choice is the number of hidden neurons. In order to experimentally find its optimal value, a large set of ANNs (i.e., above one thousand), with various number of hidden layer neurons was identified. Then, for each neuron number, the mean and minimum errors were analyzed to find the optimum.

The first case considered is the interpolation, so the measurement at $V_{DS} = 6\ V$ was removed from the training set, and the predicted output for $V_{DS} = 6\ V$ was compared with the measured one in all the considered frequency band. The error (e) was defined as:

$$e = \left|\mathrm{x_{pred}} - \mathrm{x_{meas}}\right| \quad , \tag{2.84}$$

where x_{pred} is the ANN prediction and x_{meas} is the measurements.

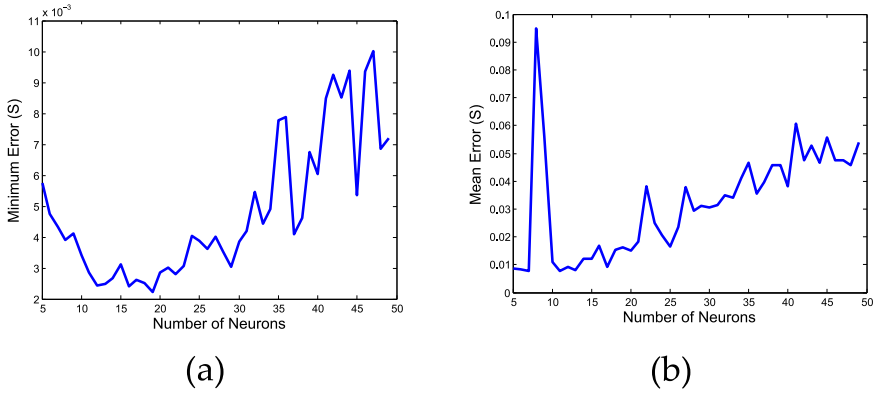

Fig. 2.18 Mean (a) and minimum (b) errors as a function of the number of middle layer neurons relative to the interpolation case study.

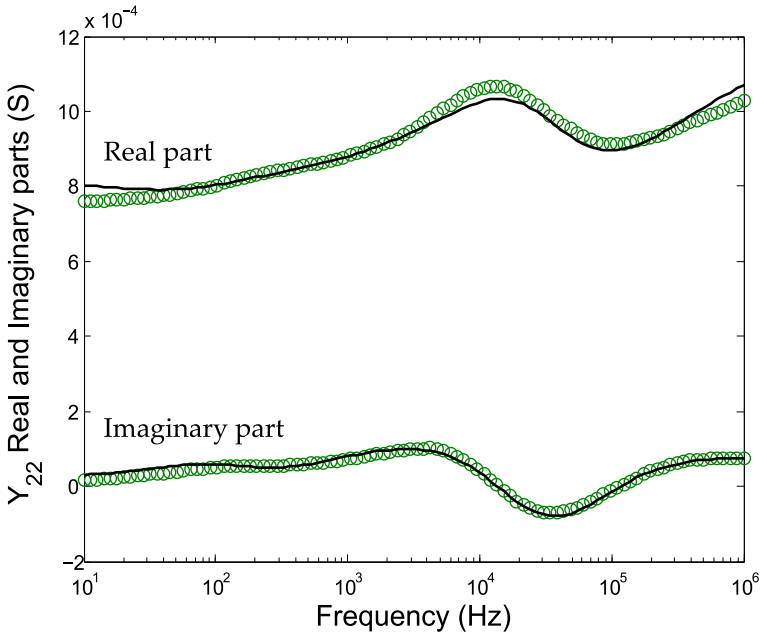

Fig. 2.19 Predictions of the identified ANN on real and imaginary parts of Y_{22} for the bias point $V_G = -0.6\ V$, $V_D = 6\ V$. The ANN predicts in a very accurate way the low frequency deviations.

The minimum (a) and the mean (b) errors as a function of number of neurons are reported in **Fig. 2.18**, it is clear that the optimal number of hidden layer neurons is between 10 and 22. The measured small-signal Y_{22}, real and imaginary part, are compared to the predicted ones by an ANN with the optimal number of hidden neurons (i.e., 19) in **Fig. 2.19**: the ANN is clearly able to correctly predict the measured data.

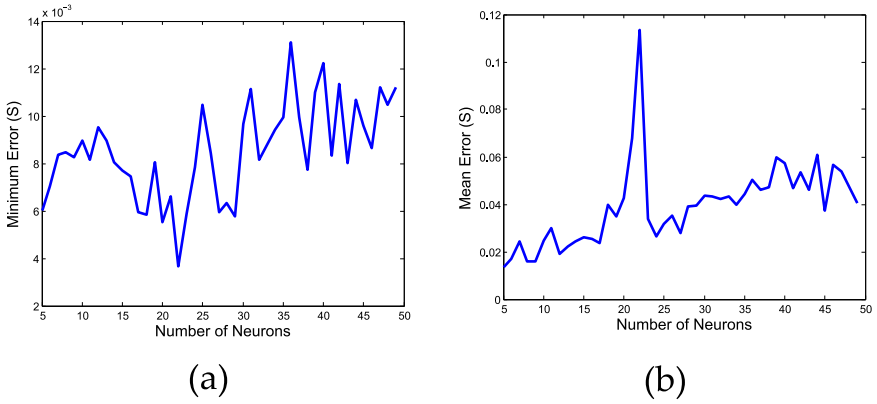

Fig. 2.20 Mean (a) and minimum (b) errors as a function of the number of middle layer neurons relative to the extrapolation case study.

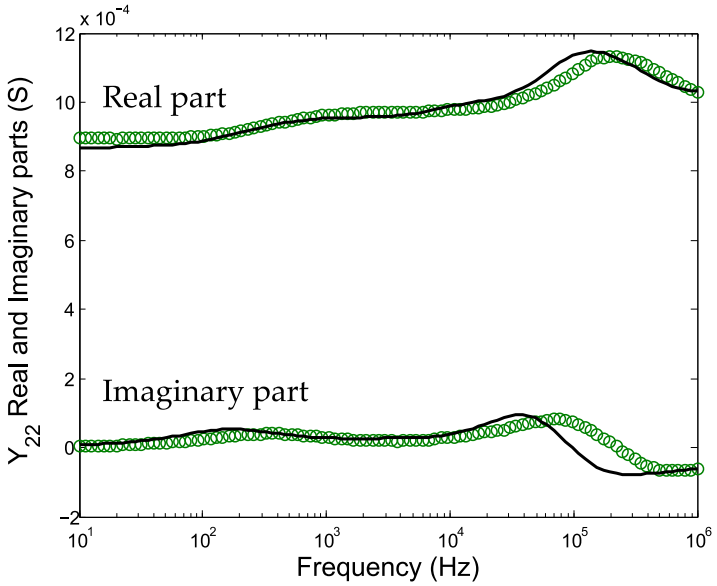

Fig. 2.21 Predictions of the identified ANN on real and imaginary parts of Y_{22} for the bias point $V_G = -0.6\ V$, $V_D = 9\ V$. The ANN predictions and the measurements are in good agreement.

A more challenging task is to predict the transistor response beyond the measured data set (i.e., extrapolation). So, this time, the measurement at $V_{DS} = 9\ V$ was removed from the training set, then the response of the ANN for this drain voltage was compared with the measured data in the entire frequency band. Like in the previous case, minimum (a) and mean (b) error is represented in **Fig. 2.20**. This time it is harder to identify an optimal range of number of neurons, but the previously adopted range (10 – 22 neurons) seems to be a good choice. An ANN with 22 hidden layer neuros was extracted and **Fig. 2.21** presents a comparison between the predicted and the measured small-signal low-frequency response. The predictions are still good, even if the accuracy is slightly worse than in the previous case.

Considering the overall complexity of the task, the presented approach gives very interesting results with reduced efforts: ANNs are able to accurately model a highly non-linear behavior, like low-frequency output conductance dispersion due to trapping effects.

2.3 CONCLUSION

In this section the VNA has been described: its architecture and its components have been reported, moreover different calibration techniques have been detailed.

In the second part of the chapter low-frequency dispersive phenomena have been analyzed with a simplified analytical formulation. This formulation allows to identify the causes of the deviations of the transistor measured parameters under low frequency operation. By adopting the described approach it is possible to identify which measured quantity gives more information about the observed phenomenon. This allows a more clear interpretation of the measured trends.

In the last part of the chapter, it has been investigated the use of an ANN to model the low-frequency output conductance of a microwave transistor. In particular, the extracted network has shown adequate performance both in interpolation and extrapolation tests.

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3 NOISE CHARACTERIZATION AND MODELING

The communications between humans or machines are made through signals. A signal can be defined as a variation of a physical phenomenon associated in some ways to an information.

Once transmitted, signals are always received with some form of degradation, mainly:

ATTENUATION, due to the propagation of the signal into the environment, like open-space geometrical attenuation or attenuation due to losses into a communication cable. If the attenuation is too strong the signal can't be received, thus the communication fails.

NOISE, due to fluctuations in the environment, like a conversation between two people interrupted by the passage of a car or a transmission between an earth station and a satellite disturbed by ionosphere scintillation. These fluctuations in the environment cause unpredictable modifications of the physical phenomenon exploited for the communication. If these modifications are too strong it is no more possible to extract the transmitted information, thus the communication fails.

In this chapter, after a brief introduction on noise in electronic devices with the related measurement systems, the most important electromagnetic simulation techniques will be reported. Successively, an innovative noise model and its related extraction procedure are presented [1]. Finally, a low-noise amplifier, designed exploiting the proposed model, is reported.

3.1 NOISE MEASUREMENTS

Electronic noise is a random fluctuation of an electronic signal. Noise is produced by several sources:

THERMAL NOISE (Johnson [2] or Nyquist [3] noise) is generated by random thermal agitation of the electrons.

FLICKER NOISE, it has a $1/f$ or "pink" power spectrum and is due to various causes, like channel impurities or generation–recombination of charges.

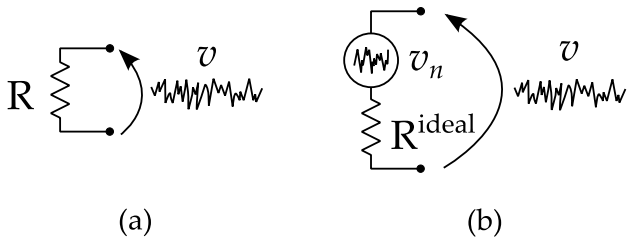

Fig. 3.1 Resistor generating thermal noise (a) and its equivalent circuit (b) where the noise source is treated separately.

SHOT NOISE, is originated by the fact that current is the flow of *discrete* electrons.

BURST NOISE, called also pop-corn noise, consists in step-like transitions between two voltage (or current) levels, at unpredictable times. The most common cause of this noise is random charge trapping and emission in defects of the semiconductor.

The thermal noise is the main noise source in microwave circuits, so generally all the other types of noise are treated in terms of an equivalent thermal noise [4].

Let us consider a resistor. Its electrons have a kinetic energy function of the temperature (T in kelvin degree). Thus the electrons move with a random motion, producing small voltage fluctuations at the resistor terminals (**Fig. 3.1a**). This voltage has a null mean value but its mean RMS value ($\overline{v_n^{RMS}}$) can be calculated using the Plank black-body radiation law [5]:

$$\overline{v_n^{RMS}} = \sqrt{\frac{4hfBR}{e^{hf/kT} - 1}} \quad , \tag{3.1}$$

where h is the Plank constant, k the Boltzmann constant, f is the center frequency of the bandwidth B, and R is the considered resistor resistance.

For frequencies up to some terahertz and temperature above 100 K $hf/kT \ll 1$ so the denominator of equation (**3.1**) can be substituted by its first order Taylor series expansion; this leads to:

$$\overline{v_n^{RMS}} = \sqrt{4kTBR} \quad . \tag{3.2}$$

So the noisy resistor in **Fig. 3.1a** can be separated in an ideal noiseless resistor plus a noise source v_n (**Fig. 3.1b**). In addition the maximum noise power that can be transferred to a load (available noise power) can be expressed as:

$$N = \frac{\left(\overline{v_n^{RMS}}\right)^2}{4R} = \frac{4kTBR}{4R} = kTB \quad , \tag{3.3}$$

where N is the available thermal noise power. It is worth noticing that the available noise power is not a function of the frequency, thus the thermal noise is called a "white" noise.

3.1.1 Noise Figure and Noise Parameters

Noise is ubiquitous in communications: each transmitted signal, in a circuit interconnection or in the air, is received with some noise added. If the received signal power is comparable to the noise power, it can be difficult to separate the meaningful information (i.e., the signal) from the noise, thus the communication can fail. So signal to noise ratio is a very important figure of merit of the quality of a received signal, it is defined as:

$$SNR = \frac{S}{N} \quad , \tag{3.4}$$

where S is the signal available power, and N is the noise available power.

Noise is somewhat related to the entropy (i.e., a measure of the disorder in a system), if another element is added to a system its entropy, and so the noise, can only increase, thus the signal to noise ratio decreases. The noise factor is the figure of merit of this degradation, it is defined as the ratio between the signal to noise ratio at the input and at the output:

$$F = \frac{SNR_{IN}}{SNR_{OUT}}\bigg|_{T=T_0} = \frac{\frac{S_{IN}}{N_{IN}}}{\frac{S_{OUT}}{N_{OUT}}}\bigg|_{T=T_0} \quad , \tag{3.5}$$

where SNR_{IN} is the signal (S_{IN}) to noise (N_{IN}) ratio at the input, SNR_{OUT} is the signal (S_{OUT}) to noise (N_{OUT}) ratio at the output and T_0 the temperature. As said before the signal to noise ratio is always degraded by a system, so for any real system $F > 1$.

Considering a generic two-ports with a noise source at temperature T_0 and a signal source whit S_{IN} available input power, its noise factor (F) can be written as:

$$F = \frac{\frac{S_{IN}}{N_{IN}}}{\frac{S_{OUT}}{N_{OUT}}}\bigg|_{T=T_0} = \frac{\frac{S_{IN}}{kT_0B}}{\frac{GS_{IN}}{GkT_0B + N_{ADD}}} = \frac{GkT_0B + N_{ADD}}{GkT_0B} \quad , \tag{3.6}$$

where G is the available power gain of the two-ports [4] and N_{ADD} the noise added by the two-ports.

When the temperature is the reference temperature (290 K) this definition for the noise figure is the one adopted by the IEEE [6].

Another noise parameter, directly derivable from the noise factor, is the noise figure (NF):

$$NF = 10 \log_{10} F \quad . \tag{3.7}$$

Another figure of merit, derived from the noise factor, is the effective input noise temperature (T_e). It can be seen as the additional source temperature that ensures the same available noise output power if the two-ports would be noiseless. So:

$$N_0 = GkT_0B + N_{ADD} = GkB(T_0 + T_e) \Rightarrow T_e = \frac{N_{ADD}}{GkB} \quad , \tag{3.8}$$

and:

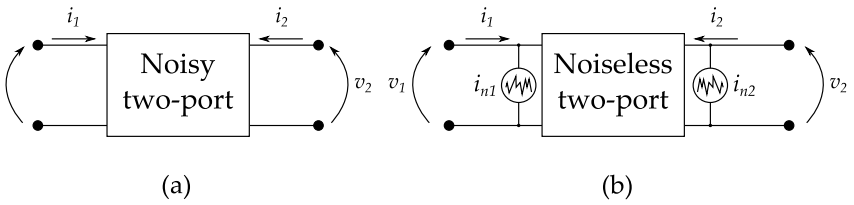

Fig. 3.2 Noisy two-ports (a) and its equivalent description as a noiseless two-ports with two correlated noise sources (b).

$$F = \frac{GkT_0B + N_{ADD}}{GkT_0B} = \frac{GkB(T_0 + T_e)}{GkT_0B} = \frac{T_0 + T_e}{T_0} = 1 + \frac{T_e}{T_0} \quad . \tag{3.9}$$

The noise behavior of a two-port network (**Fig. 3.2a**) can be described by two correlated noise sources connect to a noise-free equivalent of the two-port network [4], as represented in **Fig. 3.2b**. Other equivalent representations are also possible (Z, ABCD, etc.).
The matrix representation for the Y description is:

$$\begin{bmatrix} I_1 \\ I_2 \end{bmatrix} = \begin{bmatrix} Y_{11} & Y_{12} \\ Y_{21} & Y_{22} \end{bmatrix} \begin{bmatrix} V_1 \\ V_2 \end{bmatrix} + \begin{bmatrix} i_{n1} \\ i_{n2} \end{bmatrix} \Rightarrow \underline{I} = \underline{\underline{Y}} \cdot \underline{V} + \underline{I_n} \quad , \tag{3.10}$$

where i_{n1} and i_{n2} are the noise sources at the input and at the output, $\underline{\underline{Y}}$ the small-signal parameters matrix of the noiseless two-ports and $\underline{I_n}$ the noise vector.

As the noise sources i_{n1} and i_{n2} are random variables, it is convenient to convert this information into a deterministic number, like it has been done previously with the single noise voltage source. For this reason the noise correlation matrix is introduced: it is defined as the mean value of the multiplication of the noise vector for its complex-conjugate. For example the Y-parameters noise correlation matrix (i.e., $\underline{\underline{C_Y}}$) relative to equation (**3.10**) is:

$$\underline{\underline{C_Y}} = \overline{\begin{bmatrix} i_{n1} \\ i_{n2} \end{bmatrix} * \begin{bmatrix} i_{n1}^* & i_{n2}^* \end{bmatrix}} = \begin{bmatrix} \overline{i_{n1}i_{n1}^*} & \overline{i_{n1}i_{n2}^*} \\ \overline{i_{n2}^*i_{n1}} & \overline{i_{n2}i_{n2}^*} \end{bmatrix} \quad , \tag{3.11}$$

where with $\overline{x}$ denotes the mean value of x and x^* its complex-conjugate. This matrix has similar properties to small-signal parameter matrixes, so in a parallel combination of two networks the Y-parameter noise correlation matrix of the total network is the sum of the Y-parameter noise correlation matrix of each network.

So the noise behavior of a two-port network depends on four parameters, $C_{Y_{11}}$ and $C_{Y_{22}}$, both real and describing the mean square fluctuations of the noise sources and $C_{Y_{12}} = C_{Y_{22}}^*$, complex, describing the correlation existing between the noise sources [7]. In a similar way the noise factor of a two-port network depends on the source termination through a set of independent noise parameters [8]. The most used are:

MINIMUM NOISE FACTOR (F_{MIN}), minimum achievable noise factor of the considered two-port network.

OPTIMUM SOURCE REFLECTION COEFFICIENT (Γ_{OPT}), at this source termination F is equal to F_{MIN}. As the optimum source reflection coefficient is complex it counts as two parameters.

EQUIVALENT NOISE RESISTANCE (R_N), this parameter characterizes how rapidly the noise factor F diverges from F_{MIN} as the source reflection coefficient (Γ) diverges from Γ_{OPT}.

The noise factor can be written as a function of the source reflection coefficient (Γ) [4]:

$$F = F_{MIN} + 4\frac{R_N}{Z_0}\frac{|\Gamma - \Gamma_{OPT}|^2}{|1 + \Gamma_{OPT}|^2(1 - |\Gamma|^2)} \quad , \qquad (3.12)$$

where Z_0 is the reference impedance.

A three-dimensional representation of equation (**3.12**) is reported in **Fig. 3.3**, the noise factor F is a paraboloid centered in Γ_{OPT} and with vertex F_{MIN}.

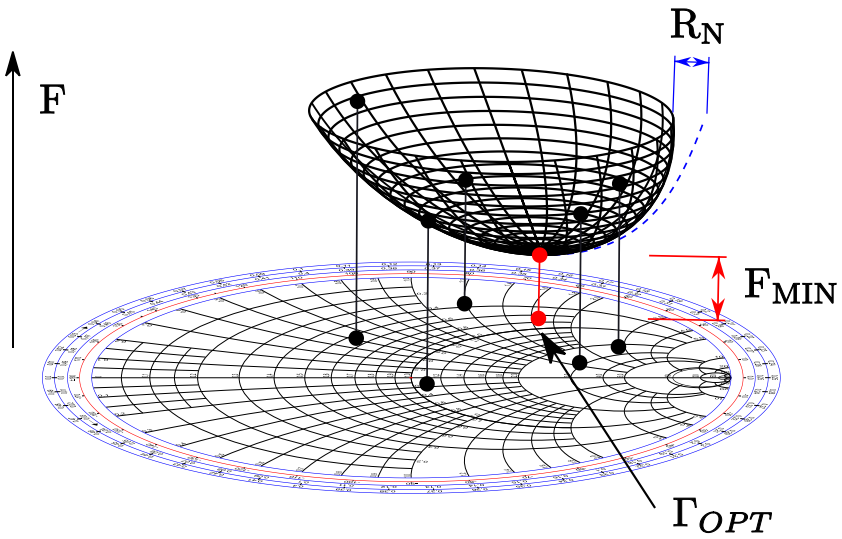

Fig. 3.3 Three-dimensional representation of noise factor as a function of the source reflection coefficients.

3.1.2 *Noise Measurements*

Source-pull techniques are exploited to obtain the noise parameters of a two-port network [9]: the source termination is varied and for each point the noise factor is measured. Two main techniques are exploited to measure the noise parameters.

THE Y-FACTOR TECNIQUE, where the noise factor is obtained from two measurements with two different noise powers (N_{HOT} and N_{COLD}) corresponding to two different temperatures (T_{HOT} and T_{COLD}):

$$N_{HOT} = kBG(T_{HOT} + T_e) \quad , \tag{3.13}$$

$$N_{COLD} = kBG(T_{COLD} + T_e) \quad , \tag{3.14}$$

The parameter to be measured is the Y-factor, defined as the ratio between N_{HOT} and N_{COLD}:

$$Y = \frac{N_{HOT}}{N_{COLD}} = \frac{T_{HOT} + T_e}{T_{COLD} + T_e} \quad , \tag{3.15}$$

it is now possible to achieve the effective input noise temperature T_e and so the noise factor F (see equation (**3.9**)):

$$T_e = \frac{T_{HOT} - Y\,T_{COLD}}{Y - 1} \Rightarrow F = 1 + \frac{T_{HOT} - Y\,T_{COLD}}{T_0\,(Y - 1)} \quad . \tag{3.16}$$

An avalanche diode is often used as noise source [10]: when the diode is not biased (cold) there is only some thermal noise at its output, instead when the diode is polarized near the breakdown region it generates a lot of noise (hot). This "hot" state is quantified by the Excess Noise Ratio (ENR):

$$ENR = 10\log_{10}\left(\frac{T_{HOT} - T_{COLD}}{T_0}\right) \quad . \tag{3.17}$$

Naturally also additional noise coming from the interconnections and the receiver input circuitry is measured in this way, but it can be compensated by performing additional measurements: one with a thru connected in place of the DUT and one connecting the noise source directly to the receiver.

THE COLD-SOURCE TECHNIQUE, the main draw-back of the Y-factor technique is that two measurements, and the relative change of the noise source status, are required. So the Y-factor techniques could be quite slow, and not suitable for noise-parameter extraction, where a lot of measurements are needed. The cold-source technique overcomes these problems, performing a single measurement of the output noise power to extract T_e, according to equations (**3.8**) and (**3.9**). In order to correctly achieve the effective input noise temperature both the device available gain G and the receiver gain-bandwidth product must be previously determined. Other calibration steps are also necessaries to identify the noise added by the interconnections and the receiver (for further details see [11]).
In conclusion the cold-source technique has a longer and more complex calibration than the Y-factor technique but it is overall faster and preferable if a lot of measurements must be carried out.

Once obtained a large set of noise factors as a function of the source reflection coefficient (minimum 4 but to minimize the uncertainty a lot more are used) the four noise parameters can be obtained through fitting of the measurement data. Several techniques are present in literature [12, 13, 14, 15, 16].

3.2 ELECTROMAGNETIC ANALYSES

In theory, the electromagnetic properties of every structure can be described by using the Maxwell equations:

$$\nabla \times \vec{E} = -\frac{\partial \vec{B}}{\partial t} \quad , \tag{3.18}$$

$$\nabla \times \vec{H} = \vec{J} + \frac{\partial \vec{D}}{\partial t} \quad , \tag{3.19}$$

$$\nabla \cdot \vec{D} = \rho \quad , \tag{3.20}$$

$$\nabla \cdot \vec{B} = 0 \quad , \tag{3.21}$$

with the associated constitutive equations:

$$\vec{B} = \mu \vec{H} \quad , \tag{3.22}$$

$$\vec{D} = \epsilon \vec{E} \quad . \tag{3.23}$$

So every problem concerning the computation of electrical and magnetic fields, from antenna analyses or microwave circuit design to the most basic circuits, theoretically could be solved using the equations above.

Nevertheless, to be able to predict the behavior of a real structure is a far cry from to have a complete set of laws: for realistic problems, approximations are usually required because of the high complexity of the real environment.

The approximation of Maxwell's equations is known as Computational ElectroMagnetics (CEM).

Various types of CEM techniques have been developed and two main groups can be identified [17]:

FULL-WAVE methods approximate the Maxwell equations numerically. The most important techniques are:

- Method of Moments (MoM) [18];
- Finite Elements Method (FEM) [19];
- Finite Differences in Time Domain (FDTD) [20].

All these methods discretize the structure to be analyzed into a number of smaller elements (i.e., a mesh is defined). These techniques are potentially very accurate, depending on the discretization (i.e., mesh size): a finer mesh leads to more accurate predictions but longer simulation time.

ASYMPTOTIC methods are based on an approximation of the Maxwell equations, whose validity increases with frequency. Examples of these methods are:

- Physical Optics (PO), where the Maxwell's equations short-wavelength approximation is used [21];
- Geometrical Optics (GO) is a ray-based method, so the electromagnetic waves are treated like rays. It is intended for the analysis of electrically large dielectric structures [22];
- Uniform Theory of Diffraction (UTD), where also the edge diffraction, ignored by the two previous techniques, is considered [23].

In the following part of this section the MoM will be described, as this is the one exploited in the EM simulator used in this work.

The MoM is probably the most used CEM for microwave and RF applications, because it has a very good accuracy and computational efficiency in these application fields.

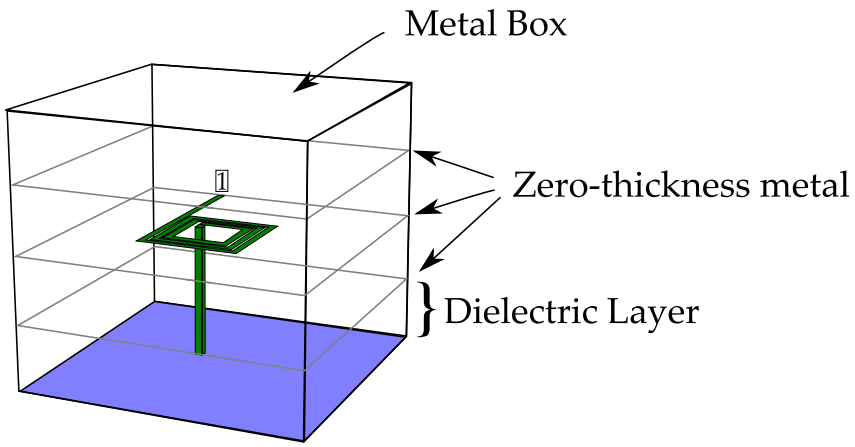

Fig. 3.4 3-Dimensional structure divided into four different dielectric layers. Between each layer a zero-thickness metal layer is present. The whole structure is inserted into a metal box.

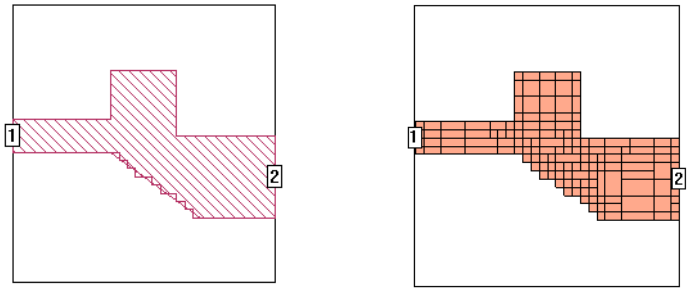

Fig. 3.5 Metallization (left) and its division in numerous subsections (right).

A 3D-complex structure is dived into some layers, as seen in **Fig. 3.4**. The metallization is modeled as a zero-thickness metal between dielectric layers [24].

Then the metallization is divided in several subsections (i.e., meshes), like in the example reported in **Fig. 3.5**. Now the effect of the surface current of each subsection on the surface current in every other subsections is calculated and stored into a matrix. These interactions are computed using a specific Green function.

Boundary conditions are applied to all the interactions and the surface currents in each section is calculated. As an example for a lossless conductor, its total tangential electric field must be null, so the currents in each section of the conductor are adjusted so that its total generated tangential electric field is equal to zero. If a non-lossless conductor is involved, its tangential electric field is imposed proportional to the current in the subsection, according to the Ohm's law.

The MoM is very accurate if high-conductive surfaces are involved: it is worth noticing that only the metallization is discretized, and not the dielectric parts around it. Moreover a lot of important parameters (e.g., small-

signal parameters) can be directly derived from the calculated surface currents.

One of the weak points of the MoM is the impossibility to handle inhomogeneous materials (e.g., highly doped regions where dielectric constant changes as a function of the density of impurities, and so the position); in these cases a volumetric mesh is required, but it is computationally very expensive. Another draw-back is the required mesh size: for higher frequencies a more fine mesh is needed (subsection dimensions must be more or less one tenth of the wavelength), it can be seen that the problem complexity scales as f^6, so if the frequency doubles then the simulation time increases of 64 times.

In the next part of the chapter an innovative noise and small-signal model based on EM-analyses and noise measurements will be presented.

3.3 GaN Noise Model Based on EM-Simulations

Low-Noise Amplifiers (LNAs) play a very important role in receiver front-ends, being the most important contributor to the overall system receiving performance.

The GaN HEMT is a promising candidate for robust low-noise applications [25, 26] due to its good noise performance, excellent linearity and robustness. Additionally, by using GaN HEMTs, the entire transmitter/receiver front-end could be integrated in the same chip, with significant advantages in terms of cost and occupied space. However, the proper identification of a model able to accurately predict GaN HEMT noise performance is not trivial and many studies have been devoted to accomplish this challenging task [27, 28, 29, 30, 31, 32, 33, 34].

In the following will be developed a new procedure for the definition and identification of a low-noise transistor model suitable for LNA design. Such a kind of application poses tight modeling requirements since it is necessary a sound physical basis of the transistor parasitic network elements in order to accurately reproduce noise behavior and properly account for those transistor layout modifications (e.g., inductive source degeneration) needed for LNA performance optimization.

Source degeneration is widely used in LNA design and consists in inserting a lossless inductance (or a microstrip line) between the transistor source and the via hole to ground. This introduces a series feedback that reduces the transistor available gain but moves the best input termination for noise closer to the conjugate match termination.

As an example, **Fig. 3.6** shows the noise factor measured with 50-Ω source impedance and the parameter S_{11} for a degenerated 8x50-μm GaN HEMT (degeneration equivalent inductance is 110 pH) predicted by a model where the parasitic network is identified by using the procedure described in this work and a simpler one, based on DC and S-parameters measurements [35]. The different accuracy level is well evident even if without source degeneration the quality of the small-signal response and noise performance predicted by the two models would be exactly the same.

Moreover, the noise contribution of the parasitic network is generally not negligible, as evident in **Fig. 3.7**, where the minimum noise figures for a 2x50-μm GaN HEMT with and without parasitic noise contribution are compared (in this second case the parasitic network temperature was set to 0 K).

In particular, a modeling procedure usable by designers without specific modelling knowledge has been developed. To this end, iterative and optimization-based model identification procedures are not a good choice as they can lead to incorrect and non-physical results if not carried out by people with in-depth experience in device modeling. As an alternative, a model identification procedure based on linear regression is proposed here. Indeed, linear regression requires only few interactions by the user (in this case just the frequency range should be defined) and is clearly more straightforward.

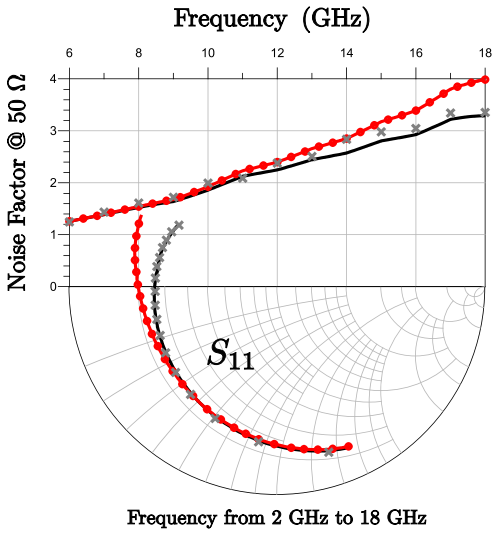

Fig. 3.6 Prediction of the noise factor with 50-Ω source impedance (upper) and S_{11} (lower) for a degenerated 8x50-μm GaN HEMT where layout parasitic elements are correctly taken (black line) and not taken (red line with dots) into account; measurements in frequency range 2 – 18 GHz are also reported (crosses).

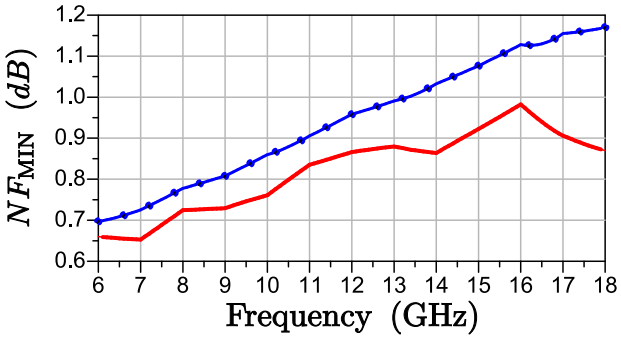

Fig. 3.7 Minimum noise figure for a 2x50-μm GaN HEMT where noise introduced by the parasitic network is taken (blue line with dots) and not taken (red line) into account.

The linear parasitic effects due to the transistor layout are modeled by a lumped-element network, identified by means of an analytical procedure exploiting several full-wave electromagnetic (FW-EM) simulations. On the other hand, the active intrinsic core of the device is modeled by means of a black-box noiseless two-ports having input and output correlated noise sources.

Performing FW-EM simulations of the different layout regions of the device allows one to develop a parasitic model where the contributions of each region is well determined; thus, layout parts can be modified (e.g., the via holes can be removed) preserving the accuracy of the model noise-performance and small-signal response.

As far as the intrinsic core is concerned, a black-box representation is chosen as it is very easy to be identified and implemented since parame-

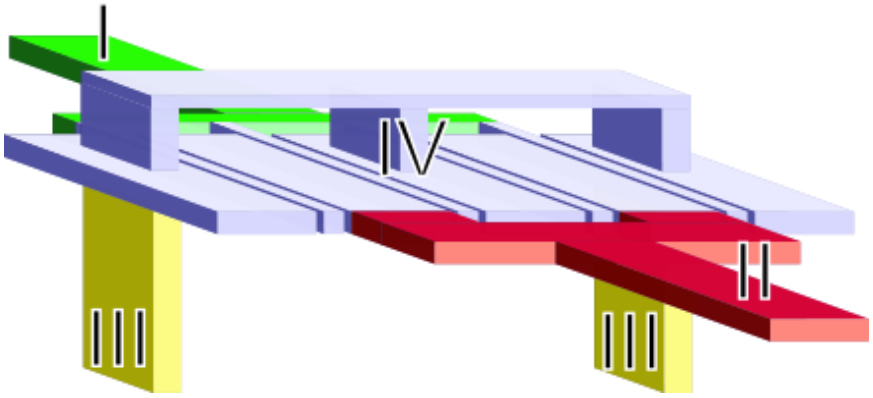

Fig. 3.8 Parasitic effects in the device layout: gate (I) and drain (II) manifolds, via-holes (III) and finger regions with air bridges (IV).

ters associated with the intrinsic core are process-related and cannot be modified by the designer.

An important benefit of the developed technique is that very simple scaling rules can be straightforwardly applied to the proposed model to get the noise and small-signal performance for differently sized devices.

3.3.1 Manifold parameters extraction

A classic transistor device model can be divided into two fundamental parts: the parasitic network and the intrinsic device or "intrinsic core". The latter represents the active area of the device, including the current generator, while the parasitic network takes into account the access structures to the intrinsic device.

Through FW-EM simulations of the device layout, the effects of the parasitic network can be characterized and modelled properly. In this context, coupling phenomena associated with the doped semiconductor substrate are not taken into account, as they have been found generally negligible [36, 37, 38, 39]. This assumption is further confirmed by the experimental validation.

The robustness of the transistor model is strongly dependent on the accuracy of the parasitic network description. In this respect, the typical layout of a HEMT device has been subdivided in four different regions (**Fig. 3.8**):

REGIONS (I) AND (II) enclose gate and drain manifolds, which feed the signal to the fingers.

REGION (III) encloses the via holes, which provide connections to the backplane metallization.

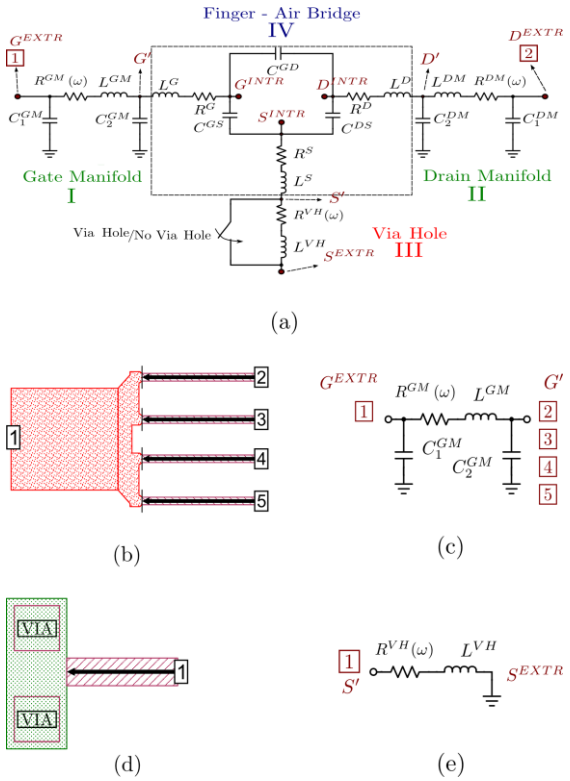

Fig. 3.9 Whole parasitic network of the transistor (a). Gate manifold (b) and associated lumped element description (c) (identical for the drain manifold). Via hole (d) and associated lumped element description (e).

REGION (IV) encloses the fingers and the air bridges, which connect the source fingers to the via hole pads.

A lumped-element network can be associated with each region as shown in **Fig. 3.9a**. For the manifolds (i.e., regions I and II), whose layout is reported in **Fig. 3.9b**, a resistor R^{GM} (R^{DM}) and an inductor L^{GM} (L^{DM}) (where "M" stands for manifold, "G" for gate and "D" for drain) model the series parasitic effects. Instead, the parasitic capacitive coupling between the manifold and the substrate is modeled by two capacitors: C_1^{GM} (C_1^{DM}) and C_2^{GM} (C_2^{DM}), forming with the other elements the PI-shape network in **Fig. 3.9c**.

It is worth noticing that, with the aim of preserving a high computational efficiency, the intrinsic device is modelled by a two-port network. This choice necessary leads to *compact* all the ports which give access to the intrinsic device (e.g., ports 2,3,4,5 in **Fig. 3.9c**) into a single one. The accuracy of this approximation has been largely demonstrated in [38], [39] and is confirmed by all the parasitic network lumped descriptions (e.g., [40]), which are inherently based on the same hypothesis. This greatly reduces the complexity of the model and speeds up the model extraction.

The parasitic effects associated with the via holes (i.e., region III), whose layout is shown in **Fig. 3.9d**, are modeled by a simple series connec-

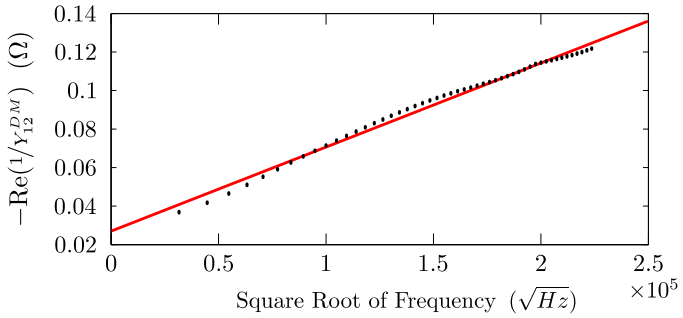

Fig. 3.10 Resistive coefficient of the drain manifold of a 4x50-μm GaN HEMT vs. square root of frequency. FW-EM simulations (dots) are fitted with the formulation reported in equation (**3.25**) (line).

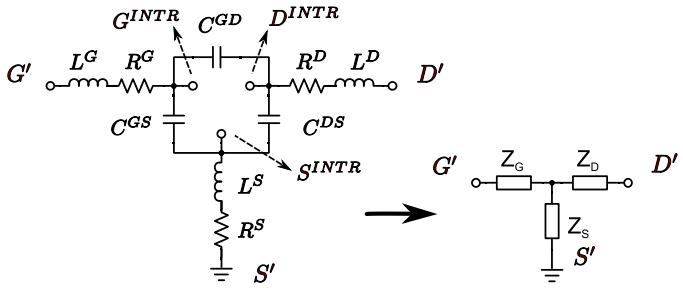

Fig. 3.11 Finger region parasitic model and associated equivalent representation adopted for parameter extraction.

tion of the resistor R^{VH} and the inductor L^{VH}, as reported in **Fig. 3.9e**. Finally, considering region (IV), three capacitors (C^{GS}, C^{DS} and C^{GD}) model the capacitive coupling between the fingers and between the fingers and the air-bridge, whilst the series parasitic effects of the fingers and the air-bridge are taken into account by three resistor-inductor series (R^G, L^G and R^D, L^D and R^S, L^S) forming with the other elements the whole parasitic network reported in **Fig. 3.9a**.

As shown in **Fig. 3.9d**, the manifolds are considered as two-port networks, where one port is at the extrinsic plane of the transistor and the other one connects to the finger region (i.e., gate or drain fingers). The Y matrix associated with the manifold network in **Fig. 3.9d** is:

$$\underline{\underline{Y}}^{XM} = \begin{bmatrix} j\omega C_1^{XM} + \dfrac{1}{j\omega L^{XM} + R^{XM}(\omega)} & -\dfrac{1}{j\omega L^{XM} + R^{XM}(\omega)} \\ -\dfrac{1}{j\omega L^{XM} + R^{XM}(\omega)} & j\omega C_2^{XM} + \dfrac{1}{j\omega L^{XM} + R^{XM}(\omega)} \end{bmatrix}, \quad (3.24)$$

where X stands for G or D.

As an example, **Fig. 3.10** shows, for a 4x50 μm GaN HEMT, the real part of $-(Y_{12}^{DM})^{-1}$, corresponding to $R^{DM}(\omega)$, obtained by an FW-EM simulation of region (II). The parameter is clearly linear with the square root of the frequency. This shape is reasonably due to the skin effect, and it is clearly not negligible since the parameter variation is very large. In this

respect, the resistors $R^{DM}(\omega)$ and $R^{GM}(\omega)$ are assumed frequency dependent to model such a variation.

In literature, several types of formulations are available to model the skin effect [41], [42]. In our case, the following simple analytical expression has been empirically found to be suitable:

$$R^{XM}(\omega) = R_{DC}^{XM} + (1+j)R_{RF}^{XM}\sqrt{\omega} \quad , \tag{3.25}$$

where X stands for G or D.

All the manifold model parameters can be easily extracted from FW-EM simulations of regions (I) and (II). The elements R_{DC}^{XM} and R_{RF}^{XM} can be determined by a linear regression:

$$-\Re\left(\frac{1}{Y_{12}^{XM}}\right) = R_{DC}^{XM} + R_{RF}^{XM}\sqrt{\omega} \quad . \tag{3.26}$$

Successively, the inductance can be straightforwardly extracted with the following formula:

$$L^{XM} = mean\left(\Im\left(-\frac{1}{\omega Y_{12}^{XM}}\right) - \frac{R_{RF}^{XM}}{\sqrt{\omega}}\right) \quad , \tag{3.27}$$

where the mean value is calculated over the whole frequency range.

Once obtained the value of L^{XM}, the elements C_1^{XM} and C_2^{XM} can be determined by:

$$C_1^{XM} = mean\left(\frac{1}{\omega}\Im\left(Y_{11}^{XM} - \frac{1}{j\omega L^{XM} + R^{XM}(\omega)}\right)\right) \quad , \tag{3.28}$$

$$C_2^{XM} = mean\left(\frac{1}{\omega}\Im\left(Y_{22}^{XM} - \frac{1}{j\omega L^{XM} + R^{XM}(\omega)}\right)\right) \quad . \tag{3.29}$$

Also in this case the mean value is calculated over the whole frequency range.

The Z parameter associated with the via hole model in **Fig. 3.9e** is:

$$Z^{VH} = R^{VH}(\omega) + j\omega L^{VH} \quad , \tag{3.30}$$

where the skin effect is taken into account with

$$R^{VH}(\omega) = R_{DC}^{VH} + (1+j)R_{RF}^{VH}\sqrt{\omega} \quad . \tag{3.31}$$

Analogously to equation (**3.26**), R_{DC}^{VH} and R_{RF}^{VH} can be extracted by a linear regression of the real part of Z^{VH} on the FW-EM simulation data of region (III):

$$\Re(Z^{VH}) = R_{DC}^{VH} + R_{RF}^{VH}\sqrt{\omega} \quad , \tag{3.32}$$

while L^{VH} can be determined by:

$$L^{VH} = mean\left(\frac{\Im(Z^{VH}) - R_{RF}^{VH}\sqrt{\omega}}{\omega}\right) \quad , \tag{3.33}$$

where the mean value is calculated over the whole frequency range.

The small-signal response of region (IV) can be extracted from FW-EM simulations of the whole parasitic network by de-embedding the contribution of regions (I), (II) and (III).

The model parameter extraction of this layout region can be more conveniently carried out by exploiting an equivalent "T" representation (see **Fig. 3.11**) of the finger region sub-network in **Fig. 3.9a**. The Z matrix associated with this representation can be expressed by:

$$\underline{\underline{Z}} = \begin{bmatrix} Z^G + Z^S & Z^S \\ Z^S & Z^D + Z^S \end{bmatrix} \quad , \tag{3.34}$$

where:

$$Z^X = R^X + j\omega L^X + \frac{1}{j\omega C^X} \quad , \tag{3.35}$$

in which X stand for G, D, or S.

Starting from Z^S, the elements C^S and L^S can be extracted by the linear regression of:

$$\omega\Im(Z^S) = \omega\Im(Z_{12}) = \omega^2 L^S - \frac{1}{C^S} \quad , \tag{3.36}$$

and R^S can be determined by the regression:

$$R^S = mean\left(\Re(Z_{12})\right) \quad , \tag{3.37}$$

where the mean value is calculated over the whole frequency range.

Once obtained the source parasitic parameters, an identical procedure can be applied to $Z^G = Z_{11} - Z^S$ and $Z^D = Z_{22} - Z^S$ to obtain the gate and drain parasitic parameters.

Finally, a $\Delta - Y$ transformation applied to the capacitors allows getting the parasitic elements of the network in **Fig. 3.9a**:

$$C^{GS} = \frac{C^G C^S + C^D C^S + C^G C^D}{C^D} \quad , \tag{3.38}$$

$$C^{DS} = \frac{C^G C^S + C^D C^S + C^G C^D}{C^G} \quad , \tag{3.39}$$

$$C^{GD} = \frac{C^G C^S + C^D C^S + C^G C^D}{C^S} \quad . \tag{3.40}$$

The FW-EM simulations (DC to 50 GHz), needed for the identification of the parasitic network model previously discussed, have been carried out by means of a 3-D planar FW-EM solver [43].

The geometry of the metal layer and the physical constants of interest have been determined by the foundry manual. **Fig. 3.12a**, **Fig. 3.12b**, and **Fig. 3.12c** show the layouts exploited to perform the FW-EM simulations. The structures described in the foundry design kit (i.e., GDSII files) were slightly simplified in order to improve the simulation speed by reducing the number of dielectric layers to the ones reported in **Fig. 3.13** (e.g., the four simulations needed to extract the lumped parasitic network of a 4x50-μm transistor required less than 2 hours by means of an 8-core Intel-Xeon mini-workstation with 32 GB of RAM).

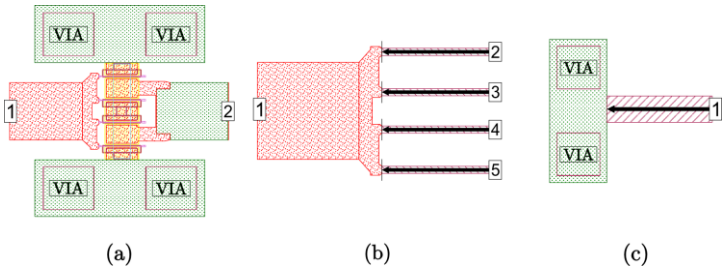

Fig. 3.12 Transistor (a), gate manifold (b) (identical for drain manifold) and via hole (c) layouts exploited to perform the FW-EM simulations.

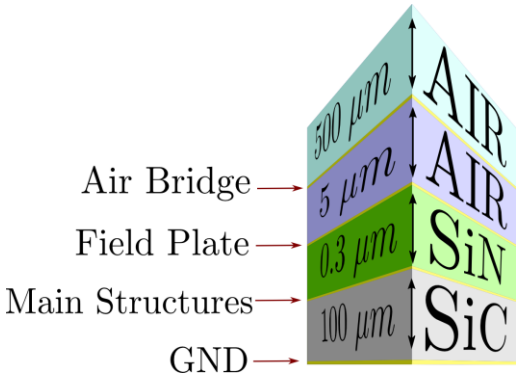

Fig. 3.13 Dielectric layers used for the FW-EM simulations. Thickness and dielectric types are reported, as well as the structures present between the layers.

As discussed in the previous section, in the FW-EM simulations the manifolds are described as n-port networks (see **Fig. 3.12b**) and successively reduced to two-port networks by using the formulation reported in [38].

The great advantage of the procedure proposed in this work is that it can be straightforwardly implemented in any numerical computing environment or by means of a custom program in high-level language. In our case, a MATLAB [44] script has been developed that automatically extracts the values of the parasitic-network lumped elements starting from the FW-EM simulations.

As a case study three GaN HEMTs have been considered with a gate length of 0.25 μm and a gate width of 8x50 μm, 4x50 μm, and 2x50 μm. A comparison between the parasitic elements of these three devices is reported in **Table I**.

As an example, **Fig. 3.14** shows the S-parameters of the extracted parasitic network for the 8x50 μm device. The plot shows only the small-signal parameters of the passive parasitic network of the device, without the active part. It is clear that the model not only reproduces perfectly the FW-EM simulations in the extraction range, but the predictions are still very

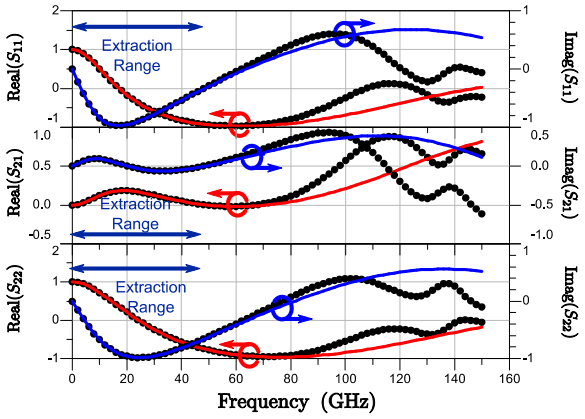

Fig. 3.14 Real and imaginary parts of S_{11}, S_{22}, and $S_{12} = S_{21}$ for the parasitic network of an 8x50-µm GaN HEMT. FW-EM simulations (dots) and extracted model predictions (lines) are in excellent agreement in the extraction range and in quite good agreement up to tens of gigahertz beyond it.

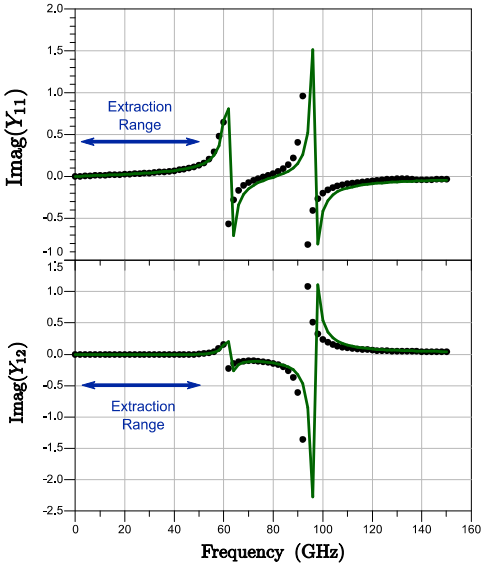

Fig. 3.15 Imaginary parts of Y_{11} and Y_{12} for the parasitic network of an 8x50-µm GaN HEMT. The extracted model (lines) predicts very accurately the resonance visible in the FW-EM simulations (dots) even far beyond the extraction frequency range.

accurate at higher frequencies. This assertion is confirmed in **Fig. 3.15**, where the prediction of the Y-parameters is shown. In particular, it has to be emphasized that the developed model shows good accuracy in reproducing the resonance frequencies even if they are well above the extraction frequency range.

TABLE I: COMPARISON BETWEEN PARASITIC ELEMENTS OF THE CONSIDERED DEVICES

	2x50		***4x50***		***8x50***	
Gate Manifold	R_{DC} = 5 mΩ	L = 9 pH	R_{DC} ≈ 0 Ω	L = 51 pH	R_{DC} ≈ 0 Ω	L = 52 pH
	C_1 = 6 fF	C_2 = 7 fF	C_1 = 12 fF	C_2 = 14 fF	C_1 = 15 fF	C_2 = 24 fF
	R_{RF} = 202 nΩ(Hz)$^{-0.5}$		R_{RF} = 714 nΩ(Hz)$^{-0.5}$		R_{RF} = 763 nΩ(Hz)$^{-0.5}$	
Drain Manifold	R_{DC} ≈ 0 Ω	L = 9 pH	R_{DC} = 27 mΩ	L = 42 pH	R_{DC} = 30 mΩ	L = 41 pH
	C_1 = 6 fF	C_2 = 4 fF	C_1 = 18 fF	C_2 = 22 fF	C_1 = 20 fF	C_2 = 51 fF
	R_{RF} = 231 nΩ(Hz)$^{-0.5}$		R_{RF} = 440 nΩ(Hz)$^{-0.5}$		R_{RF} = 370 nΩ(Hz)$^{-0.5}$	
Via Hole	R_{DC} = 6 mΩ	L = 27 pH	R_{DC} = 9 mΩ	L = 18 pH	R_{DC} = 9 mΩ	L = 18 pH
	R_{RF} =203 nΩ(Hz)$^{-0.5}$		R_{RF} =384 nΩ(Hz)$^{-0.5}$		R_{RF} =384 nΩ(Hz)$^{-0.5}$	
Fingers Air Bridges	C_{GS} = 41 fF	L_G = 23 pH	C_{GS} = 82 fF	L_G = 0.5 pH	C_{GS} = 163 fF	L_G = 0.4 pH
	C_{DS} = 9 fF	L_D = 29 pH	C_{DS} = 18 fF	L_D = 37 pH	C_{DS} = 33 fF	L_D = 29 pH
	C_{GD} = 9 fF	L_S = 15 pH	C_{GD} = 12 fF	L_S = 2.5 pH	C_{GD} = 25 fF	L_S = 16 pH
	R_G = 1000 mΩ		R_G = 327 mΩ		R_G = 143 mΩ	
	R_D ≈ 0 Ω		R_D = 249 mΩ		R_D = 172 mΩ	
	R_S = 226 mΩ		R_S = 147 mΩ		R_S = 132 mΩ	

One of the main advantages of the parasitic element identification based on this technique is the accurate definition of the transistor intrinsic planes. As a matter of fact, the small-signal models extracted by DC and S-parameter measurements [35], [40], like conventional foundry models, cannot separate the contribution to the source parasitic elements related to the via-holes from the one associated with the finger region. As a consequence, it is not possible to accurately identify the plane where the source degradation line has to be connected. For such a reason, conventional models are not very accurate for the performance prediction of degenerated devices. Indeed, as an example, the elimination of the source parasitic elements from the transistor equivalent circuit model and its replacement with a source degeneration line necessarily leads to neglect the parasitic contribution related to the source fingers.

This assumption is confirmed by the experimental results and is true even when an accurate model of the degeneration line is available. However, the reliable performance prediction of a degenerated device is possible by using the proposed technique, which exploits accurate EM simulations of the different regions of the transistor layout to provide an accurate definition of the intrinsic planes. In such a case, the simple addition of a suitable degeneration line model provides accurate results.

3.3.2 Noise and parasitic de-embedding procedure

Once the lumped parasitic network elements have been identified, the small-signal and noise intrinsic core model can be extracted by de-embedding the parasitic network contributions.

To this end, the noise correlation matrix $\underline{\underline{C_A}}$ is defined starting from the transistor noise parameters by using the formulation in [45, 46, 7]:

$$\underline{\underline{C_A}}^{EXTR} = 2kT\Delta f \cdot \begin{bmatrix} R_N & \frac{F_{MIN}-1}{2} - R_N Y_{OPT}^* \\ \frac{F_{MIN}-1}{2} - R_N Y_{OPT} & R_N |Y_{OPT}|^2 \end{bmatrix} \quad , \tag{3.41}$$

where F_{MIN} is the minimum noise factor, Y_{OPT} the optimal source termination for noise, R_N the noise equivalent resistance, k the Boltzmann constant, T the reference temperature (290 K) and Δf the noise bandwidth (i.e., 1 Hz).

The de-embedding of the parasitic element noise contributions is similar to a classic small-signal parameter de-embedding procedure [40]: the contributions of series elements are eliminated by using Z-representations, while the shunt elements are eliminated by means of Y representations. The formulae used for this de-embedding are [45, 46, 7]:

$$\underline{\underline{C_Y^D}} = \underline{\underline{C_Y}} - 2kT\Delta f \Re(\underline{\underline{Y}}^-) \quad , \tag{3.42}$$

for the shunt elements and:

TABLE II: NOISE CORRELATION MATRIX CONVERSION PARAMETERS

	$\alpha = A$	$\alpha = Y$	$\alpha = Z$
$\beta = A$	$\mathbf{I}$	$\begin{bmatrix} 0 & A_{12} \\ 1 & A_{22} \end{bmatrix}$	$\begin{bmatrix} 1 & -A_{11} \\ 0 & -A_{21} \end{bmatrix}$
$\beta = Y$	$\begin{bmatrix} -Y_{11} & 1 \\ -Y_{21} & 0 \end{bmatrix}$	$\mathbf{I}$	$\mathbf{Y}$
$\beta = Z$	$\begin{bmatrix} 1 & -Z_{11} \\ 0 & -Z_{21} \end{bmatrix}$	$\mathbf{Z}$	$\mathbf{I}$

A, **Y** and **Z** are the matrices representing the small-signal response of the network at the section where the conversion has to take place; **I** is the identity matrix.

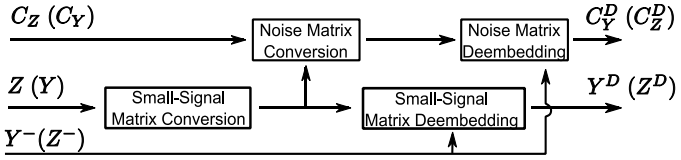

Fig. 3.16 De-embedding "core-function" flowchart: this function performs matrix representation conversion and de-embeds the noise correlation matrix C_Z (C_Y) as well as the small-signal parameter matrix Z (Y) from the matrix Y^- (Z^-).

$$\underline{\underline{C}}_Z^D = \underline{\underline{C}}_Z - 2kT\Delta f\Re(\underline{\underline{Z}}^-) \quad , \tag{3.43}$$

for the series elements. In (17) - (18), $\underline{\underline{C}}_Y^D$ and $\underline{\underline{C}}_Z^D$ are the resulting de-embedded noise correlation matrices, $\underline{\underline{C}}_Y$ and $\underline{\underline{C}}_Z$ are the starting noise correlation matrices, while $\underline{\underline{Y}}^-$ and $\underline{\underline{Z}}^-$ are the small-signal parameter matrices associated with the passive network to be de-embedded.

In the noise de-embedding procedure, the noise correlation matrix representation must be converted from Y to Z or ABCD, and vice versa. The formula to properly convert those matrices is the following one:

$$\underline{\underline{C}}_\beta = \underline{\underline{T}} \times \underline{\underline{C}}_\alpha \times \underline{\underline{T}}^* \quad , \tag{3.44}$$

where the value of $\underline{\underline{T}}$ as a function of α and β is reported in **Table II**.

It is clear that also the small-signal parameters at each section of the parasitic network are needed in order to convert the noise correlation matrix representation (e.g., $\underline{\underline{C}}_Z$ to $\underline{\underline{C}}_Y$). Thus, also the small-signal parameters $\underline{\underline{Y}}^{extr}$ have to be measured and a well-known small-signal de-embedding procedure [40] is exploited to achieve the small-signal response of the device at every section where a noise correlation matrix conversion is performed.

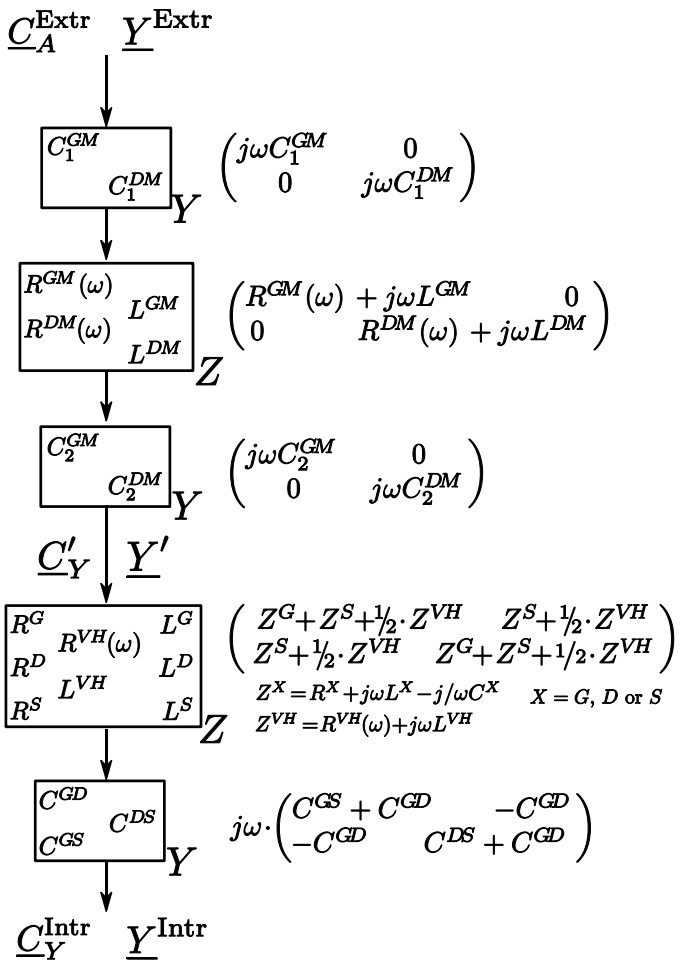

Fig. 3.17 Noise and small signal de-embedding procedure flowchart. Each box represent one step of the procedure: the elements to be de-embedded are reported inside the boxes and the corresponding matrices are on the right of the boxes. Also the formulation used (Y or Z) is reported at the corner of the boxes.

Based on the above considerations, the flow-chart of the "core-function", which performs noise de-embedding, small-signal de-embedding, and matrix conversion, is shown in **Fig. 3.16**.

The complete de-embedding procedure is composed of five steps, as represented in **Fig. 3.17**.

The procedure is applied starting from the extrinsic plane of the device going towards the intrinsic core. At each step, the core-function in **Fig. 3.16** is applied to de-embed a group of lumped elements (in Y-formulation for shunt elements or Z-formulation for series ones).

Thus, starting from the extrinsic plane, the first capacitor of the drain and gate manifold is de-embedded using a Y-formulation, successively the procedure de-embeds resistors and inductors of the gate and drain manifolds using a Z-formulation; finally, after de-embedding the last two capacitors, the drain and gate manifold contributions are completely de-

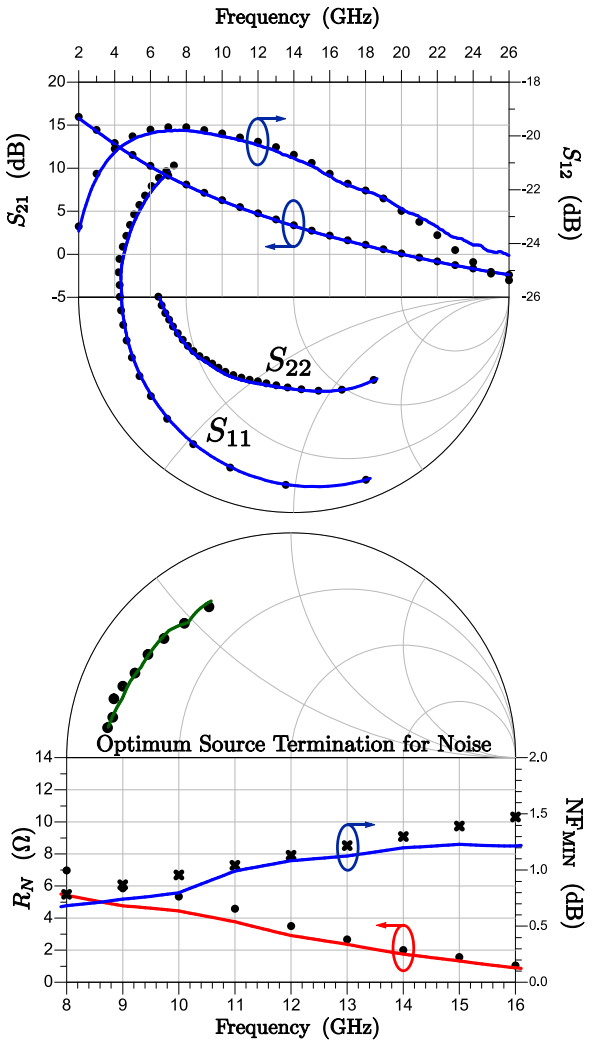

Fig. 3.18 Small-signal (upper figure) and noise parameters (lower figure) for the 8x50-μm GaN HEMTs. Measurements (symbols) and simulations (lines) obtained through scaling from the 4x50-μm model are in very good agreement

embedded.

The successive step of the procedure is to de-embed the via-hole and the series finger parasitic contributions by using a Z-representation. Once removed the final contribution of the shunt parasitic capacitances associated with the fingers, the intrinsic noise and small-signal matrices are achieved. It is worth noting that even the noiseless elements, such as capacitors or inductors, are taken into account in this procedure, because they are needed to compute the intrinsic-core small-signal model.

It should be observed that very simple scaling rules can be defined at the intrinsic plane of the transistor. In particular, the intrinsic small-signal and noise correlation matrices in Y-representation of the 2x50-μm and 8x50-μm transistor can be determined, respectively, by dividing and multiplying by 2 the response of the 4x50-μm device. As an example, **Fig. 3.18**

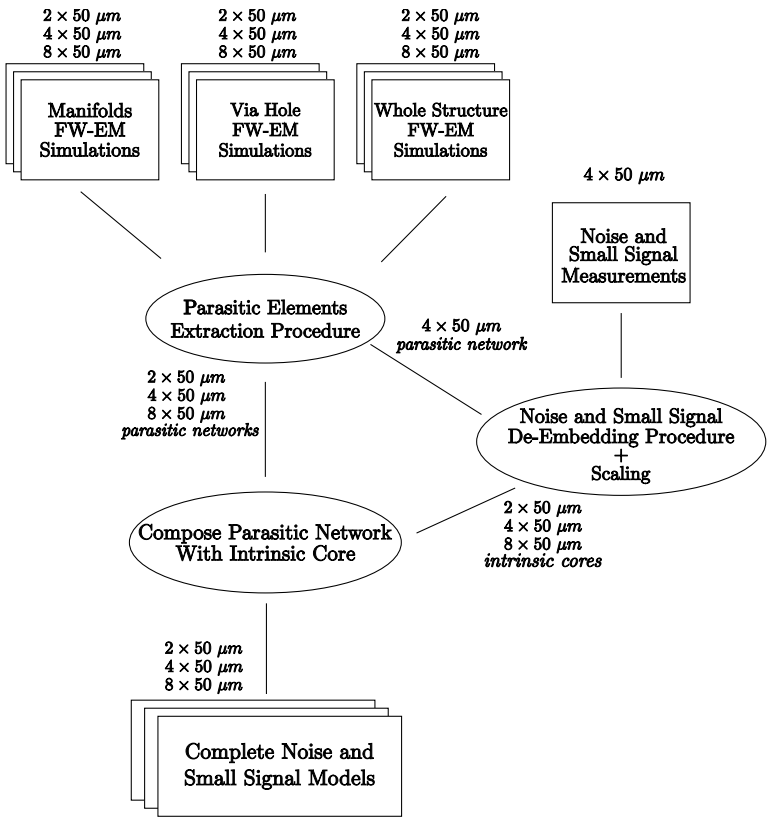

Fig. 3.19 Extraction flow-chart for the low-noise transistor model.

shows the predicted small-signal response and noise behavior of the entire 8x50-μm device scaled from the 4x50-μm transistor. It is evident the very good agreement between the model predictions and the measurements.

The scaling procedure and the one described in **section 3.3.1** jointly create a powerful, fast, and simple model identification technique (the model extraction flow-chart is shown in **Fig. 3.19**), which is able to provide robust low-noise, scalable device models for LNA design. To this end, the intrinsic device noise and small-signal parameters can be stored in a Touchstone [47] file which can be read natively by the most diffused CAD tools [48].

The 4x50-μm GaN HEMT (bias: V_{D0} = 10 V and I_{D0} = 100 mA/mm) noise parameters have been measured at various frequencies by using a source-pull procedure based on noise figure measurements at different source impedances synthesized by a tuner [49], [50]. Also S-parameters have been measured at the same bias condition. The intrinsic noise behavior and small-signal response of the 4x50-μm device have been achieved by exploiting the procedure previously described, and scaled on the 2x50-μm and 8x50-μm devices by simply dividing and multiplying by 2 the response of the 4x50-μm device. Once obtained the information about the intrinsic core of all the devices of interest, the parasitic lumped network, extracted separately for the 2x50-μm, 4x50-μm and 8x50-μm devices by

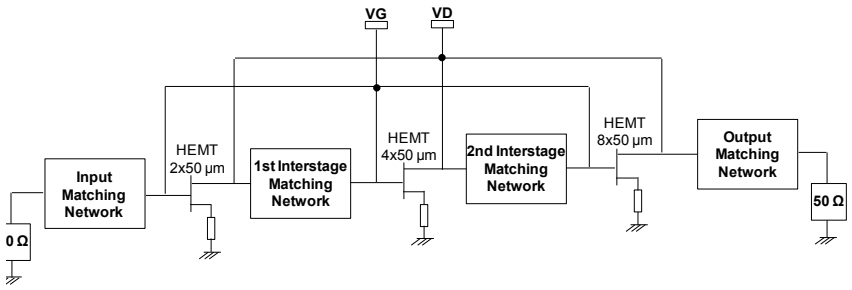

Fig. 3.20 Schematic representation of the LNA.

FW-EM simulations, has been added to the intrinsic model, in order to obtain the complete device model for the selected bias point. In fact, simple scaling rules, which can be effectively used for the intrinsic transistor, cannot be applied to the parasitic network, due to the complex relationships between the lumped component values and the layout geometry. The choice of using a separated parasitic network descriptions is a clear advantage of the proposed approach, since conventional models need to adopt *peculiar* scaling rules, which necessarily degrade performance predictions for the scaled device.

3.3.3 Low-noise amplifier design

The 0.25-µm AlGaN/GaN on SiC GH25-10 process of UMS (United Monolithic Semiconductors) has been used to develop a LNA operating in the 12.75 – 14.8 GHz frequency band. The main design goals were 20 dB of gain and less than 2.0 dB of noise figure. In the preliminary design phase, the foundry model was adopted to determine that a three stage LNA was needed to fulfill the specifications. In particular, in the first stage a 2x50-µm transistor minimizes noise and in addition is more easily matchable to 50 Ω. In the second stage, a 4x50-µm transistor allows low-loss inter-stage matching, while providing fair good noise figure and gain. Finally, in order to fulfill output power at 1 dB of gain compression and linearity requirements, a 8x50-µm transistor has been chosen for the third stage. The optimal bias point has been found to be 10 V of drain voltage and 100 mA/mm of drain current for all the three stages. A block diagram of the designed LNA is represented in **Fig. 3.20**.

As described in **section 3.3.2**, noise and small signal measurements were carried out on the 4x50-µm GaN HEMT at the selected bias point and, as described in **section 3.3.1**, all the FW-EM simulations needed were performed, in order to develop the model by following the procedure outlined in **Fig. 3.19**. Once measurements and FW-EM simulations were carried out, model extraction took only few minutes of work and computation. By using the developed transistor models, it was possible to accurately study the effects of the source degeneration on the three transistors. In particular, the first transistor source degeneration was designed to get the

optimum source impedance for gain (i.e., conjugate match) very close to the optimum impedance for noise. This enables to match the device for the best noise performance with a reasonable mismatch to the optimum source impedance for gain, thus preserving a good LNA input return loss. The second stage source degeneration was designed to have a good tradeoff between noise figure, gain and stability. A little source degeneration was exploited also in the third stage 8x50-μm transistor for device in-band stabilization.

A lot of care was taken in the matching network design. Since the losses of the input matching network directly add to the LNA noise figure, it was exhaustively optimized to keep losses below 0.2 dB.

The LNA was designed in order to comply with robustness constraints. The maximum level of input power it can withstand is mainly related to the active device maximum electrical and thermal ratings defined by the foundry. Both the maximum voltage swings as well as the gate current limitation have been carefully controlled during the circuit design.

In particular the gate current limitation was obtained by placing a series integrated resistor on the DC gate path of each transistor properly dimensioned to obtain, at increasing input power levels, a progressive voltage drop that safely switches off the transistors.

The fully monolithic integration of the limiting resistors was optimized to ensure reliable operation of the active and passive components up to the maximum input power level of 25 dBm according to the target specifications.

The manufactured LNA and the transistor cut-outs (included for model validation purpose), are shown in **Fig. 3.21**.

In **Fig. 3.22** a comparison between the measured S-parameters and noise performance of the three degenerated devices and the model predictions are reported; the agreement is very good. It is worth noticing that the predictions are still very good even if the 2x50-μm and the 4x50-μm have a single-side degeneration (i.e., one via-hole is absent) and the device is not symmetrical anymore.

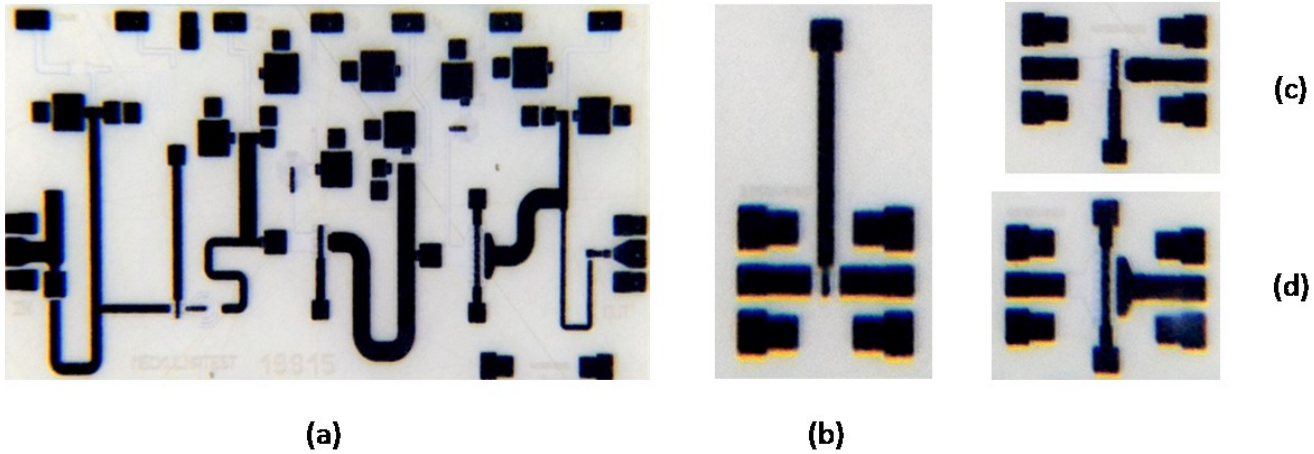

Fig. 3.21 Photos of the developed MMIC LNA (a), chip size is 4x2 mm^2 and of the degenerated 2x50-μm (b), 4x50-μm (c) and 8x50-μm (d) transistors.

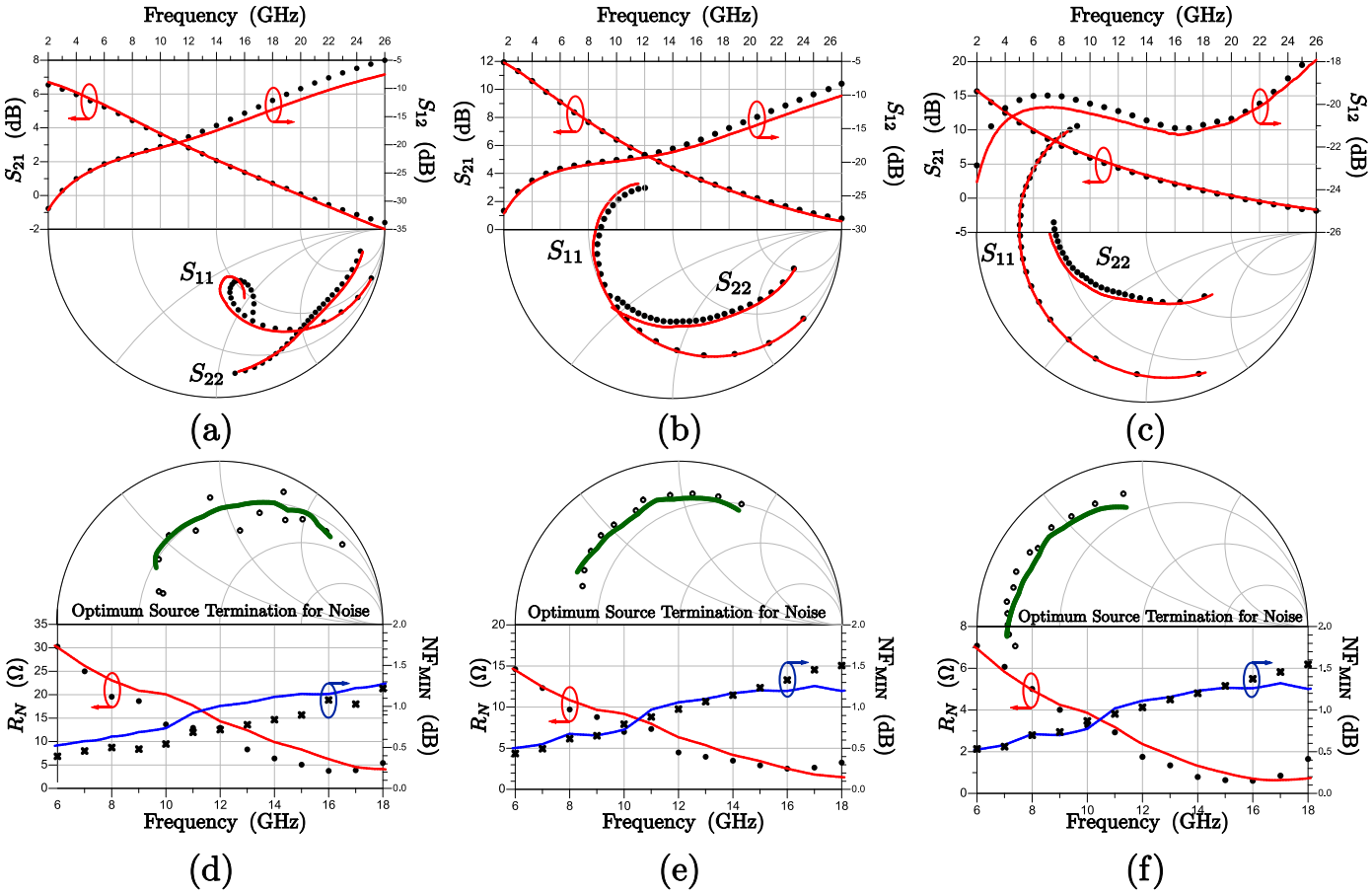

Fig. 3.23 Small-signal (a, b, c) and noise parameters (d, e, f) of the degenerated 2x50-µm (a,d), 4x50-µm (b,e) and 8x50-µm (c,f) devices. Measurements (symbols) and model predictions (lines) are in good agreement. Bias condition: V_{D0} = 10 V and I_{D0} = 100 mA/mm.

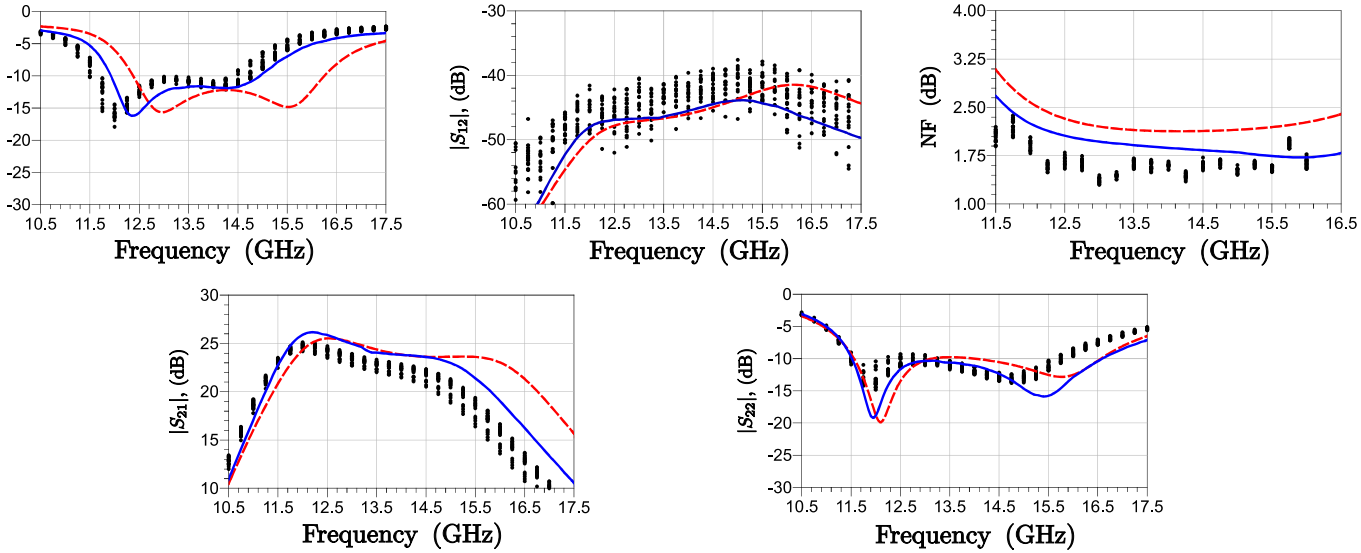

Fig. 3.24 Small-signal and noise performance of the three-stage LNA designed. Predictions with the proposed model (blue continuous lines) and with a small-signal model (red dashed line), extracted by DC and S-parameter measurements [30], are compared with the measurements carried out on 37 samples (circles). The accuracy improvement is well evident.

In **Fig. 3.24** the performance of the designed LNA is reported; the simulated predictions are in good agreement with the measurements, carried out on 37 samples and the gain and noise figure specifications are completely fulfilled in the band of interest. To provide a clearer comparison of the proposed approach with existent ones, the figure also reports, for a degenerated device, predictions of a conventional model extracted on the basis of DC and S-parameter measurements [35]. It should be pointed out that the two models show the same accuracy level when the non-degenerated device is considered. Whereas, the different level of accuracy in the presence of source degeneration is well evident. As previously discussed, the poor predictions of the conventional model are due to an incorrect identification of the device intrinsic plane. This is clearly independent on the particular model formulation adopted. On the contrary, an EM-based model can identify with high accuracy the intrinsic plane position and provide great accuracy in the performance estimation of a degenerated device. These results definitely confirm that an approach based on EM simulations is useful not only when the design involves frequencies near the upper limit of the chosen technology [38] (i.e., 20 GHz), but also when non-standard device configurations have to be used.

3.4 CONCLUSION

A new low-noise transistor model and the associated identification procedure have been developed. The model is based on FW-EM simulations as well as noise and S-parameter measurements. The proposed technique allows to identify in a short time a robust scalable low-noise model suitable for LNA design. In particular, layout modifications can be accounted for, thus accurately predicting the noise behavior and small-signal response of degenerated devices. Moreover, the described procedure is very robust, since it does not require any numerical optimization.

The described procedure has been exploited to identify three low-noise HEMT models starting from a single set of small-signal and noise measurements. Successively, a LNA has been designed by using the extracted models and the high accuracy level of the predictions on both the degenerated devices and the LNA has been definitely proved.

3.5 REFERENCE

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