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Relaxed germanium epilayers on porous silicon buffers for low dislocation content Ge on Si virtual substrates

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Publications

This thesis is based on data presented in the following papers:

- G. Calabrese, S. Baricordi, P. Bernardoni, D. De Salvador, M. Ferroni, V. Guidi, V. Morandi, D. Vincenzi, *Enhanced Threading Dislocation Reduction In Germanium Grown On Porous Silicon On Annealing Due To Porous Buffer Reconstruction*, submitted to Applied Physics Letters

- G. Calabrese, S. Baricordi, P. Bernardoni, D. De Salvador, M. Ferroni, V. Guidi, V. Morandi, D. Vincenzi, *Ge Growth On Porous Silicon: The Effect Of Buffer Porosity On The Epilayer Crystalline Quality*, Applied Physics Letters 105, 122104 (2014)

- G. Calabrese, S. Baricordi, P. Bernardoni, S. Fin, V. Guidi, D. Vincenzi, *Towards III-V Solar Cells On Si: Improvement In The Crystalline Quality Of Ge-On-Si Virtual Substrates Through A Low Porosity Porous Silicon Buffer Layer And Annealing*, AIP Conf. Proc. 1616, 37 (2014).

Other papers I published as corresponding author not related to this thesis work:

- G. Calabrese, F. Gualdi, S. Baricordi, P. Bernardoni, V. Guidi, L. Pozzetti, D. Vincenzi, *Numerical Simulation Of The Temperature Distortions In Ingap/Gaas/Ge Solar Cells Working Under High Concentrating Conditions Due To Voids Presence In The Solder Joint*, Solar Energy 103 (2014) 1–11.

- F. Aldegheri, S. Baricordi, P. Bernardoni, M. Brocato, G. Calabrese, V. Guidi, L. Mondardini, L. Pozzetti, M. Tonezzer, D. Vincenzi, *Building Integrated Low Concentration Solar System For A Self-Sustainable Mediterranean Villa: The Astonyshine House*, Energy and Buildings 77 (2014) 355–363.

- S. Baricordi, G. Calabrese, F. Gualdi, V. Guidi, M. Pasquini, L. Pozzetti, D. Vincenzi, *A Joint Thermal-Electrical Analysis Of Void Formation Effects In Concentrator Silicon Solar Cells Solder Layer*, Solar Energy Materials and Solar Cells Volume 111 (2013) 133-140.

Abstract

While silicon represents the dominant material in the semiconductor industry, the continuous improvement in the performance of Si based devices is reaching its upper bound due to the approaching of insuperable physical limitations intrinsic to Si, which requires the introduction of new semiconductor materials and the development of new assembly techniques to guarantee the future performance improvement and reduction in fabrication costs. The integration of high-quality germanium epilayers on Si substrates has received great attention from the semiconductor community due to the chance to extend the range of performance offered by Si-based technology by taking advantage of both the superior properties of Ge such as a higher carrier mobility, a lattice constant close to that of GaAs which enables III-V epitaxy and a quasi-direct bandgap, and of the possibility of strain and bandgap engineering offered by the formation of a heterojunction.

To overcome the 4.2% lattice constant mismatch existing between Ge and Si which hamper the direct integration approach, this thesis investigates a novel technique for the realization of high-quality Ge on Si virtual substrates (VSs), consisting in the introduction of a porous silicon (pSi) buffer layer in between Ge and Si. pSi is a versatile, self-assembled, nanomaterial which can be realized at very high growth rates through electrochemical etching of Si. Thanks to its reduced Young's and shear moduli pSi can deform during epitaxy, potentially alleviating part of the lattice mismatch between Ge and Si and reducing the density of misfit dislocations and associated threading segments necessary for complete Ge relaxation. Together with the very high throughput of the anodization process, other fundamental advantages of the proposed approach are its low cost, its simple scalability to large area Si substrates and the possibility to lift-off the grown epilayers from the starting substrates, giving Ge on pSi VSs the possibility to outperform other existing techniques for Ge integration on Si.

During the course of this work, several Ge on pSi VSs have been grown through low energy plasma enhanced chemical vapor deposition (LEPECVD) technique, and the resulting crystalline quality has been compared to that of Ge on Si VSs. Using X-ray diffraction techniques, together with electron microscopy analysis and selective etching techniques, it will be shown how the main physical parameters of pSi buffers affect the crystalline quality of Ge heteroepilayers. Finally, it will be demonstrated that strong threading dislocation reduction is possible in Ge grown on low porosity pSi buffers compared to Ge on bulk Si, at parity of experimental conditions, and the main mechanisms responsible for crystalline quality improvement in Ge grown on pSi will be uncovered.

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Chapter 1

Introduction

1.1 Motivation of the work

Although silicon has enabled the growth of the semiconductor electronic industry, it was not the first investigated material for this kind of application. The first transistor was realized in 1947 using germanium bulk crystal as a raw material, and the germanium diode and bipolar-junction-transistor technology largely dominated the initial years of the solid-state industry [1,2]. Only the discovery of SiO_2 dielectric passivation and the metal-oxide-semiconductor-field-effect-transistor (MOSFET) process in the mid-1960s made silicon to become the dominant semiconductor in industry [1]. Today silicon based semiconductor devices account for over 97% of all the microelectronic devices [3] which represent the large portion of the several hundred billion dollars semiconductor industry.
Silicon represents the ideal semiconductor from a fabrication point of view, but it is hardly the best available material from a device perspective. Both the electron and hole mobility in Si are smaller than that of Ge and III-V semiconductors, which can take advantage of improved device performance and reduced power consumption, while the indirect bandgap of Si limits its application in optoelectronic devices. Among all known semiconductor materials, germanium offers the highest hole mobility, making it the most promising material for p-type MOSFETs (PMOSs) capable to outperform the current strained silicon PMOSs [1]. Apart from high mobility applications, Ge can take advantage of a lattice constant close to that of GaAs, thus enabling the epitaxy of III-V semiconductors, and of a quasi-direct bandgap, suggesting the possibility of light emission and detection in Ge by employing strain and bandgap engineering [4,5]. To be fully compatible with the current complementary metal-oxide-semiconductor (CMOS) manufacturing process, the integration of germanium based devices on silicon substrates is of foremost importance, so that the strong increase in manufacturing cost that would arise from the use of non –silicon substrates can be avoided [1].
The direct integration of Ge on silicon substrates is hampered by the 4.2% lattice mismatch existing between Ge and Si, leading to the nucleation of a high density of dislocations, which increases device dark current and introduces non-radiative

recombination centers degrading device performance. To overcome this issue, Si substrate pattern techniques have been recently developed, taking advantage of confinement and expulsion of generated threading dislocations (TDs) which can glide at the edges of grown mesas [6,7] and towers [8,9] and annihilate, resulting in excellent Ge crystal perfection. However, geometrical considerations cause these techniques to effectively reduce the dislocation density when the growth region is small enough (typically < 40 μm [5]), making the reduced area of the high-quality Ge crystals, together with the use of typically time-consuming and costly substrate pattern techniques, the main limitation of these approaches.

A maskless substrate pattern technique which can potentially reduce to the device grade the dislocation density in large area Ge epilayers on Si, while taking advantage of very high throughputs and low fabrication costs, consists in the introduction of a porous silicon (pSi) buffer layer in between the Si substrate and the Ge epilayer. If the compliant structure of pSi could be finely tuned to accommodate a large portion of the lattice mismatch existing between Ge and Si, pSi would likely represent the ideal buffer for Ge integration on silicon, for the realization of Ge based devices or for the growth of III-V semiconductors on Si.

1.2 Thesis outline

This thesis is devoted to the investigation of mesoporous silicon as a buffer layer for the growth of high-quality Ge epilayers integrated on silicon substrate with reduced dislocation content compared to Ge directly grown on bulk Si. In Chapter 2 will be discussed the main challenges in Ge epitaxy on Si and will be presented a description of the low energy plasma enhanced chemical vapor deposition (LEPECVD) tool used for epitaxial growth. In Chapter 3 it will be investigated the formation mechanism of pSi buffers, their growth using a double tank etching cell developed during the course of this thesis and their characterization. In Chapter 4 the epitaxial growth of Ge on the realized porous buffers will be investigated and compared with the direct integration of Ge on bulk Si. In chapter 5 will be discussed the effect of high temperature annealing on the crystalline quality of grown Ge on Si VSs, and the main mechanisms for crystalline quality improvement in Ge grown on pSi buffers will be revealed. Finally, the main conclusions of this thesis will be summarized in chapter 6, together with some suggestions on how to improve the obtained results in future investigations starting from the data presented in this work.

Chapter 2

Germanium heteroepitaxy on bulk silicon

2.1 Introduction

In the past decades, Ge on Si virtual substrates (VSs) have been extensively investigated due to a wealth of applications in a wide range of high-performance optoelectronic and microelectronic devices and their compatibility with silicon CMOS technology. The first successful approach to grow high-quality Ge epilayers on Si substrate is dated 1984, when Luryi and collaborators employed a graded SiGe buffer layer to reduce the dislocation content within the Ge upper layer [10]. Graded SiGe buffers have been successively investigated by Fitzgerald and collaborators, which demonstrated a strong reduction in the nucleation of dislocations by employing a low grading rate of ~10%/μm and ex-situ chemical mechanical polishing to reduce both the surface roughness introduced by cross-hatch pattern and dislocation pile-up that hinders dislocation gliding requiring the nucleation of additional defects [11]. Good crystalline quality Ge epitaxial layers on Si have also been obtained by direct Ge epitaxy without the introduction of SiGe buffers, which main disadvantage consist in increasing the total thickness of the device, increasing its thermal resistance and the fabrication cost. Different groups investigated direct Ge epitaxy on Si using chemical vapor deposition (CVD) through a double-step epitaxial process: according to this approach a thin Ge seed layer is initially grown on Si at the low temperature of 320-360°C resulting in an almost flat epitaxial layer, as islanding is effectively suppressed by the low Ge surface diffusivity at low temperature. Afterwards, a homoepitaxial Ge layer is grown at higher temperature (> 600°C) on the grown Ge seed in order to increase the growth rate [12, 13]. Other investigated techniques for the realization of high-quality Ge epilayers on Si involve ion implantation followed by high temperature annealing [14, 15], surfactant-mediated epitaxy [16] and substrate pattern techniques such as shallow trench isolation [6,7] and growth on pillars [8,9].

With the continuous improvement in the crystalline quality of Ge heteroepilayers on Si, Ge on Si VSs have been used in the realization of high mobility p-MOS devices [17, 18], near-infrared photodetectors [19-21], Light Emitting Diodes (LEDs) [22-24] electrically

pumped lasers [25-26], and modulators [27]. Apart from Ge based devices, great interest towards Ge on Si VSs arise from the possibility to integrate III-V semiconductors or GeSn alloys on Si, making these substrates the ideal platform for high-efficiency multijunction solar cells [28-31], high-performance Ge/III-V MOS devices [32,33] and group IV direct-bandgap semiconductors useful for optoelectronic applications [34-36]. Even though in the last years layer transfer technique combined with semiconductor wafer bonding has led to excellent crystalline quality of bonded III-V layers on silicon characterized by low dislocation density [37**]** the direct epitaxy approach to integrate Ge and III-V semiconductors on Si still remains very attractive due to its relative simplicity and the possibility to reduce fabrication costs.

Recently, plasma enhanced chemical vapor deposition (PECVD) has been developed to allow high-quality Ge epilayers on Si at high growth rate and reduced thermal budget thus positioning this technique in advantage with respect to standard techniques such as chemical vapor deposition (CVD) and molecular beam epitaxy (MBE) [38].

Even though low values of threading dislocation density (TDD) suitable for subsequent epitaxial growth have been demonstrated using different techniques, there is still the lack for a low-cost, high-throughput technique easy scalable to large wafers size able to provide high-quality Ge on Si VSs to the optoelectronic and microelectronic industry.

2.2 Ge on Si VSs for III-V solar cells on silicon

One of the main applications of high-quality, relaxed, Ge epilayers on Si is the possibility to integrate III-V semiconductors on a low-cost, large availability, high thermal dissipation and light substrate for the realization of very-high efficiency and low-cost III-V solar cells on Si. Most multijunction solar cells, both for terrestrial and space applications, typically employs a Ge bottom cell to convert the infrared portion of the solar spectrum on top of which III-V semiconductors are epitaxially grown. As an example, the III-V multi junction solar cell concepts under investigation at Fraunhofer ISE are shown in Figure 2.1. Lattice matched triple-junction and quadruple-junction solar cells (a-c) employing a Ge bottom cell are under investigation, as well as lattice mismatched metamorphic devices (d) and inverted metamorphic (e) grown on Ge [39]. The use of a Ge substrate provides lattice matching with the upper subcells and mechanical stability to the device during fabrication steps, but is unnecessary from an electrical point of view and contribute in large part to the final cost and weight of the device. 5 µm of Ge absorb 85% of the GaAs-filtered sunlight compared to the absorption of a thick Ge wafer [40], which thickness is typically in the rage 130-180 µm. As a consequence a thickness comprised between only 2 and 5

μm is necessary for the Ge sub-cell in a multi-junction device in order to ensure current matching with other sub-cells [41]. For space applications, the Ge substrate is typically removed from the solar cell at the end of the growth process with a selective chemical etching or with a wafer cutting. This reduces the weight of the device but the expensive Ge substrate is lost during the cutting process. For terrestrial applications the situation is more critical as final cost of the PV device is of paramount importance in determining the success of the technology, so that the use of thick and electrically inactive Ge substrate is of particular disadvantage. The epitaxial integration of III-V solar cells on silicon substrate could lead to a great advantage in terms of final device cost, weight, mechanical resistance, thermal conductivity, availability and wafer size. High-quality, smooth and relaxed Ge on Si virtual substrates with low dislocation content represents hence the ideal platform for the successive epitaxy of III-V semiconductors for very high-efficiency multi-junction solar cells thanks to the possibility of a net cost saving as high as 75% by switching from small area 100-150 mm Ge wafers to Ge virtual substrates grown on cheaper Si wafers having a larger area up to 300 mm [40].

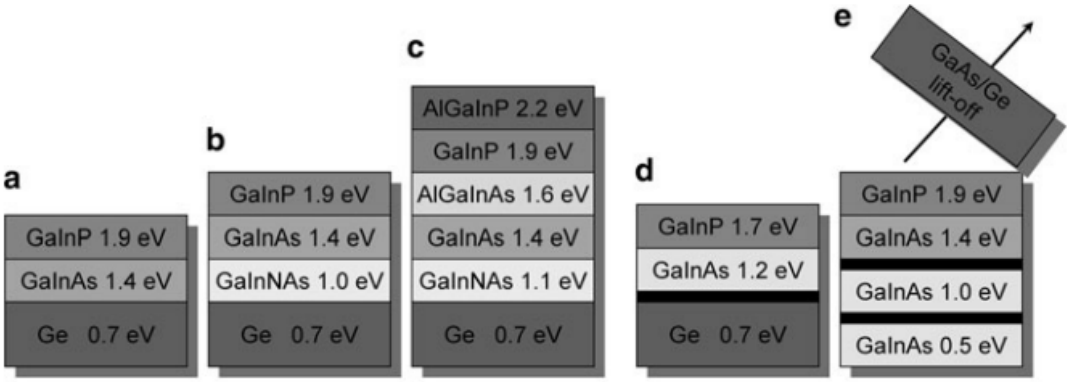


Figure 2.1: Fraunhofer ISE roadmap for the development of III-V multi-junction solar cells. Four different solar cell concepts employing a Ge bottom cell are shown, both lattice matched (a-c), metamorphic (d) and inverted metamorphic (e). After Ref [40].

2.3 Basics of Ge and SiGe epitaxy

2.3.1 Lattice constant, critical thickness and relaxation

The epitaxial growth of high-quality lattice mismatched epitaxial layers represents one of the most investigated and challenging researches in the field of semiconductors. In particular the heteroepitaxal growth of Ge on Si has been deeply investigated for more than 30 years because of the large number of high-performance and cost-effective

potential applications it offers. Ge and Si are both group IV materials with face centered cubic (fcc) diamond-like lattice structure. Si and Ge lattice constants are $a_{\mathrm{Si}} = 5.4307\ \text{Å}$ and $a_{\mathrm{Ge}} = 5.6580\ \text{Å}$ respectively, and their lattice constant mismatch is 4.18%. This value represents a very large lattice mismatch for epitaxial systems, causing the introduction of a high density of defects In the epitaxial layer when pure Ge is grown directly on bulk Si above the critical thickness (h_c). $Si_{1-x}Ge_x$ alloys of any concentration x can be grown, which lattice constant $a_{\mathrm{Si1-xGex}}$ is given by a small parabolic deviation of the Vegard's rule, which states that there is a linear relation between the lattice parameter of a solid solution alloy and the concentrations of the constituent elements.

The relative variation in lattice constant ε of a $Si_{1-x}Ge_x$ alloy is given by [42]:

$$\varepsilon = \frac{a_{\mathrm{Si1-xGex}} - a_{\mathrm{Si}}}{a_{\mathrm{Si}}} = 0.00501x^2 + 0.03675\ \mathrm{x} \qquad 2.1$$

It follows that, in order to accommodate the lattice mismatch, a $Si_{1-x}Ge_x$ layer grown on a Si substrate results under compressive stress. This mismatch can also be accommodated by the introduction of dislocations at the epilayer/substrate interface to partially or totally relieve the accumulated stress, when the thickness of the layer exceeds h_c.

During heteroepitaxy, if the thickness of the epitaxial layer does not exceed h_c, no dislocations are created at the growing interface and within the epitaxial layer and only elastic deformation occurs. In this case the epilayer is described as pseudomorphic. In particular cases the thickness of the epilayer can also exceed h_c without nucleation of dislocations. As an example when low thermal budgets are employed during film growth, dislocation formation can result energetically unfavorable. Such film is described as metastable and subsequent thermal treatment will cause the film relaxation through the formation of dislocations at the interface. The critical layer thickness strongly depend on the lattice constant mismatch between the epilayer and substrate and hence on the Ge content when SiGe in grown on Si. for pure Ge on bulk Si h_c is comprised between 1 and 2 nm [43], making this small thickness practically not useful for device applications. On the other hand, for Ge concentrations lower than 25% more than 10 nm can be grown without dislocation formation. Matthews and Blakeslee studied the critical layer thickness related to the mechanical equilibrium of an existing threading dislocation [44], obtaining the maximum layer thickness for stable layers. Also People and Bean investigated the critical layer thickness of an epitaxial system assuming that the generation of misfit dislocations to be determined solely by energy balance and they obtained the maximum thickness for metastable epilayers [45]. The critical layer thickness for a SiGe alloy grown on Si as a function of Ge percentage obtained with the different approaches of Matthews

and Blakeslee and People and Bean is shown in Figure 2.2 a), after Ref. [42]. Apart from the lattice mismatch, additional factors may influence the critical layer thickness such as the eventual the presence of a Si cap layer, which for example can double the value of h_c. (see Figure 2.2 b)).

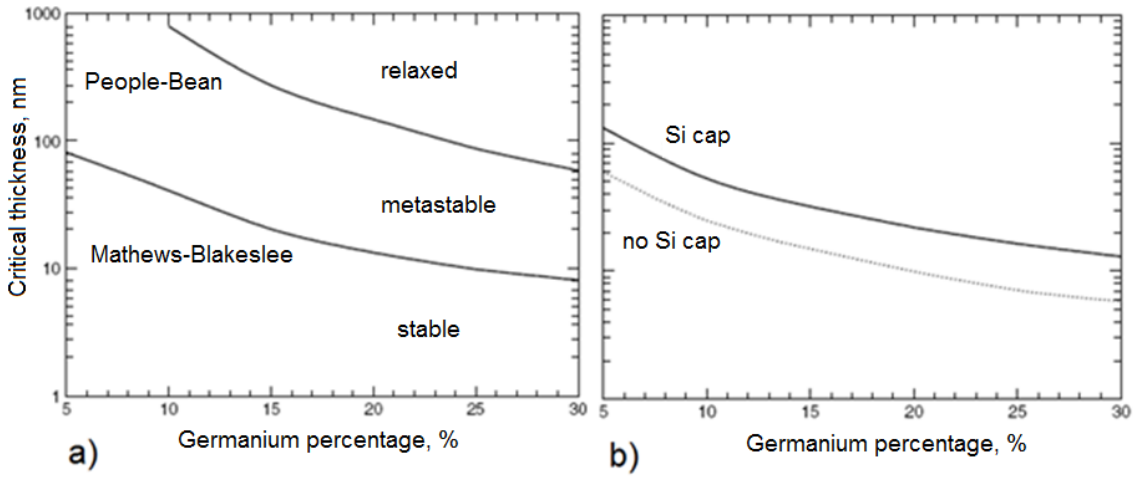


Figure 2.2: a) Critical thickness of $Si_{1-x}Ge_x$ layer as a function of Ge content and b) maximum critical thickness of a $Si_{1-x}Ge_x$ stable layer with and without Si cap layer. After Ref. [42].

A pseudomorphic dislocation free SiGe layer grown on a (001) Si substrate has a tetragonally distorted unit cell with in-plane lattice constant:

$$a_{SiGe||} = a_{Si} \tag{2.2}$$

and out-of-plane lattice constant:

$$a_{SiGe\perp} = a_{Si}(1 + k\varepsilon) \tag{2.3}$$

where k is an adimensional coefficient which takes into account the material stiffnes and for SiGe is:

$$k = 1 + \frac{2C_{12}}{C_{11}} \approx 1.75 \tag{2.4}$$

$C_{12}$and C_{11} are the elastic stiffness constants relating the fraction change in length (ε_{xx} for C_{11} and ε_{yy} , ε_{zz} for C_{12}) to the stress components.
For any Ge concentration the degree of relaxation is defined as:

$$R = \frac{a_{SiGe||} - a_{Si}}{a_0 - a_{Si}} \tag{2.5}$$

where $a_{SiGe||}$ is the in-plane lattice constant of the epilayer and a_0 is the relaxed epilayer lattice constant. For a pseudomorphic layer R=0 while in general $0 \leq R \leq 1$. As for partially relaxed epilayers the lattice constants depend on the Ge content and the degree of relaxation, in this case both lattice constants must be measured to obtain Ge content and *R*. Directly measuring the in-plane lattice constant, for example through high-resolution x-ray diffraction reciprocal space maps, has the advantage that no assumption has to be made on Ge or SiGe elastic constants, thus resulting in a more accurate measure.

2.3.2 Growth modes in epitaxial systems

In general three different growth modes exist for heteroepitaxial processes: the Frank-van der Merwe (F-vdM) or two dimensional layer by layer growth mode, the Volmer-Weber (V-W) or three dimensional island growth mode and the Stranski-Krastanov (S-K) growth mode, given by a combination of the former modes (Figure 2.3). Which growth mode occurs depends on the free-energy balance between the surfaces and the interface involved in the reaction and is determined by the simple following equation [46]:

$$\gamma_{LS} + \sigma_L \leq \sigma_S \tag{2.6}$$

where γ_{LS} represents the sum of the interface energy, σ_L the surface energy of the epilayer and σ_S the surface energy of the substrate. The F-vdM growth mode occurs when disequation (2.6) is satisfied: this is the case of homoepitaxial processes where $\gamma_{LS} = 0$ and $\sigma_S = \sigma_L$ as not lattice mismatch exist between the substrate and the growing epilayer. In F-vdM growth mode the growing layer wets the surface of the substrate completely. On the other hand V-W growth mode occurs when disequation (2.2) isn't satisfied from the beginning of the epitaxial deposition.

If at the start of the growth disequation (2.6) is satisfied and becomes unsatisfied as the epitaxial growth continues, i.e. if the balance of the existing forces results modified during epitaxy, S-K growth mode proceeds. This occurs when the growing epilayer and the substrate have a relatively large lattice mismatch, which cause the accumulation of the large strain in the epilayer during the initial stage of epitaxy. This is the case of Ge epitaxy on Si, where the first few monolayers of Ge are grown under compressive strain in a layer by layer mode, up to h_c. For larger thicknesses the accumulated strain is relaxed by the introduction of dislocations and the Ge growth proceeds by islands as the growing layer tries to minimize both its surface and interface energy.

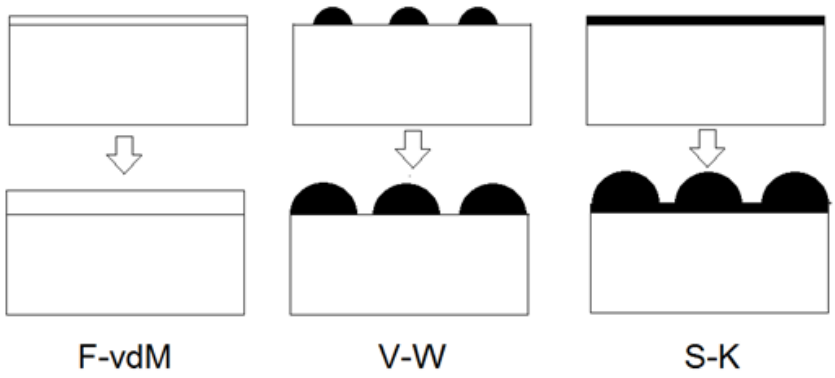


Figure 2.3: Schematic representation of the different growth modes found in epitaxial processes. Adapted from Ref. [46].

2.3.3 Dislocations in Ge

When Ge is grown on Si above h_c, misfit dislocations (MD) are nucleated at the epilayer/substrate interface to relieve the strain accumulated in the epitaxial layer, which relax plastically. MDs do not degrade the crystalline quality of the active Ge epilayer since these are confined at the growing interface. However, their nucleation is always associated with the formation threading dislocation (TD) segments within the epitaxial layer, which introduce non-radiative recombination centers in the active layers degrading carrier lifetime and increasing the device dark current. In the core of a dislocation dangling bonds and large local strains are present, while near the core the inter-atomic bonds are only weakly distorted [47]. Each dislocation is characterized by a dislocation line and a Burgers vector *b*, which defines the magnitude and the direction of the crystal lattice distortion introduced by the dislocation. TDs, which do not relax the lattice constant mismatch, can't end inside the crystal and thread within the epilayer until they encounter a free interface such as a semiconductor/air or semiconductor/oxide interface. Usually, dislocations thread within grown epilayers and terminate at the top epilayer surface, which is typically the nearest interface to the growth interface. Otherwise dislocations can form a closed loop or branch into other existing dislocations [47] and TDs that meet at a point with opposite Burgers vector annihilate. When three or more dislocations meet at a point, these form a node, and Burgers vector must conserve.

Two main kinds of dislocations exist depending on the mutual orientation of the dislocation line and the Burgers vector. Edge dislocations are line defects with perpendicular dislocation line and Burgers vector, while screw dislocations present parallel dislocation line and Burgers vector. In Ge and SiGe typically dislocations are of

mixed character (i.e. an arbitrary angle exists between dislocation line and Burgers vector) and pure edge and screw dislocations are rarely observed. In particular, 60° MDs which have a 60° angle between the Burgers vector and the line vector, are often observed in Ge in Si epilayers, with dislocation lines along the orthogonal [110] and [$\bar{1}$10] directions. Their large diffusion in Ge on Si systems depends on the fact that these dislocations can glide without the necessity of diffusion of single atoms, making their glide an energetically favored process [47]. Two basic types of dislocation movement exist: glide and climb. Glide in a conservative motion characterized by movement of dislocations in the plane containing both the dislocation line and the Burgers vector. The glide of several dislocations leads to slip, which consists in the displacement of one plane of atoms over another. The second type of movement is called climb and is a non-conservative motion in which dislocations exit the glide surface normal to Burgers vector [47]. 60° dislocations glide preferentially on {111} slip planes because they have the highest in-plane density of atoms and the lowest density of atomic bondings in the out-of-plane direction. The direction of slip is the <110>, which is the direction in the slip plane in which the atoms have the smaller distance each other. 60° MDs have Burgers vector $b = \frac{a_{Ge}}{2} < 110 >$ which forms an angle of 60° with the <110> direction and which magnitude is about 4Å . As the vector ½ <110> is a translation vector for the Ge (FCC) lattice, a dislocation with this Burgers vectors leaves a perfect crystal after gliding and is called perfect dislocation.

For Ge eight slip systems exist for 60°dislocations, which are schematized in Figure 2.4 [48]. Two pairs of orthogonal {111} glide planes exist, each plane presenting a MD at the epilayer-substrate interface and two different TDs propagating in the epilayer along the preferential <110> directions.

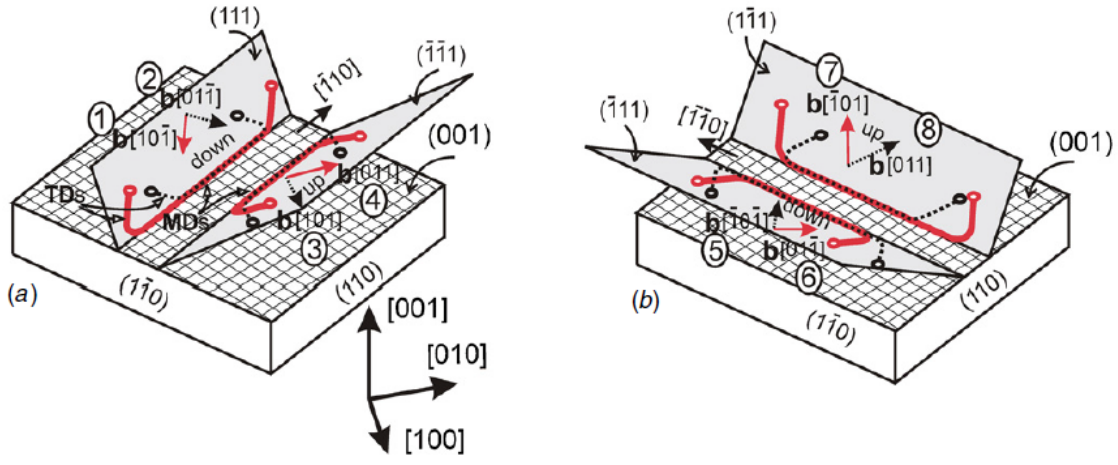


Figure 2.4: Schematic representation of the eight slip systems existing for 60° dislocations in Ge epitaxial layers grown on (001) Si. After Ref. [48].

Edge 90° MDs with Burgers vector and dislocation line in the plane of the epilayer-substrate interface would represent the most effective kind of dislocation to accommodate the strain in the growing epilayer, as in this case the crystal deformation is exactly in the plane of the interface. However, the (001) plane is not a glide plane for dislocations, so that 90° MDs are non-moving dislocations, or sessile dislocations. As a consequence, the nucleation of pure edge MDs is energetically unfavorable compared to the formation of mobile (glissile) 60° MDs [48]. The screw component of such dislocations causes the degradation of the epilayer not just in the interface region but also at large distance from it. Even though 90° MDs have low formation probability, these defects are observed in large quantities in annealed Ge epilayers grown on Si. One model to account for this considers that, during gliding, two 60° dislocations can interact and form one 90° MD if the sum of the Burgers vectors of the original MDs has no component in z direction (the direction of film growth) as in the proposed reaction:

$$\frac{a_{Ge}}{2}[10\bar{1}] + \frac{a_{Ge}}{2}[011] = \frac{a_{Ge}}{2}[110] \qquad 2.7$$

The resulting dislocation line lies at the intersection of the {111} gliding planes and has an orthogonal Burgers vector which is in a plane parallel to the interface. Annealing of Ge on Si substrates, which causes the motion of existing dislocations due to expansion and contraction of the Ge lattice, promotes the interaction of 60° dislocations which can combine to form pure edge 90° MDs, while TDs result actively annihilated.

In absence of non-equilibrium concentrations of point defects and at low temperatures where diffusion is difficult, the movement of dislocations is limited on the {111} glide planes. With increasing annealing temperature, the density and length of MDs is found to increase [49]. The velocity of glide v_g of dislocations, which is a thermally activated process, can be expressed as [50]:

$$v_g = B\varepsilon\, e^{\frac{-E_g}{KT}} \qquad 2.8$$

where B is a constant value, T is the annealing temperature and E_g is the glide energy barrier which is 1.6 eV for bulk Ge.

2.4 Main challenges in Ge epitaxy on Si

The main requirements for high-quality Ge on Si VSs useful for device integration are a low threading dislocation density (TDD), complete relaxation, a low surface roughness, the absence of cracks and a controlled bowing. High degree of relaxation close to 100% is necessary in order to avoid subsequent epilayer relaxation during further wafer processing, which could promote the further nucleation of TDs in the grown epilayers degrading their electrical properties. Cracks can originate in the Ge epilayer during cooling down the VS from growth temperature to room temperature, as a consequence of the large thermal expansion coefficient mismatch of 125% existing between Ge and Si ($\propto_{Si} = 2.6 \times 10^{-6}\ K^{-1}$ and $\propto_{Ge} = 5.8 \times 10^{-6}\ K^{-1}$ at 300 K) and they can be eliminated by adjusting the process conditions. Low TDD and surface roughness are hampered by the large lattice mismatch existing between Ge and Si, which leads to the nucleation of a large number of dislocations in the order of 10^{10}-10^{12} cm^{-2} at the growth interface which thread in the upper layers [51] and to S-K island growth.

When Ge on Si VSs are used as a platform for subsequent epitaxial growth of III-V semiconductors it is necessary to take into account the polar on non-polar nature of the epitaxial process. The growth of III-V semiconductors on (001) oriented group IV semiconductors typically leads to the formation of antiphase domains (APDs) and associated antiphase boundaries (APBs), the latter acting as preferential centers for minority carrier recombination thus degrading minority-carrier lifetime [52, 53]. The use of vicinal Si substrates, characterized by a surface which is not flat but constituted by many terraces separated by atomic steps, hamper the formation of APDs and APBs thanks to a layer by layer Ge growth which proceeds by completion of existing terraces. Typically, (001) vicinal Si wafers with 6° offcut towards [111] direction are used as starting substrates for Ge epitaxy when the grown VSs are used as a platform for the subsequent growth of III-V semiconductors. While the use of 6° offcut Si wafers can effectively suppress the formation of APDs and APBs in the upper III-V semiconductors [54], their use increases both the dislocation content and Ge RMS roughness compared to the case of Ge grown on 0° offcut Si wafers. This is mainly attributed to an imbalance in Burgers vectors for Ge grown on 6° offcut Si, which promote dislocation nucleation over annihilation [55].

To allow the integration of III-V semiconductors, Ge on Si VSs with a maximum TDD ~10^6 cm^{-2} are required. This TDD represents the threshold value for which the lifetime of minority carriers in n-type GaAs grown on Ge on Si VSs is comparable with that of the same semiconductors grown on lattice matched substrates (see Figure 2.5, after Ref. [56]).

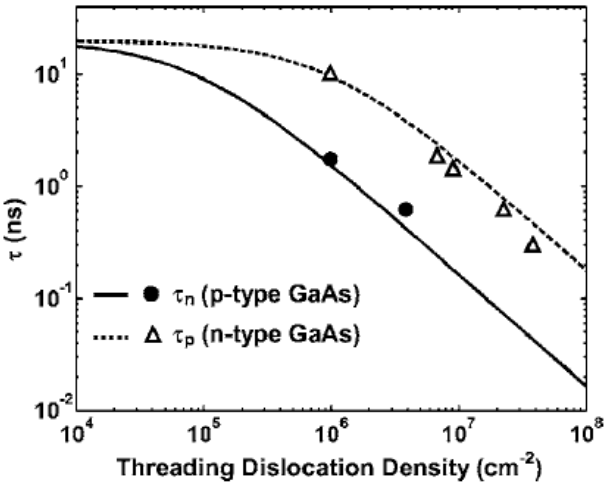


Figure 2.5: Lifetime of electrons and holes minority carriers as a function of TDD in GaAs epilayers grown on Ge on Si VSs. After Ref. [56]

2.5 Assessment of threading dislocation density

TDs represent the main issue in Ge epitaxy on Si so that an assessment of TDD within grown Ge epilayers is of extreme importance. The main used techniques to assess the density of threading dislocations in heteroepitaxial layers are both plan-view and cross sectional transmission electron microscopy (TEM), etch pit density (EPD) and high-resolution X-ray diffraction (HR-XRD).

TEM cross sectional (XTEM) analysis is a powerful technique for defects visualization and is only limited by the small viewing area. Typical sample dimensions which can be investigated are about 20μm of width and 0.7 μm of depth, corresponding to a maximum observable area of about 10^{-7} cm^{-2} [57]. As a consequence, the observation of threading dislocations using TEM is only significant for threading dislocation densities above about $10^{7}cm^{-2}$ and for lower TDD values EPD is typically employed. EPD is the easiest way to reveal dislocations, which employs preferential etching and inspection of the resulting etch pits using an optical microscope or an atomic force or scanning electron microscope. The sample is treated with an etching solution which comprises an oxidizer (HNO_3, H_2O2, $K_2Cr_2O_7$, CrO_3), a complexing agent (HF) and a diluent (water or organic solvents). The etch pits, which are created due to the preferential oxidation and removal of material in the strain field which surround each dislocation, are formed in correspondence to the crossing point of the dislocation line with the surface of the sample. TDD at sample surface is determined by counting the pits across a known area and the higher dislocation density that can be determined in this way is about 10^{8} cm^{-2} because for higher density

the etch pits start to overlap. In this case the dislocation density is usually determined through XTEM analysis. EPD technique typically gives a lower limit for the threading dislocation density because dislocations which run parallel to the surface can't be detected and single dislocations can't be resolved if dislocation pile-ups occurs. Even though the sample preparation for X-TEM analysis is very long, this technique can provide a wealth of information about sample morphology, allowing for observation of single defects, their structure and propagation. Compared to X-TEM, plan-view TEM analysis has the advantage of a faster sample preparation and of the possibility to observe a much larger area of the sample, so that a minimum observable defects density in the order of 10^5 cm^{-2} can be assessed using this technique. In this thesis TDD will be assessed using both plan view TEM analysis and EPD.

HR-XRD is a not-destructive technique which can provide a lot of structural information about grown epilayers such as lattice constants, crystallographic orientations, strain and tilt together with defect density [58]. Typically, rocking curve (RC) analysis is carried out to assess the TDD in heteroepitaxial layers, by studying the dislocation induced broadening of the full-width at half maximum (FWHM) of one or different families of diffracting planes, after deconvolution of the collected signal from other broadening effects [58]. Since RC analysis is expected to have a minimum sensitivity for dislocation density in the order of 5 x 10^5 cm^{-2} [59], it is perfectly suitable for dislocation assessment in pure Ge on Si heterostructures, where an average dislocation density in the whole Ge epilayer in the order of 10^5 cm^{-2} represents an extremely low value perfectly suitable for subsequent epitaxial growth. For direct Ge integration on Si, a TDD at Ge surface > 10^6 cm^{-2} is typically obtained and in these conditions primary and secondary extinction of X-rays are often negligible, causing X-rays to penetrate several μm within the epitaxial layer [60]. As a consequence, the whole epilayer thickness results investigated during RC analysis and the obtained TDD represents an average value which also takes into account the highly dislocated Ge/Si interface.

2.5.1 High Resolution X-Ray diffraction analysis (HR-XRD)

Different models have been proposed to assess the TDD in heteroepitaxial layers studying the broadening of the diffraction peak of a single or multiple families of atomic planes. At first, Gay and Hirsh develop a model for TDD assessment in annealed metals, which reported an upper limit for total dislocation density which depends on the ratio $\left(\frac{FWHM}{3\times b}\right)^2$ [61]. An empirical correlation between TDD at Ge surface and the change in measured FWHM before and after EPD analysis was reported by Sous and collaborators

[62], which found a TDD dependence on $C \times \left(\frac{FWHM}{3 \times b}\right)^2$, where C is a correction factor <1. Successively, Ayers extended the model of Gay and Hirsh to heteroepitaxial layers by considering the diffraction peaks as Gaussian functions resulting from the convolution of different Gaussian intensity distributions given by: the intrinsic rocking curve of the layer being examined, the instrumental broadening, finite thickness broadening, curvature broadening and dislocation broadening [63]. Later, Kaganer et al. shown that MDs and TDs have similar effects on the broadening of the epitaxial layer diffraction peaks, making it difficult to assess the TDD from FWHM broadening [64]. However, very recently Kopp, Kaganer and collaborators demonstrated the contribution of MDs on the FWHM broadening is negligible, so that TDD can be effectively determined from the broadening of collected diffraction peaks without the need to consider the effect of MDs [65].

The model proposed by Ayers was successfully applied to the GaAs/Si epitaxial system, since the GaAs diffraction peaks for different families of scattering planes are very well approximated by Gaussian functions, with the exception of the tail regions which are typically underestimated by the Gaussian fit. However, only small diffracted intensity is found in the tails so that the model does not introduce significant sources of errors in this case [63, 66]. On the other hand, the application of the same model to the Ge/Si epitaxial system is not straightforward, as the good agreement existing between GaAs diffraction peaks and Gaussian approximation is not valid for the Ge diffraction peaks. The (004) diffraction peak for a Ge epilayer integrated in silicon via a porous buffer is reported in Figure 2.6, together with the best Gaussian function approximating the peak. Similar results have been obtained for different families of scattering planes both in presence and absence of a porous buffer layer in between Ge an Si. The Gaussian function underestimates both the tail regions as well as the central region of the diffraction peak, where most intensity resides.

It follows that the assumption of a Gaussian distribution would lead to an overestimation of the Ge FWHM, and a consequent overestimation of TDD. For an accurate analysis of the TDD within Ge by means of HR-XRD techniques, more complex functions such as Lorentzian function and Voigt function should be used to fit the Ge diffraction peak [67].

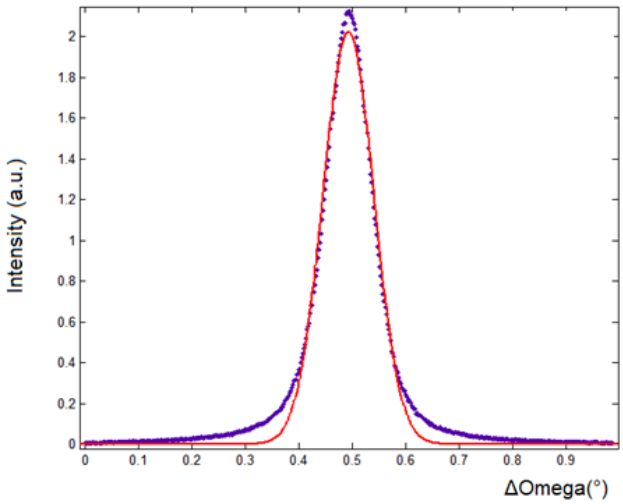


Figure 2.6: (004) Ge RC for Ge grown on pSi and its best Gaussian approximation (in red). Deviations from the ideal Gaussian behavior are found in the tail regions as well as in the central region of the Ge diffraction peak.

While an assessment of TDD by using HR-XRD is not straightforward for Ge epilayers, it is possible to determine in an approximate manner the relative change in TDD for two Ge on Si VSs, provided that TDs represent the only non-negligible contribution to FWHM broadening.

In this case the relative change in TDD can be expressed as:

$$\frac{\mathrm{TDD}_1}{\mathrm{TDD}_2} = \left(\frac{\mathrm{FWHM}_1}{\mathrm{FWHM}_2}\right)^2 \qquad 2.9$$

where TDD_1 and TDD_2 represent the TDD for sample 1 and 2, while FWHM_1 and FWHM_2 represent the FWHM of a selected family of scattering planes for sample 1 and 2, respectively. The dependence of TDD on FWHM^2 has been observed for both Gaussian [58, 63, 66] and non-Gaussian [61, 62] diffraction peaks, suggesting that Eq. (2.9) can be applied to non-Gaussian Ge epilayers without introducing a large error. Eq. (2.9) will be used to assess the change in TDD in presence and absence of a compliant porous buffer in the VSs structure, while a quantitative analysis of TDD will be carried out using TEM plane view analysis and EPD, in combination with scanning electron microscopy (SEM) imaging.

2.6 Low energy plasma enhanced chemical vapor deposition (LEPECVD)

The large-scale fabrication of Ge on Si VSs requires a growth technique which can take advantage of very high growth rates, thus allowing for high throughputs. Low energy plasma enhanced chemical vapor deposition (LEPECVD), which is an epitaxial technique developed for the growth of Ge, Si and SiGe alloys at very high deposition rates up to 10 nm/sec, represents the ideal technique from this point of view [68]. Despite the very high achievable growth rate, which is more than 10 times faster than other epitaxial techniques such as MBE and ultra-high vacuum CVD (UHV-CVD), epitaxial layers grown by LEPECVD presents similar or better electrical properties compared to those grown with other techniques [69].

In LEPECVD non-thermal energy is furnished by a dense and low-energy plasma for the dissociation of the reactive molecules, so that very low substrate temperatures can be adopted during epitaxy the same being not possible for thermal techniques. The generated plasma promotes the formation of highly reactive radicals and energetic ions, which strike the sample surface and cause a great enhancement of the hydrogen removal rate, which in turn leads to the above mentioned high growth-rate. The arrival of energetic ions on the sample surface leads also to an enhancement in the particles mobility, which is of great importance when epitaxial growth is performed at low thermal budgets. The PECVD process investigated in this thesis is based on radio-frequency inductively coupled plasma (ICP) excitation at the frequency of 13.56 MHz inside a quartz chamber embedded in the high vacuum reactor. This process, also known as radio frequency plasma enhanced chemical vapor deposition (RF-PECDV), differs from other PECVD techniques because the substrate is not biased and ions are accelerated in every direction. Plasma formation involves the generation of an alternate current in an aluminum antenna, which in turn result in the formation of a variable magnetic field. This magnetic field generates a variable electric field in orthogonal direction which accelerates the electrons of the carrier gases introduced in the growth chamber promoting plasma formation. To start the plasma reaction H_2 or Ar gases are typically fluxed in the growth chamber while precursor gases are added in a subsequent moment, when the plasma is already generated. All the samples realized in this thesis work have been grown using H_2 to start the plasma reaction and as carrier gas, which is introduced in the growth chamber in proximity of the antenna. In the LEPECVD reactor located in the cleanrooms of the Physics and Earth Science Department at Ferrara University the plasma source is located in the bottom part of the growth chamber and the samples are introduced in the reactor facing down, in order to avoid dust to fall and accumulate on the Si polished

surface. A graphite heater positioned a few centimeters above the wafer provides it the necessary thermal energy during epitaxial growth. Typical growth temperatures for pure Ge epilayers are in the range 400 to 600°C and a constant temperature of 500°C is employed for the samples grown in this thesis.

Germane (GeH_4), is used as precursor gas and is introduced in the growth chamber through a gas ring positioned just below the Si substrate. Using a turbo molecular pump and a rotary pre-vacuum pump the main chamber of the LEPECVD reactor is pumped at a base pressure of 2 x 10^{-8} mbar, while during the deposition process the working pressure is 2 x 10^{-2} mbar. A load lock prevent contamination of the growth chamber during wafer loading and, thanks to a set of IR lamps, promotes desorption of residual diluted HF from Si wafer surface after native oxide removal. During epitaxy the energy of the ions incoming on the substrate should be lower than 15 eV, in order to avoid the formation of bulk defects and the formation of stacking faults which could eventually lead to a polycrystalline growth [69]. A schematic representation of the LEPECVD system used in this work is reported in Figure 2.7. Together with the reduced thermal budget and high growth rates, another great advantage of LEPECVD over conventional techniques is the possibility to suppress island formation in Ge epilayers on Si, by taking advantage of out-of-equilibrium growth conditions [9].

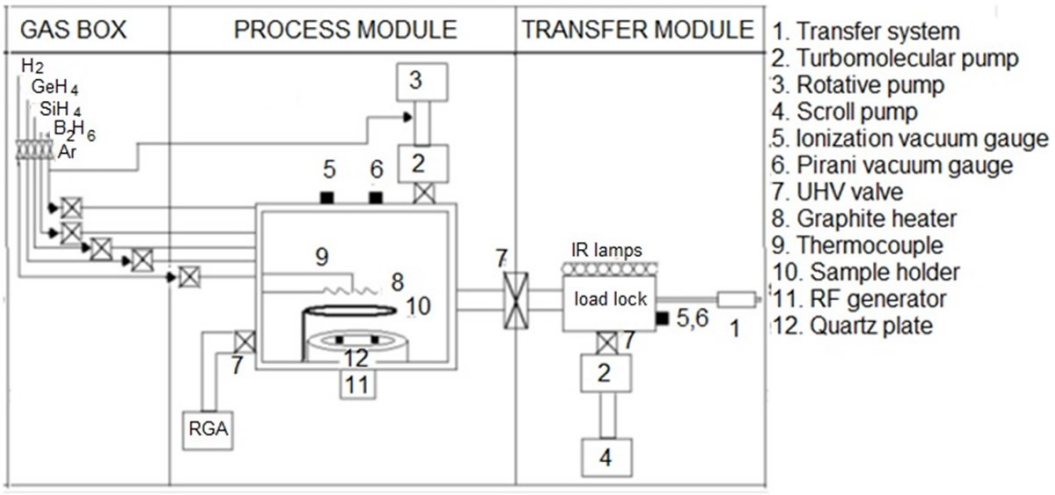


Figure 2.7: Schematic diagram of the LEPECVD system installed at Ferrara University.

2.7 First experimental results

At the beginning of this thesis work several attempts have been made to grow monocrystalline Ge epilayers on bulk Si, resulting in strongly polycrystalline Ge as assessed from very broad (004) ω–scan FWHM values in the order of 2000 arcsec for 5 μm-thick Ge epilayers, and to the lack of the Ge diffraction peak in ω/2θ scans collected in triple axis diffraction mode. The main cause for this polycrystalline growth has been ascribed to the incomplete desorption of water from wafer surface before epitaxial growth. The desorption time in the load lock has been than increased from 5 minutes at 150°C to 10 minutes at 200°C, resulting in monocrystalline Ge epilayers on bulk Si and (004) FWHM in the order of 1000 arcsec or less. However, desorption of hydrogen and other adsorbed species from bulk Si and porous Si internal surface was observed at temperatures > 400 °C [70, 71], which is much larger than the maximum desorption temperature of 200°C possible in the load lock in the present reactor configuration. As a consequence, complete water desorption for the samples grown during this thesis's work has been carried out within the main reactor chamber, possibly introducing here some contaminants.

Despite the high growth rate of several nm/sec obtainable using LEPECVD, in the present configuration the maximum wafer throughput is limited to 0.5 wafer per day as a consequence of the necessity to perform a NF_3 plasma cleaning after each single growth to remove the germanium accumulated within the growth chamber and restore a base pressure of 2 x 10^{-8} mbar before successive growth, as the non-thermal dissociation of GeH_4 leads to Ge deposition not only on the starting substrate but also on the chamber sidewalls and other mechanical parts. In particular, it is believed that germanium accumulated on the quartz shield used to protect the aluminum antenna used to generate the plasma from the plasma itself shields the H_2 carrier gas from the variable electric field generated by the antenna, thus hampering plasma formation. About 1 hour NF_3 cleaning resulted hence necessary in order to remove the accumulated Ge as the growth of two 5μm-thick Ge epilayers without intermediate plasma cleaning step resulted in the impossibility to start again the plasma and the necessity to expose in air the reactor chamber and clean manually the quartz shield. A different reactor configuration is mandatory in which no plasma cleaning is necessary after epitaxy in order to take full advantage of the high growth rates typical of LEPECVD technique.

Chapter 3

Porous silicon buffer layers

3.1 Introduction

In the last years there has been an increasing interest towards nanostructured systems and their application in microelectronic and optoelectronic devices as new physical properties appears when the physical dimensions of a structure becomes smaller than a characteristic length scale. Although photolithography represents one of the main techniques for the realization of nanostructured devices, self-assembled structures are of great interest because of their simpler fabrication processes, which can lead to higher throughputs while decreasing fabrication costs [72].

As silicon represents the most widely used semiconductor for microelectronic applications, Si based nanostructures are of particular interest because of their enhanced functionality and compatibility with CMOS technology. In particular, porous silicon (pSi) is a very versatile self-organized material which mechanical, optical, transport and absorption properties can be finely tuned by modifying the growth parameters. pSi was discovered by Uhlir in 1956 during experiments concerning the electropolishing of silicon however, is only from the 1990 that pSi started to be extensively investigated as a consequence of the discovery of room-temperature photoluminescence in nanoporous silicon layers [73]. pSi presents peculiar characteristics which can be exploited in a wide range of optoelectronic and microelectronic devices such as light-emitting diodes [74], gas sensors [75], transistors [76], photodetectors [77], waveguides [78], modulators [79] and solar cells [80, 81]. In particular, for what concerns solar cell applications, electrochemically etched pSi layers have been investigated as anti-reflection coating for high efficiency devices [82] and pSi multilayers have been proposed as Bragg reflectors in thin-film Si solar cells [83] or for lift-off of ultra-thin Si solar cells for wafer reuse [84].

Even though deep investigation of pSi started around 25 years ago, there is renewed interest towards this material due the possibility of monolithical integration with electronics on one chip, to its simple and easy preparation, and to the existence of an extremely broad space parameter for pore formation, making pSi properties tunable over

a very large interval which is not fully explored up to date [85]. Moreover, also the high-throughput and low-cost of electrochemical etching process and its scalability to large wafers play an important role in making porous silicon an appealing candidate for novel microelectronic and optoelectronic applications.

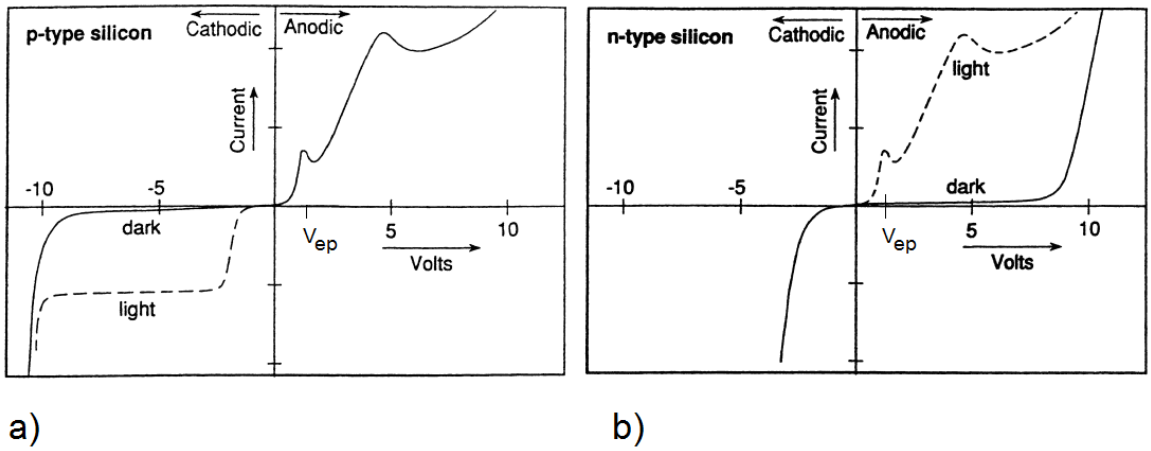
3.2 Fabrication and characterization of porous silicon

Two main techniques exist for the fabrication of porous silicon layers: electrochemical etching and stain etching. While electrochemical etching is based on holes availability at the interface between Si and the electrolyte, stain etching consists in etching of Si using an aqueous solution which involves HF and an oxidizing agent e.g. HNO_3. Among these two techniques stain etching of Si allows higher throughputs, as a whole batch of wafers can be etched at the same time, the same being not possible through electrochemical etching which requires the realization of an electric contact for each single wafer to be processed. Even though stain etching can take advantage of extremely high throughputs, stain etched substrates typically result in porous layers of low homogeneity and poor reproducibility making this technique difficulty applicable in an industrial environment [86]. This is mainly a consequence of the fact that in stain etching the already porosified porous layer is continuously attacked by the HF based solution as the process continues, so that the porous layer starts to dissolve for long etching times. It follows that the porosity of stain etched porous layers decreases with the depth of the porous layer [86].
This is not the case of electrochemical etching, where the already porosified region is fully depleted of holes and results hence passivated, so that thick porous layers can be realized without degradation of the pSi surface. In practice, however, together with electrochemical etching slow pure chemical dissolution of pSi in HF containing electrolyte occurs. Pure chemical etching of pSi does not require hole availability to proceed and its effect increases with increasing residence time of pSi in HF solutions. In contrast with stain etched porous layers, in electrochemically etched layers grown at fixed current density, and when pure chemical etching is negligible, the porosity increases with the thickness of the porous layer. This is a consequence of the reduced density of F^- ions which reach the pore tip for increasing depth of the porous layer.
In this thesis porous silicon will be investigated as possible buffer layer for germanium heteroepitaxy. Since the surface quality of the starting substrate is of foremost importance in epitaxial processes, only electrochemical etched porous layers will be here investigated.

3.2.1 Current-voltage characteristic

The traditional way to investigate the formation mechanism of pSi has been the study of the current-voltage (I-V) characteristic of the Si/electrolyte system during electrochemical etching [87, 88]. pSi is realized applying a difference of potential to a silicon substrate immersed in an electrolyte, which induce the formation of an electric current across the Si/electrolyte interface. At this interface, a specific chemical reaction occurs, allowing for the transformation of electronic current into ionic current and vice versa and making the realization of pSi possible. In Figure 3.1 an example of I-V curve for p-type and n-type doped Si substrates is reported, after Ref. [89]. Figure 3.1 shows qualitatively the I-V curves for moderately doped Si substrates, while the real shape of the curve is a function of the anodization conditions. The I-V curves are similar to those of semiconductor-metal junctions (Schottky diodes): under reverse polarization and in the dark only a small leakage current flows and breakthrough is observed at a specific voltage. However two main differences exist compared to the I-V curve of Schottky diodes. At first, the electrochemical reaction at the interface does not change while the sign of majority carriers changes with the type of doping. Secondly, the dark current observed in inverse polarization mode is typically much higher than that observed for Schottky diodes [87].
Under negative polarization, when the Si substrate acts as cathode of the electrochemical cell, electrochemical etching is not observed, neither for n-type nor for p-type wafers. In this case hydrogen evolution is observed on wafer surface, as a consequence of the reduction of water. On the other hand, when the Si substrate acts as anode of the electrochemical cell electro dissolution of Si occurs and pSi forms on wafer surface. In this regime, p-type electrodes in the dark and n-type electrodes under illumination behave in similar ways and two current maxima are observed in the corresponding I-V curve. When the current density across the Si/electrolyte interface exceeds a critical value which depends on etching parameters, electro polishing of Si occurs instead of porosification, leaving a smooth surface free of pores. The transition between the pore formation regime and the electro polishing regime occurs at the potential V_{ep} in correspondence of the first current maxima (the electropolishing peak), while above the second current maxima the system start to show oscillations.For p-type Si substrates, when $V < V_{ep}$, the I-V curve is similar to the exponential I-V curve of Schottky diodes. On the other hand, n-type Si is under reverse polarization and only a small dark current is observed in this case [90]. It follows that moderately doped n-type substrates require illumination of the Si wafer is order to achieve a not negligible current density during anodization [91]. The situation is different for highly doped n-type Si, as in this case the space charge region at the semiconductor/electrolyte interface is sufficiently thin that charges can tunnel across it.

As a consequence, highly doped n-type Si substrates with doping density $N_d > 10^{18}$ cm^{-3} does not require illumination for electrochemical etching resulting in the formation of mesoporous silicon layers [92].



a) b)

Figure 3.1: Typical I-V curve for the electrochemical etching of moderately doped a): p-type Si and b): n-type Si. After Ref. [89].

3.2.2 Theory of electrochemical etching

Three different types of electrolytes exist for electrochemical etching of Si, which can be distinguished in: aqueous electrolytes, organic electrolytes and oxidizing electrolytes [85]. Aqueous electrolytes are mainly mixtures of hydrofluoric acid (HF), ethanol (C_2H_4OH) and eventually water, acetic acid (C_2HOH) and glycerol ($C_3H_8O_3$). Organic electrolytes are mixtures of HF and organic solvents such as dimethilformamide (DMF) or acetonitrile (MeCN). Oxidizing electrolytes are composed by mixtures containing an oxidizing reagent but no HF. In this thesis porous silicon realized using aqueous electrolytes will be investigated, as these electrolytes are the more commonly used for pSi fabrication and do not contain organic solvents which are possible carcinogen. In general, depending on growing conditions different pSi morphologies can be observed, from a columnar one to a sponge-like one, while pore dimensions ranges over 4 orders of magnitude form about 1 nm to 10 μm. According to IUPAC classification, three different categories exist for pSi, depending on the average size of pores and inter-pore distance:

- Microporous Si, characterized by average pore size and interpore distance smaller than 10 nm,
- Mesoporous Si, characterized by average pore size and interpore distance comprised between 10 and 50 nm,

- Macroporous Si, characterized by average pore size and interpore distance larger than 50 nm.

The most important growth parameters for pSi formation, which determine pore size and interpore distance, pore morphology, thickness of the porous layer and etch rate are: the type of doping (p-type or n-type), the doping density, the crystallographic orientation of the Si substrate, the used electrolyte, the electrolyte volume ratio, the applied current density, the presence of front and/or backside illumination, the anodization temperature and the eventual stirring of the electrolyte during the electrochemical etching process. The effect of the main electrochemical etching parameters affecting pSi formation is summarized in Table 3.1 [87].

Table 3.1: The effect of the main electrochemical etching parameters affecting pSi formation

Increasing parameter	Porosity	Etch rate	Pore dimension
Current density	↑	↑	↑
% HF	↓	↑	↓
Etching time	↑	↓	
Wafer doping (p-type)	↓	↑	↑
Wafer doping (n-type)	↑	↑	

The current density is one of the main parameters affecting pSi morphology, porosity and etch rate and is the simpler parameter to control in order to obtain a stack of porous layers having different porosities. An increase in holes supplied at pore tip causes an increase in etch rate as well as an increase in porosity and pore dimensions. Depending on wafer doping and HF concentration, a critical current density exists above which electropolishing of Si occurs instead of electrochemical etching.

Concentration of HF in the electrolyte is another fundamental parameter in pSi formation: an increase in the % of HF leads to an increase in etch rate, as a larger number of F^- ions are available for Si electrodissolution. At the same time the porosity and average pore dimensions both decrease as a consequence of the higher availability of F^- ions at pore tips which promote the electrochemical etching to proceed in vertical direction [93,94].

Increasing the etching time leads to an increase in the average porosity of grown porous layers due to pure chemical dissolution of already formed pSi while the average etch rate decreases, as a consequence of the reduction of the concentration of HF at pore tips with

increasing thickness of the porous layer, caused by the hydrophobic nature of bulk Si. [95].

The reduction of HF concentration at pore tips with increasing pSi thickness also causes an increase in layer porosity as the anodization proceeds in depth, this effect being employed for lift-off of pSi layers without the need of a change in current density [96]

The concentration of doping has a strong impact of the resulting pSi morphology even though it does not affect the nature of the electrochemical etching process. In general heavily doped regions are attacked faster than lower doped regions. The electrochemical etching of heavily doped both p-type and n-type Si wafers leads to the formation of mesoporous layers, which is the kind of porous layer investigated in this thesis.

3.2.3 Electrochemistry of silicon

Different dissolution mechanisms have been formulated to account for the electrochemical etching and electropolishing of Si, all of them indicating that both mechanisms require the presence of holes at the Si/electrolyte interface. This depends on the fact that, when Si is immersed in a solution containing HF, its surface is hydrogen terminated [97]. When a hole reaches the Si/electrolyte interface, it can weaken the Si-H bond and hydrogen can be replaced with a fluorine ion (F^-) to form a Si-F bond. The polarization introduced by fluorine promotes the replacement of another hydrogen atom with a fluorine ion, causing the generation of hydrogen gas. The formed Si-F groups induce a further polarization which lowers the electron density of the Si-Si backbonds, which result weakened and are easily attacked by HF or H_2O molecules. During the formation of pSi, two atoms of hydrogen evolve for each atom of Si dissolved (Figure 3.2). The product of the reaction is SiF_4 which would leave the solution in gaseous form, but it reacts with two HF to from SiF_6^{2-} and two protons remaining in the solution [98].

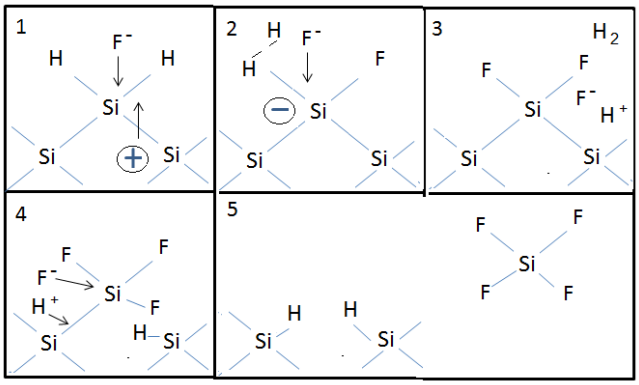


Figure 3.2: Reaction mechanism for the electrochemical etching of Si in HF solution. Adapted after Ref. [99]

Below the critical current density, the anodic reaction for pSi formation is [87]:

$$Si + 6HF \rightarrow H_2SiF_6 + H_2 + 2H^+ + 2e^- \quad (3.1)$$

while during electropolishing regime the reaction at wafer surface is:

$$Si + 6HF \rightarrow H_2SiF_6 + 4H^+ + 4e^- \quad (3.2)$$

When pSi is formed, the interpore region results fully depleted of holes, and is hence passivated from further electrochemical dissolution. The electrochemical etching only proceeds at the pore tips where holes are available.

3.2.4 Characterization of porous silicon layers

A very important parameter of pSi layers is the porosity *P,* defined as the volume fraction of the removed material i.e. the volume of the pores divided by the volume of the whole porous layer. The simpler method to calculate the porosity of grown pSi layers, which is the one employed in this thesis, consists in weighting the Si sample before and after electrochemical etching (obtaining $m_1$andm_2, respectively), and after the complete dissolution of the formed porous layer in a diluted solution of KOH or NaOH (obtaining m_3).
The porosity is than calculated using the equation:

$$P = \frac{m_1 - m_2}{m_1 - m_3} \quad 3.3$$

Employing gravimetric measurements, also the thickness *d* of the grown pSi layer can be easily assessed using the equation:

$$d = \frac{m_1 - m_3}{\rho_{Si} \times A} \quad 3.4$$

where ρ_{Si} is the silicon density and A is the etched surface.

Another important parameter, which determines how fast the etching front proceeds towards the bulk material, is the etch rate τ defined as:

$$\tau = \frac{d}{T} = \frac{m_1 - m_3}{\rho_{Si} \times A \times T} \qquad 3.5$$

where *T* is the duration of electrochemical etching process.

In this thesis grown pSi layers have been characterized through gravimetric measurements for porosity and thickness assessment, using electron microscopy to study the sample morphology and by means of X-Ray diffraction techniques to investigate their lateral homogeneity and strain distribution.

3.3 Porous silicon buffers grown at Ferrara University

3.3.1 Double tank etching cell

As a part of this thesis work, two double tank etching cells have been designed and realized for the formation of pSi layers having high lateral homogeneity, i.e. suitable for subsequent epitaxial growth. One cell has been designed to allow the growth of small surface area (3.8 cm^2) pSi layers on both small Si pieces or on entire 100 mm Si wafers, while the second cell has been designed to allow the porosification of whole 100 mm Si wafers.

The double tank etching cell configuration is chosen in order to obtain more homogeneous porous buffers in terms of thickness and porosity compared to typical pSi layers grown using single tank cells. In fact single tank etching cells, which geometry is simpler, typically suffer for low homogeneity of grown pSi layers as a consequence of a difference of potential existing between the top and the bottom of the Si substrate (which acts as anode of the cell), leading to different values of current density [87]. Single tank etching cells which do not employ the Si substrate as anode also exist, but in this case a metal backside contact is necessary, which would have been not compatible with subsequent epitaxial growth. In Figure 3.3 an image of the etching cell developed for the growth of small area pSi buffers is shown, together with a CAD drawing showing the cross-section of the realized cell. The etching cell is basically composed by two identical cylinders made of PolyTetraFluoroEthylene (PTFE) in order to be HF resistant. The Si wafer is placed in between the two cylinders and is sealed and held in place by two HF

resistant Viton® O-rings. The cylindrical shape of the cells allows the flow of a homogeneous current density through the substrate, which is of foremost importance for the realization of homogeneous porous layers. A circular opening is created in each cylinder at about 1 cm of distance from the Si wafer to allow the introduction of the electrodes in the electrolyte. The lateral caps of the etching cell are made of high-density polyethylene covered by a PTFE film to ensure chemical resistance to the electrolyte also for high HF concentrations. Four threaded rods and eight wing nuts made of nylon are used to create adhesion between the O-rings and the Si substrate. Used electrodes are made of high-purity graphite (>99.999%) in order to avoid metal contamination of pSi buffers from commonly used silver or platinum electrodes.

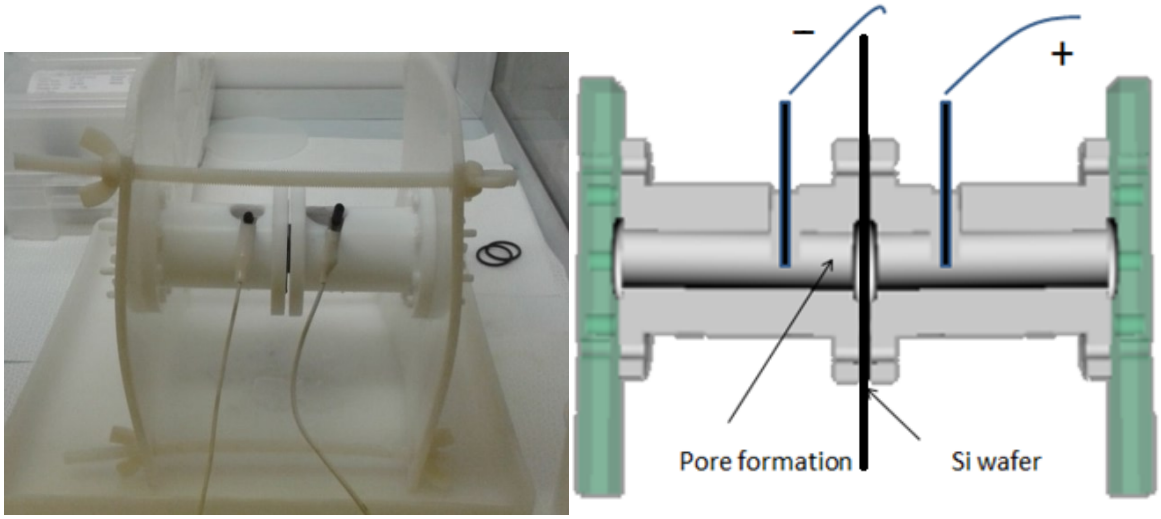


Fig 3.3: Image of the double tank etching cell developed for the electrochemical etching of small area pSi buffers (left) and CAD drawing showing the cross-section of the realized double tank etching cell.

Used electrolytes are different solutions of HF and ethanol (CH_3CH_2OH). Since hydrogen-terminated Si has a fairly hydrophobic surface, the addition of ethanol is necessary in order to reduce the surface tension and wet the substrate. Anodization of Si in solutions of HF and water without the addition of ethanol caused the growth of strongly inhomogeneous porous layers not suitable for subsequent epitaxy. The addition of glycerol, which increase the electrolyte viscosity possibly improving the buffer lateral homogeneity, if found to not improve noticeably the pSi buffer quality and is hence avoided.In the double tank configuration the Si substrate separates the two half-cells in which the graphite electrodes are immersed, forcing the current density to flow across it. On wafer front-side, which acts as secondary anode of the etching cell, the pSi layer forms. On the other hand on wafer backside, which acts as secondary cathode, proton reduction occurs causing the evolution of hydrogen.

First electrochemical etching experiments lead to strongly inhomogeneous porous layers, in particular for high current density in the order of 200 mA cm^{-2} or above, this result being attributed to the sticking of H_2 bubbles on wafer backside which hamper the flow of a homogeneous current density across the whole Si exposed area. As a consequence, a channel has been realized in the upper part of the etching cell in correspondence of wafer backside, in order to promote removal of desorbed H_2 hampering its sticking. This resulted in pSi layers with much larger lateral homogeneity suitable for subsequent epitaxial growth.

High current density values in the order of 200 mA cm^{-2} or above have been found to cause strong electrodissolution of the high purity graphite electrodes, causing the deposition of graphite on the bottom of the etching cell. On the other hand no strong electrodissolution has been observed for grown buffers employing current densities < 200 mA cm^{-2} for different concentrations of HF in the electrolyte, so that low current densities are preferable in terms of electrode lifetime and carbon contamination of grown buffers. Carbon contamination of pSi buffers, however, may not represent a major issue during subsequent epitaxy as germanium has a large tolerance to C, which in particular cases is deliberately added to Ge to form $Ge_{1-y}C_y$ alloys for lattice constant and bandgap engineering purposes [100]. In this work, when high current densities ($J \geq 200$ mA cm^{-2}) have been employed for the realization of the pSi buffers, the electrolyte has been replenished after each porosification process in order to ensure homogeneity of starting conditions for grown pSi layers. Otherwise, when no strong electrodissolution of the electrodes occurs, the electrolyte has been reused for several anodization processes as the mass removed from the Si substrate for each process is in the order of just few μg so that no significant changes in the pH of the electrolyte is expected, considering an electrolyte volume of about 70 ml in the etching cell. Changes in the pH of the electrolyte would in fact cause problems of reproducibility during electrochemical etching, modifying the physical parameters of grown samples.

At first, small Si samples have been anodized in order to investigate the physical properties of grown pSi layers as a function of growth parameters (wafer doping, electrolyte volume ratio, current density). After growth conditions for homogeneous and reproducible porous layers have been determined, different pSi buffers have been grown before Ge epitaxy on the same Si substrate. In this way it has been possible to investigate the effect of pSi buffer porosity on the Ge crystalline quality under the same growing conditions, and saving time and consumables.

The distribution of dopants in silicon wafers is typically not perfectly homogeneous, and this can in turn lead to local differences in thickness and porosity of grown pSi layers which results in differently colored adjacent regions. In Figure 3.4 a pSi patterned wafer is

shown, together with a magnified image showing a detail of one porous layer. Periodic color variations distributed along concentric rings are observed, which are attributed to a doping inhomogeneity characteristic of Si wafers, known as growth striations. As the doping density of the starting material strongly influences the parameters of grown pSi layers, striations introduce local variations in buffer thickness and porosity. Excellent doping uniformity of the starting Si substrate is hence a very important prerequisite for homogeneous electrochemical etching of Si.

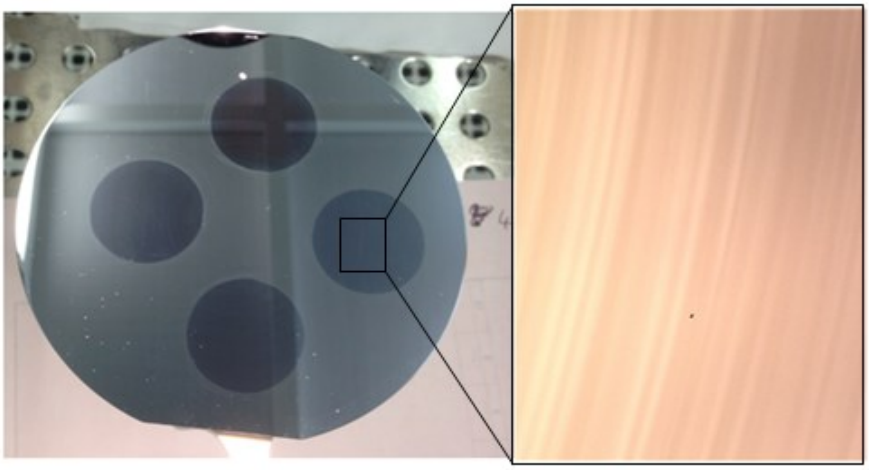


Figure 3.4: 100 mm n-type Si wafer (001) oriented with resistivity of 2.5 mΩ cm showing different porous buffers on its surface. A magnified image of one porous layer reveals the presence of striations in the starting Si substrate.

Good lateral homogeneity pSi buffers have been obtained for highly doped Si substrates both p-type and n-type, having a resistivity of 3.9 and 2.5 mΩ cm, respectively, and a relative resistivity variation across the surface area smaller than 2%. On the other hand, p-type Si substrates with relative change in resistivity as high as 4% or more resulted in strongly inhomogeneous pSi buffers having large local differences in porosity and thickness as observed by naked eye. Since a resistivity variation < 2% has been found to be necessary for homogeneous porosification of Si, this indicates a maximum resistivity variation <±0.005 mΩ cm is necessary for anodic etching of substrates with resistivity of 2.5 mΩ cm. As this value is too tight in view of high volume production [86], it follows that the use of highly doped Si wafers with larger resistivity than that of substrates here investigated could be advantageous.

To measure the bulk resistivity of starting Si wafers, four-point probe measurements are carried out using a Keithley 2400 Source Meter. Sheet resistance measurements are performed at wafer center and in different regions of the starting substrates close to wafer center in order to avoid edge effects. Sheet resistance $\rho_{\square}\left(\frac{\Omega}{\square}\right)$ is determined using the

equation $\rho_{\square}\left(\frac{\Omega}{\square}\right) = \left(\frac{\pi}{ln2}\right) x \frac{V}{I}$ where *I and V* are the injected current and measured voltage, which is valid in the approximation *s>>t* where *t* is the wafer thickness and *s* is the probe spacing. The bulk resistivity ρ is than determined using the equation:

$$\rho = \rho_{\square}\, x\, t \qquad 3.6$$

The values for *P* and *d* of different pSi layers obtained from gravimetrical measurements are reported in Figure 3.5, as a function of applied current density and keeping fixed the other growth parameters. *S*tarting substrate is a 3.9 mΩ cm p-type Si wafer.

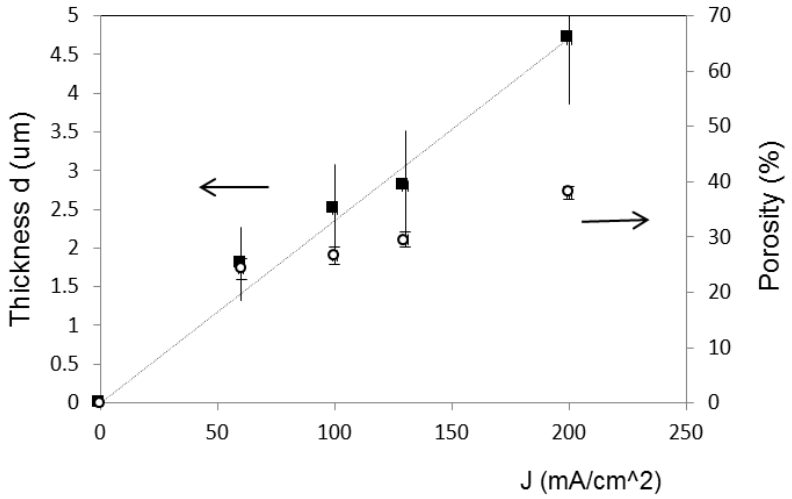


Figure 3.5: Thickness and porosity of grown pSi layers as a function of provided current density for 20s anodization time of 3.9mΩcm p-type Si (001) oriented with 6° offcut towards [111]. Used electrolyte is a solution of HF and ethanol in the volume ratio (3:1).

A linear increase in the thickness of the porous buffer is observed with increasing current density while maintaining fixed the other growth parameters. Also porosity increases with applied current density as a consequence of the higher availability of holes [101], and an almost parabolic-like dependence is observed in this case. The error bars reported in Figure 3.5 are obtained from the classical theory of propagation of errors considering an uncertainty of 1 mm on the radius of the surface area of grown porous layers and an uncertainty of 30 µg on the gravimetrical measurements performed using a Sartorius CP-225D high precision balance. Similar behaviors for both porosity and thickness have been found for the other buffers grown in this work for increasing current density.

3.4 Microscope analysis of grown porous buffers

Cross section SEM and TEM analysis of grown pSi layers is carried out to directly measure their thickness and to obtain information about sample morphology. At first, four different pSi buffers having porosity of 22%, 30%. 40% and 48% have been investigated to assess the effect of pSi buffer porosity on the crystalline quality of epitaxial Ge subsequently grown on top of them. Low magnification cross section SEM images of 22%, 30%, 40% and 48% pSi layers are reported in Figure 3.6, showing a sponge-like morphology for all grown layers.

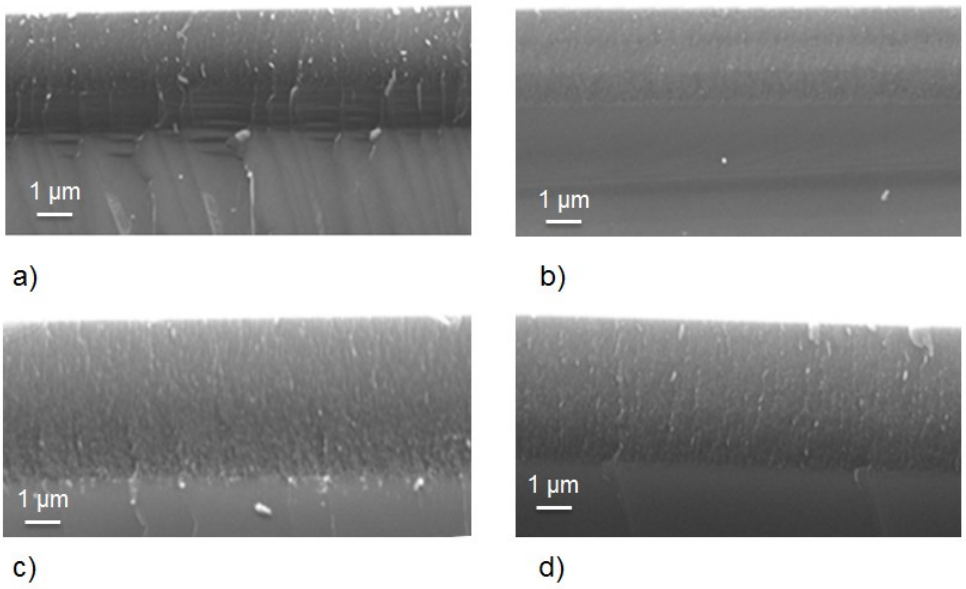


Figure 3.6: Low magnification (20K) cross-section SEM images of a) 22% pSi, b) 30% pSi, c) 40% pSi and d) 48% pSi.

A magnified image of 22% and 48% pSi buffers is reported in Figure 3.7 showing in detail the pore morphology. Both samples have pores of about 5 - 15 nm and a much larger density of pores is observed for the higher porosity buffer.

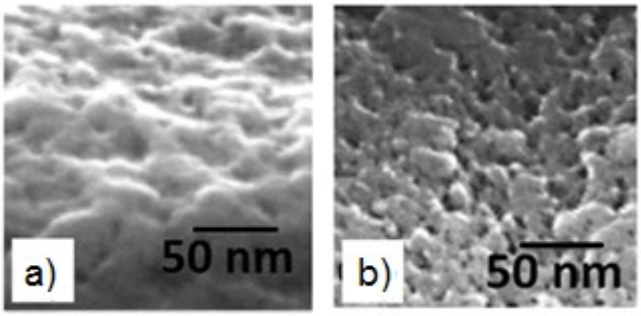


Figure 3.7: Magnified SEM image of a) 22% pSi and b) 48% pSi showing the pore morphology.

High-magnification bright field XTEM images of 22% pSi are reported in Figure 3.8. A very large pSi surface roughness with a peak-to-valley distance of ~40 nm is observed for the as-grown porous layer. Moreover, despite growth parameters have not been changed during Si anodization, the first 150 nm of the grown porous layer shows a higher porosity compared to the bottom part of the same layer. In the insets magnified images of the top and bottom part of the porous layer are reported. The top part of the pSi layer shows pores ~10 nm in size, which is consistent with the dimensions of pores observed in Figure 3.7. On the other hand the bottom part of the pSi layer shows a smoother surface with very small pores having sizes of few nm. The interface between the top and bottom morphologies is not perfectly flat and a peak-to-valley distance of several tens of nm is observed. Although the pSi layer reported in Figure 3.8 is etched for a short anodization time of 30 sec. to reduce the effect of pure chemical etching on already formed pSi, the higher porosity observed in the top part of the grown pSi layer actually indicates its contribution on the pSi resulting morphology is not negligible.

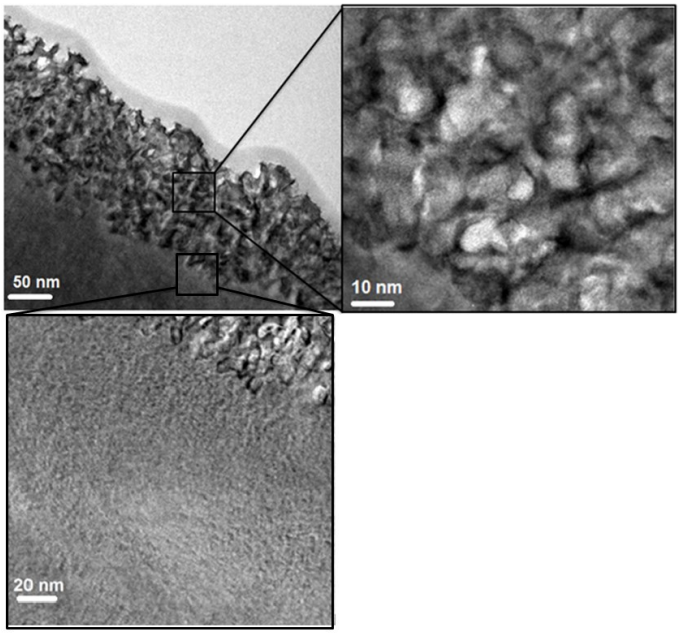


Figure 3.8: Bright field XTEM micrographs of as-grown pSi having porosity of 22%

High-temperature annealing is known to promote strong morphological reorganization of pSi, driven by energy minimization [102]. The change in morphology for the 22% pSi layer is investigated after 1 hour annealing at 500°C in H_2 atmosphere and at the pressure of 2 x 10^{-2} mbar, carried out within the same LEPECVD reactor used for Ge heteroepitaxy. Annealing is carried out in a non-oxidizing atmosphere as the presence of native oxide on the internal surface of pSi strongly reduces the mobility of Si atoms thus hampering reorganization [103]. In Figure 3.9 XTEM images of annealed 22% pSi are shown. After annealing the thickness of the more porous pSi layer is almost doubled to

about 300 nm indicating vacancies have diffused from the less porous region to the upper part of pSi. Moreover, a smooth region about 50 nm in thickness almost free of pores is observed at pSi surface after annealing. This effect is attributed to the diffusion of vacancies at the pSi surface, which acts as a sink for voids [104].

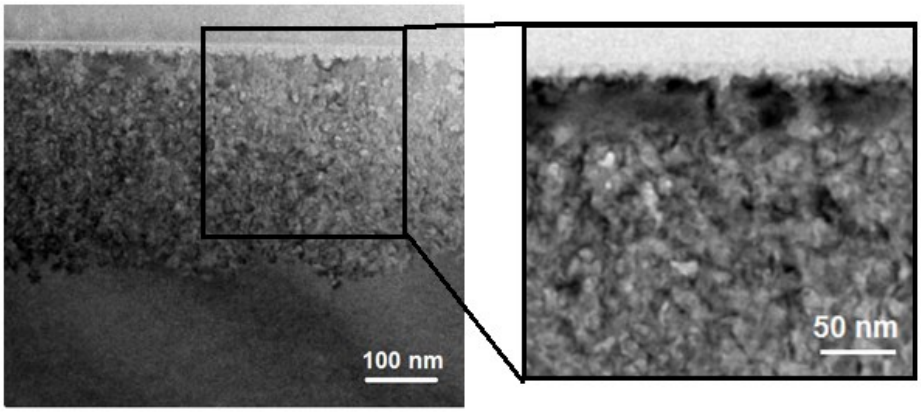


Figure 3.9 XTEM micrographs of annealed 22% pSi showing a region almost depleted of pores at pSi surface

Scanning TEM (STEM) images of 22% pSi collected after annealing are reported in Figure 3.10. Figure 3.10 a) confirms the existence of a porosity gradient in the grown pSi layer. Image analysis carried out using ImageJ® software indicate porosity levels of ~25% and ~18% for the more and less porous regions, respectively, which is in accordance with the porosity of 22% determined before annealing.

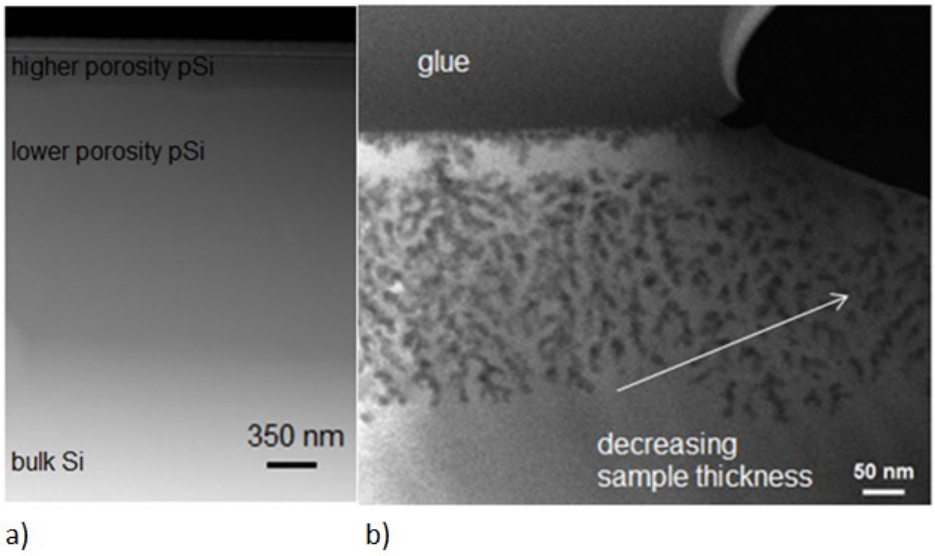


Figure 3.10: a) low magnification STEM image of annealed 22% pSi showing a porosity gradient within the grown buffer and b) high magnification STEM image of the top part of annealed 22% pSi.

Figure 3.10 b) reveals that, although the pSi top layer results almost fully depleted of pores, small sized pores are still present in the topmost ~10 nm of pSi. This incomplete reconstruction of pSi is ascribed to the low employed annealing temperature of 500°C, which is smaller than the temperature for which complete pSi reconstruction is observed in the order of 1000 °C [105].

In right side of Figure 3.10 b), which is the region where the sample is thinner as a consequence of ion bombardment during the mechanical preparation, large isolated spheroids are visible with average size of several tens of nm. This again confirms strong morphological reconstruction of the porous layer occurred during annealing. The physical reason for the observed morphology resides in the fact that at high temperature the pores try to minimize their surface energy by transforming into larger voids having a smaller surface to volume ratio, in a process called Ostwald ripening [104]. Moving on the left side of Figure 3.10 b), the thickness of the porous layer investigated with STEM increases. Here spheroids lying in different planes parallel to the cross-section overlap each other, giving the idea of a columnar morphology. The upper part of the lower porosity layer shows a compact layer with no strong evidence of pore presence, which is attributed to void migration from the low porosity layer to the higher porosity layer driven by surface energy minimization.

When pSi is used as a starting material for subsequent Si homoepitaxy, the formation of a smooth layer free of voids at top pSi surface is typically desired in order to obtain a smooth epilayer [106]. However, the epitaxial growth of lattice mismatched semiconductors on the rough surface of as-grown pSi could result in the introduction of some air/semiconductor interfaces at the growth interface, which could eventually block dislocation propagation preventing their threading in the upper part of grown epilayers in a similar way to what is observed using not maskless substrate pattern techniques [8].

In this thesis Ge epitaxy is directly performed on the rough surface of as-grown pSi without any intermediate high-temperature annealing step. It is the aim of this work to investigate whether an improvement in Ge crystallinity and in particular a reduction in TDD can be achieved by taking advantage of pSi deformation during epitaxy and/or of the eventual introduction of dislocation blocking interfaces at the heterointerface. In the next Chapter the growth of Ge on different pSi buffers will be investigated to understand if and how one or both of these mechanism could improve the Ge crystalline quality and the role of the main buffer parameters in this improvement.

Chapter 4

Ge epitaxy on porous silicon buffer layers

4.1 Introduction

Group IV porous semiconductors have been widely investigated in the last years as the enabling technology for layer transfer of homoepitaxial epilayers grown on thick substrates. In particular, pSi double layers have attained great interest because of the possibility to grow high-quality silicon on insulator (SOI) structures [107] and large-area thin-film Si solar cells for substrate reuse, thus reducing the fabrication costs [108,109]. In this process a low (~20%) porosity pSi layer few μm-thick is grown at the top of the Si substrate followed by a higher porosity (≥~40%) layer, which is typically obtained by increasing the current density during the electrochemical etching process. After anodization of the Si substrate a high-temperature annealing promotes the formation of a smooth surface at the top of the low porosity layer, which serves as seed layer for the subsequent homoepitaxial growth. On the other hand, the higher porosity buffer reorganizes during annealing in a layer with large cavities separated by thin Si columns, making the entire structure suitable for lift-off [110]. In analogy to the pSi double-layer process, porous germanium double layers have been proposed as starting material for the epitaxial growth of lattice matched GaAs, for lift-off of III-V solar cells from expensive Ge substrates [111].

More recently, porous silicon (pSi) has been also proposed as possible buffer layer in the epitaxial growth of lattice mismatched semiconductors on Si, such as Ge [105, 112-116] and GaAs [117]. As a consequence of its soft and compliant nature, pSi could deform during epitaxy this effect possibly accommodating part of the lattice mismatch existing between the Si substrate and the lattice mismatched epitaxial layers. The Young's and shear moduli of pSi, which determine its main mechanical properties, can be varied over more than one order of magnitude [118] by simply modifying the growth parameters, thus allowing for the realization of a large variety of porous buffers having very different physical properties.

If TDD within Ge epitaxial layers grown on Si can be sufficiently reduced using porous silicon layers, it follows that pSi could represent the ideal buffer for Ge integration on Si wafers. This depends on the fact that pSi offers several advantages compared to the other existing techniques for low dislocation content Ge epilayers on Si reviewed in Chapter 2. At first, the electrochemical etching of Si to produce pSi is a low-cost maskless process which can take advantage of very-high throughputs. The physical and mechanical properties of pSi can be finely tuned by simply modifying the growth parameters, the electrochemical etching of Si to produce pSi does not require costly machinery, and the fabrication process does not introduce new foreign chemicals in the semiconductor industry. Moreover, pSi layers with thickness variation < ±1% have been demonstrated for large wafer sizes up to 300 mm [119] making the epitaxial growth of Ge on pSi suitable for large-scale fabrication and compatible with recently developed MOCVD reactors for the epitaxial growth of III-V semiconductors on 300 mm substrates. In addition, the use of pSi would also enable layer transfer of deposited epilayers by employing a low-porosity high-porosity pSi double layer, which could be of interest for very-low thermal and electrical impedances substrates and for eventual reuse of large area Si wafers which could further reduce the fabrication costs. In addition, thanks to the compliant nature of pSi, crack formation due to the large thermal expansion coefficient mismatch existing between Ge and Si can be prevented [120].

The main advantages of using pSi as a buffer for low TDD Ge on Si VSs are of particular importance when Ge on Si substrates are to be used as a platform for high-efficiency and low-cost multijunction solar cells on silicon. Very high-throughputs and low fabrication costs are mandatory in this case, as the final cost of a PV technology plays a fundamental role in determining its success [121]. Moreover, multijunction solar cells are large area devices compared to other Ge based devices in the semiconductor industry, and hence a technique able to reduce uniformly the density of threading defects over an area of several squared millimeters is necessary.

Up to date only very few works exist concerning the growth of Ge on pSi and a systematic investigation of how the main parameters of porous buffers affect the crystalline quality of epitaxial Ge, and if TDD within Ge epilayers can be reduced by using pSi is not provided yet to our knowledge. In the next Paragraphs those aspects will be investigated.

4.2 The effect of pSi buffer porosity on the Ge crystalline quality

4.2.1 HR-XRD and SEM analysis

In porous silicon the space parameter for pore formation is broad, and porous layers with very different pore size (from few nm up to several μm) and morphologies (sponge like or columnar, with or without branches) can be grown by simply modifying the growth conditions. As a consequence, together with the epitaxial growth parameters, also the conditions employed during electrochemical etching strongly influence the crystalline quality of epitaxial films grown on top of pSi.

One of the main parameters of pSi layers, which strongly influence the mechanical, optical, transport, absorption and reorganization properties of grown layers, is the porosity. Layer porosity plays a fundamental role in the lift-off process of lattice matched semiconductors grown on porous semiconductors double-layers, determining the crystalline quality of the grown epilayers and enabling layer transfer [110]. In analogy to this, the porosity of pSi buffer layers could also play an important role during Ge epitaxy, giving rise to different relaxation mechanisms of the Ge epilayers and hence affecting the Ge crystalline quality.

To investigate the crystalline quality of Ge as a function of pSi buffer porosity, 5 μm-thick Ge epitaxial layers are grown on different porosity pSi buffers and obtained results are compared with those for Ge directly grown on bulk Si under the same growing conditions. The Ge deposited thickness is selected in order to investigate the possible use of Ge on pSi virtual substrates as a platform for high-efficiency III-V solar cells integrated on silicon. However, obtained results are general and can result useful and be exploited also for different applications. pSi buffers with maximum porosity of 48% have been considered in this thesis, higher porosity values being excluded to avoid possible self-delamination of the epilayer which would lead to contamination of the growth chamber.

Starting substrates have been very-highly boron doped (2-20 mΩ cm) and phosphorus doped (< 5 mΩ cm) 100 mm Si wafers (001) oriented with 6° offcut toward [111] to allow the subsequent growth of APDs-free GaAs on grown VSs. Very highly doped substrates have been selected as starting material as the homogeneous anodization of such substrates does not require the formation of an ohmic contact on wafer backside and, for n-type wafers, no illumination is required. The formation of a metallic ohmic contact on wafer backside would have been not compatible with subsequent LEPECVD growth, while the formation of an ohmic contact through ion implantation would have increased the complexity of the process. In addition, the electrochemical etching of highly doped p-type and n-type substrates is known to produce mesoporous silicon (mpSi), which is

considered the ideal kind of porous layer for successive epitaxial growth [122]. Finally, the pores in mpSi have the correct dimensions (2-50 nm) to eventually allow the diffusion of Ge in the porous network. Filling of the porous network of mpSi during Ge epitaxy, which has been observed using both CVD [114] and MBE [115] deposition tools, could modify the lattice constant of the buffer layer thus possibly contributing in alleviating the lattice mismatch existing between Ge and Si and resulting in a smaller TDD.

To investigate the effect of pSi buffer porosity on the crystalline quality of the Ge epilayers grown on top of them, the growth parameters for pSi formation have been finely tuned in order to obtain four porous layers having different porosity levels and similar thickness vales. pSi buffers having a surface area of 3.8 cm^2 have been grown in different areas of the same substrate by electrochemical etching in the dark using the developed home-made double tank etching cell described in Chapter 3. pSi buffers are grown at the same radial distance from wafer center in order to ensure uniformity of growing conditions during subsequent Ge epitaxy. This aspect is of great importance in order to understand how different buffers affect the Ge crystalline quality, as variations in the Ge deposited thickness as high as 25% have been observed between wafer center and wafer side In the first epitaxial experiments on bulk Si. An image of a patterned wafer showing four different pSi buffers on its surface is shown in Figure 4.1.

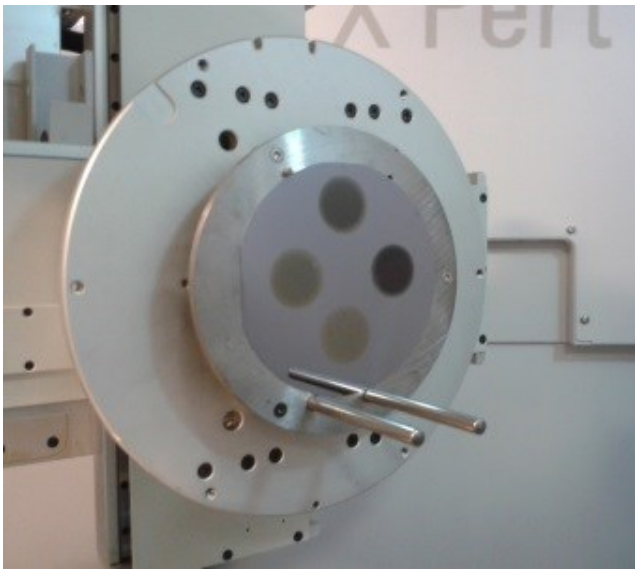


Figure 4.1: Different pSi buffers having porosity values of 22%, 30%, 40% and 48% grown on the same 100 mm Si wafer (001) oriented.

The different pSi buffers have been grown using various solutions of HF and ethanol at different concentration ratios and different current densities, supplied by a Keithley 2400 SourceMeter. The growth parameters of the different porous buffers retrieved from weighting the sample before electrochemical etching and before and after pSi dissolution

in KOH solution as described in Chapter 3 are reported in Table 4.1. For the electrochemical etching of 40% and 48% pSi buffers the ethanol content in the electrolyte has been increased as the solely increase of the current density would have led to much smaller porosity/thickness ratios for the grown buffers, making more difficult to just investigate the effect of buffer porosity on the crystalline quality of the Ge epilayers.

Table 4.1: Growth parameters of electrochemical etched pSi samples (p-type, nominal resistivity 2-20 mΩ cm) and their physical parameters determined by gravimetric measurements.

Electrolyte volume ratio (HF:ethanol)	Current density (mA/cm^2)	Etching time (s)	Porosity (%)	Thickness (μm)
3:1	40	30	22	2.5
3:1	130	20	30	3.2
5:2	250	15	40	4.3
3:2	250	17	48	4.5

Grown pSi buffers have been characterized using gravimetrical measurements to assess the porosity value and thickness, SEM and XTEM for analysis of the morphology and a direct measure of the buffer thickness and HR-XRD for lattice constant assessment. Successively, grown Ge on pSi and on Si VSs are characterized using SEM and XTEM for morphology and defects observation, HR-XRD for lattice constants and crystalline quality assessment and EPD and plan view TEM imaging for defect visualization. HR-XRD measurements are carried out using Panalytical X Pert PRO MD four circle diffractometer; Cu k Alpha 1 radiation having a wavelength of 1.54056 Å is selected using a four bounce Ge (220) Bartels monocromator.

An Omega/2Theta scan of as-grown pSi buffers collected around the (004) diffraction peak of bulk Si is shown in Figure 4.2. For all grown buffers the diffraction peak of pSi is found at smaller diffracting angle than that of bulk Si, indicating that the out-of- plane lattice constant of pSi is larger than that of Si. This is attributed to a compressive strain of the porous layer in the in-plane direction, caused by the absorption of OH groups on the inner surface of pSi [114]. The angular difference between the peak of pSi and bulk Si increases with the porosity of the pSi buffer, indicating that the out-of-plane lattice constant of pSi increases with porosity. This is attributed to the increase in the internal surface of pSi available for hydrogen bonding with porosity [123]. On the other hand pSi is lattice matched to bulk Si in the in-plane direction, independently on the buffer porosity, as observed from (004) reciprocal space maps (RSMs) of grown buffers not reported here.

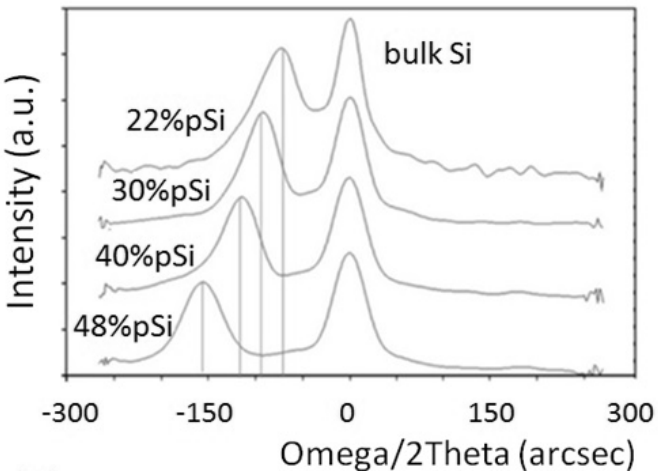


Figure 4.2: Omega/2Theta semi-log plot of the (004) diffraction peak of as-grown pSi samples.

The thickness of grown pSi layers has been measured by secondary-electrons SEM imaging of the cross section of the specimens, reported in Chapter 3. Grown samples show a sponge-like structure typical of mesoporous silicon layers and no evident variations in sample morphology are observed between the different samples. The measured thickness of the porous buffers and their porosity are reported in Table 4.2, together with the relative lattice constant variation in the out-of-plane direction and the pSi full width at half maximum (FWHM) retrieved from Figure 4.2. For all grown buffers the FWHM of pSi is comparable with that of bulk Si (14 arcsec), indicating that a homogeneous stress is introduced in all the pSi layers and thus confirming their high lateral homogeneity. Form the lattice constant variation of pSi in the out-of-plane direction a strain in the buffers which increases almost linearly with increasing porosity is observed.

Table 4.2. Physical parameters of grown pSi buffers.

Porosity (%)	Thickness (μm)	Lattice constant relative variation $\Delta a_{\perp}/a_{Si}$ x 10^{-4}	FWHM of pSi peak (arcsec)
22	2.3	5.2	19
30	2.6	6.4	17
40	3.9	7.8	17
48	4.1	10.9	19

The values of thickness of the pSi buffers obtained from gravimetrical measurements and reported in Table 4.1 are in accordance (by considering the instrumental errors) with

those obtained through SEM imaging and reported in Table 4.2, thus confirming the goodness of the obtained pSi porosity values.

The thickness of the grown pSi buffers is selected in order to eventually allow the subsequent detachment of Ge epilayers from the Si substrate by employing a selective etching technique able to attack faster the porous region compared to the bulk material. Investigation of how pSi buffer thickness affects the Ge crystalline quality is reported in Par. 4.3.

After electrochemical etching the substrates have been rinsed in deionized water, dried under N_2 flux, cleaned in diluted HF (2.5%) for 30 seconds to remove the native oxide and dried again using N_2. After that the Si wafers have been readily inserted in the load lock to avoid surface contamination. Once in the load lock, the substrates have been heated at 200°C for 25 minutes using IR lamps in order to promote the desorption of water from wafer surface and of the electrolyte from pSi internal surface. The same desorption time of 10 minutes employed for the desorption of bulk Si wafers resulted in amorphous or strongly polycrystalline Ge epilayers on pSi, which has been attributed to the presence of the much larger quantity of adsorbed species on the wide pSi internal surface. After loading the substrate in the main chamber of the LEPECVD reactor, few minutes are necessary before the base pressure of 2×10^{-8} mbar is restored. The substrate is than heated to 500°C with an average rate of 25°C/minute.

Before Ge epitaxy, H_2 plasma etching is performed for 5 minutes in order to remove residual contaminants from Si wafer surface and prepare it to epitaxy. Amorphous Ge epilayers were obtained removing the H_2 plasma etching step before epitaxial growth, indicating that residual contaminants remain on Si wafer surface after HF cleaning, hampering successive epitaxy. While residual adsorbed species on Si wafer surface may act as contaminants requiring the plasma etching step for their complete removal before epitaxy, the use of higher annealing temperatures to promote desorption within the growth chamber still resulted in an amorphous Ge growth in absence of H_2 plasma cleaning. Further investigation is ongoing in order to understand this effect.

The most important aspect in growing Ge on Si and on pSi is to obtain good crystalline quality from the beginning of the crystal growth, as the first nm of deposited Ge strongly influences the crystalline quality and defect propagation in the upper part of the epitaxial layer. In order to obtain high Ge crystalline quality at the beginning of the epitaxial growth, while maintaining a high growth rate, Ge epitaxy is performed by using a double step approach developed at Ferrara University in collaboration with Dichroic Cell s.r.l.. At first, a thin Ge seed layer~150 nm in thickness is deposited at the reduced growth rate of about 0.5 nm/sec in order to achieve high crystal perfection by employing a low plasma power of 350 W. Successively, the growth rate is increased to 2 nm/sec in order to

maximize the throughput by increasing the power of the plasma up to 1000 W for the subsequent Ge thickness of 4.8 µm. During epitaxy the growth temperature is kept constant at 500°C.

(004) Omega/2Theta scans for Ge grown on Si and on pSi buffers are shown in Figure 4.3. Each scan shows a sharp high intensity peak at large diffraction angle corresponding to bulk Si and a broader peak at smaller angle corresponding to Ge. From the latter a monocrystalline growth of Ge is deduced for all samples. The Omega/2Theta scans of Ge grown on pSi also show the diffraction peaks arising from the porous buffers, close to the bulk Si peak and having a lower intensity. The growth of Ge on low porosity buffers (Figs. 4.3 b) and c)) results in an improvement in the Ge crystalline quality compared to Ge grown on bulk Si, as deduced from the sharper Ge diffraction peak. For Ge grown on buffer porosities of 30%, 40% and 48%, a single pSi peak, at smaller diffracting angle than that of Si, is visible. For these samples a small shift of the pSi peak toward larger diffraction angles is observed after epitaxy ($\Delta a_{pSi\perp}/a_{Si} \sim 10^{-4}$), which is attributed to the desorption of OH groups which is expected at temperatures higher than 350°C [102]. On the other hand two different peaks are found after epitaxy close to that of the substrate and at larger diffracting angle for Ge grown on the 22% buffer (Figure 4.3. b)), indicating the presence of two porous sublayers with smaller out-of-plane lattice constant than that of Si. The lattice mismatch in the out-of-plane direction retrieved from (004) Omega/2Theta scan is 0.076% and 0.21% for the less strained and the more strained pSi sublayer, respectively. This corresponds to a relative lattice constant variation after epitaxy about one order of magnitude larger than that observed for higher porosity buffers.

The diffraction peak of annealed 22% pSi in case of no epitaxy has been superimposed to the collected Omega/2Theta scan in Figure 4.3 b). The porous buffer has been annealed under the same temperature conditions employed during Ge epitaxy in order to attribute the change in the strain state of pSi either to the epitaxial process or to high temperature annealing. After annealing, but in case of no epitaxy, the pSi peak is still at the left of the bulk Si peak, indicating that its splitting and shift towards larger diffracting angles observed after epitaxy cannot be ascribed to the desorption of adsorbed species. The observed effects can neither be ascribed to the formation of SiGe alloys at the Ge/pSi interface, since in this case the resulting lattice constant and the corresponding diffraction peak would have been in between that of Si and Ge.

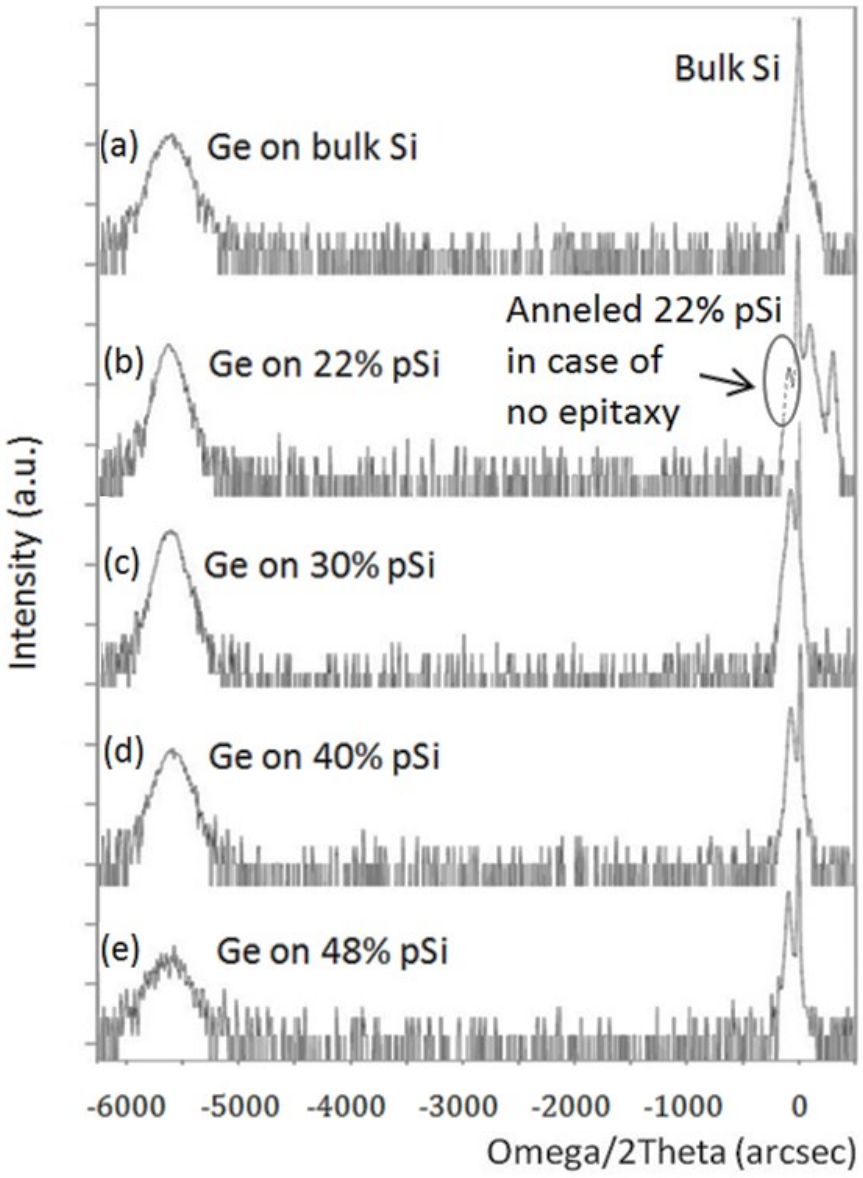


Figure 4.3: a) – e) Omega/2Theta semi-log plot of the (004) diffraction peak of Ge grown on Si and on pSi. In Figure 4.3 b) the diffraction peak of annealed 22% pSi in case of no epitaxy has been superimposed to the collected Omega/2Theta scan. After epitaxy a single pSi peak at small diffracting angle is observed for all samples except Ge on 22% pSi, which shows two peaks arising from pSi at large diffracting angle indicating separation of pSi in two sublayers and contraction in the out-of-plane direction.

The only explanation consists in considering the 22% pSi buffer has been tensile strained during epitaxy, as a consequence of the in-plane tensile stress introduced on pSi by the uppermost Ge epilayer having a larger lattice constant. Due to tensile strain the out-of plane lattice constant of pSi results reduced and the Ge crystalline quality improves, since the lattice mismatch between Ge and Si results partially accommodated at the Si/pSi interface. This indicates that not all the accumulated strain as the growth proceeds is relaxed by plastic deformation of the epitaxial layer accompanied with generation of MDs and associated TD segments, as occurs for lattice mismatched epitaxy on bulk substrates due to the typically much larger thickness of the substrate compared to that of grown epilayers. The use of a low porosity pSi buffer introduces a deformable layer within the substrate which can strain in order to absorb part of the lattice mismatch existing between the substrate and the epilayer. It follows that also the substrate participates in strain accommodation in this case, so that the nucleation of a lower density of defects within the epitaxial layer is necessary for complete Ge relaxation.

Increasing the porosity of the pSi buffer the Ge diffraction peak becomes broader, indicating a degradation of the Ge crystalline quality. This result can be interpreted by considering Figure (4.4), which shows the cross section SEM images of Ge grown on low porosity (22%) and high porosity (48%) pSi buffers. Figure 4.4.a) and b) show that, on a micrometer scale, the Ge film is rather homogeneous and the Ge/pSi interface is uniform independently on buffer porosity. The parallel lines visible in both samples are artifacts introduced during substrates grinding and polishing and do not represent the actual morphology of the samples. While at low magnification the 22% porosity buffer looks like a compact layer, the 48% buffer shows several cracks and fractures indicating a much more fragile layer. In Figure 4.4 c) a magnified image of the Ge/22% pSi interface is reported, showing an almost planar interface also on a nanometric scale. Very small pores with sizes of few nm and large valleys are visible in the buffer, indicating reconstruction of pSi occurred during epitaxy at the temperature of about 500°C. A magnified image of the Ge/48% pSi interface is reported in Fig 4.4 d), showing a wavy interface and indicating either a not homogeneous growth of pSi or an inhomogeneous deformation of the porous buffer during epitaxy.

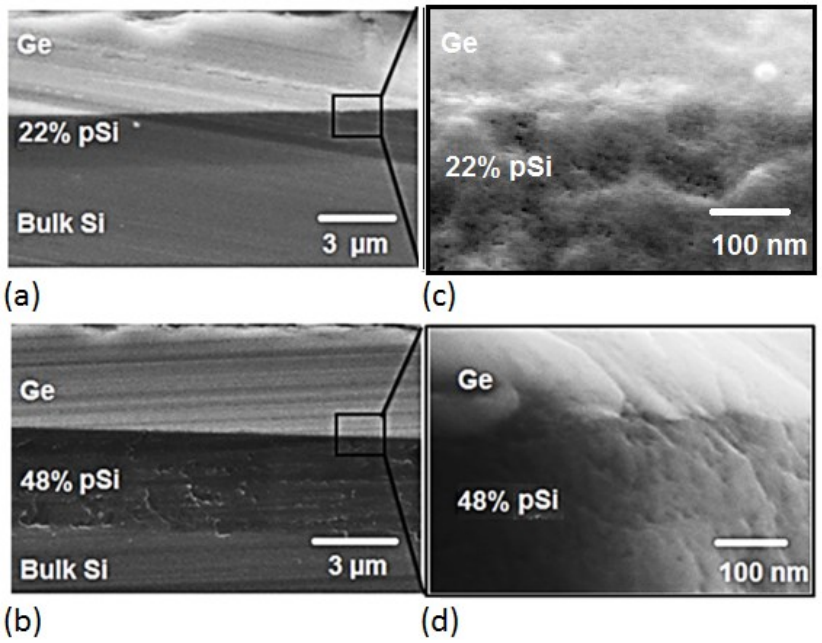


Figure 4.4: a) and b) cross section SEM images of Ge grown on 22% and 48% porous buffers. c) and d): magnified SEM images of the Ge/pSi interfaces.

Obtained results indicate that in the investigated porosity range the best crystalline quality is obtained for Ge grown on the less porous and hence less compliant substrate. While low porosity buffers (P ≤ 30%) resulted in an improvement in the Ge crystalline quality compared to Ge grown on bulk Si, the growth of Ge on 40% and 48% pSi resulted in a degradation if the Ge crystallinity. This is attributed to the low fragility of the 22% porosity buffer which, having a Young's modulus about 54% that of bulk Si [118], is still sufficiently compliant to be strained accommodating part of the lattice mismatch between Ge and Si. On the other hand, higher porosity buffers, which could take advantage of even smaller Young's moduli and hence of a more compliant matrix, are too fragile to strain under the in-plane tensile stress introduced by Ge. For such fragile structures the stress introduced by Ge can lead to local collapses of the porous network (as shown in Figure 4.4 d)), which is considered the main cause for the growth of a more disordered Ge epilayer (Figure 4.3 e)). There is no evidence of the formation of air/semiconductor interfaces in the bottom part of the Ge epilayer neither for low nor for high porosity buffers, so that that this mechanism is not considered to have a role in Ge on pSi epitaxy. This is attributed to the large compliance of pSi which deforms during Ge epitaxy even for low (22%) porosity of the investigated buffer.

In Figure 4.5 a magnified cross-section SEM image of as-grown Ge on 22% pSi is reported. Small pores with dimensions of few nm are found in the Ge epilayer, which have been found to be almost confined in the first ~100 nm. Pore presence in Ge depends on the fact that the Ge epilayer acts as a sink for the vacancies in pSi, causing void migration from the porous buffer to the Ge epilayer during pSi reorganization at high

temperature [124]. Pore presence in Ge could negatively affect transport properties introducing preferential recombination sites and reducing the average minority carrier lifetime. However, due the very small size and low density of observed pores, as well as their confinement close to the interface, the presence of pores within Ge may actually not represent a major issue in Ge epitaxy on pSi. Moreover, the introduction of a high temperature annealing step of the pSi substrate before Ge epitaxy could suppress void migration within grown epilayers by promoting depletion of pores in the upper part of pSi [110].

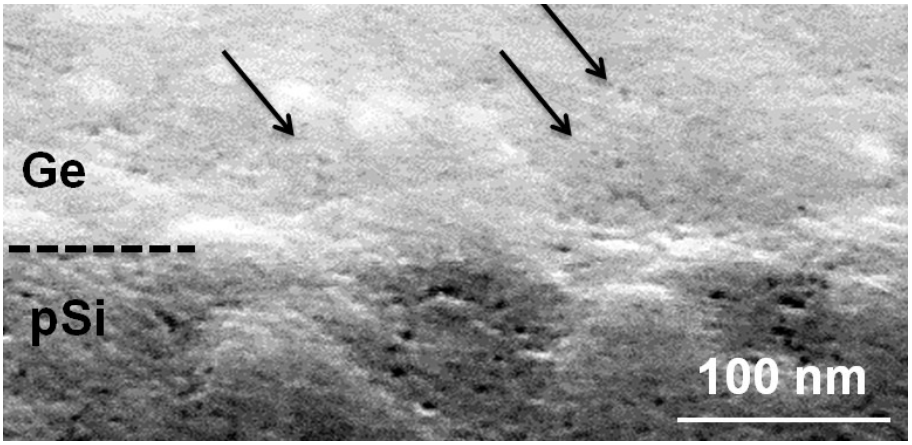


Figure 4.5: Cross-section SEM images of the Ge/22% pSi interface. The arrows indicate small voids in the bottom part of the Ge epilayer.

EPD analysis is carried out to assess the TDD at the surface of grown Ge epilayers. Alternate Secco etch is used to reveal the etch pits, which consists in a solution of HF and CrO_3 (0.15M) in the volume ratio 2:1. SEM plan view images collected after defect etching for Ge grown on bulk Si and on 22% and 30% pSi buffers are reported in Figure 4.6. Fewer defects are visible at the top surface of Ge grown on 22% and 30% pSi compared to those obtained for Ge on bulk Si. Particle contaminants is visible at Ge surface for Ge on 22% and 30% pSi, increasing the difficulty in TDD assessment. For quantitative analysis, TDD is obtained by averaging the etch pits counts obtained from two different images of the same sample. The obtained density of etch pits for Ge on bulk Si and on the different investigated pSi buffers is reported in Table 4.5, together with the results of HR-XRD measurements.

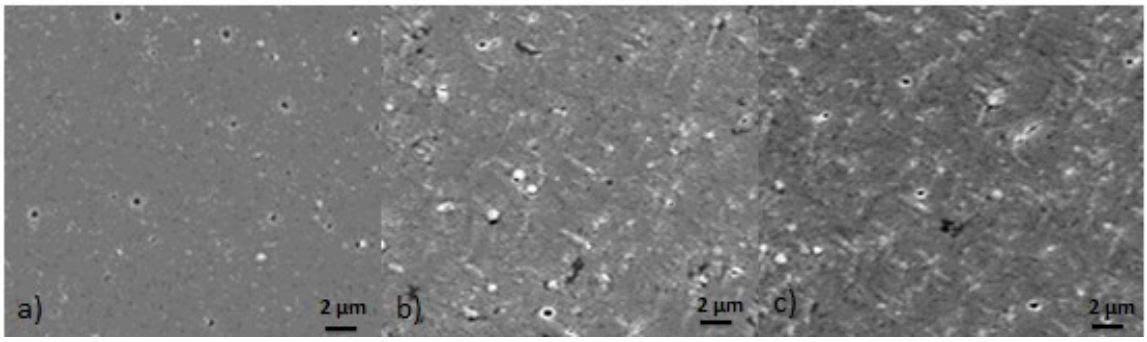


Figure 4.6: Plan-view SEM images of sample surface after EPD analysis for Ge grown on a) bulk Si, b) 22% pSi, c) 30% pSi.

4.2.2 Reciprocal space maps analysis

The in-plane ($a_{Ge||}$) and out-of-plane ($a_{\mathrm{Ge}\perp}$) Ge lattice constants of grown Ge on Si and on pSi VSs are retrieved from symmetrical (004) and asymmetrical (224) RSMs of grown samples, by considering the bulk Si reciprocal lattice point (RELP) as an un-strained internal standard with lattice constant $a_{\mathrm{Si}} = 5.4307$ Å. Each RSM is collected by carrying out several coupled Omega/2Theta scans for a range of incident angles Omega ± iΔOmega with i=0,1,2,…n. Symmetrical RSMs have been collected to separate the effect of epilayer tilt and strain, while asymmetric RSMs are collected to separate the effect of composition and strain.

(004) and (224) RSMs for Ge grown on bulk Si and on different porosity buffers are shown in Figure 4.7. For all samples the Ge RELP is broadened in the $k_{||}$ direction indicating mosaicity, which is caused by dislocations introduced during the relaxation process. A magnified image of Si and pSi RELPs for Ge grown on 22% and 48% pSi is shown in the insets of Figure 4.7. Evident lattice mismatch between the pSi buffers and bulk Si is only observed in the out-of-plane direction while in the in-plane direction pSi is lattice matched to bulk Si, this effect being attributed to the reorganization of pSi at the high temperatures reached during epitaxy.

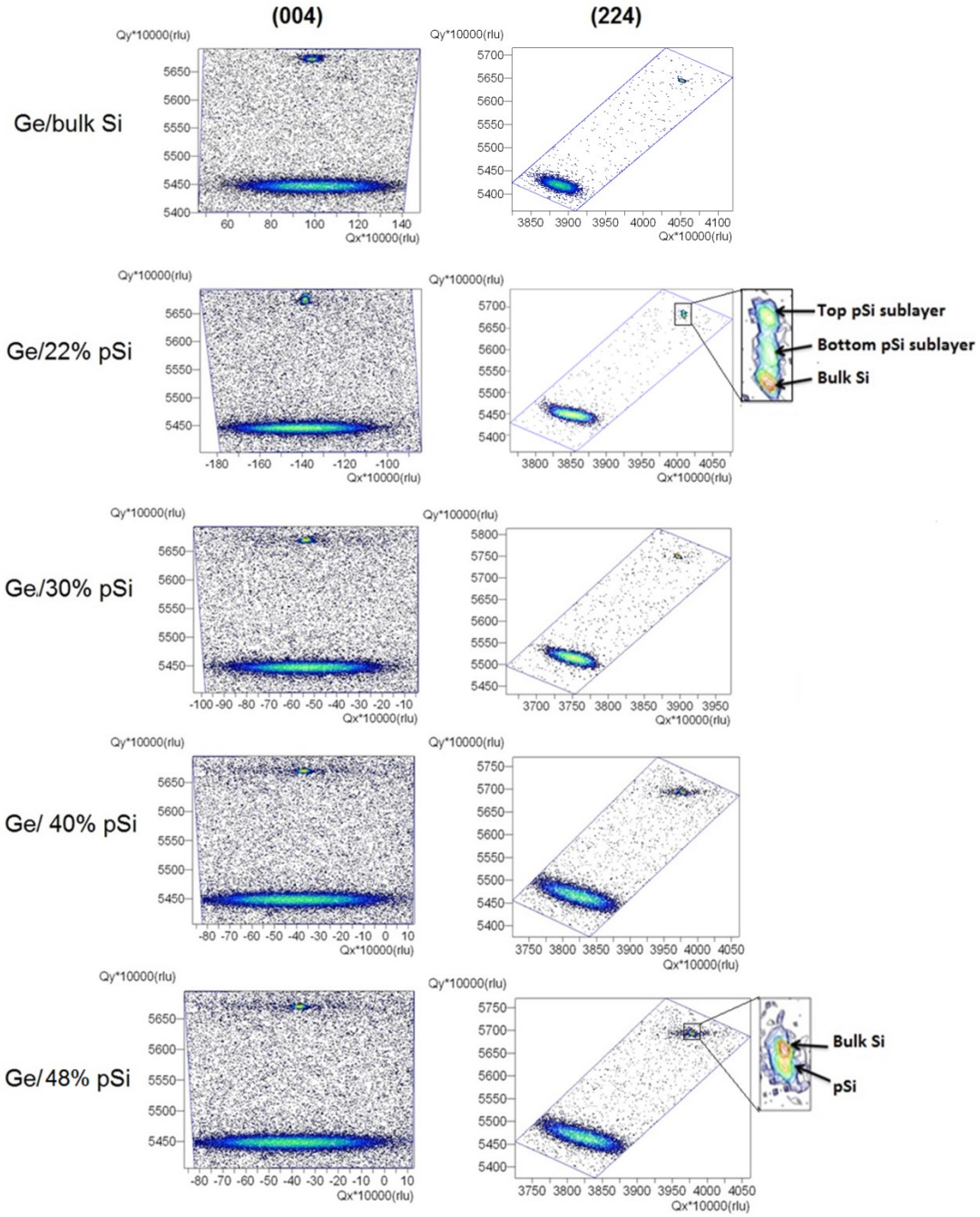


Figure 4.7: (004) and (224) RSMs iso-intensity contour plots of Ge grown on bulk SI and on different porosity pSi buffers. In the insets the magnified Si and pSi RELPs for Ge grown on 22% and 48% pSi are shown. A magnified image of the 30% and 40% pSi RELPs is not reported as the strain state of these buffers is very similar to that of 48% pSi.

By comparing Figs. 4.3 b) and 4.7 we observe in grazing incidence analysis a relative increase in the intensity of the X-rays diffracted by the more strained sublayer of the 22% porous buffer, indicating it lays at the top of the pSi buffer. This means that the in-plane

tensile stress introduced by Ge has separated the buffer in two sublayers, the more strained one being that directly in contact with Ge, the less strained being the bottom one, which is bounded to the Si lattice constant. The presence of two different sublayers in the 22% pSi buffer after epitaxy can be ascribed to the presence of a porosity gradient in as-grown and annealed 22% pSi, as shown in Chapter 3. The existence of a higher porosity layer at pSi surface with smaller Young's modulus compared to that of the underlying pSi buffer, but still large enough Young's modulus to allow tensile strain, can promote a larger strain of the upper part of pSi compared to the bottom part.

From symmetrical RSMs, (004) ω-scan are extracted for grown Ge epilayers (Figure 4.8). Gaussian fit of the Ge diffraction peaks is carried out using Matlab software, to study the change in Ge mosaic broadening as a function of buffer porosity.

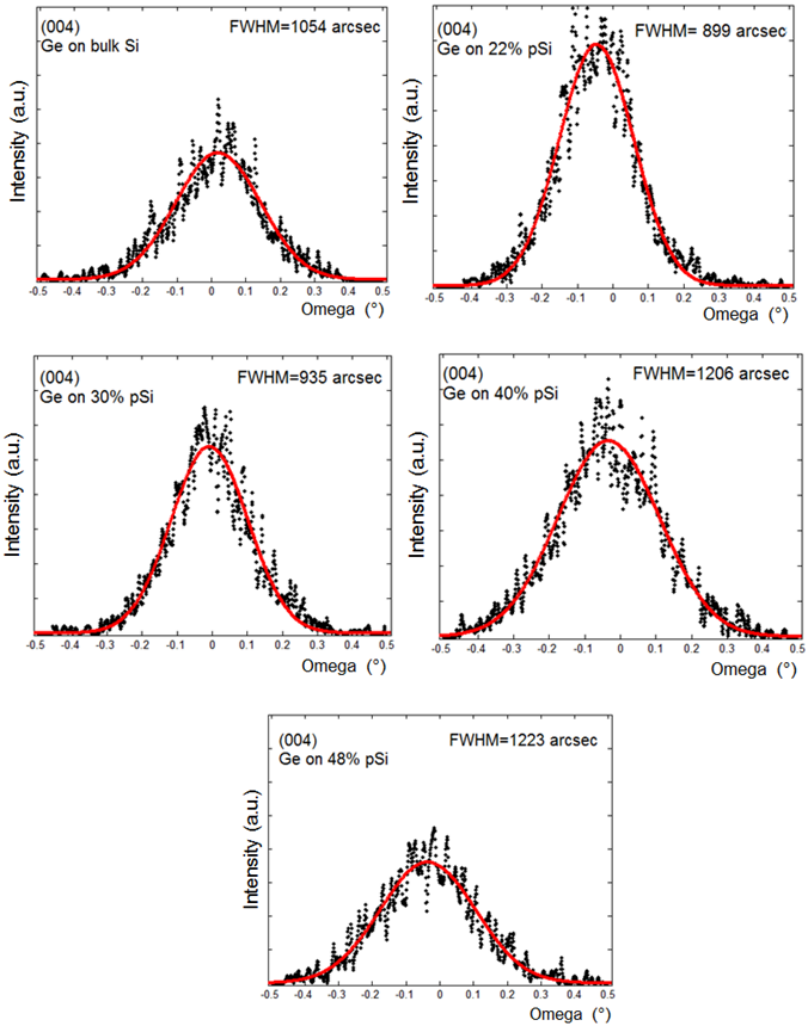


Figure 4.8: (004) RCs for Ge grown on bulk Si and on the different investigated buffers extracted from symmetrical RSMs. The reported FWHM are obtained from Gaussian fitting of the RC, which are shown in Figure.

The (004) Ge FWHM is found to increase with increasing buffer porosity indicating the Ge mosaic broadening increases with porosity. In particular, the mosaic broadening for Ge grown on 22% and 30% pSi is smaller than that observed for Ge grown on bulk Si, thus confirming the improvement in Ge crystalline quality for Ge grown on low porosity pSi buffers compared to Ge on bulk Si.

From (004) symmetrical RSMs the tilt (γ) of the epilayer with respect to the substrate is determined using the equation [125]:

$$\tan(\gamma) = \frac{(k_{\mathbf{Si}||} - k_{\mathbf{Ge}||})}{\frac{4}{a_{Si}} - |\Delta k_{\perp}|} \tag{4.1}$$

which can be approximated using the following equation:

$$\gamma = (k_{\mathbf{Si}||} - k_{\mathbf{Ge}||})\, a_{\mathrm{Si}}/4 \tag{4.2}$$

when $\Delta k_{\perp} \ll \frac{4}{a_{\mathrm{Si}}}$ and γ is small.

From asymmetrical (224) RSMs the relative lattice mismatch in the in-plane ($m_{||}$) and out-of-plane ($m_{\perp}$) directions is assessed using the equations:

$$m_{||} = \Delta a_{||}/a_{Si} = \left(k_{\mathbf{Si}||} - k_{\mathbf{Ge}||}\right)/k_{\mathbf{Ge}||} \tag{4.3}$$

and

$$m_{\perp} = \Delta a_{\perp}/a_{Si} = (k_{\mathbf{Si}\perp} - k_{\mathbf{Ge}\perp})/k_{\mathbf{Ge}\perp} \tag{4.4}$$

where $k_{\mathbf{Si}||}$, $k_{\mathbf{Ge}||}$, $k_{\mathbf{Si}\perp}$ and $k_{\mathrm{Ge}\perp}$ are the Si and Ge reciprocal lattice vectors in the in-plane and out-of-plane directions, respectively. No tilt of the Ge epilayer is observed for grown VSs, as shown in the (004) RSMs in Figure 4.7. The absence of tilt indicates that the same 6° offcut of Si substrate is maintained for the Ge epilayer even when Ge is grown on top of pSi , which is beneficial in view of subsequent epitaxy of APDs and APBs free III-V semiconductors.

The in-plane and out-of-plane Ge lattice constants $a_{Ge||}$ and $a_{\mathrm{Ge}\perp}$ are obtained from (224) RSMs by using the equations:

$$a_{Ge||} = a_{\mathbf{Si}} \times \left[1 + \left(\left(k_{\mathbf{Si}||} - k_{\mathbf{Ge}||}\right)/k_{\mathbf{Ge}||}\right)\right] \tag{4.5}$$

and

$$a_{Ge\perp} = a_{\mathbf{Si}} \times [1 + ((k_{\mathbf{Si}\perp} - k_{\mathbf{Ge}\perp})/k_{\mathbf{Ge}\perp})] \quad (4.6)$$

while the degree of relaxation R of the Ge epilayer has been directly obtained from the collected data without any assumption on Ge elastic constants by using Eq. (2.5).
In case of intermixing between Ge and Si, the epilayer lattice constant differs from a_{Ge} and the relaxed epilayer lattice constant a_0 must be determined in order to obtain R. If it would be possible to detach the grown epilayer from the Si substrate allowing for its complete relaxation, than the relative lattice constant mismatch between the two bulk-like materials would be given by the lattice misfit m which is, according to Hornstra and Bartels [126]:

$$m = \frac{a_L - a_{Si}}{a_{Si}} = \left(m_\perp - m_{||}\right)\frac{\varepsilon_{||}}{\varepsilon_{||} - \varepsilon_\perp} + m_{||} \quad (4.7)$$

where $\varepsilon_{||}$ and $\varepsilon_\perp$ are the in-plane and out-of-plane components of strain. This result, which is based on the bulk elastic theory for homogeneous deformations, shows a relationship between the lattice misfit, the lattice mismatch and the elastic constants of the material. It considers an isotropic stress $\epsilon = \varepsilon_{||}$ is applied to the material and coherent epitaxy is than modeled by removing the normal component of the applied strain $\varepsilon_{||} - \varepsilon_\perp$. By considering a not complete strain relaxation, $m_\perp$ is reduced by a factor $m_{||}$ to obtain Eq. (4.7) [126]. In case of a (001) oriented crystal, eq. (4.8) becomes:

$$m = \left(m_\perp - m_{||}\right)\frac{c_{11}}{c_{11} + 2c_{12}} + m_{||} \rightarrow m = \left(m_\perp - m_{||}\right)\frac{1 - \nu}{1 + \nu} + m_{||} \quad (4.8)$$

where $\nu = \frac{c_{12}}{(c_{12}+c_{11})}$ is the Poisson's ratio of the material, equivalent to 0.278 for Si and to 0.273 for Ge, while for a SiGe alloy with any arbitrary composition it is given by the linear interpolation between these values. The lattice misfit calculated for Ge grown on bulk Si and on the different investigated pSi buffers is reported in Table 4.3:

Table 4.3: Lattice misfit for Ge grown on bulk Si and on the different grown pSi buffers.

Buffer porosity	Lattice misfit *m* (%)
No buffer	4.18
22%	4.16
30%	4.13
40%	4.15
48%	4.18

For Ge grown on bulk Si a lattice misfit of 4.18% corresponding to the theoretical lattice mismatch existing between Ge and Si is found, indicating pure Ge is grown on top of Si and no evident intermixing occurs at the interface, as expected from the low provided thermal budget during epitaxy. On the other hand for Ge grown on 22%, 30% and 40% pSi buffers the lattice misfit is slightly smaller, indicating a small intermixing of Ge and pSi or an unintentional carbon contamination of Ge caused by the dissolution of graphite electrodes during Si anodization. However, for Ge grown on 48% pSi the observed lattice misfit is as high as the theoretical lattice mismatch, even though the growth interface was found to be wavy. As the main difference between investigated buffers with porosity ≤40% and the one with porosity of 48% is a strong degradation in crystalline quality observed for the latter, which is attributed to local collapses of the porous structure, we speculate that pSi collapse degrades the crystalline quality of the uppermost Ge epilayer and prevents the intermixing of Ge in the porous network. Since a more severe dissolution of the graphite electrodes is observed during the formation of 48% pSi compared to other pSi buffers, as a consequence of the larger current density employed during electrochemical etching of the Si substrate, we attribute the shrink of the lattice constant of the Ge epilayer observed for Ge epitaxy on low porosity buffers to Ge and Si intermixing rather than to the presence of C atoms in the Ge epilayers.

Assuming intermixing of Ge and Si is the only cause for the observed reduction in the epilayer lattice constant compared to the case of pure Ge growth, the Ge fraction in grown epilayers is calculated as a function of buffer porosity by using the parabolic deviation of the Vegard's law reported in Eq. (2.1). The results of the modified Vegard's law are presented in Table 4.4.

Table 4.4: Ge fraction in the epitaxial layer for different buffer porosity

Buffer porosity	Ge fraction (%)
No buffer	100.0
22%	98.7
30%	97.5
40%	98.4
48%	100.0

In Table 4.5 the main results of HR-XRD analysis are reported together with the results of EPD analysis. Etch pits in grown Ge on Si VSs are found to increase with increasing buffer porosity, following the same trend observed for the (004) FWHM. This suggests that the improvement observed in Ge crystalline order for decreasing porosity can be mainly ascribed to a reduction in TDD. For low buffer porosity (≤30%) both the Ge FWHM and EPD counts are lower than that of Ge grown on bulk Si: for Ge grown on 22% pSi the TDD is reduced by 40%, while a small TDD reduction of about 15% is observed for Ge grown on 30% pSi. For Ge grown on 30% pSi the porous buffer does not undergo tensile strain, suggesting the presence of an additional mechanism for dislocation reduction in presence of pSi. This aspect is investigated in the next Chapter.

For Ge grown on 40% pSi both FWHM and EPD counts are comparable with those obtained for Ge grown on bulk Si, while for Ge grown on 48% pSi both FWHM and EPD counts exceed those of Ge on bulk Si, indicating degradation of the epilayer caused by the high buffer fragility.

Complete epilayer relaxation is observed for Ge grown on bulk Si, despite the low growth temperature. On the other hand a small residual compressive strain is found for Ge grown on the different pSi buffers. This different behavior can be attributed to the larger thermal expansion coefficient of pSi compared to bulk Si [127], which leads to the existence of a smaller thermal coefficient mismatch between Ge and pSi compared to Ge and Si. As Ge has a thermal expansion coefficient which is more than double than that of Si (α_{Ge}= $5.9 \cdot 10^{-6}$ °C $^{-1}$ and α_{Si}=$2.6 \cdot 10^{-6}$°C $^{-1}$ at room temperature), it contracts faster than Si when cooling down, resulting in the introduction of a tensile strain in Ge when the substrate goes from the growth temperature to room temperature. If we now assume incomplete relaxation for Ge grown on Si at the growth temperature (500°C), than the above described mechanism could explain the obtained results: not complete relaxation for Ge grown on pSi could be attributed to the larger thermal expansion coefficient of pSi

which introduces a smaller tensile strain within Ge during cooling-down, while for Ge grown on bulk Si the introduced tensile strain is sufficient for complete Ge relaxation.

Table 4.5: Physical parameters of grown Ge epilayers

Buffer Porosity (%)	$a_{Ge//}$ (Å)	$a_{Ge\perp}$ (Å)	*R* (%)	Triple axis Omega/2Theta $FWHM_{004}$ (arcsec)	EPD x 10^6 (cm^{-2})
No buffer	5.6581	5.6581	100	202	13
22	5.6547	5.6584	99	159	8
30	5.6421	5.6655	94	188	11
40	5.6492	5.6618	97	204	20
48	5.6526	5.6619	98	257	28

4.2.3 Surface roughness analysis

5 μm x 5 μm AFM micrographs reported in Figure 4.9 are collected in contact mode for Ge grown on bulk Si and on the different investigated pSi buffers to study how the presence of pSi affects the Ge surface morphology and RMS roughness. Ge grown on bulk Si shows an ordered array of square-based pyramids with a side of about 3 μm indicating 3D S-K growth mode occurs during epitaxy. A slightly asymmetric shape is observed for these islands, which is ascribed to the 6° misalignment angle of (001) planes with respect to wafer surface. For Ge grown on bulk Si cross-hatch pattern with a cross-hatching wavelength corresponding to the side of the pyramids is observed, which is consistent with the typical cross-hatch wavelength of few μm observed in Ge epilayers grown on Si [128]. The presence of a cross-hatch pattern in Ge on Si VSs is attributed to the formation of spatially non-uniform growth rates caused by a not homogeneous strain associated with MDs aligned along [110] orthogonal directions and associated TDs gliding on {111} planes [129-130]. Cross-hatch has been found to appear at the surface of Ge grown on Si after annealing as a consequence of the formation of a confined network of TDs in proximity of the Ge/Si interface, which introduces a strain field within Ge responsible of Ge surface migration [131]. In general, crosshatching in large misfit systems such as the Ge/Si system has been frequently observed when the density of defects is low [132].

In contrast with what is observed for Ge grown on bulk Si, for Ge grown on pSi no cross-hatch pattern is observed, independently on buffer porosity. The lack of a clearly visible cross-hatch pattern for Ge on pSi suggests that the presence of pSi introduces another

source of Ge growth inhomogeneity which overlap with that generated by MDs and TDs, resulting in a disordered Ge surface. This is possibly a consequence of the random distribution of pores within mesoporous silicon layers, which likely introduce local differences in pSi physical properties and Ge growth rates. Moreover, local deformations or collapses of pSi during epitaxy could introduce further sources of growth inhomogeneity responsible for the observed surface morphology.

The absence of cross-hatch pattern for Ge grown on pSi has been also observed by I Berbezier et al., which reported the formation of dots the surface of Ge grown on pSi [115]. This is very similar to what we observed for Ge grown on 48% pSi, for which large dots with size of ~500 nm are observed. Decreasing the buffer porosity to values ≤ 40% the surface morphology changes and rather small grains coalesced in larger hillocks up to 400 nm in height are observed instead of Ge dots. Since the provided thermal budget is the same for all grown Ge epilayers, the observed difference in Ge surface morphology is only ascribed to the different parameters of the investigated porous buffers.

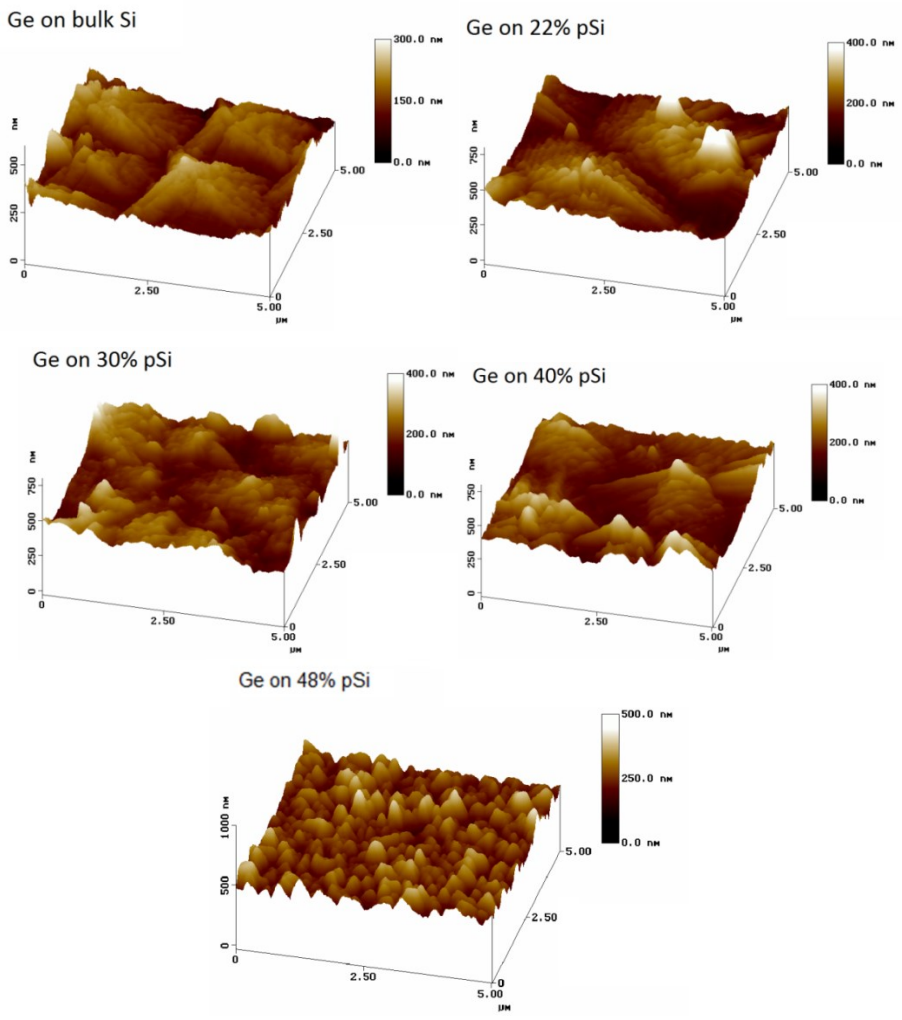


Figure 4.9: 5 μm x 5 μm AFM micrographs of Ge grown on bulk Si and on the different investigated pSi buffers.

The main observed difference between the 48% pSi buffer and lower porosity buffers is the very high fragility of the former one, as deduced from SEM cross-section imaging (Figure 4.4 d)). As a consequence, it seems that high buffer fragility hamper the growth of a continuous epilayer promoting the formation of dots. On the other hand, tensile strain of 22% pSi seems to have not a major effect on Ge surface morphology, as Ge epilayers grown on 22% 30% and 40% pSi buffers show similar morphologies even though only the 22% pSi buffer undergoes a strong change in its strain state during epitaxy.

The RMS roughness of as-grown Ge epilayers as a function of buffer porosity is reported in Figure 4.10. For Ge grown on bulk Si a very large RMS roughness of 38.5 nm is observed, which further increases for Ge grown on pSi up to 48 nm. Even though a not obvious dependence of Ge RMS roughness on pSi buffer porosity is observed, Ge grown on the different porosity buffers has always a larger roughness compared to Ge directly grown on bulk Si, this effect being attributed to the larger roughness of pSi compared to the planar surface of bulk Si.

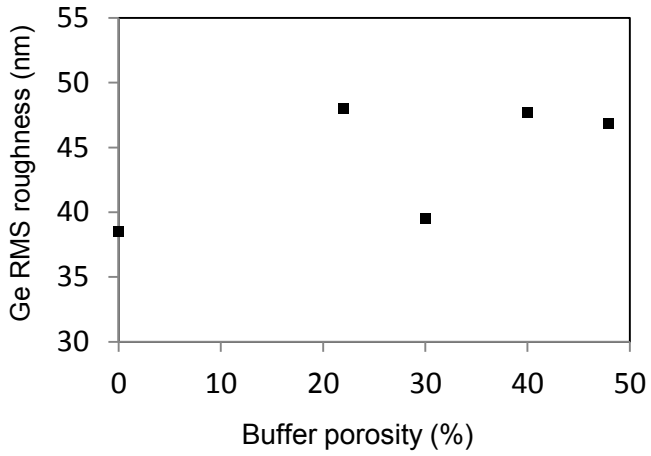


Figure 4.10: RMS roughness of as-grown Ge epitaxial layers on bulk Si and on the investigated porous buffers

The very large RMS roughness obtained for both Ge on bulk Si and on pSi is attributed to both the 3D S-K island growth and to the H_2 plasma etching process carried out just before epitaxy. H_2 plasma etching, which is carried out within the same LEPECVD reactor used for Ge epitaxy, removes residual contaminants from Si surface after diluted HF dip, etching the Si substrate with both isotropic and anisotropic contributions depending on etching conditions [30]. As a consequence, the smoothness of the starting substrate results degraded by plasma etching, resulting in the observed very large values for Ge

RMS roughness which exceed the typical values found in other works when plasma etching of Si is not performed [133, 134].
EPD carried out on such high surface roughness substrates could result in difficult counting of pits and hence in large errors in TDD assessment. Nevertheless, former unpublished results show that the number of etch pits observed before and after CMP does not change significantly, so that the technique can be applied with good results also for Ge epilayers with large RMS roughness as in our case.

4.3 The effect of pSi buffer layer thickness on the Ge crystalline quality

The effect of pSi buffer layer thickness on the crystalline quality of epitaxial Ge is investigated by growing Ge on four different pSi buffers anodized under the same etching conditions but for increasing etching time (*T*). Starting substrate is n-type Si (001) oriented with resistivity ρ= 3.6 mΩ cm. n-type doped Si is used to understand whether the kind of doping, and hence the different resulting pSi morphology, may lead to the same mechanism for Ge crystalline quality improvement using p-type Si, i.e. tensile strain of pSi and fracture of the buffer in two sublayers. Moreover, a highly doped n-type substrate is used to avoid illumination of wafer backside.
Electrochemical etching is performed in the dark using a solution of HF and ethanol (volume ratio 7:1) and providing a constant current density J=45 $mAcm^{-2}$. pSi buffer thickness (*d*) increases with increasing anodization time from 30 sec. up to 900 sec. The porosity and thickness of pSi anodized for 30 sec. are 25% and 2.3 μm, respectively, as assessed from gravimetrical measurements. Increasing the etching time both buffer thickness and porosity increase. A thickness of 8.1 μm is assessed for 120 sec. anodization time and of 18.3 μm for 300 sec. anodization time. For 900 sec. anodization time the thickness of the pSi buffer is very large, exceeding 50 μm. Also in this case uniformity of growing conditions during Ge epitaxy is obtained by growing the different pSi buffers on the same 100 mm Si wafer at the same radial distance from wafer center and the observed differences in Ge crystalline quality are solely attributed to the different properties of investigated pSi buffers.
In Figure 4.11 the (004) Omega/2Theta scans collected in double-crystal diffracting mode are reported for 5 μm-thick Ge epilayers grown on the different pSi buffers. Two different pSi sublayers compressively strained in the out-of-plane direction are visible for each grown sample, as already observed for Ge grown on 22% p-type pSi, except for the buffer anodized for 900 sec. for which the pSi diffraction peak is very broad and overlap

with that of bulk Si. For 30 sec., 120 sec. and 300 sec. anodization time the lattice constant mismatch $\left(\frac{\Delta a_{\perp}}{a_{Si}}\right)$ of the pSi sublayers increases with *T* and hence with pSi buffer thickness. This effect is attributed to both a small increase in buffer porosity with increasing *T,* which increases the compliance of the buffer, and to a larger increase in buffer thickness, which leads to an increase in the distance between the upper part of pSi and bulk Si. Larger is the thickness of pSi and less bounded is the buffer to the bulk Si lattice constant, thus allowing a larger strain of pSi during epitaxy at parity of in-plane tensile stress introduced by Ge. Strain of the upper region of pSi induces a strain also in the bottom part of pSi, which undergoes a smaller deformation which increases with buffer thickness too (see Figure 4.11).

As we have attributed the compressive strain of pSi in the out-of-plane direction to an in-plane tensile stress introduced on pSi by Ge having a larger lattice constant, an improvement in Ge crystalline quality is expected with increasing strain of pSi as this indicates a larger part of the lattice constant mismatch between Ge and Si is relaxed through plastic deformation of the buffer. This suggests that the larger is the strain of the pSi sublayers in the out-of-pane direction, the better would be the Ge crystalline quality. This is exactly what is observed by increasing the anodization time from 30 sec. to 120 sec., for which a 10.3% reduction in (004) Omega/2Theta Ge FWHM collected in double-crystal configuration is found, as reported in Table 4.6.

Increasing the anodization time to 300 sec. the compressive strain of the pSi sublayers further increase. In this case very similar out of-plane lattice constants are observed for the two sublayers, indicating an almost homogeneous deformation of the entire porous buffer. However, while further improvement in Ge crystalline quality is expected, a small degradation in Ge crystallinity is observed in this case, as deduced from a small increase in Ge FWHM of 3%. The not monotonic improvement in Ge FWHM with increasing pSi strain indicates that accommodation of the lattice mismatch by pSi deformation is not the sole mechanism determining the Ge crystalline quality and at least another factor influencing Ge crystallinity exists. We attribute the observed increase in Ge FWHM with increasing pSi strain to the pure chemical etching of already formed pSi. As anodization time increases pure chemical etching becomes increasingly important, this effect possibly degrading the upper part of the pSi buffer for long etching times possibly leading to a degradation in Ge crystalline quality even though the pSi sublayers accommodate a larger part of the lattice mismatch between Ge and Si.

Further increasing the anodization time to 900 sec., no sharp pSi diffraction peak is observed after epitaxy. In this case the pSi buffer originates diffuse scattering which overlap to the bulk Si peak broadening it in an asymmetric manner, indicating a large strain inhomogeneity exists within pSi.

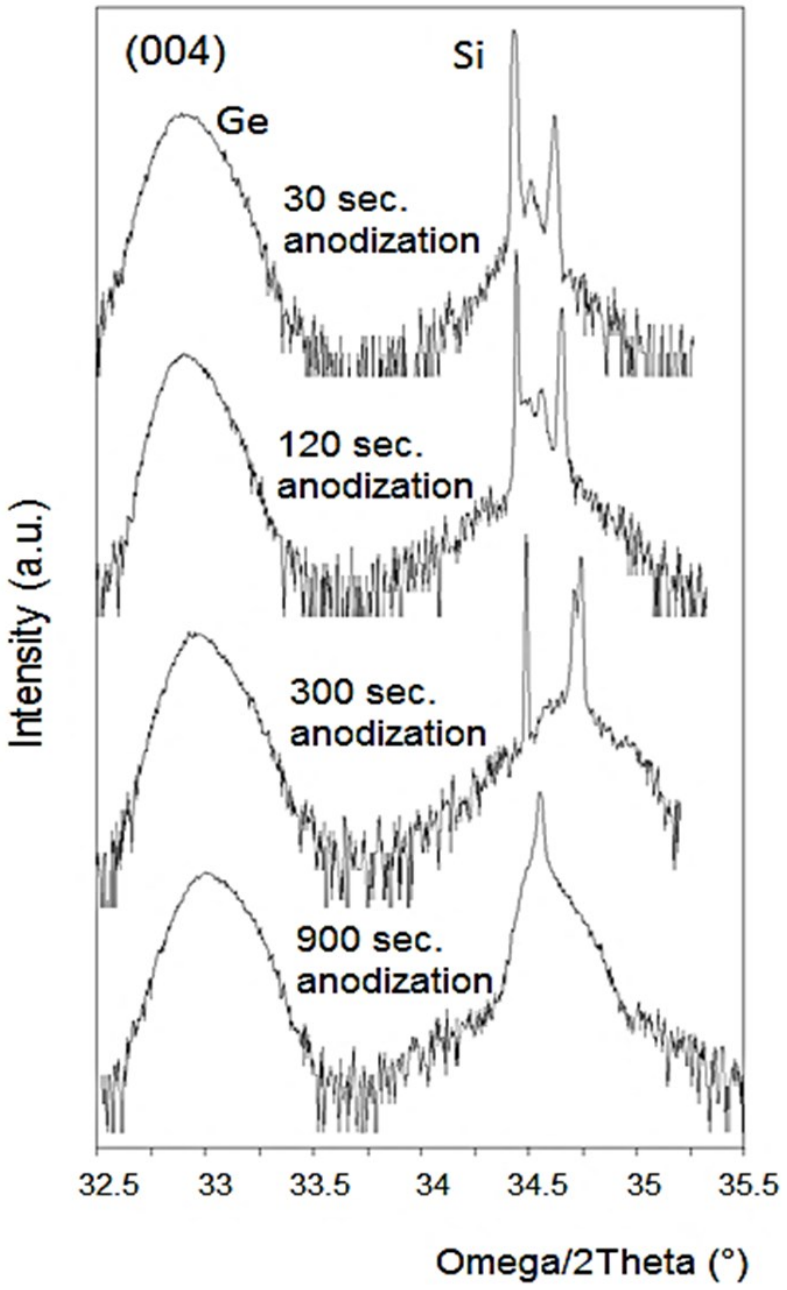


Figure 4.11: (004) Omega/2Theta scans collected in open detector diffraction mode for Ge epilayers grown on n-type pSi buffers anodized for different etching times. The HF:ethanol volume ratio is 7:1 and the current density is fixed at 45 $mAcm^{-2}$.

This result is again ascribed to the pure chemical etching of already formed pSi. Moreover, for the large investigated buffer thickness, the decrease in F^- ions concentration at pore tip with increasing depth of the pSi layer is known to cause an increase in buffer porosity with depth. For long anodization times and large buffer thicknesses both these effects could be of some importance modifying locally the mechanical properties of grown buffers and introducing different sources of porosity

gradients in vertical direction, which could be responsible for the large observed pSi strain inhomogeneity after epitaxy.

The best Ge crystalline quality is thus obtained for Ge grown on about 8 μm pSi buffer, which thickness roughly corresponds to the Ge epilayer thickness. Low porosity psi buffers having larger thickness could even be more beneficial in terms of Ge crystalline quality if pure chemical etching of already formed pSi could be suppressed. This could be obtained by increasing the etch rate of pSi in order to reduce the etching time and hence the permanence of pSi in the electrolyte.

Table 4.6: Ge FWHM and pSi lattice mismatch for different anodization times of 3.6 mΩ cm (001) oriented n+ Si anodized in the dark. All buffers are grown at a constant current density of 45 $mAcm^{-2}$ and using a HF:ethanol volume ratio of 7:1.

Anodization time (sec.)	(004) Omega/2Theta Ge FWHM (arcsec)	$\frac{\Delta a_\perp}{a_{Si}}$ upper pSi sublayer (%)	$\frac{\Delta a_\perp}{a_{Si}}$ bottom pSi sublayer (%)
30	937	-0.47	-0.20
120	840	-0.53	-0.30
300	868	-0.63	-0.55
900	960	no peak	no peak

The electrochemical etching of highly doped n-type Si substrates resulted in columnar pSi, with pore diameter and interpore spacing of about 10nm, as shown in Figure 4.12 for a thin pSi buffer anodized under the same etching conditions used for the realization of n-type pSi in this Paragraph. The columnar morphology of highly doped n-type pSi depends on the fact that significant hole concentration necessary for Si anodization is only found at pore tips, as a consequence of hole injection on wafer backside, in accordance with the mass-action law. This causes the electrochemical etching process to proceed in vertical direction, promoting the formation of vertical channels. Despite the different morphology, columnar n-type pSi undergo tensile strain and buffer fracture as observed for p-type sponge-like Si indicating the main mechanism for TDD reduction in Ge on pSi does not depend on pSi morphology but only on the reduced Young's modulus of the employed buffer.

In Figure 4.12 not complete adhesion between the Ge epilayer and pSi is visible at the interface which is attributed to the large surface roughness of n-type pSi introduced by

the H_2 plasma etching process carried out before epitaxy. Moreover, 3D island growth is visible at Ge surface.

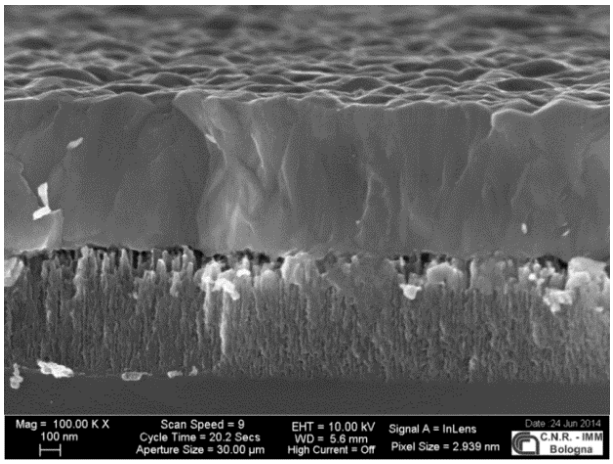


Figure 4.12: Cross section SEM image of 750 nm-thick Ge epilayer grown on a 600 nm-thick n-type pSi. pSi buffer porosity is 26%. 3D island growth is visible at Ge surface.

Chapter 5

Annealing of Ge on porous silicon virtual substrates

5.1 Introduction

The high-temperature annealing of Ge on Si VSs in hydrogen atmosphere has been extensively investigated by different research groups in order to reduce both the TDD in Ge epilayers grown on Si (also using nitrogen atmosphere) and the typically large RMS roughness found in as-grown substrates [48, 134-141]. The driving forces for these mechanisms are the motion of dislocations during expansion and contraction of Ge at high temperatures, which promote their annihilation [48], and the formation of Ge-H clusters, which presence is believed to enhance of Ge surface mobility [134]. In particular, the effect of post-growth H_2 annealing and of cyclic thermal annealing on the crystalline quality of Ge epilayers on Si has been deeply investigated [135-138], as well as the introduction of different deposition-annealing cycles [142], showing a Ge crystalline quality improvement with increasing number of cycles. This result depends on the "grown-in" nature of defects in Ge on Si heteroepitaxial systems, which typically are not in an equilibrium state even if they are relaxed so that annealing results in a more stable configuration accompanied by dislocation annihilation [143].

Post-growth ex-situ and in-situ techniques for flat Ge epilayers on Si have been developed to obtain very low values of RMS roughness in the nm or sub-nm range suitable for device integration or subsequent epitaxial growth. RMS roughness below 0.2 nm has been demonstrated for Ge on Si after CMP [144] while RMS roughness values below 1 nm have been demonstrated through in-situ H_2 annealing [145]. Very low values of RMS roughness suitable for subsequent epitaxy have been also demonstrated for thin Ge heteroepilayers grown on pSi [114,115]. However, a post-growth technique for TDD reduction to levels suitable for device integration similar to those employed for RMS roughness reduction does not exist. Even after cyclic annealing, the high TDD within Ge

epilayers typically > 10^6 cm^{-2} [146-149] limit the lifetime of minority carriers, degrading device performances [150,151].

In this Chapter we mainly focus on threading dislocation reduction in Ge epilayers grown on pSi through annealing. In particular we investigate the effect of N_2 and H_2 annealing on the crystalline quality of Ge grown on bulk Si and on 22% and 30% pSi buffers, for which a reduction in mosaic broadening has been observed compared to Ge directly grown on bulk Si. To our knowledge the effect of high temperature annealing on Ge on pSi VSs has never been investigated before. Nevertheless, the Ge epilayer grown on top of pSi has higher degrees of freedom compared to Ge directly grown on Si, since in this case the Ge lattice constant is not as strongly bounded to the bulk Si lattice constant as in the case of direct Ge epitaxy on Si. This effect could in turn lead to a stronger reorganization of Ge grown on pSi during high temperature annealing. In addition, pSi is known to undergo strong morphological reorganization at high temperatures [102] and the expected simultaneous reorganization of Ge and pSi during annealing, driven by energy minimization, could have a major effect on the final Ge crystalline quality and TDD.

5.2 High-resolution X-ray diffraction analysis

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Annealing is carried out at different temperatures on 8x8 mm^2 5 μm-thick Ge epilayers grown on bulk Si and on 22% and 30% pSi to study how the presence of the porous buffer affects the reorganization of the Ge epilayer at high temperature. While after epitaxy the 22% pSi buffer is found to be under compressive strain in the out-of plane direction, the 30% pSi buffer is still found under tensile strain as before epitaxy, allowing us to study the effect of annealing on differently strained systems.

At first, (224) Omega/2Theta scans are collected for the investigated VSs both in grazing incidence diffraction (GID) and in grazing exit diffraction (GED) configurations at room temperature and at different annealing temperatures using an Anton Paar High-Temperature X-Ray Diffraction (HT-XRD) chamber. HT-XRD measurements presented in this thesis have been collected at the physics Department of Padova University in collaboration with Prof. D. De Salvador. To resist the high annealing temperatures, tantalum springs have been used to maintain the substrate fixed to the holder of the X-ray diffractometer. These springs press the substrate introducing a small deformation of the sample and leaving an area of about 5 x 5 mm^2 visible to the x-rays. In order to reduce the effect of substrate deformation on the collected scans, 1/8 degree divergence slit is used for the following measurements.

The FWHM of the Ge diffraction peak retrieved from GID and GED scans is used for a qualitative analysis of the Ge crystalline quality evolution with temperature in presence and absence of pSi buffers. For Ge grown on bulk Si, Omega/2Theta scans in GID and GED configurations are collected for both 0° and 180° azimuth angles from which a maximum uncertainty of about 30 arcsec is assessed for the obtained FWHM values, which is mainly attributed to an asymmetric deformation of the investigated substrate introduced by tantalum springs.

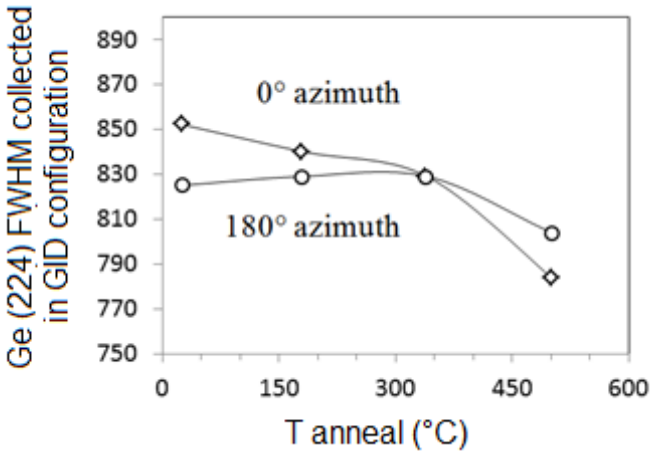

Figure 5.1: Evolution of the Ge FWHM collected in GID configuration for both 0° and 180° azimuth angles as a function of annealing temperature.

In particular, it is reasonable to attribute the increase in FWHM with temperature in the range 26°C-340°C for Omega/2Theta scans collected at 180° azimuth angle to this deformation effect as an increase in strain inhomogeneity within Ge is not expected during annealing. Although the observed difference is smaller than 4% of the measured FWHM, for a coherent assessment of crystalline quality evolution with temperature, in the following analysis the FWHM of Ge epilayers grown on both bulk Si and on pSi always refers to data collected at 0° azimuth angle.

HT-XRD measurements are carried out at 26°C, 180°C, 340°C and 500°C under N_2 atmosphere for 1 hour per selected temperature. After HT-XRD analysis, the grown substrates are annealed under H_2 atmosphere to investigate the evolution in Ge crystalline quality under semi-standard annealing conditions. Three annealing cycles of 30 minutes each are carried out at about 750°C and 1.2 10^{-1} mbar and TDD within grown Ge epilayers is evaluated from plan view TEM analysis.

To correlate the expected reorganization of the pSi buffer with the high-temperature evolution of the Ge crystalline quality, (224) RSMs around the pSi and bulk Si reciprocal lattice points of Ge grown on 22% pSi are reported for the different investigated annealing temperatures (Figure 5.2). For annealing temperatures <500°C two different diffraction

peaks arising from the 22% pSi buffer are visible, as observed for the as-grown sample. On the other hand, after annealing at 500°C a single pSi peak is visible, indicating macroscopic reorganization of the porous sublayers in a single coherently diffracting layer occurred. After annealing the porous buffer is still pseudomorphic to bulk Si and compressively strained in the out-of-plane direction, as before annealing.

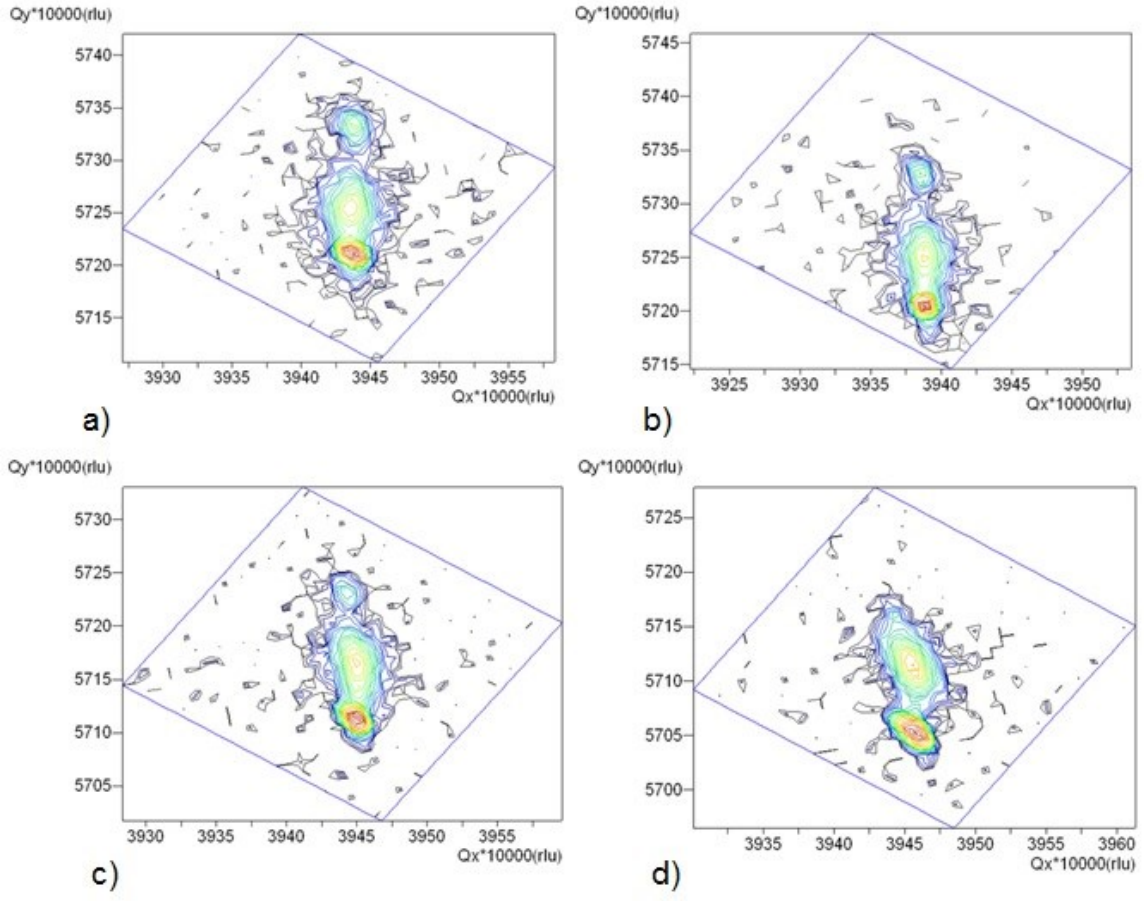

Figure 5.2: (224) RSMs of Ge grown on 22% pSi around the pSi and bulk Si reciprocal lattice points collected at a) 26°C, b) 180°C, c) 340°C and d) 500°C, respectively.

(224) RSMs collected at the same annealing temperature around the Si and pSi reciprocal lattice points for Ge grown on 30% pSi are reported in Figure 5.3. The 30% pSi reciprocal lattice point is also in this case lattice matched to bulk Si in the in-plane direction, while it is tensile strained in the out-of-plane direction for annealing temperatures < 340°C. In contrast to what is observed for Ge grown on 22% pSi, in this case reorganization of the pSi buffer is already observed at 340°C. At this temperature pSi is found to change its strain state from being tensely strained to compressively strained in the out-of-plane direction, the compressive strain further increasing at 500°C.

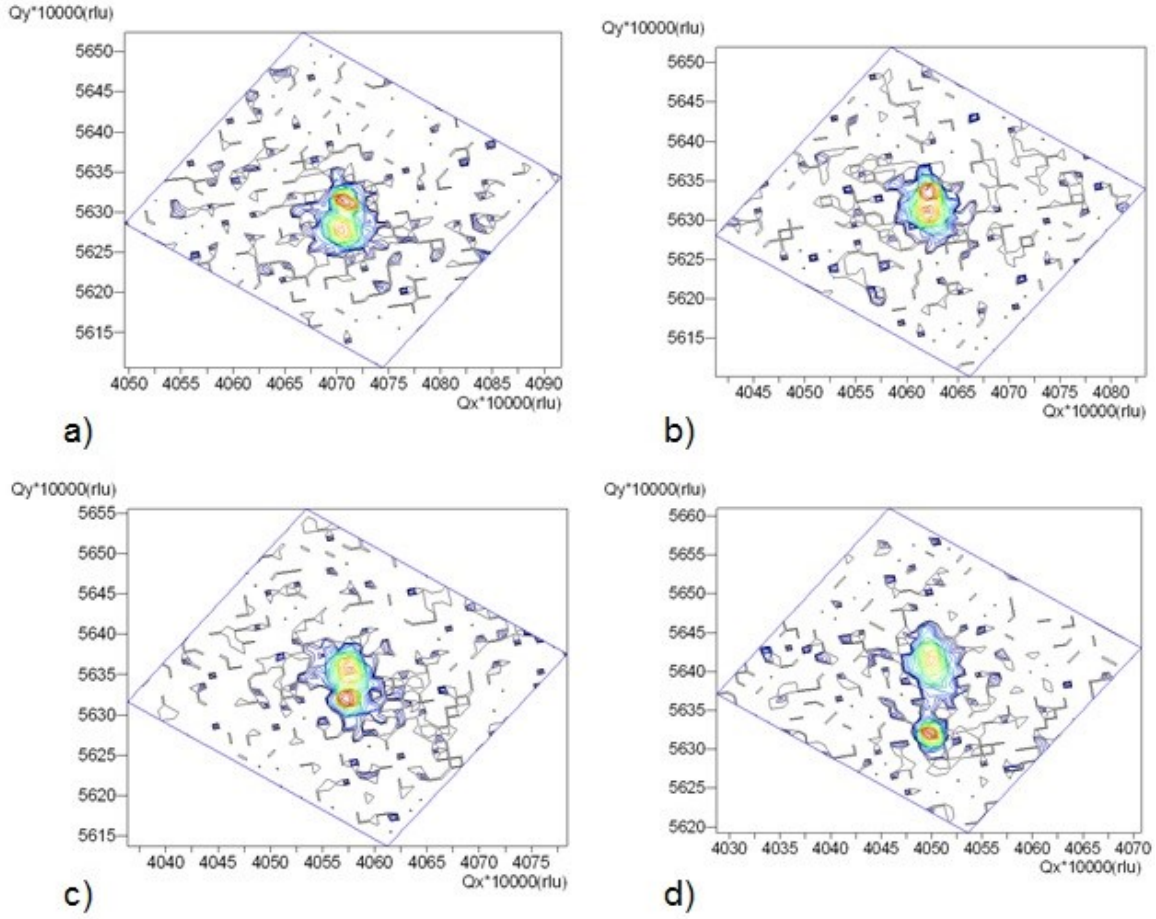

Figure 5.3: (224) RSMs of Ge grown on 30% pSi around the pSi and bulk Si reciprocal lattice points collected at a) 26°C, b) 180°C, c) 340°C and d) 500°C, respectively.

The final strain state of 30% pSi is very similar to the final strain of 22% pSi and also in this case the existence of a compressive strain in the out-of-plane direction is attributed to an in-plane tensile stress introduced by Ge on pSi. However, for the more porous 30% pSi buffer tensile strain does not occur during epitaxial growth but during annealing, leading to the formation of a single pSi peak in contrast to what is observed for 22% pSi, indicating an homogeneous strain within the whole 30% pSi buffer after epitaxy. A possible explanation for the different observed thermal budget necessary for change in pSi strain state in the two different cases consists in considering that the 30% pSi buffer is too fragile to undergo tensile strain during Ge epitaxy, but it can strain during the first stages of annealing which likely leads to initial reorganization of the porous buffer. After initial pSi reconstruction driven by high temperature conditions Ge can strain pSi, this effect being attributed to a reduction in pSi Young's and shear moduli during reorganization of the porous network which could be ascribed to migration of small pores within Ge acting as vacancy sink, as observed from cross-section SEM imaging. This suggests that even though no macroscopic reorganization of the 30% pSi buffer is

observed from X-Ray analysis for annealing temperatures < 340°C, microstructural changes already occurs in pSi at this low temperature. This is in accordance with what observed by M. Joshi et al., which reported coarsening of the pSi layer already at temperatures of 300°C [147].
We conclude that, for Ge grown on 30% pSi a significant variation in the strain state of the buffer during annealing occurs at lower thermal budget compared to what is observed for the 22% pSi buffer, as in this case the observed pSi lattice constant variation is not solely ascribed to a thermal process, as is the case of 22% pSi. A reduced thermal budget is necessary in this case as also the in-plane stress introduced by Ge on pSi is believed to participate in the lattice constant modification of the pSi buffer, the same effect for 22% pSi being observed during epitaxy.

5.2.1. Grazing incidence diffraction (GID) analysis

In Figure 5.4 the double-crystal (224) Omega/2Theta scans collected in GID configuration for Ge grown on 22% pSi and on bulk Si are shown for the different investigated annealing temperatures. The same scans collected for Ge grown on 30% pSi are not reported here as the obtained results are very similar to those of the other investigated VSs. At room temperature, while the diffraction peak of the more strained pSi sublayer is clearly visible, the diffraction peak of the less strained sublayer partially overlap with that of bulk Si as a consequence of small substrate deformation introduced by the tantalum springs.
In GID configuration the geometry is sensitive to vertical strain distribution or interplanar distance [152]. As a consequence, the FWHM of the Ge epilayer retrieved from GID Omega/2Theta scans is here used for a qualitative assessment of strain distribution variation within Ge as a function of temperature.

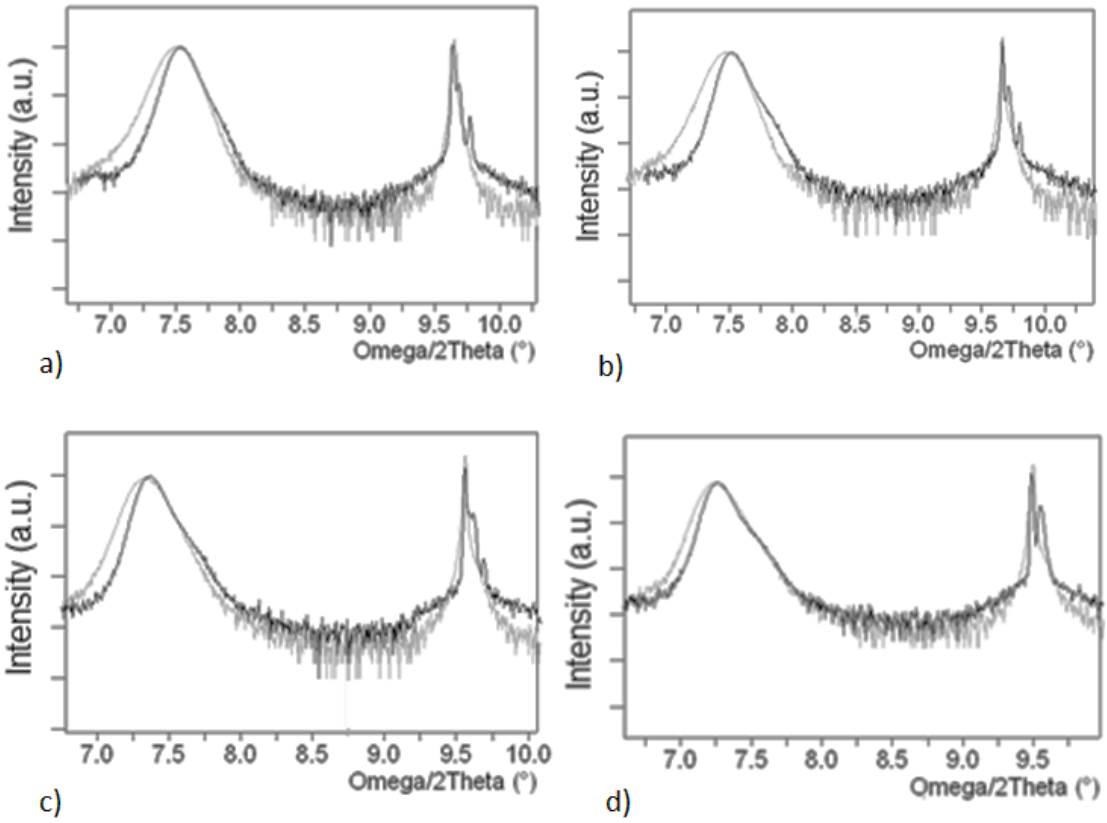

Figure 5.4: Omega/2Theta scans collected in GID configuration for Ge grown on bulk Si (grey line) and on 22% pSi (black line) during N_2 annealing at the temperature of a) 26°C, b) 180°C, c) 340°C and d) 500°C.

At room temperature almost symmetric Ge diffraction peaks are observed for both Ge grown on bulk Si and on 22% pSi, with the latter being slightly sharper thus indicating a more homogeneous strain distribution or interplanar distance within Ge in presence of pSi, as already observed in Chapter 4. Increasing the annealing temperature the diffraction peak for both Ge grown on bulk Si and on pSi becomes asymmetric towards larger 2Theta angles, suggesting the formation of a SiGe alloy at the Ge/Si and Ge/pSi interfaces. While for Ge grown on pSi the Ge diffraction peak becomes asymmetric already at 180°C (Figure 5.4 b)), for Ge grown on bulk Si the broadening of the diffraction peak towards larger 2Theta angles starts at 340°C, indicating that a smaller thermal budget is necessary for intermixing of Ge in the porous matrix of pSi compared to intermixing of Ge in bulk Si. This is possibly attributed to the diffusion of Si in Ge via the vacancy mechanism [153], which population might increase in presence of pSi thus resulting in an enhanced mechanism for Ge and Si intermixing, or to infiltration of Ge within the pores of pSi. In addition, pSi reorganization during annealing could further promote diffusion of Si in the Ge lattice compared to the case of annealed Ge grown on bulk Si. At 500°C a single pSi peak is observed for Ge grown on pSi, as already observed in Figure , 5.3 as a consequence of pSi reorganization. After HT-XRD analysis three

cycles of H_2 annealing at about 750°C and 1.2 x 10^{-1} mbar have been carried out. Annealing is performed within the same LEPECVD reactor used for crystal growth fluxing 40 sccm of H_2 in the growth chamber after switching off the turbo molecular pump used to maintain a base pressure of 3 x 10^{-1} mbar. In Figure 5.5 the (224) Omega/2Theta scans for Ge grown on bulk Si and on pSi collected in GID configuration after H_2 annealing are reported.

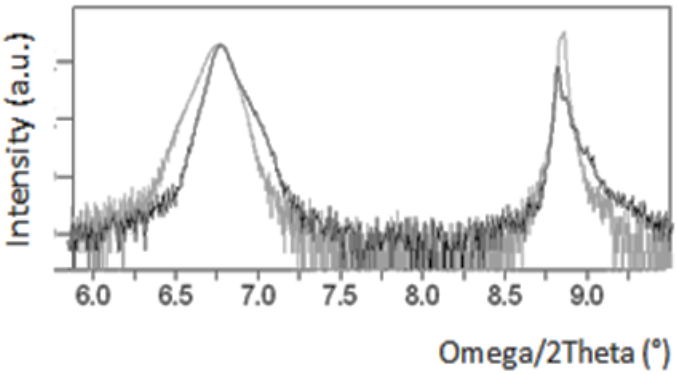

Figure 5.5: (224) Omega/2Theta scans for Ge grown on bulk Si (grey line) and on 22% pSi (black line) in GID configuration after 3 cycles of H_2 annealing at 750°C.

The sharp and well defined pSi diffraction peak observed during annealing at 500°C is no more visible in this case and a wide pSi diffraction peak which overlaps to the bulk Si peak is observed, broadening the latter towards larger 2Theta angles. This indicates pSi has undergone further reorganization during annealing at 750°C and a large strain inhomogeneity exist within the porous buffer after annealing at this temperature. After annealing the Ge diffraction peak for Ge grown on pSi is still sharper than that of Ge grown on bulk Si and is still strongly asymmetric towards larger 2Theta angles, thus confirming the formation of a SiGe alloy at the Ge/pSi interface. On the other, the Omega/2Theta scan collected at room temperature for Ge on bulk Si after cyclic annealing shows an almost symmetric Ge diffraction peak, indicating there is actually no strong intermixing between Ge and Si in absence of pSi at the provided thermal budget. It follows that the asymmetric shape of the Ge diffraction peak observed for Ge on bulk Si during HT-XRD analysis has actually to be ascribed to a –at least partially- reversible process. The absence of intermixing for Ge grown on bulk Si after annealing at 500°C is confirmed by observing the evolution of the Ge diffraction peak for Ge on bulk Si while heating up and cooling down the substrates during HT-XRD annealing (Figure 5.6.). For Ge grown on bulk Si the Ge diffraction peak becomes symmetric already at 340°C when cooling down the substrate to room temperature and becomes asymmetric towards smaller 2Theta angles at room temperatures. On the other hand the same scans for Ge grown on 22% pSi reveal a slightly asymmetric Ge peak towards larger 2Theta angles

both during heating up and cooling down the substrate The obtained result is in accordance with the results of J. Woicik et al. [149] which found strong intermixing for annealed Ge on Si for temperatures of 800°C or higher.

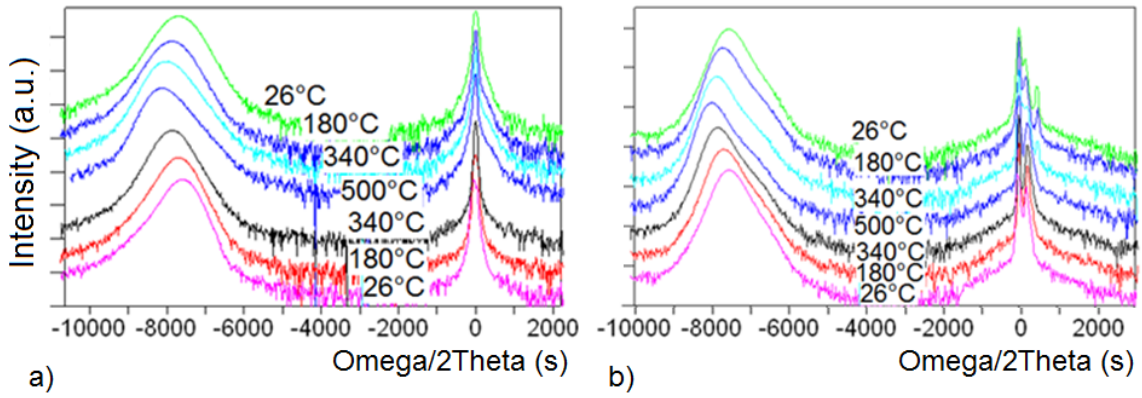

Figure 5.6. (224) GID Omega/2Theta scans during heating up (top curves) and cooling down (bottom curves) the substrate for a) Ge grown on bulk Si and b) Ge grown on 22% pSi.

In Figure 5.7 the comparison between FWHM values of the Ge diffraction peak retrieved from (224) GID Omega/2Theta scans for Ge grown on bulk Si and on the different investigated pSi buffers are reported as a function of annealing temperature. A more homogeneous strain distribution is found for the Ge epilayer grown on top of the pSi buffers compared to Ge directly grown on bulk Si for all considered annealing temperatures, this effect being attributed to the compliant nature of pSi. The FWHM of both Ge grown on bulk Si and on pSi decreases with increasing temperature, indicating the strain distribution improves during annealing as a consequence of Ge reorganization at high temperature. However, while the Ge FWHM for Ge on bulk Si and on 22% pSi is found to monotonically decrease with increasing temperature, the same is not valid for Ge on 30% pSi, which FWHM increases with increasing annealing temperature in the range 180-340°C. This indicates an increased disorder in the Ge epilayer in correspondence of the annealing temperature at which pSi changes from being compressively strained to tensile strained. However, further increasing the annealing temperature the Ge FWHM starts again to decrease with increasing *T* as observed for the other grown VSs.

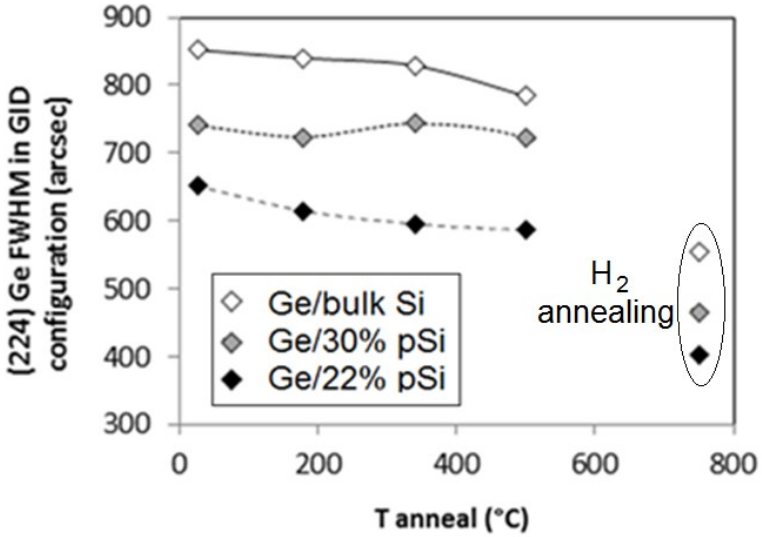

Figure 5.7: FWHM of the Ge epilayers retrieved from HT-XRD (224) Omega/2Theta scans in GID configuration as a function of annealing temperature. The FWHM measured after 3 cycles of H_2 annealing at 750°C is also reported.

The Ge FWHM for Ge grown on the different pSi buffers is always smaller than that of Ge grown on bulk Si, indicating Ge on pSi has always a better strain distribution compared to Ge on Si. After H_2 annealing the Ge FWHM retrieved from GID analysis is 27% smaller for Ge grown on 22% pSi compared to Ge grown on bulk Si, while a FWHM improvement of 23% is observed at room temperature in presence of 22% pSi. It follows that pSi buffer reorganization does not have a major effect on the evolution of strain distribution within Ge during annealing. The FWHM for Ge grown on 30% pSi is found in between that of Ge grown on bulk Si and on 22% pSi both for as-grown samples and after H_2 annealing, suggesting that the larger porosity of the buffer is not sufficient to compensate the better Ge crystalline quality of Ge grown on 22% pSi.

5.2.2 Grazing exit diffraction (GED) analysis

In the case of GED configuration, the direction of integration of the diffracted X-rays by the detector makes the geometry mainly sensitive to the broadening of the investigated reciprocal lattice point in the Omega direction[28]. It follows that the change in Ge FWHM measured in GED configuration during annealing strongly depends on the variations in sample curvature and mosaicity[29] introduced by TDs nucleated during the Ge relaxation process. Again, Ge grown on bulk Si as well as on 22% and 30% pSi buffers are investigated but the omega/2Theta scans for Ge on 30% pSi are not reported here.

During annealing an increase in the bulk Si (004) FWHM from 57 to 60 arcsec for Ge on bulk Si and from 45 to 72 arcsec for Ge grown on 22% pSi suggests thermal effects are influencing the Ge FWHM only for what concerns Ge grown on pSi. However, as the provided thermal budget is the same for both VSs and significant curvature of the Si substrate is not expected as a consequence of the much larger thickness of the Si wafer compared to that of the grown Ge epilayers, the observed FWHM increase for the Si peak in presence of pSi is possibly ascribed to the introduction of some defects from pSi within bulk Si. In particular, introduction of defects in Si could be due to incomplete desorption of pSi internal surface before epitaxy or to void migration from pSi within bulk Si at high temperature. The large observed values for the Si (004) FWHM in the order of 50 arcsec collected before annealing are mainly a consequence of the deformation of tantalum springs introduced on the substrates mounted on the HT-XRD holder. As the increase in Si FWHM for Ge on bulk Si during annealing is very small, this indicates that changes in Ge FWHM during annealing are not strongly influenced by variations in sample curvature, and hence the relative variation in FWHM for Ge grown on pSi and on bulk Si collected in GED configuration as a function of temperature can be used for a qualitative analysis of dislocation content variation during annealing in presence and absence of the pSi buffer. The Omega/2Theta scans for Ge grown on bulk Si and on pSi collected in GED configuration for the different investigated annealing temperatures are reported in Figure 5.8.

The signal arising from the pSi buffer is not visible in the collected Omega/2Tetha GED scans as the intensity diffracted by pSi and bulk Si are within the detector acceptance angle at the same time, thus resulting in a single diffraction peak with intensity given by the sum of the intensities of the two peaks. The Ge diffraction peak collected in GED configuration is always larger than that collected in GID configuration, both for Ge on bulk Si and on pSi. This is a consequence of the fact that, during the scan, the Ge reciprocal lattice point passes through the Ewald sphere slower in the GED geometry, thus resulting in larger peaks [152]. The collected scans for Ge on bulk Si and on 22% pSi are very similar each other, with the Ge diffraction peak for Ge on pSi being always slightly sharper than that of Ge grown on bulk Si.

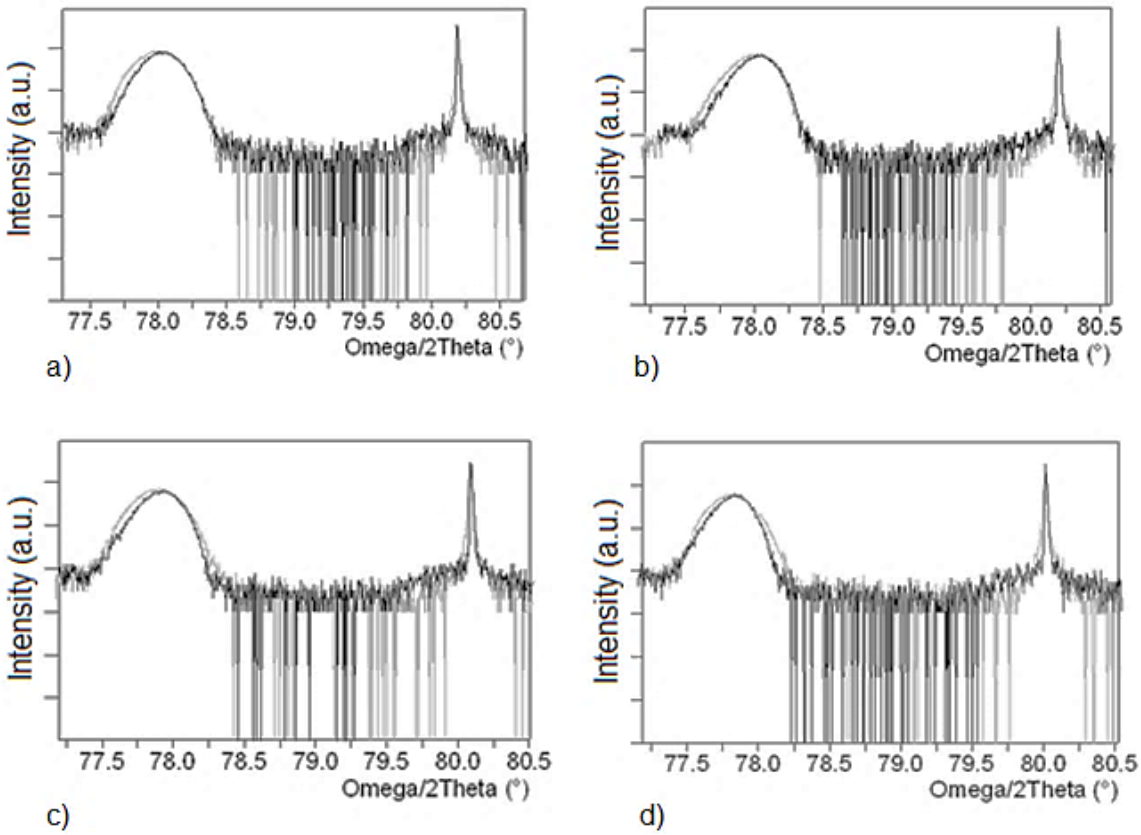

Figure 5.8: Omega/2Theta scans collected in GED configuration for Ge grown on bulk Si (grey line) and on 22% pSi (black line) during N_2 annealing at the temperature of a) 26°C, b) 180°C, c) 340°C and d) 500°C.

The Omega/2Theta scans for Ge grown on bulk Si and on 22% pSi collected in GED configuration after 3 cycles of H_2 annealing at 750°C are reported in Figure 5.9. After H_2 annealing the Ge diffraction peak for Ge grown on pSi is much sharper than that for Ge grown on bulk Si, indicating a much stronger reduction in Ge mosaic broadening occurred in presence of the pSi buffer after annealing at high temperature. Again, the Ge diffraction peak for Ge grown on 22% pSi shows an asymmetric broadening towards larger 2Theta angles confirming the formation of a SiGe alloy at the Ge/pSi interface which is believed to have a role in te observed crystalline quality improvement by modifying the buffer lattice constant.

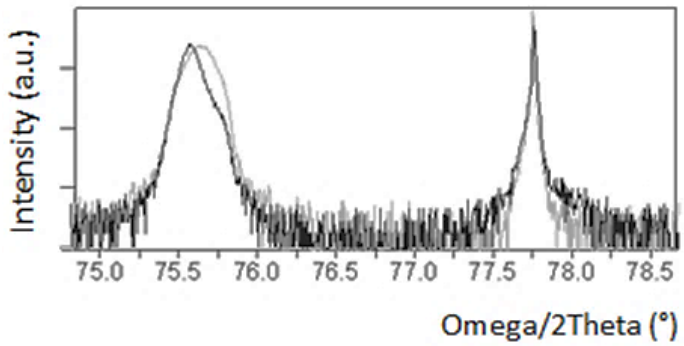

Figure 5.9:.(224) Omega/2Theta scans for Ge grown on bulk Si (gray line) and on 22% pSi (black line) in GED configuration after 3 cycles of H_2 annealing at 750°C.

The FWHM values of the Ge diffraction peak retrieved from (224) GED Omega/2Theta scans for both Ge grown on bulk Si and on the 22% and 30% pSi buffers are reported in Figure 5.10 as a function of temperature. Increasing the annealing temperature the mosaic broadening of the Ge epilayer decreases for both Ge on bulk Si and on 22% pSi, the key factor being dislocation motion and annihilation driven by high temperature conditions. On the other hand, the Ge FWHM for Ge grown on 30% pSi is again found to increase for low temperature annealing, as already observed in GID configuration thus confirming the change in strain state for 30% pSi is accompanied with increased disorder within Ge. Again, further increasing the annealing temperature the Ge FWHM for Ge on 30% pSi starts to decrease as observed for the other grown samples.

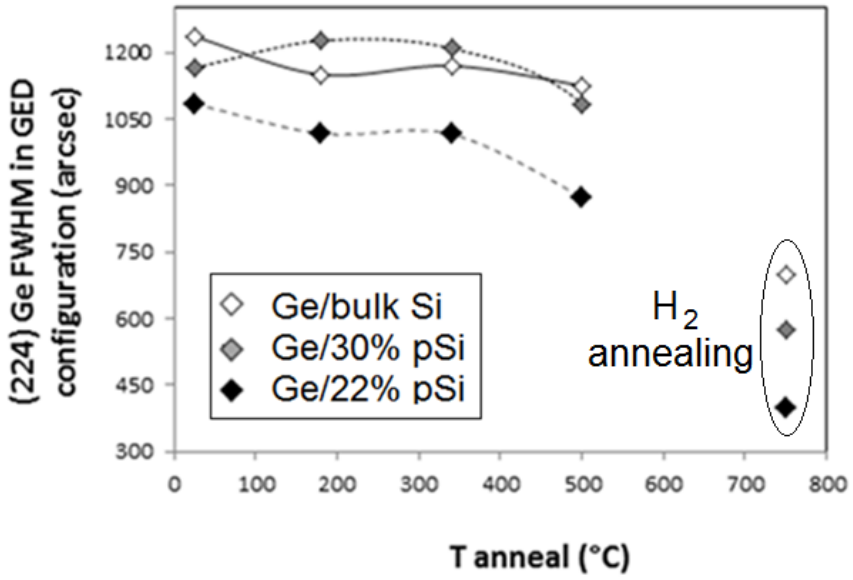

Figure 5.10: FWHM of the Ge epilayer retrieved from HT-XRD (224) Omega/2Theta scans in GED configuration as a function of annealing temperature. The FWHM measured after 3 cycles of H_2 annealing at 750°C is also reported in Figure. The data for both Ge grown on bulk Si and on 22% and 30% pSi are shown.

For Ge grown on bulk Si and on 22% pSi, the decrease in Ge FWHM for annealing temperatures <500°C is similar in the two cases. This indicates that the presence of the 22% pSi buffer does not strongly affect Ge mosaic broadening for low annealing temperatures. However at 500°C, which corresponds to the reorganization temperature of 22% pSi, a strong reduction in FWHM is observed for Ge grown on pSi, the same effect being not observed for Ge grown on bulk Si. Increasing the annealing temperature to 750°C the difference in measured FWHM for Ge on 22% pSi and on bulk Si further increases. A relative FWHM improvement of 12% is been observed for Ge on 22% pSi compared to Ge on bulk Si for as-grown samples, while a very large improvement of 43% is observed for Ge on 22% pSi after cyclic annealing. Again, after H_2 annealing the Ge FWHM for Ge grown on 30% pSi is found in between that of Ge grown on bulk Si and on 22% pSi, confirming Ge on 22% pSi has the best crystalline quality.

The enhanced mechanism for Ge crystalline quality improvement in Ge grown on 22% pSi compared to Ge on Si is found to start at the temperature for which macroscopic reorganization of 22% pSi occurs (500°C). As a consequence we believe porous buffer reconstruction to play a key role in the stronger reduction in Ge mosaic broadening observed for Ge grown on pSi during annealing. In particular, we attribute this effect to a stronger TDD reduction in Ge grown on pSi compared to Ge on bulk Si, during annealing, which could be a consequence of a higher degree of freedom for the Ge epilayer grown on pSi during annealing, promoting dislocation motion and annihilation at high temperature. Moreover, interdiffusion of Ge in the pSi lattice is believed to have an active role in Ge mosaicity reduction, by modifying the lattice constant at the Ge/pSi heterointerface, further alleviating the lattice constant mismatch existing between Ge and Si. TEM analysis has been carried out to understand the main mechanism for dislocation reduction in annealed Ge on pSi and to assess the TDD of the annealed epilayers. The results of TEM analysis are presented in Paragraph 5.3.

5.2.3 Reciprocal space map analysis

The Ge diffraction peak for Ge grown on pSi is shifted of 0.1° towards larger 2Theta angles compared to the peak of Ge grown on bulk Si. This effect is attributed to a larger tilt of the Ge epilayer for Ge grown on bulk Si compared to Ge grown on pSi, as observed from the (004) RSMs of annealed VSs which are reported in Figure 5.11. A smaller spreading in both Q_x and Q_Y directions is observed for Ge grown on pSi compared to Ge on Si, as already discussed in this Chapter. From symmetric (004) RSMs a net average

crystallographic tilt of the Ge epilayer with respect to the Si substrate of 0.04° is obtained for Ge on 22% pSi and of 0.08° for Ge on bulk Si. The appearance of a net crystallographic tilt for annealed samples, which was not observed for as-grown samples, is attributed to the smaller surface area (~ 8 x 8 mm^2) of the samples investigated after high-temperature treatment compared to that of investigated samples before annealing. This suggest that an inhomogeneous tilt distribution was present for as-grown samples, which average value was zero for large area VSs and becomes different from zero for small area annealed samples. The appearance of a net crystallographic tilt between the Ge epilayer and the Si substrate after annealing could also be attributed to the existence of an asymmetric slip system for dislocations caused by the 6° offcut of used Si substrates, which hamper dislocation annihilation in the offcut direction introducing preferential directions for Ge tiling [143]. However, in this case a larger tilt would have been expected for Ge on pSi and not for Ge on bulk Si, as a consequence of the much larger annihilation of TDs deduced from HR-XRD analysis for the former sample, so that it is more reasonable to attribute the appearance of tilt to the different area of the investigated substrates.

As a net average crystallographic tilt which is half of that found for Ge on bulk Si is observed for Ge on pSi, this suggests that the presence of the compliant pSi buffer is effective in accommodating part of the strain induced misorientation of the Ge epilayer. Reduction of the tilt of the Ge epilayer for Ge grown on pSi is beneficial in view of the subsequent epitaxy of APD and APB-free III-V semiconductors on Ge on Si VSs as the tilt of the starting substrate, which is necessary to ensure double steps are formed at Si surface, results almost maintained at Ge surface.

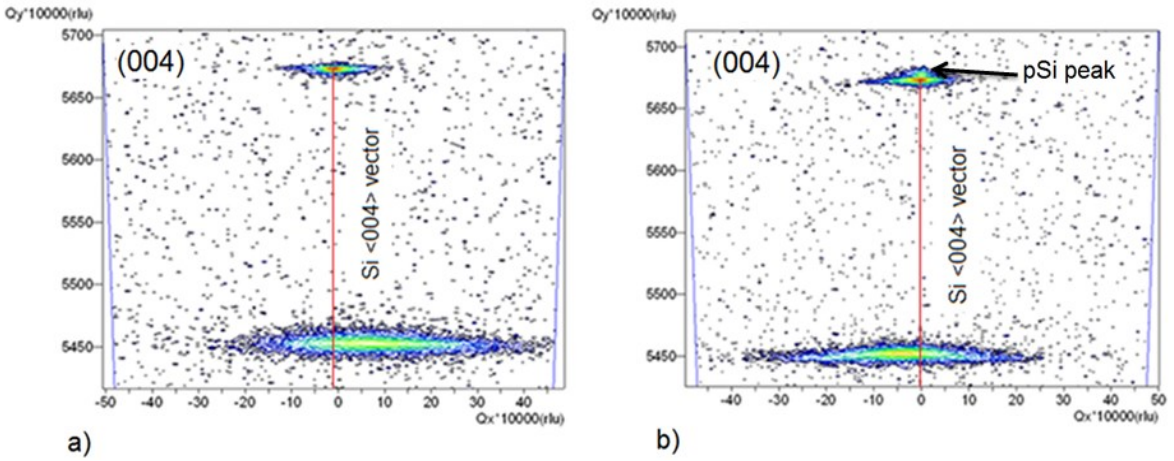

Figure 5.11: (004) symmetrical RSMs after three cycles of H_2 annealing at 750°C for: a) Ge grown on bulk Si and b) Ge grown on 22% pSi. A smaller spreading of the Ge reciprocal lattice point is observed in both Q_Y and Q_X direction for Ge grown on 22% pSi, together with a smaller net average crystallographic tilt of the Ge epilayer with respect to the Si substrate.

In order to obtain the values for $a_{Ge||}$ and $a_{Ge\perp}$and the degree of relaxation *R* of Ge grown on pSi after annealing, asymmetric (224) RSMs is collected.

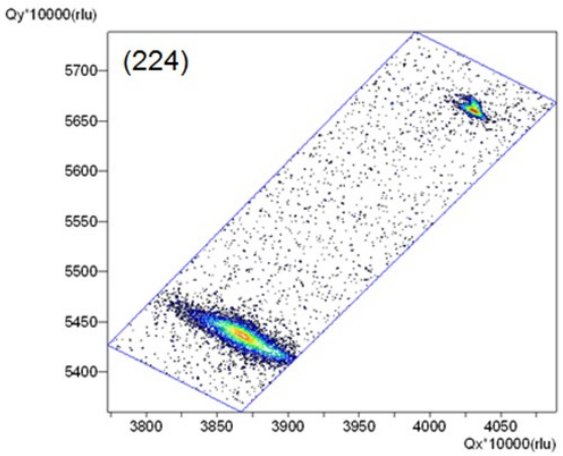

Figure 5.12: (224) RSMs after three cycles of H_2 annealing at 750°C for Ge grown on 22% pSi.

As the Ge tilt is different from zero in this case, it is necessary to correct the epilayer coordinates by rotating the Ge RELP around the bulk Si RELP by an angle γ so that the Ge RELP is located underneath the RELP of Si at the same Q_X value [154]. In this way the effect of tilt on the epilayer coordinates results eliminated and the coordinates of the Ge RELP are only representative of its strain state and composition. The tilt is removed using the following rotation for each set of Ge coordinates in (004) and (224) RSMs [155]:

$$\begin{pmatrix} k_{Ge||}^{hh4} \\ k_{Ge\perp}^{hh4} \end{pmatrix}_{corrected} = \begin{pmatrix} cos\,\gamma & -\sin\gamma \\ \sin\gamma & \cos\gamma \end{pmatrix} \begin{pmatrix} k_{Ge||}^{hh4} \\ k_{Ge\perp}^{hh4} \end{pmatrix}_{tilted} \qquad 5.1$$

where h=0 for the symmtric RSMs and h=2 for the asymmetric one.

The lattice constants and degree of relaxation of annealed Ge on pSi are reported in Table 5.1. The presence of the porous buffer is found to not degrade the degree of relaxation of the Ge epilayer indicating Ge on pSi VSs are suitable for subsequent epitaxial growth. Since complete relaxation is observed for annealed Ge on pSi, further relaxation of the Ge epilayer and further nucleation of TDs during subsequent wafer processing is not expected.

Table 5.1: Epilayer tilt, lattice constants and degree of relaxation for annealed Ge on 22% pSi VSs.

	γ (°)	$a_{Ge\|\|}$ (Å)	$a_{Ge\perp}$ (Å)	R (%)
Ge on 22% pSi	0.04	5.6577	5.6552	101

5.3 TEM analysis

XTEM micrographs of the Ge epilayers grown on bulk Si and on 22% pSi are collected after 30 minutes of H_2 annealing at 750°C to obtain information about sample morphology and defect distribution in presence and absence of the pSi compliant buffer. A low magnification cross-section image of Ge grown on bulk Si collected in two beam condition is reported in Figure 5.13. The strong contrast between adjacent regions in Ge indicates the presence of defects which locally tilt the crystalline lattice from the diffracting condition thus resulting in darker regions. At the Ge/Si heterointerface, a high density of defects is visible, which extends across the entire epitaxial layer. In particular, a large TDD is observed close to the growth interface with TDs gliding on {111} slip planes and preferentially annihilating within the first ~ 400 nm of Ge. Above this strongly defected region a brighter Ge region is found, indicating coherent diffraction and hence a rather good crystalline quality. Fewer defects are visible here, this better crystalline quality region extending for about 500 nm within Ge. However, further increasing the distance from the growth interface the Ge crystalline quality degrades. This represents an unexpected result as TDD in heteroepitaxial layers is known to decrease with incresing film thickness, as a consequence of the incresing probability for TDs to meet at a point and annihilate [143].

Degradation of Ge cristallinity with increasing epilayer thickness is expected as a consequence of the double step growth process employed during epitaxy. However, a very thin Ge seed layer with a thickness of only ~150 nm is deposited at the lower growth rate and better cristallinity, so that a degradation in Ge crystalline quailty due to the increased growth rate is expected at this distance from the heterointerface rather than at a distance of about 1µm as observed in Figure 5.13. While some contaminants could be responsible for the observed incrase in TDD with thickness, further analysis is necessary to understand this phenomenon.

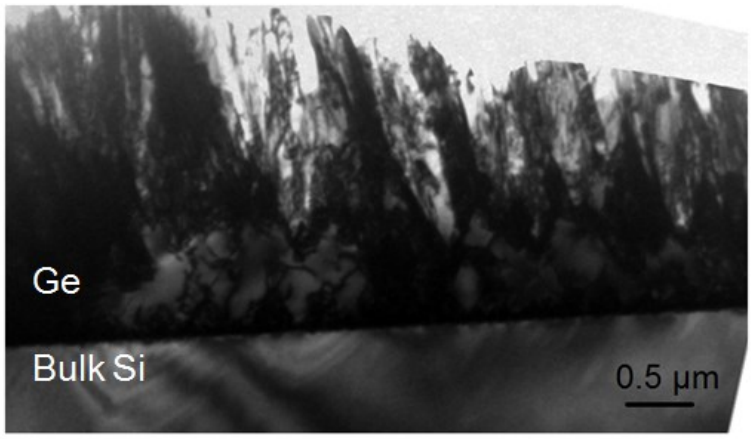

Figure 5.13: Low manification XTEM image of Ge grown on bulk Si collected in two-beam condition.

High magnification XTEM micrographs of Ge grown on bulk Si are reported in Figure 5.14 to better investigate the growth interface. Again, a region with low density of defects is observed few hundreds on nm above the growth interface in Figure 5.14 a). Above this region a strongly defected Ge crystal is present with several slanted TDs propagating within Ge. Figure 5.14 b) reveals that the Ge/Si interface is very rough, with a peak to valley distance larger than 30 nm. This large interface roughness is attributed to the H_2 plasma etching of the Si substrate performed before epitaxy, and is considered one of the main causes for the large observed Ge RMS roughness for Ge grown on bulk Si. Apart from the large interface roughness, Figure 5.14 b) shows the typical features observed for direct Ge epitaxy on bulk Si, consisting in a confined dislocation network at the heterointerface and 60° TDs glinding within the Ge epilayer on {111} slip planes.

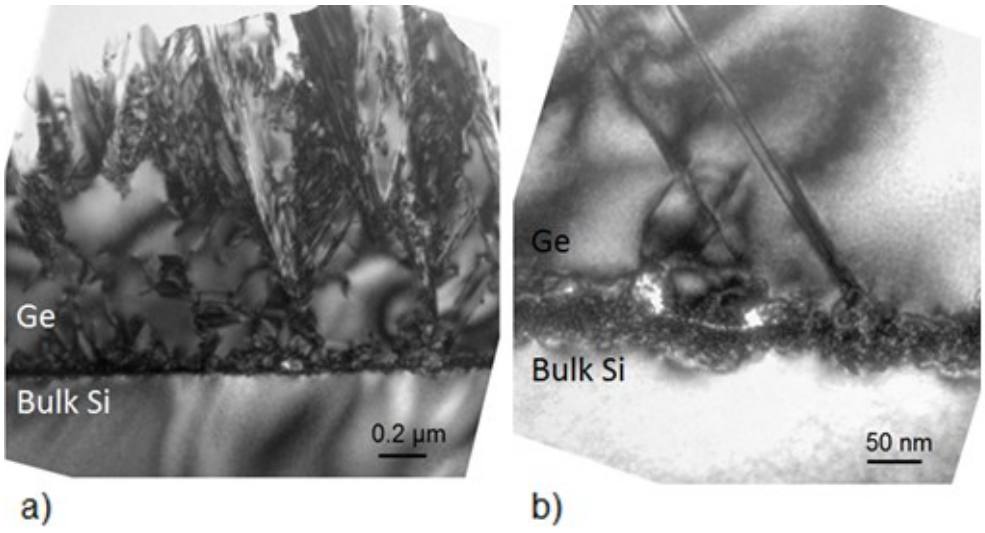

Figure 5.14: XTEM micrographs collected at a) low mangification and b) high magnification of Ge grown on bulk Si showing a high TDD within Ge and a confined dislocation network at the interface.

The confined dislocation network extends within Ge for ~50 nm, the same result being obtained by Professor R. Loo and collaborators [6]. From cross-sectional TEM images a higher density of extended defects is observed within Ge, as compared to that assessed at top Ge surface using EPD analysis.To investigate the mechanism behind the stronger reorganization of Ge grown on pSi, XTEM micrographs of the germanium epilayer grown on 22% pSi are also collected after a single annealing at 750°C. A low magnification XTEM micrograph of Ge grown on 22%pSi is reported in Figure 5.15. In contrast to what is observed for Ge grown on bulk Si, for Ge grown on pSi most extended defects are find confined within the first μm of Ge, with the upper part of the grown epilayer showing only very few propagating defects.

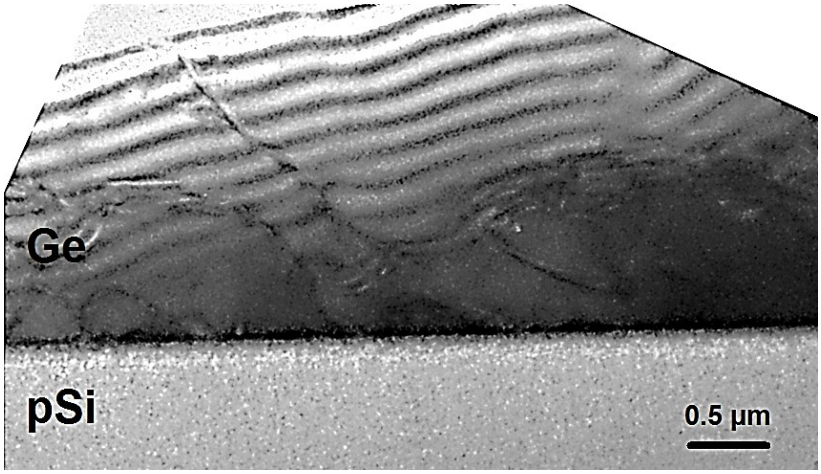

Figure 5.15: Low magnification XTEM micrograph of Ge grown on 22% pSi after 30 minutes H_2 annealing at 750°C. Extended defects are mainly confined in the first μm of the Ge epilayer.

In Figure 5.16 high magnification XTEM images of the Ge/22% pSi heterointerface are reported.The density of extended defects visible for Ge grown on pSi in Figure 5.16 a) is smaller than that observed for Ge grown on bulk Si, in accordance to the data of HR-XRD analysis. In addition, Figure 5.16 a) reveals that, together with slanted dislocations, also defects propagating parallel to the growth interface are present in the Ge epilayer grown on top of pSi, the same being not observed for Ge on bulk Si.

In contrast with what is observed for Ge grown on bulk Si, Figure 5.16 b) shows that the growth interface for Ge grown on 22% pSi is almost flat. This indicates that the thermal budget provided to the growing substrate before and during epitaxy is sufficient for reorganization of pSi resulting in a smooth pSi surface even after the H_2 plasma cleaning process. Despite the flat pSi surface, the top part of pSi in not depleted of pores, as a consequence of the reduced thermal budget provided before epitaxy.

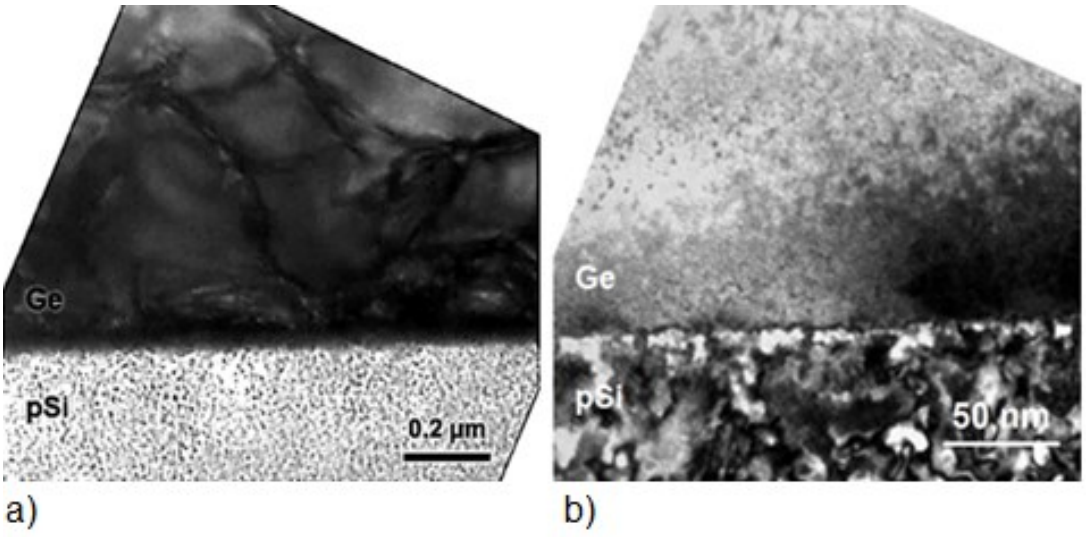

Figure 5.16: XTEM images of the Ge/pSi heterointerface after 30 minutes H_2 annealing at 750°C collected at a) low magnification and b) high magnification.

The confind dislocation network visible across the entire growth interface for Ge on bulk Si, which is shown in Figure 5.14 b), is not always visible for Ge grown on pSi, as shown in Figure 5.16 b). The presence of an inhomogeneous dislocation network at the Ge/pSi heterointerface indicates that in presence of pSi the accomodation of the lattice mismatch is not homogeneous across the whole heterointerface. Moreover, this indicates that local deformaton of the pSi buffer during epitaxy may locally suppress dislocation nucleation, the same being not possible for Ge on bulk Si.

Figure 5.17 shows another magnified image of the Ge/pSi interface revealing that, where the confined network of dislocations is present, it is confined in a thinner part of the Ge epilayer ~ 30 nm compared to a thickness of ~50 nm observed for Ge grown on bulk Si. This is ascribed to the reduced density of strain-relieving MDs expected to be necessary for complete relaxation of Ge grown on pSi, as a consequence of partial accomodation of lattice mismatch due pSi tensile strain. This reduced density of MDs is in turn expected to lead to the threading of a reduced density of TDs across the Ge epilayer and hence to the formaton of a thinner network of confined TDs in the interface region.

Even though strong intermixing between Ge and 22% pSi is deduced from HR-XRD analysis after cyclic annealing at 750°C, Figure 5.17 shows that the thermal budget provided after a single annealing step is not sufficient for evident intermixing.

Penetration of Ge within the pores of pSi has been recently observed after reorganization of pSi in a layer with large voids promoted by high temperature annealing [114, 115]. While the high temperature annealing of low porosity pSi layers results in a sealed surface, higher porosity layers transform into large cavities during annealing [156], suggesting that a higher porosity pSi buffer was investigated in [114, 115] compared to the 22% pSi buffer investigated here, and for which Ge crystalline quality improvement

has been observed. As in this thesis a degradation in Ge crystaline quality with increasing pSi buffer porosity has been observed, it seems that the use of high porosity buffers for which strong intermixing of Ge in the porous network is possible also for as-grown samples could be disadvantegeous in terms of the resulting Ge crystallinity. In fact, the large porosity and hence fragility of pSi needed for the formation of large cavities at pSi surface hamper pSi tensile strain, which is found to be the main mechanism for crystalline quality improvement in as-grown Ge on pSi.

In Figure 5.17 typical 60° TDs which characterize crystal lattices with a diamond or zinc blende structure are also visible in Ge grown on pSi, since the presence of pSi does not modify the slip planes for TDs. However, we observe that after glinding within Ge for a certain distance from the growth interface, TDs in annealed Ge on pSi tend to bend in a plane parallel to the growth interface, the same being not observed for Ge on bulk Si. Propagation of TDs parallel to the growth interface, which is ascribed to the presence of pSi, has been previously reported for Ge on Si epitaxial systems employing graded SiGe buffers [157, 158], or terrace graded virtual substrates [159, 160].

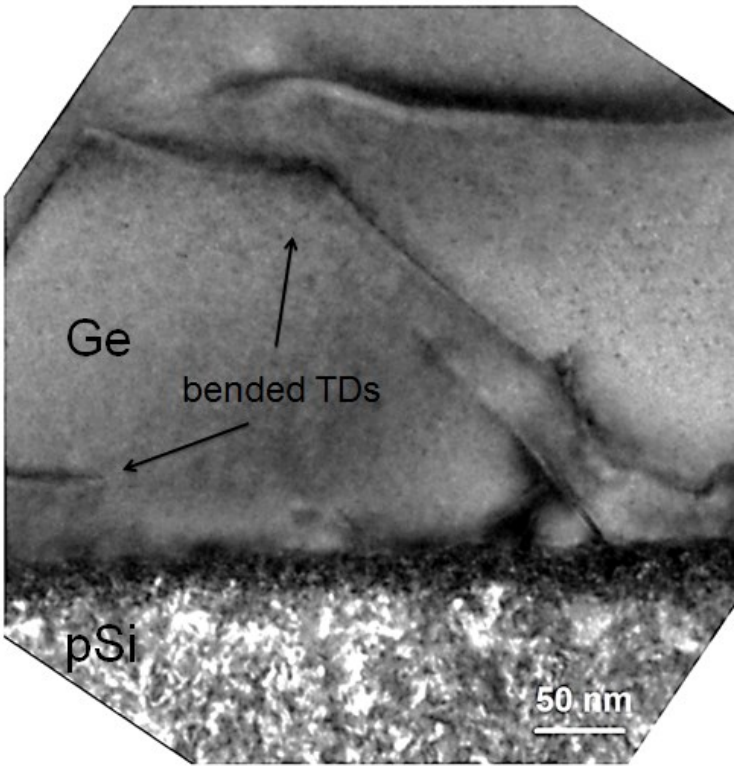

Figure 5.17: XTEM micrograph of the Ge/22% pSi interface after 30 minutes H_2 annealing at 750°C. TDs propagating parallel to the growth interface are visible.

In the case of linearly graded or terrace graded SiGe buffers, bending of dislocations in a plane parallel to the growth interface has been ascribed to a stress field generated at the interface by a change in composition larger than a crytical value [34]. Bending of

dislocations reduce the density of TDs in the upper part of the Ge epitaxial layer and TDD values in the order of 10^6 cm^{-2} have been obtained using thick graded SiGe buffers [64]. In analogy with this, dislocation bending in Ge on pSi confines most defects in the bottom part of the Ge epilayer (as also observed in Figure 5.15) and this is considered to be the main mechanism for the observed stronger reduction in mosaicity observed for Ge on pSi during annealing. Since the stronger improvement in Ge cristallinity in presence of pSi is found to start at the pSi reorganization temperature (i.e. 500°C), we believe dislocation bending to be introduced by pSi during its reorganization at high-temperature. In particular, we believe reorganization of pSi during annealing is believed to introduce a strain field within Ge which is responsible for the observed bending of dislocations, as observed using linearly graded or terrace graded SiGe buffers [158, 159].

A very high magnification XTEM image of the Ge/22% pSi interface is reported in Figure 5.18, revealing an almost flat and clean interface between Ge and pSi, with an array of MDs separated about 10 nm each other which are pinned at the heterointerface. This is similar to what is typically observed for Ge epilayers grown on bulk Si [161]. A selected area diffraction pattern of the Ge/pSi interface is shown in the inset of Figure 5.18. The pattern shows well aligned bright spots indicating the presence of two different crystal lattices having the same structure but different atomic spacings, indicating crystalline Ge is grown on top of pSi with the same crystallographic orientation.

Figure 5.18 shows that both amorphous and crystalline regions are present in pSi, the presence of amorphous regions being attributed to voids in the buffer. Below each MD an amorphous region is found within pSi, while the Ge crystalline structure is maintained also in correspondence of MDs. This suggests that part of the strain field introduced by each single MD is partially relaxed by local deformation of pSi thus possibly reducing the density of nucleated TDs within Ge. The same effect was not observed for Ge grown on bulk Si [161] as the larger Young's modulus of bulk Si compared to that of pSi makes it energetically favourable nucleation of defects and deformation of the epilayer rather than substrate deformation. On the other hand, in between a MD and the successive one the pSi buffer shows a well ordered crystalline stucture at the heterointerface, which extends from pSi into Ge. Partial accomodation of the strain field introduced by single MDs by local deformation of the pSi buffer is believed to contribute in the observed crystalline quality improvement observed for Ge grown on top of low porosity pSi buffers, making it less favourable the nucleation of TDs within Ge. In particular, this mechanism is considered the main mechanism for the observed crystalline quality improvement in Ge grown on 30% pSi, which shown a more homogeneous strain distribution and a smaller Ge mosaic broadening compared to Ge on bulk Si, even in absence of tensile strain of the pSi buffer.

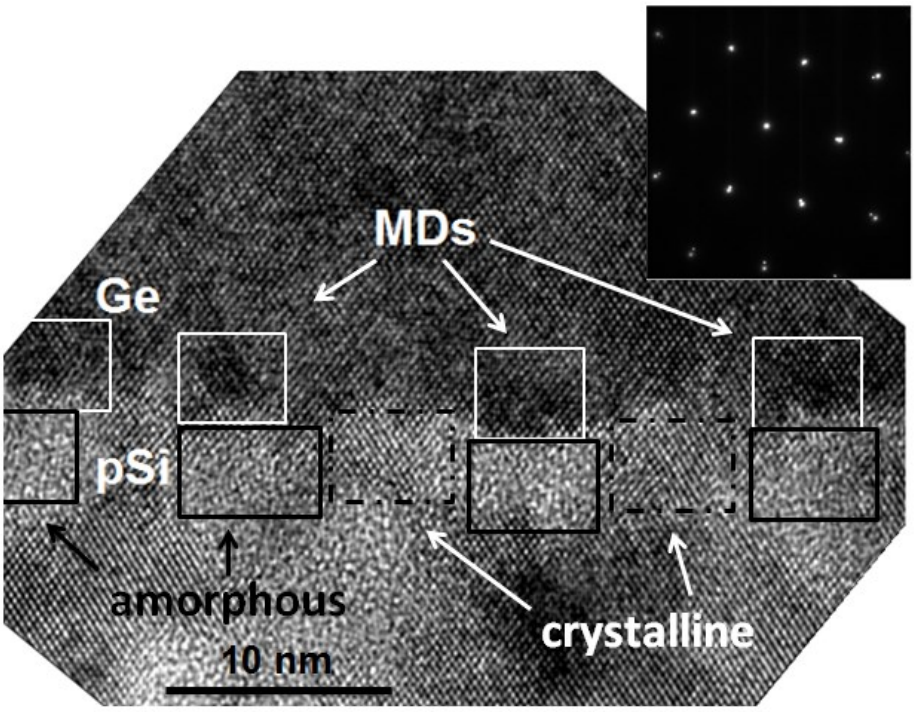

Figure 5.18: High magnification XTEM micrograph of the Ge/22%pSi heterointerface showing pinned MDs at the growth interface. Red squares indicate MDs while orange rectangles indicate amorphous regions in pSi in correspondence of each MD. In beetween two distinct MDs pSi exhibits a well ordered pattern in the green rectangles, indicating a monocrystalline structure at the growth interface far from MDs. A selected area diffraction pattern shows crystalline Ge is grown on top of pSi with the same crystallographic orientation.

5.4Twin content in grown Ge epilayers

pSi is created starting from a monocrystalline Si substrate from which a part of the Si atoms are removed, thus still resulting in a monocrystalline structure. Nevertheless, crystal planes having orientations which differ from the original (001) surface of the starting substrate appear at wafer surface after mesoporous silicon formation. During Ge heteroepitaxy the presence of different crystal orientations exposed at Si wafer surface could lead to the growth of Ge epilayers with a large content in stacking faults (SFs) and twins compared to Ge grown on bulk Si, this effect possibly degrading Ge crystalline quality. SFs and microtwins have been largely observed in epitaxial layers grown on porous substrates such as GaAs grown on pSi, where they represent the dominant defects [162].

Twins and SFs have been also observed in Ge on Si and Ge on pSi substrates grown during this thesis work. An example of extended defect in Ge grown on bulk Si is reported

in Figure 5.19, together with the corresponding selected area diffraction pattern, showing well defined Bragg diffraction spots together with lower intensity spots lying at ±1/3 of the distance from the main spots along <111> directions. The main intensity spots are associated to the main Ge orientation while lower intensity spots are associated to presence of twins.

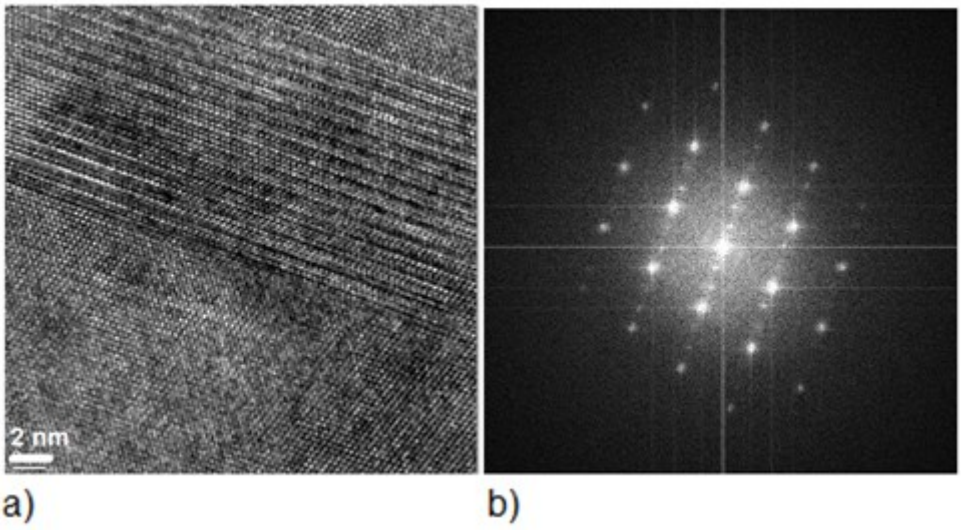

Figure 5.19: a) Magnified XTEM image showing twinned planes in Ge grown on bulk Si and b) the corresponding selected area diffraction pattern.

Although twins are electrical inactive defects as don't introduce broken bonds in the crystal lattice, a misorientation of the boundary from the twinning plane causes their electrical activity [163]. Moreover, twins are believed to arrest the glide of dislocations causing the nucleation of additional defects which increases the TDD [164], so that an assessment on twin presence in Ge on pSi and a comparison with twins in Ge on bulk Si is of interest in evaluating the Ge cristallyne quality.

In order to investigate the presence of twins in Ge grown on bulk Si and on pSi, X-ray Pole Figures (PFs) are collected for grown samples. To reveal the presence of twinned Ge regions, Ge {111} PFs are collected by fixing 2θ=27.28°, corresponding to Bragg angle for (111) diffracting planes of Ge. The diffracted intensity of x-rays is collected while rotating the χ (zenithal) angle from 0° to 90° and the φ (azimuthal) angle from 0° to 360° for each value of χ. In this way all the families of diffracting planes having an interplanar distance close to that of Ge {111} planes are represented in the PFs as different RELPs. The PFs for Ge grown on bulk Si and on pSi are represented in Figure 5.20. In both PFs the four RELPs located at χ= -22° φ= 0°, χ= -18° φ=60°, χ=-15° φ= -60° and χ= -10° φ= 180° are attributed to the (111),$(\bar{1}11)$ $(1\bar{1}1)$ and $(11\bar{1})$ planes of the same Ge single crystal. The other visible RELPs in the PFs indicate the presence of twins in the Ge epilayer.

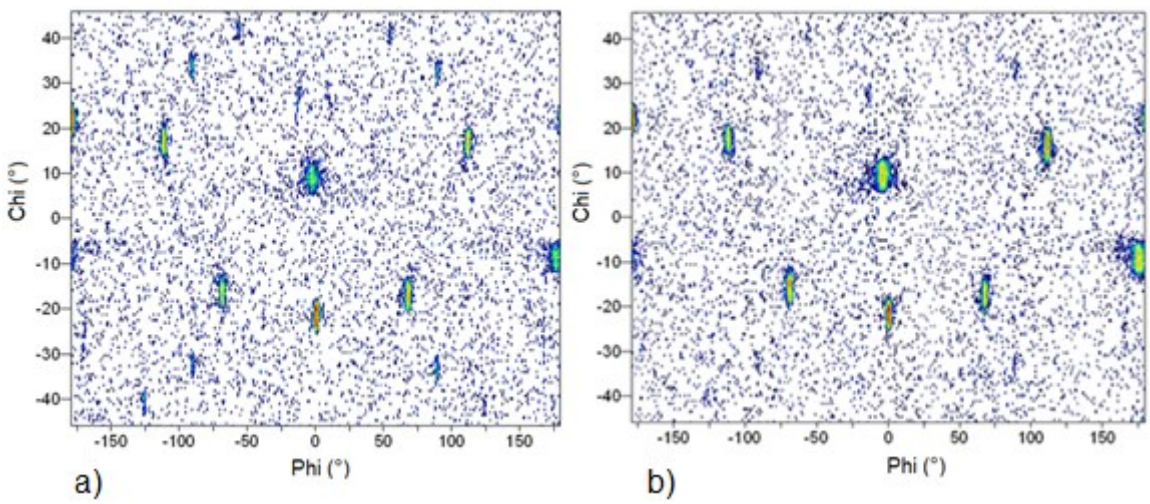

Figure 5.20: Ge (111) pole Figure for a) Ge grown on bulk Si and b) Ge grown on 22% pSi.

In Figure 5.20 a large twin content is observed for Ge grown on bulk Si, with slightly less Ge varieties observed for Ge on bulk Si. A large number of twins was observed for Ge on Si heterostructures as a consequence of the very-high employed growth rates >8 nm/s [165]. However, Ge on Si VSs realized in this work have been grown at a rate of about 2nm/s, which is about one half than that for which twins were no more observed in [165]. We believe observed twins have not to be ascribed to the relatively high employed growth rate during epitaxy, also considering that this would not explain the observed difference in twin content between Ge on bulk Si and on pSi. Twins in Ge grown on bulk Si are rather attributed to the H_2 plasma etching process performed before epitaxy which leads to a large Si surface roughness together with the appearance of different crystallographic orientations at Si surface. The reduced twin content in Ge on pSi is attributed to partial reconstruction of the surface of pSi after H_2 plasma etching step, resulting in a smoother surface thus partially compensating the negative effect introduced by plasma etching.
In order to improve the crystalline quality of grown Ge epilayers, a growth technique which does not require plasma cleaning of the Si substrate before epitaxy is necessary.
When epitaxy is carried out on pSi the situation is more complex as several families of atomic planes already appear at wafer surface as a consequence of electrochemical etching. A high temperature annealig step would transform low porosity pSi buffers in monocrystalline Si with embedded small spheroidal voids [110], this possibly resulting in a reduction in Ge twins. However, reconstruction of the pSi top surface and depletion of pores could hamper the observed deformation of the buffer in correspondence of single MDs, as a consequence of the increased Young's modulus of the buffer surface after reconstruction, which could in turn reduce the accomodation of the lattice mismatch within pSi. In addition, we speculate that avoiding strong pSi reconstruction before and during crystal growth could represent an important aspect in Ge epitaxy on pSi. This

depeds on the fact that strong improvement in Ge cristallinity has been observed during post-growth annealing in correspondence of pSi reorganization, the same effect possibly resulting hampered in case of strong pSi reorganization already during epitaxy. Based on these considerations we believe that fine tuning of the thermal budget to be provided before and during epitaxy to pSi would have a great impact on the resulting Ge crystalline quality. LEPECVD could hence represent one of the most promising techniques for Ge epitaxy on pSi thanks to the possibility to employ reduced thermal budgets and to tune the growth temperature over a large range without degrading the growth rate.

5.5 Threading dislocation density assessment

In Figure 5.21 the (004) RC for Ge grown on bulk Si and on 22% pSi after cyclic annealing are reported. A FWHM of 561 arcsec is obtained for annealed Ge grown on bulk Si, compared to a FWHM of 343 arcsec for annealed Ge grown on pSi, corresponding to a strong FWHM improvement of 39%.

The obtained (004) FWHM for Ge grown on bulk Si exceeds the typical values obtained for high-quality thick Ge epilayers on Si, indicating a large mosaic broadening and the necessity to further improve the Ge epitaxial conditions. On the other hand, the (004) FWHM for Ge grown on pSi is comparable with that obtained in other works for 5 μm-thick Ge epilayers on Si [161] indicating rather good Ge crystallinity is obtained for Ge on pSi.

After annealing, the average reduction in TDD for Ge on pSi compared to Ge on Si can be assessed from Eq. 2.9 by considering that the other contribution to RC broadening are very similar for the two investigated samples and are negligible. In particular, in our experimental conditions finite thickness broadening, intrinsic RC broadening and instrumental broadening can be neglected, their contribution to the measured FWHM being in the order of 10 arcsec or less [63, 66]. Moreover, from the broadening of the RC of the substrate, sample curvature is found to broaden the Ge RC for less than 3% both for Ge on Si and on 22% pSi, so that its contribution can be neglected too. By using Eq. (2.9) we obtain an average TDD reduction of a factor ~ x 2.7 in presence of 22% pSi for annealed samples.

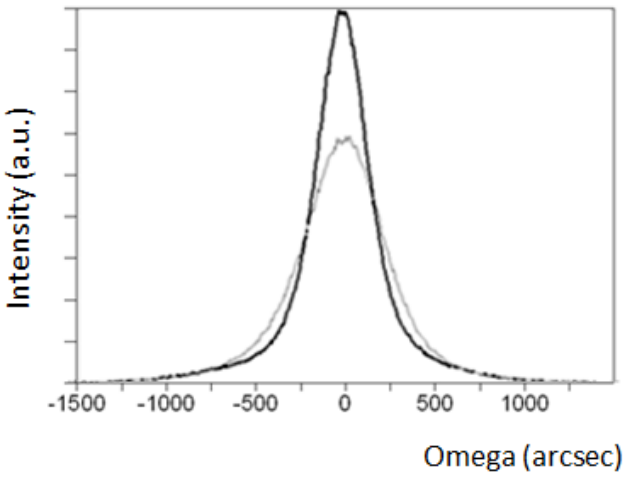

Figure 5.21. Double-crystal (004) RCs for Ge grown on bulk Si (gray line) and on pSi (black line) collected after three cycles of H_2 annealing at 750°C.

TEM plan view analysis has been carried out to assess the TDD at Ge surface after annealing, in presence and absence of 22% pSi. Some contamination is observed for both samples, indicating contaminants are introduced before or during epitaxial growth. Plan view images of not contaminated Ge regions are reported in Figure 5.22. A TDD of 1.8 x 10^8 cm^{-2} and of 2.4 x 10^7 cm^{-2} is assessed for Ge grown on bulk Si and on pSi respectively, corresponding to a TDD reduction in presence of pSi of almost one order of magnitude at Ge surface. This is much larger than the TDD reduction of a factor x 2.7 obtained from RC analysis, which considers the average change in TDD across the whole epilayer thickness. The large difference in TDD reduction is attributed to the fact that bended TDs found in Ge on pSi which do not contribute to the TDD measured at Ge surface using TEM still contribute in the broadening of the measured RC. Moreover, together with TDD reduction the introduction of 22% pSi also resulted in a suppression of dislocation pile-up, which is only observed for Ge grown on bulk Si in the form of a large number of surface TDs laying in close proximity each other.

The TDD obtained for Ge on bulk Si exceeds the typical values reported in literature, the TDD observed for Ge grown on pSi is consistent or only slightly larger than that observed by other groups for thick Ge epilayers [131, 146]. In particular, the result obtained in this work for annealed Ge grown on pSi is very similar to that reported by A. Nayfeh in his Ph.D. thesis at Stanford University [166] after cyclic H_2 annealing at 850°C of a 4.5 μm thick Ge epilayer directly grown on bulk Si. While in our case the TDD of Ge grown on bulk Si after annealing is one order of magnitude larger than that observed by A. Nayfeh, the much stronger improvement in Ge crystalline quality observed for Ge on pSi during annealing compensates for the poorer Ge epitaxial conditions resulting in a similar TDD.

The TDD assessed from TEM imaging for annealed Ge epilayers is larger than that determined from EPD analysis before annealing. This result is ascribed to the higher

resolution of TEM which can distinguish between different defects very closely spaced each other, the same being not valid for EPD as a consequence of the possible overlap of two or more pits.

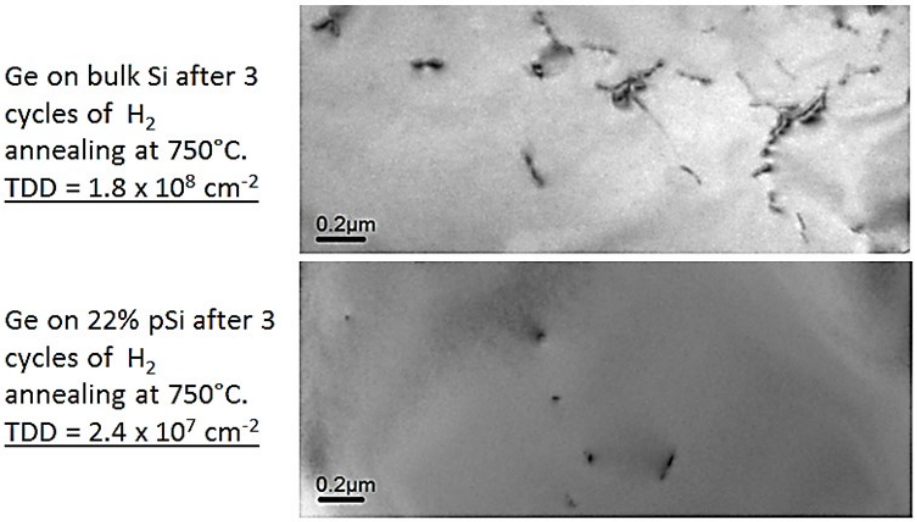

Figure 5.22: plan view TEM images of annealed Ge grown on bulk Si (top) and Ge grown on 22% pSi (bottom). TDD is reduced by one order of magnitude in presence of pSi.

The strong TDD reduction observed for Ge on pSi indicates that the use of pSi buffers for low dislocation density Ge on Si epitaxial layers could be of enormous advantage if the same improvement in Ge crystalline quality observed in the high dislocation regime ~10^8 cm^{-2} could be also obtained for germanium epilayers having a lower dislocation density in the order of 10^7 cm^{-2} or below. The results of the model of Wang and collaborators [146], which determines the lowest possible TDD in relaxed Ge epitaxial films grown on (001) Si in case of no external stress, are reported in Fig. 5.23 together with the results obtained by other research groups and in this work. According to this model the TDD at Ge surface scales down with the inverse of the thickness squared of the epitaxial layer and a TDD ~ 10^6 cm^{-2} can be achieved at Ge surface for Ge epilayers at least 5 μm-thick. This indicates that 5 μm is the minimum thickness for Ge epilayers directly grown on bulk Si for which the resulting VSs can be used as template for III-V epitaxy with minority carrier lifetime only slightly affected by dislocation presence. Provided that the same TDD reduction ~ one order of magnitude for Ge on pSi can also be demonstrated for low TDD Ge epilayers, this would allow the realization of much thinner Ge epilayers on large area Si suitable for III-V integration in the order of 1 μm [146], with the advantages of higher throughputs, reduced fabrication costs and higher thermal dissipation performance.
Moreover, It is worth noting that a TDD ~10^6 cm^{-2} represents the threshold value for which the mobility of minority carriers n-type GaAs is only slightly influenced by presence of TDs. A much smaller TDD ~ 10^5 cm^{-2} is necessary for high minority carrier lifetime in p-

type GaAs as a consequence of the much higher mobility of minority electron compared to that of holes in GaAs, which leads to a stronger interaction between electrons and TDs [167]. According to [146], a TDD as low as 10^5 cm^{-2} in GaAs grown on Ge on Si VSs would require Ge thicknesses of several tens on μm for direct Ge epitaxy on bulk Si, which is not viable from a fabrication perspective. On the other hand, the strong TDD reduction of one order of magnitude obtained by employing pSi buffers would allow the integration of few μm-thick Ge epilayers on Si with TDD~10^5 cm^{-2} suitable for the growth of large area p-type III-V epilayers. This in turn would allow the realization of III-V solar cells on p-type Ge on Si VSs, the same being hardly compatible with the direct Ge on Si approach due to the typical large TDD values [146].

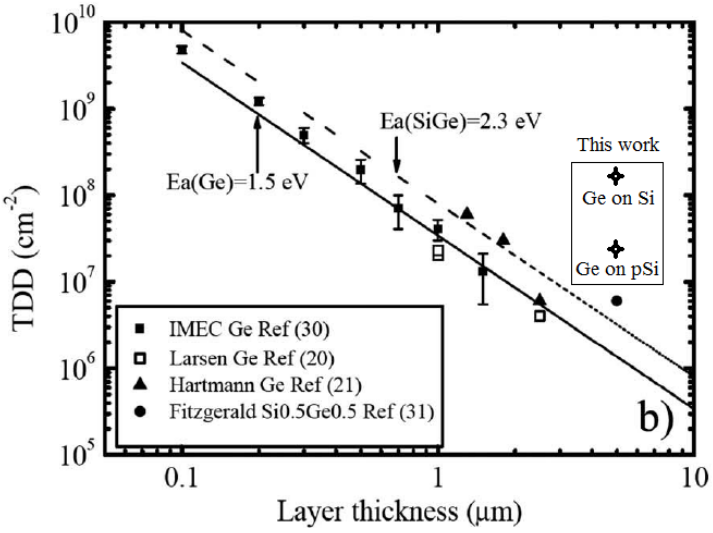

Figure 5.23: Simulation (solid and dashed lines) and experimental data of TDD at Ge surface for as-grown or single annealed Ge on Si (filled squares) or after cyclic annealing (open square and filled triangles). The TDD obtained in this work is also reported for comparison. Adapted from Ref [131].

TDD obtained in this thesis work is higher than that predicted by the model of Wang for Ge on bulk Si, both in presence and in absence of a pSi buffer. This is attributed to not optimized growing conditions and to the introduction of some contaminants during epitaxy, which is ascribed to the incomplete desorption of adsorbed species on Si surface in the load lock before crystal growth.

Nevertheless, the strong TDD reduction obtained by using pSi buffers suggests very high-quality, large-area, Ge epilayers can be integrated on Si with very low TDD values, provided that the observed dislocation reduction could also be demonstrated for excellent crystalline quality Ge epilayers.

5.6 Applicability of obtained results to the very low TDD regime

Bending of TDs in a plane parallel to the growth interface has been investigated by Hull and collaborators, by using constant composition SiGe superlattices grown on Si [159]. it was found that dislocation bending promotes the mutual interaction between dislocations, enhancing the probability of dislocations to meet at a point and annihilate. However, this mechanism was demonstrated to be not effective for low dislocation content SiGe epilayers, as the probability of dislocation annihilation was found to follow a linear dependence on TDD, thus resulting in only a negligible improvement in the crystalline quality of low TDD epilayers [159].

This result would suggest that the strong TDD reduction observed for relatively highly disclocated Ge on pSi VSs has not to be expected in the low dislocation regime. However, it is worth noting that several effects contribute in the observed improvement in Ge crystalline quality for Ge grown on pSi, and a strong dependence on TDD is not expected for all of them. In particular it is reasonable to think that the Ge crystalline quality improvement observed in as-grown Ge on pSi due to tensile strain of the buffer does not depend on dislocation content within Ge, as TDD reduction is attributed to a smaller nucleation of TDs within Ge due to the partial accommodation of the lattice mismatch between Ge and Si at the Si/pSi interface rather than to an enhanced mechanism for dislocation interaction and annihilation. While TDD reduction due to dislocation bending might still critically depend on TDD, the higher degrees of freedom of Ge grown on pSi being not strongly bounded to the bulk Si lattice constant, so as the pSi reconstruction at high temperature which is believed to further reduce the bound of the Ge lattice constant to that of Si, are expected to promote the reorganization of the Ge epilayer during annealing with possible small dependence on TDD. Finally, the observed local deformation of pSi in correspondence of single MDs, which is believed to relax part of the strain field introduced by MDs hence resulting in a reduced probability of nucleation of TDs, is not expected to depend on TDD.

In conclusion, improvement in the Ge crystalline quality by local and global pSi deformation (amorphization of pSi in correspondence of MDs and tensile strain of the entire buffer) is expected to not strongly depend on TDD. As a consequence, TDD reduction using pSi buffers is at least in part expected also in the low dislocation regime making Ge on pSi VSs a very promising technique for excellent crystalline quality Ge on Si VSs.

Chapter 6

Conclusions and further work

6.1 Conclusions

In this thesis it has been investigated a novel technique for the realization of low dislocation content and relaxed Ge on Si virtual substrates, consisting in the growth of a compliant porous silicon (pSi) buffer layer on Si wafer surface before Ge epitaxy.

We demonstrated that the crystalline quality of thick Ge epilayers grown on silicon can be strongly improved through the introduction of a low porosity pSi buffer layer in the virtual substrate architecture. In particular, both Ge strain distribution inhomogeneity and mosaic broadening have been reduced employing a 22% pSi buffer, this result being attributed to tensile strain of the buffer under the in-plane tensile stress introduced by Ge on pSi, which accommodates part of the Ge/Si lattice mismatch at the pSi/Si interface.

Buffer porosity has a key role in determining the crystalline quality of the uppermost Ge epilayer and a monotonic improvement in crystalline quality with decreasing buffer porosity in the range 22-48% has been observed, as a consequence of an increase in buffer fragility with increasing porosity, which promotes local collapses of the buffer hampering tensile strain.

Together with tensile strain, also local amorphization of the porous buffer at the growth interface in correspondence of each misfit dislocation is believed to accommodate part of the existing lattice mismatch at the Ge/pSi interface, contributing in the crystalline quality improvement observed for Ge grown on low porosity pSi.

After annealing a TDD of 2.4×10^{7} cm^{-2} has been obtained for Ge on 22% pSi, which is one order of magnitude smaller than that found in annealed Ge on bulk Si. This result, which has been attributed to bending of TDs in a plane parallel to the growth interface that confines most defects in the bottom part of Ge, is ascribed to a strain field introduced within Ge by pSi, during its reorganization at high-temperature.

LEPECVD growth technique plays a key role in the observed crystalline quality improvement for Ge on pSi allowing Ge deposition at reduced thermal budget, thus

promoting strong buffer reconstruction only during post-growth annealing which resulted in a much stronger Ge reorganization at high-temperature.
Together with a reduced dislocation content, Ge on pSi resulted in complete epilayer relaxation and a smaller Ge tilt compared to Ge on bulk Si, indicating Ge on pSi outperform Ge on bulk Si virtual substrates and are suitable for epitaxy of III-V semiconductors.
The discovery of a strong reduction in dislocation content in Ge epitaxial layers grown on pSi opens a new possibility for the integration of high-quality Ge epilayers on Si. The strength of the proposed approach consists in a strong improvement in Ge crystalline quality by means of a low-cost technique, which is easily scalable to large are Si wafers and is fully compatible with subsequent wafer processing. At the same time the possibility to perform lift-off of grown epilayers gives to the investigated technique an additional advantage over conventional methods for Ge integration on Si.
The use of pSi buffers together with LEPECVD technique allows for record high growth rates, which could transform the proposed method in an industry favored technique for the epitaxial growth of high-quality Ge and III-V semiconductors on large area Si substrates.

6.2 Further work

This work paves the basis for the integration of high crystalline quality Ge epilayers on large area Si substrates with a very high-throughput and low-cost technique. During the work done in the realization of this thesis some aspects have emerged which further investigation can improve obtained results.

- Optimization of the pSi buffer: further investigation of few μm-thick, low-porosity (≤25%) buffers grown at high rate to suppress pure pSi chemical etching could lead to an improvement of obtained results. Fine tuning of the thermal budget to be provided to pSi in order to promote its reorganization only during post-growth annealing represents another key aspect of the proposed technique.

- Improvement of Ge epitaxial conditions: the removal of H_2 plasma etching of Si wafer surface before epitaxy is mandatory in order to improve interface roughness and Ge surface roughness. To take advantage of Ge on pSi virtual substrates a further improvement in Ge growth parameters is necessary in order to reduce the TDD to ~10^6 cm^{-2}.

- Modification of the reactor configuration: the necessity to perform time-consuming NF_3 plasma cleaning of the growth chamber after each single Ge deposition limits the throughput to 0.5 wafers/day. A different reactor configuration is hence necessary to take advantage of the full potential of LEPECVD technique, for example introducing plasma confinement.

By taking advantage of the high crystalline quality achievable in Ge on pSi VSs, a method for the epitaxial growth of III-V solar cells on Si and successive lift-off by employing a low porosity/high porosity pSi double layer is proposed. This method is similar to the thin film Si solar cell approach currently under investigation by different research groups, which takes advantage of a pSi double layer as a seed layer for Si homoepitaxy and as a predetermined separation point after solar cell realiztion. In the proposed approach, pSi not only would serve to detach grown epilayers from the starting substrate, but would also provide fundamental accommodation of the lattice mismatch in accordance with the results of this thesis. In addition, Ge on pSi substrates would also enable the epitaxial growth of a SiGeSn subcell lattice matched to Ge with 1 eV bandgap, which represents the missing bandgap to push the efficiency of multijunction solar cells above the 50% limit. Ge on pSi VSs thus indicate a possible roadmap for strong cost reduction in present and future multijunction solar cells grown on Ge substrates while also showing a path for performance improvement.

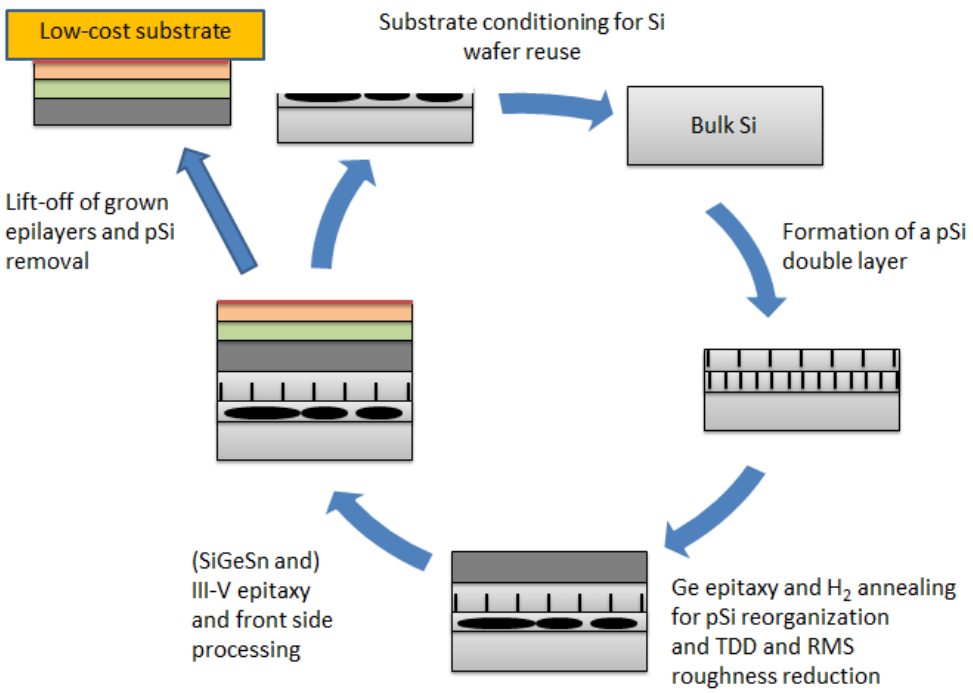

Figure 6.1: Proposed approach for the growth of III-V solar cells on silicon substrate and successive lift-off using a pSi double layer.

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