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ELECTRON DEVICE NONLINEAR MODELLING FOR MICROWAVE CIRCUIT DESIGN

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Contents

Preface

This PhD thesis contains the results of a 3-years research in the framework of microwave electron device modelling. During this time, several aspects have been faced up, from the study of new technologies to device characterization issues, from the modelling of the different dynamics coexisting in the transistor to the application of the developed models in actual designs. Nevertheless, the main topic of my research activity has been the modelling of electron devices for microwave applications and this manuscript is mainly oriented to this topic .

Electron device modelling is a research topic of great relevance, since the performance required for devices are continuously increasing in terms of frequency, power and linearity: new technologies are affirming themselves, bringing new challenges for the modelling community. In addition, the use of monolithic microwave integrated circuits (MMIC) is also increasing, making necessary the availability, in the circuit design phase, of models which are computationally efficient and at the same more and more accurate. The importance of modelling is even more evident by thinking at the wide area covered by microwave systems: terrestrial broadband, satellite communications, automotive applications, but also military industry, emergency prevention systems, medical instrumentations.

In the first chapter of this thesis, the technologies mostly used for this kind of applications will be briefly presented. Of course, the variety of microwave device is very wide, so Chapter 1 will be focused on the devices dealt with during this research activity.

In Chapter 2, a panorama will be drawn of the different type of models already present in the literature. In particular, the empirical models, which are the kind of models of our interest, will be presented and divided in two big families: equivalent-circuit-based and black-box models. For each family, some of the most known and significant modelling approaches will be summed up.

A new modelling approach for nonquasi-static effects, developed during the PhD studies, will be described in details in Chapter 3. Its empirical validation will be also reported in the chapter, by using a PHEMT in Gallium Arsenide.

The same approach has been also applied to devices in Gallium Nitride technology and the results will be shown in Chapter 4. In this chapter, the modelling of the low-frequency dispersive effects in GaN-based HEMT will be also faced up.

In Chapter 5, instead, two models for transistors in Cold-FET conditions will be presented: the models have been validated by means of two different technologies, Gallium Arsenide and Gallium Nitride.

A topic strictly related with look-up-table-based models will be dealt with in Chapter 6: the data interpolation algorithm. In this chapter, an original data approximation/interpolation algorithm will be described.

Finally, the last chapter will treat the topic of the device degradation: a new measurement setup will be presented, aimed at the characterization of the device breakdown walkout under actual operating conditions for power amplifiers.

Acknowledgment

And now, the moment of acknowledgments is arrived. First of all, I'd like to thank my tutor, Giorgio Vannini, for giving me the opportunity to work towards my PhD in the best conditions.

Thanks to Alberto Santarelli and Antonio Raffo, who shared with me their knowledge and experience: large part of my professional growth is due to them, who are great researchers, great guides and, above all, great friends.

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I want also to thank my family for the sympathy and the love they have always shown to me when I spent for the research the time owing to them. A special thanks is for David, my wonderful FM for all his moral and material support (especially in dinners and camomile teas).

Finally, I have to thank the unknown genius who invented the coffee, my best allied during the last three years.

Chapter 1

Electron Devices for Microwave Applications

Microwave applications cover several important public areas. For instance, the terrestrial broadband represents nowadays the largest commercial market for millimetre-wave MMICs: the research in this area is pushed up by vendors, whose keep on offering higher data rates and longer transmission ranges, since systems operating beyond 70 GHz are now being developed to deliver data communications at speeds up to 10 Gbps. Other applications of interest of microwave circuits are the satellite communications, with the present commercial market of two-ways transmissions at 12-18 GHz and the next-generation systems operating at 26-40 GHz. After, there are the automotive applications, whose 76-77-GHz radars are widely anticipated to be the next big microwave application. In addition, the saturated use of the spectrum at lower frequencies makes mm-waves necessary, so the increase of the current applications together with others more mass-market-oriented is unstoppable, in spite of the higher cost of the technology for these frequencies. In this framework, key technological aspects for power amplifiers become the power efficiency and the delivered output power at high frequencies, the breakdown voltage (since high level modulation formats are transmitted at high power), the thermal dissipation and the cost of the implementation.

In all the application fields, the use of the Monolithic Microwave Integrated Circuit (MMIC) is more and more preferred to the Hybrid MIC: monolithic circuits, in fact, allow high integration levels because all the components, both active and passive, are realized on the same semiconductor substrate. The main drawbacks of MMICs are the realization costs and the impossibility of posterior tuning: accurate device models are needed.

Many kinds of technologies and devices are at the design disposal for the different microwave applications. Silicon-based transistors still keep a primary role: the increasing scaling of CMOS and the birth of new devices, like BiCMOS (HBT+MOS) or SiGe HBT have considerably improved the RF performances of the Silicon family. However, GaAs technology have been for many years the main resource in high-frequency applications. The physical characteristics of GaAs and Si are compared in Table I.

TABLE I

MAIN PHYSICAL PROPERTIES OF SI- AND GAAS-MATERIALS

	Si	**GaAs**
Electron Mobility (cm^2/Vs)	1350	8800
Hole Mobility (cm^2/Vs)	480	400
Electron Diffusion Constant (cm^2/Vs)	39	220
Hole Diffusion Constant (cm^2/Vs)	13	10
Minorities life time (s)	$2.5e10^{-3}$	10^{-8}
Energy gap (eV)	1.12 (indirect)	1.42 (direct)
Breakdown field (V/cm)	$3e10^{-5}$	$4e10^{-5}$
Intrinsic resistivity (Ωcm)	$2.3e10^{5}$	$3.8e10^{8}$
Thermal conductivity (W/cm°C)	1.5	0.46
Relative dielectric constant	11.8	13
Fusion point (°C)	1415	1238

The main advantages of Gallium Arsenide on Silicon are the higher electron mobility, the semi-insulating substrate, which allows to obtain low-loss high-Q passives, the direct and higher energy-gap, which allows light radiation emission and makes these devices radiation-proof, thus particularly suitable for space applications. The main drawbacks are the complexity and expensiveness of the production process, due, for instance, to the material cost, to its minor mechanical resistance, to the missing of a good native oxide and the difficult control of the superficial states. In addition, the low thermal conductivity makes the power dissipation more difficult, even though the maximum operative temperature of GaAs devices is higher with respect to silicon ones.

GaAs MESFETs (*MEtal Semiconductor Field Effect Transistors*), after being for years the workhorse of microwave applications, are gradually replaced by HEMTs (*High Electron Mobility Transistors*) and PHEMTs (*Pseudomorphic HEMTs*), more performing in terms of noise figures and maximum operative frequency. In addition, other III-V compounds are gradually imposing themselves, like Gallium Nitride or Indium Phosphate. In particular, AlGaN/GaN HEMTs are strong candidates for high-power and high efficiency amplifiers, thanks to their high breakdown voltage and high operative temperatures, but also thanks to the ability of growing GaN epitaxial layers on different substrates, like Silicon and Silicon Carbide (SiC). GaN transistors are suitable for applications in the L, C and X bands. For higher frequencies the devices based on Indium

Phosphate provides the best performances (even over 100 GHz). The InP transistors also show good linearity properties and low noise figure, but their power handling capability is quite limited by the low breakdown voltage.

In the following, the structure and the *modus operandi* of the HEMT are briefly described (Section 1.1). The main issues related to the modelling of these devices are also outlined in Section 1.2.

1.1 The High Electron Mobility Transistor (HEMT) [1]

The High Electron Mobility Transistor is a field effect device based on a heterostructure, that is a junction between two semiconductor materials with different band-gap energies. In the GaAs HEMT the heterostructure is obtained by contacting *n*-doped AlGaAs and undoped GaAs: the band diagram of this heterostructure is illustrated in Fig. 1.1.

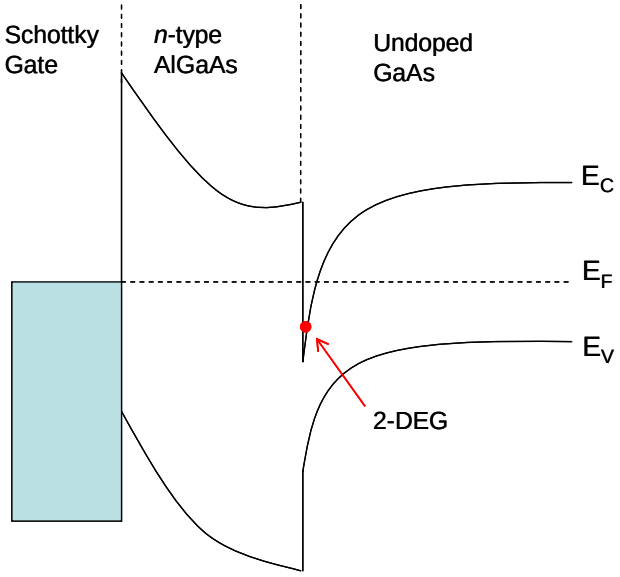

Fig. 1.1: Band diagram of the AlGaAs/GaAs heterostructure in the HEMT, under conditions of zero gate bias.

The wide-band-gap material is doped *n*-type, but is depleted of free carriers by the reverse or zero-biased Schottky contact, while the narrow-band-gap material is undoped or slightly doped *p*-type. At the boundary between the two materials the band-gap discontinuities cause the conduction band of the GaAs to dip below the Fermi level, creating a potential well with a very high carrier concentration. This region of high carrier density is very thin, so that it is named two-dimensional electron gas (2-DEG). The electrons of the 2-DEG travel into an undoped material, thus without

encountering ionized donor atoms: this make them to have the highest mobility, favouring fast response times and high-frequency operation.

The whole conventional HEMT structure is reported in Fig. 1.2. Three metal electrode contacts are made on the surface of the semiconductor structure: as in the MESFET, the source and drain contacts are ohmic, while the gate is a Schottky junction. The presence of the heterostructure makes the structure of a HEMT much more complex with respect to a MESFET, leading to higher fabrication difficulties and costs and lower yields. Nevertheless, the 2-DEG-based current transport provides important improvements in terms of noise figure and high-frequency performances. In Fig. 1.2, a spacer undoped AlGaAs layer is also inserted in the heterojunction, in order to limit the scattering effects on the 2-DEG electrons at the interface, due to ionized donor of the doped AlGaAs.

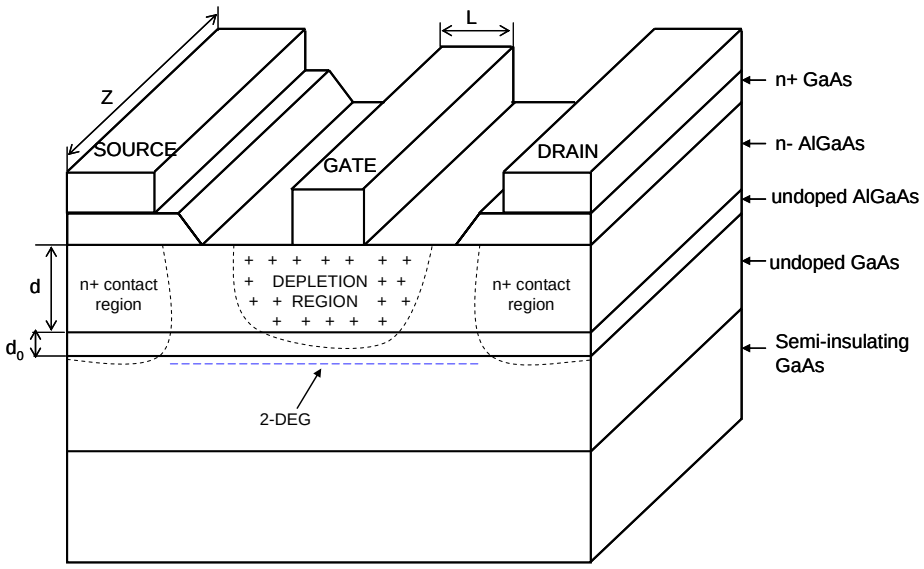

Fig. 1.2: A conventional HEMT structure.

Important geometric parameters of the device are the surface geometry dimensions, especially the ones labelled L and Z in Fig. 1.2. The gate length L determines, in fact, the maximum frequency limits for the HEMT. The device current, instead, is directly proportional to the gate width Z, thus relatively small-gate-width devices are used for low-noise and low-current applications, while large-gate-width devices are typically employed in power applications. Actual device layout are, anyway, more complex: a T-shaped gate allows to decrease the gate length without excessively increasing the gate parasitic resistance, the use of recessed gate structure decreases the source and drain parasitic resistances, the gate width is extended by repeating the same elementary cell in a multiple-fingers layout (as, for instance, in Fig. 1.3).

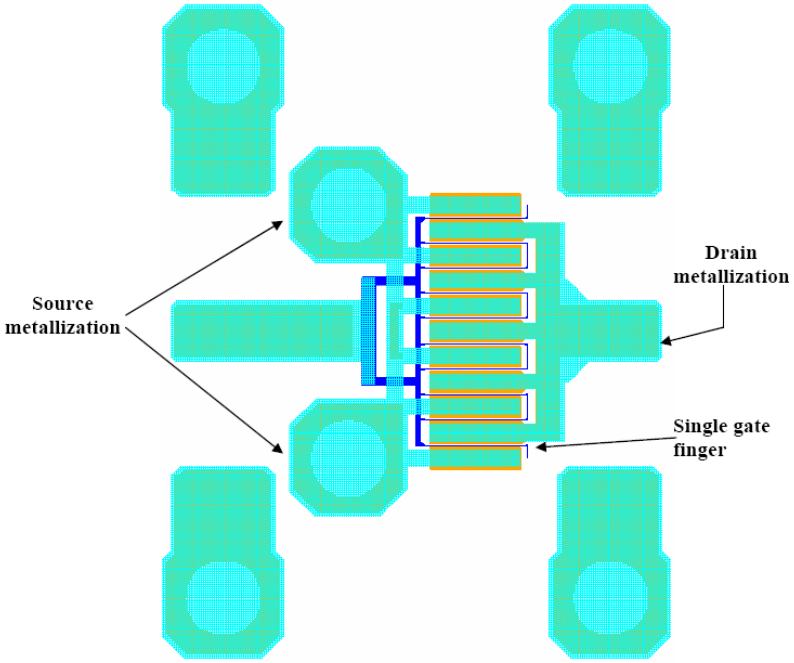

Fig. 1.3: Metallization layout for an actual FET device. The device has a gate width of 1mm, made up of ten 100-μm fingers.

The device behaviour is also determined by the thickness of both the *n*-type and the undoped AlGaAs spacer layer, labelled in Fig. 1.2 as d and d_0, respectively. These dimensions are on the order of 0.03 to 0.2 μm for the *n*-type layer and around 50 Å for the spacer layer. In particular, the thickness of the *n*-type AlGaAs is designed in such a way that this layer is completely depleted from free electrons under normal operating conditions.

Both depletion mode and enhanced mode devices can be fabricated: we focus on depletion devices for outlining the working operation. In conditions of zero gate bias the band diagram is like in Fig 1.1, and the 2-DEG is formed. The contact with the 2-DEG is made by means of heavily doped, low-resistance source and drain wells. For low value of drain-source voltage a current flows from drain to source through the electron gas. This current is initially proportional to the drain-source voltage, but as the electron velocity reaches the saturation for increasing voltage values, also the current levels saturate. The gate bias, instead, controls the 2-DEG density: as the negative gate voltage increases, the depth of the potential well decreases, resulting in a diminishing of the 2-DEG electron density and, thus, of the current levels, until reaching the pinch-off voltage. The drain current characteristic measured for a 0.25*600-μm^2 GaAs PHEMT is plotted in fig. 1.4.

The PHEMT (Pseudomorphic HEMT) has very similar characteristics with respect to the HEMT, except for the replacement of the heterojunction with a pseudomorphic junction, made up of *n*-doped AlGaAs, undoped InGaAs and undoped GaAs.

Important information on the device can be also obtained by the derivative of the current-voltage characteristic, that is from the output conductance and the transconductance, defined as:

$$g_d \doteq \frac{1}{r_{ds}} \doteq \left.\frac{\partial I_{DS}}{\partial V_{DS}}\right|_{V_{GS}=\text{const}} \quad \text{and} \quad g_m \doteq \left.\frac{\partial I_{DS}}{\partial V_{GS}}\right|_{V_{DS}=\text{const}}, \tag{1.1}$$

respectively. The output conductance plays an important role in determining the maximum voltage gain obtainable from the device and in determining the optimum output matching conditions: in general, a low value of the output conductance is desirable for a good device. On the contrary, the highest is the transconductance, the best are the gains and the high-frequency device performances.

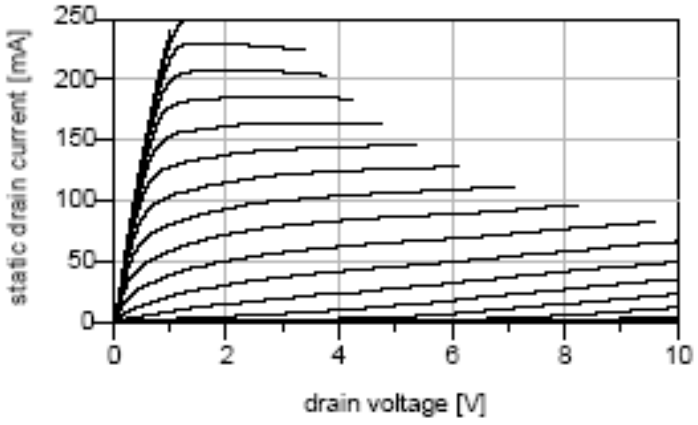

Fig. 1.4: Static drain currents of a Triquint 0.25*600-μm^2 PHEMT in GaAs technology. Gate-source Voltage V_{GS} ranging from -1.5 to 0 V, drain-source voltage V_{DS} between 0 and 10 V.

Both conductances are, of course, affected by device dimensions and channel material properties.

Finally, it must be observed that the charge distribution in the channel, that is the shape of the depletion region, is determined by both the gate-drain and gate-source potential. This leads to define two important capacitances:

$$C_{GS} \doteq \left.\frac{\partial Q_g}{\partial V_{GS}}\right|_{V_{GD}=\text{const}} \quad \text{and} \quad C_{GD} \doteq \left.\frac{\partial Q_g}{\partial V_{GD}}\right|_{V_{GS}=\text{const}}. \tag{1.2}$$

where Q_g is the charge in the depletion region, shared between gate-source and gate-drain capacitance. The gate-source capacitance has a significant impact on the input impedance and on the high frequency performances: in fact, at a high enough frequency this capacitance becomes nearly a short circuit and in these conditions the device does not produce useful gain. Thus, a low

value of the gate-source capacitance increases the maximum operative frequency. The gate-drain capacitance is mainly responsible of the reverse isolation of the device, thus a low value is desirable also for it. The two capacitance values are strongly affected by the gate dimensions: they are directly proportional to the gate width, while they do not scale strictly linearly with the gate-length.

1.2 Nonlinear Device Modelling Issues

MMIC design requires electron device models capable of predicting the device response in the different operating conditions. An accurate prediction involves the modelling of the static device behaviour and of both the fast and the slow device dynamics, that is the quasi-static and the nonquasi-static behaviour at high frequencies (short-memory effects), and the dynamic drain current I/V characteristics affected by dispersive phenomena at low-frequencies (long-memory effects).

The first important modelling issue regards the identification of the extrinsic parasitic network. This network is bias-independent, passive and lossy: it models the parasitic resistances of the electron path between the channel and the drain and source contacts (R_D and R_S), the gate resistance (R_G) and the inductive and coupling effects due to the electrodes metallization (L_S, L_G, L_D, C_{p1}, C_{p2} and C_{p3}). Different topologies can be chosen, according to the specific technology and applications, for instance classical lumped-components (e.g. Fig. 1.5) based on cold-FET identification [2], or distributed approaches based on electromagnetic simulations, the latter particularly suitable when very high frequencies are involved [3].

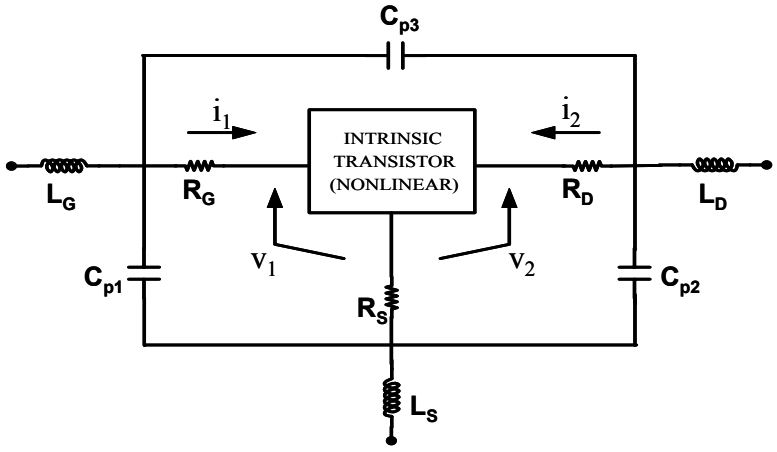

Fig. 1.5: Example of extrinsic parasitic network.

Once a suitable parasitic network is identified, the modelling of the *intrinsic* device, that is the electron device de-embedded from parasitics, can be faced up. Besides the static I/V characteristics

and the displacement currents due to the gate-source and gate-drain capacitances in quasi-static conditions, two main phenomena must be accounted for: the low-frequency dispersive effects and the high-frequency nonquasi-static behaviour.

1.2.1 Dispersive Effects

The dispersive phenomena are very-long-memory effects due to charge trapping, in surface state densities and bulk spurious energy levels, and thermal effects, such as self-heating or changes in the case-temperature.

In semiconductor materials the charge carrier can encounter deep levels, that is energy states located near the middle of the band gap, between the highest energy state of the valence band and the lowest energy state of the conduction band. In this case, the carriers tend to be trapped in the deep levels, remaining unavailable for current conduction for a relatively long time: for this reason, deep levels are also referred to as traps. Traps can result from specific impurities (such as boron or chrome in GaAs), from crystal defects and damage and from fabrication procedures. They can be located in the physical structure at the interfaces, at the surface of the material (surface state densities), or in the bulk.

The device thermal state significantly influenced the current value: when high values of V_{GS} and V_{DS} are involved, the high dissipated power causes an increase in the device channel temperature (self-heating). As a consequence, the electron mobility decreases and so also the current density: this effect is quite evident from the static characteristics of Fig. 1.4.

The presence of dispersive phenomena results in a discrepancy between the static and the low-frequency device behaviour. In particular, the pulsed I/V characteristics remarkably differ from the ones statically measured (Fig. 1.6): in dynamic conditions, the long-memory phenomena of charge-trapping and self-heating have no time enough for rearranging their status, so they result like frozen, leading to very different current levels. Another evident effect is the frequency degradation of transconductance and output resistance: as shown in Fig. 1.7, after a transition frequency region the conductances settle down to a constant AC value (till nonquasi-static effects arise), quite different from the DC one. From Fig. 1.7 we can say that the dispersion has a cut-off frequency between 100 kHz and 1 MHz (for GaAs FETs).

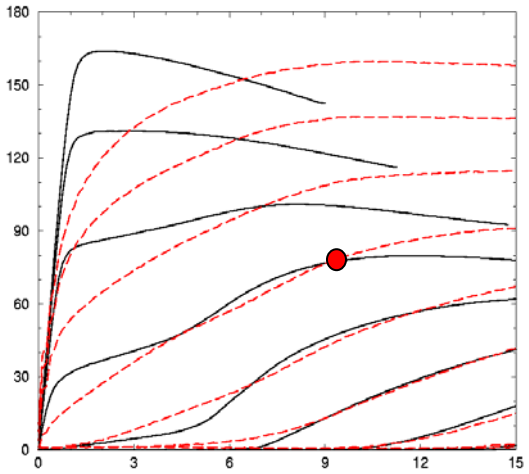

Fig. 1.6: Pulsed drain current measurements (red dashed line) compared with dc characteristic (black, continuous line). The quiescent condition of the pulsed measurements is also marked by the red point: this is the only point where the two I/V characteristics cross.

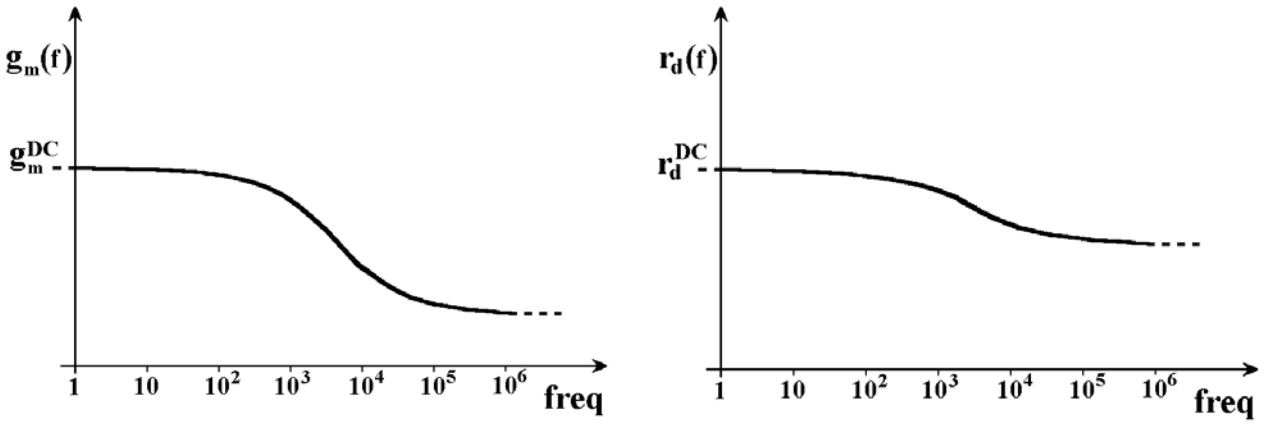

Fig. 1.7: The transconductance and the output resistance versus frequency.

In spite of the low cut-off frequency, a correct accounting for the dispersive effects is fundamental to obtain accurate prediction of the device behaviour in microwave large-signal operation. This can be empirically verified, for instance, by using the same nonlinear high-frequency electron device model [4] in two versions, with and without accounting low-frequency dispersion [5], for predicting the intermodulation distortion at 37 GHz of a Triquint 0.25*600-μm^2 GaAs PHEMT: the two predictions are compared with the measurements in Fig. 1.8, showing the importance of modelling the low-frequency dispersive effects.

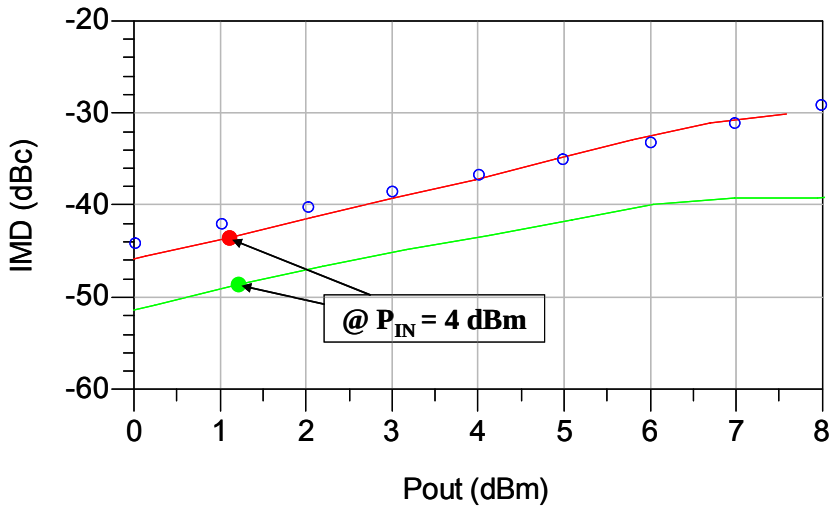

Fig. 1.8: Intermodulation distortion at 37 GHz and 10 MHz of two-tone displacement: V_{GS} = -0.55 V and V_{DS} = 6.5 V (class AB power amplifier), Z_S = 49.55-j*9.65, Z_L = 30.7-j*0.88. Measurements (circles), model accounting dispersion (red line), model without accounting dispersion (green line)

1.2.2 Nonquasi-Static Effects

The nonquasi-static effects arise at very high frequencies and are due to the delay of the charge carriers in rearranging the channel-status. The device responds with finite times to the fast voltage variations, so that the current at the time instant *t* depends of both actual and past values of applied voltages. This causes a degradation of the device performances (in terms of delivered power, for instance) and a strong deviation in the intrinsic admittance parameters from the quasi-static behaviour. In Fig.1.9 the actual nonquasi-static admittance parameters is compared with the virtual quasi-static behaviour.

The accurate prediction of nonquasi-static effects is fundamental in microwave design. We can well appreciate the importance of this modelling by comparing the prediction obtained with the nonquasi-static model [4] and the one obtained with a quasi-static model, for the same intermodulation distortion of Fig. 1.8. Both high frequency models take into account low-frequency dispersion as in [5]. It is worth noting that the quasi-static model predicts a higher output power, since it does not account for the high-frequency degradation effects due to the nonquasi-stationarity (Fig. 1.10).

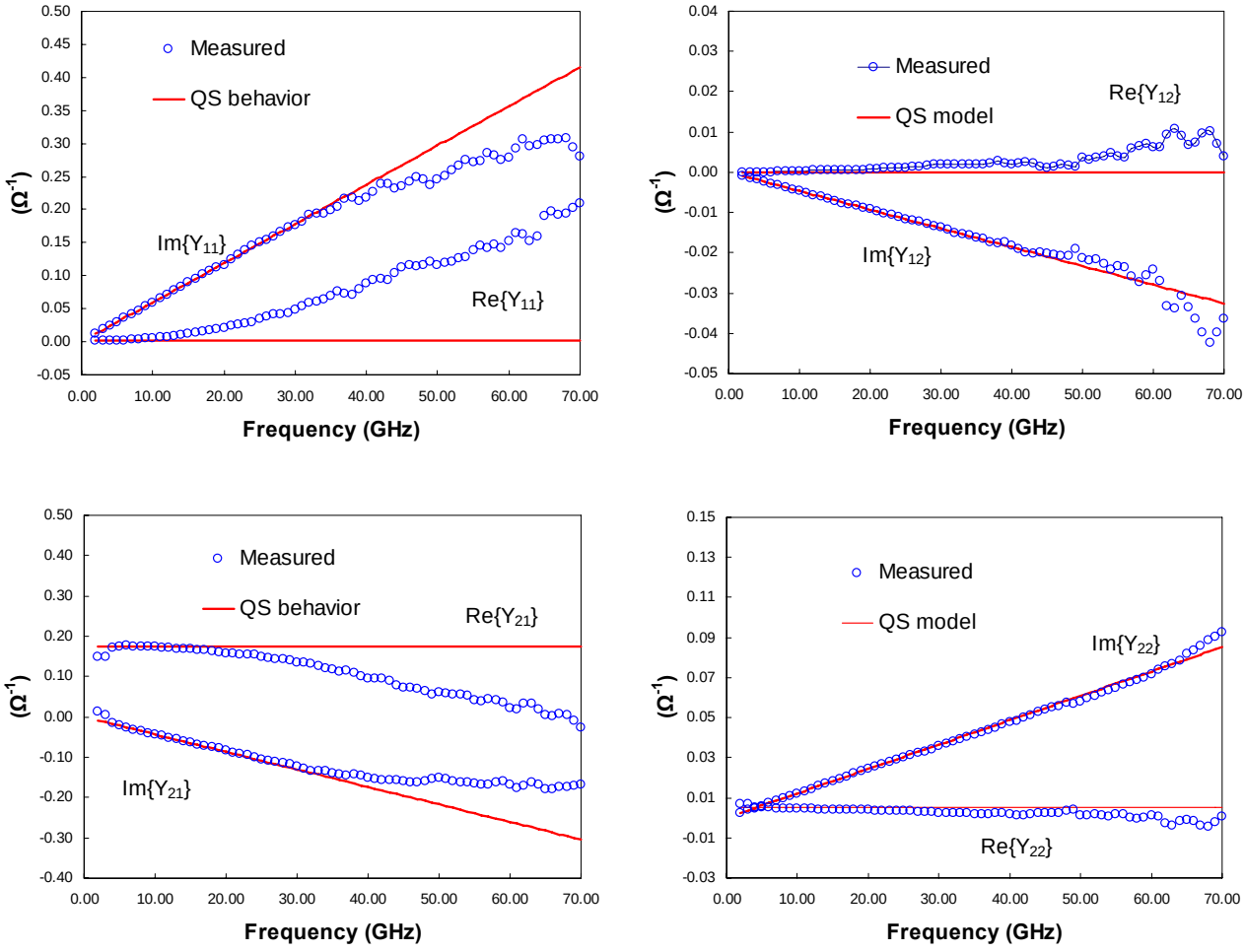

Fig. 1.9: Intrinsic admittance parameters up to high frequencies (70 GHz) at V_{GS} = -0.55 V and V_{DS} = 6.5 V. Measurements (circles) versus quasi-static behaviour (continuous line)

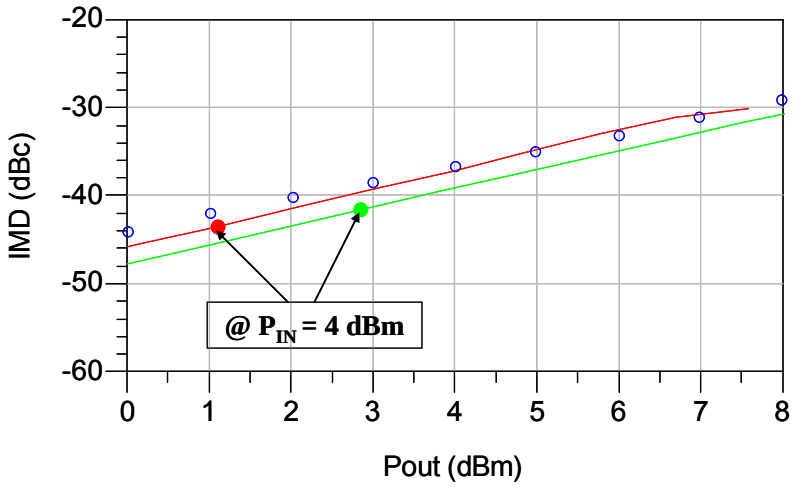

Fig. 1.10: Intermodulation distortion at 37 GHz and 10 MHz of two-tone displacement: V_{GS} = -0.55 V and V_{DS} = 6.5 V (class AB power amplifier), Z_S = 49.55-j*9.65, Z_L = 30.7-j*0.88. Measurements (circles), NQS model prediction (red line), QS model prediction (green line)

1.3 Conclusion

In this first chapter, a panoramic view of microwave applications and devices has been provided. Particular attention has been paid to the HEMT family, since these devices will be widely used in the course of this thesis: their structure and the main working principles have been described.

In addition, the main aspects to be accounted for in a device model have been discussed, in order to introduce the reader to the central topic of the following chapters: the electron device modelling.

The state of the art of nonlinear modelling will be outlined in chapter 2.

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Chapter 2

State of the Art of Nonlinear Modelling

Non linear transistor models can be divided in two big families: physics-based and empirical. Physics-based models are derived by fundamental equations describing the physics of charge transport in the electron device. According to the type of calculation required for obtaining predictions, they can be numerical or analytical, but in both cases they provide a direct link between electrical response and technological process parameters, such as device materials, geometry, doping profile etc. Therefore, they are more suitable for device analysis and design.

Empirical models, instead, are based on measurements: they use lumped circuital components or integral/differential predictive equations to reproduce the observed device characteristics. Both equivalent-circuit and black-box models can provide good small- and large-signal predictions, provided that an accurate device characterization is carried out, adequate functions are chosen for approximating the nonlinear measured characteristics and a reliable algorithm is used for model parameters extraction. In addition, they are numerically efficient, thus empirical nonlinear models are the obvious choice for MMIC design, mainly based on the iterative procedures of commercial CAD tool analysis.

This chapter focuses on empirical electron device modelling, trying to provide a comprehensive view on the various modelling approaches, their differences and their similarities.

2.1 Empirical Models

The device behaviour in large-signal RF operation is nonlinear with memory (dynamic), thus high complexity is involved in the device modelling. In compact empirical models, this problem is often faced up by separately dealing with memory and nonlinearities: device memory is described by linear operators, like time derivatives, integrals, delays; nonlinearity instead is described by nonlinear algebraic (i.e. memory-less) functions, which can be analytical, LUT-based, or use Artificial Neural Networks (ANN).

As already outlined in Section 1.2, the first step in this direction is the identification and de-embedding of the extrinsic parasitic network: this separates the linear memory effects of the

parasitic elements from the nonlinear ones of the intrinsic device. Different topologies are available according to specific technology/packaging choices (lumped [2] or distributed [3]) and efficient algorithms allow the parasitic element identification (e.g. Cold-FET based procedures [2]). Once the parasitic network is identified, it is de-embedded from the device measurements, in order to obtain the intrinsic device behaviour. The resulting intrinsic transistor is nonlinear with a "short" memory with respect to the typical operating frequencies, provided that long-memory low-frequency dispersion is separately dealt with.

Many dynamic intrinsic transistor models are based on charge- or voltage-controlled equations, obtained by applying system-theory-based input-output relationships to the electron device. For instance, by assuming internal charge distribution as state variable, these relationships are written as the well known charge-controlled quasi-static equations:

$$\mathbf{i}(t) = \mathbf{\Phi}\left\{\mathbf{q}(t), \mathbf{v}(t)\right\} + \frac{d\mathbf{q}(t)}{dt} \tag{2.1}$$

$$\mathbf{q}(t) = \mathbf{\Psi}\left\{\mathbf{v}(t)\right\}, \tag{2.2}$$

where a vector notation is adopted: **i** and **v** are the vectors of the gate-source and drain-source currents and voltages, respectively, **Φ** and **Ψ** are algebraic functions. The internal charges **q** completely define the internal device state.

From the charge-controlled model, by simply substituting the second equation in the first, the device voltage-controlled description can be obtained, that is:

$$\mathbf{i}(t) = \mathbf{F}\left[\mathbf{v}(t)\right] + \mathbf{C}\left[\mathbf{v}(t)\right] \cdot \frac{d\mathbf{v}(t)}{dt}, \tag{2.3}$$

where it holds:

$$\begin{aligned} &\mathbf{F}\left[\mathbf{v}(t)\right] = \mathbf{\Phi}\left\{\mathbf{\Psi}\left[\mathbf{v}(t)\right], \mathbf{v}(t)\right\} \\ &\mathbf{C} = \frac{d\mathbf{\Psi}\left[\mathbf{v}(t)\right]}{d\mathbf{v}(t)}. \end{aligned} \tag{2.4}$$

It is worth noting that, in this description, the current versus voltage relationship can be seen as a particular case of a nonlinear with memory relationship, when memory effects have an infinitely small duration ($\frac{d\mathbf{v}}{dt} = \lim_{\tau \to 0} \frac{\mathbf{v}(t) - \mathbf{v}(t-\tau)}{\tau}$, τ being the device memory time). Equation (2.3) also says

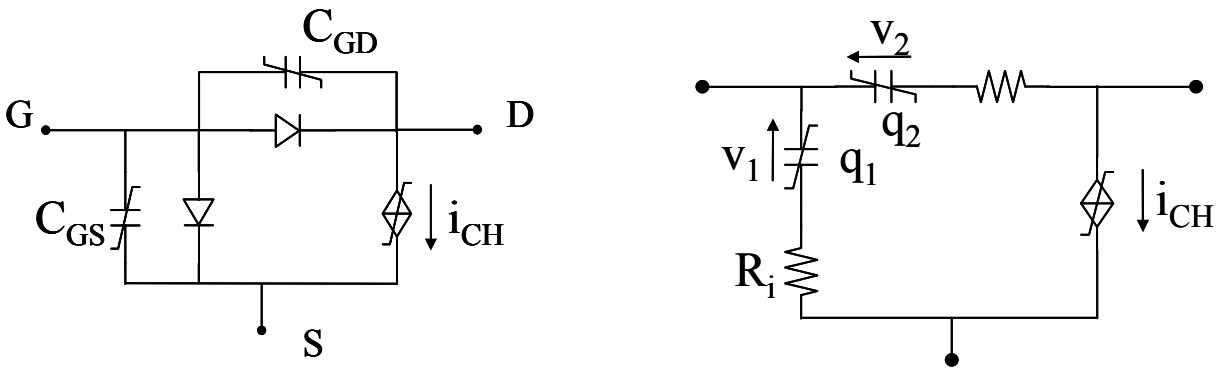
that the quasi-static intrinsic device can be represented as a parallel of nonlinear resistive and purely capacitive elements.

The charge-controlled (2.1) or the voltage-controlled description (2.3) are at the basis of both equivalent-circuit or black-box models.

2.1.1 Equivalent Circuit Models

The first target of a FET model is to reproduce the quasi-static electrical behaviour outlined in Section 1.1, that is the drain current versus voltages characteristic and its derivatives, plus the reactive effects due to the gate capacitances. One possible choice can be an equivalent-circuit approach: a classic equivalent-circuit description for a FET in common-source configuration is shown in Fig 2.1-a. It is quite clear the link between the circuit lumped components and the physical phenomena they intend to model: the charge depletion region beneath the gate is represented by the gate-source and gate-drain Schottky-barrier diodes with the voltage-dependent capacitances, while the voltage-controlled current source models the nonlinear drain I/V characteristic by means of a suitable analytical expression.

These simple models are adequate for applications in the quasi-static frequency range, while several modifications are needed for achieving a better accuracy at higher frequencies. Nonquasi-static memory effects are taken into account by adding series resistive elements (Fig. 2.1-b), which cause the capacitor charges (q_1 and q_2), the voltages (v_1 and v_2) and the controlled current source (i_{CH}) to be dependent also on past values of applied gate-source and drain-source voltages. Several models also explicitly consider delays in the expression of the current source (e.g., $g_m \cdot e^{-j\tau\omega}$).



(a) (b)

Fig. 2.1: Classic equivalent-circuits for a FET in common-source configuration. (a): Quasi-static topology; (b): Nonquasi-static model.

Of course, many different model topologies exist in the literature [4]-[7], aimed to obtained more and more accurate prediction for the specific application of interest. For instance, the MESFET equivalent circuit model by Curtice [4] is shown in fig 2.2.

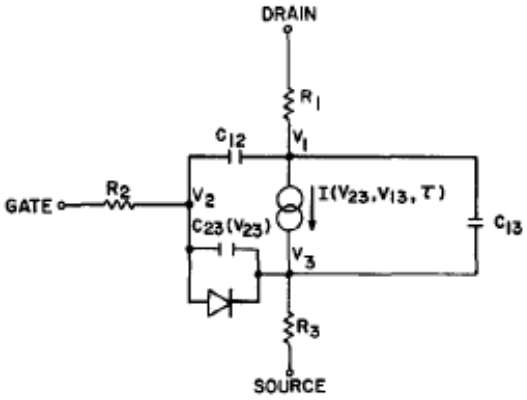


Fig. 2.2: Curtice GaAs MESFET model (figure from [4])

The elements R_1, R_2 and R_3 account for the parasitic resistances, thus V_1, V_2 and V_3 are the intrinsic drain, gate and source potentials, respectively. The gate-drain and gate-source capacitances (namely, C_{12} and C_{23} in the figure) represent the charge depletion region. Since in normal operating conditions (i.e. saturated drain current region) it holds $C_{12} \ll C_{23}$, the gate-source capacitances dominates the input impedance, thus its modelling assumes an important role. Curtice used an analytical expression drawn from the ideal semiconductor junctions:

$$C_{23}(V_{23}) = \frac{C_{23}(0)}{\sqrt{1 - V_{23}/V_{BI}}}, \tag{2.5}$$

where V_{23} is the intrinsic gate-source voltage and V_{BI} is the built-in voltage. The dependence on the drain-source voltage is instead neglected. The gate-drain and the drain-source capacitances are considered linear.

As far as the nonlinear drain current source is concerned, Curtice adopted the following analytical function:

$$I(V_{23}, V_{13}) = \beta \cdot \left(V_{23} + V_T\right)^2 \cdot \left(1 + \lambda V_{13}\right) \cdot \tanh\left(\alpha V_{13}\right), \tag{2.6}$$

where V_{23} and V_{13} are the intrinsic gate-source and drain-source, respectively, and β, λ and α are constant model parameters, identified on the basis of best-fit procedures on the experimental data. In particular, $\beta = I_p / V_p^2$, I_p and V_p being the saturated current and the pinch-off voltage, λ is

channel length modulation parameter (determined from the slope of the I_{ds}-V_{ds} characteristic) and α is the saturation voltage parameter.

It is worth explicitly noting that expression (2.6) is the product of two factors, in which the dependences of the drain current on the gate-source and drain-source voltages are separated:

$$I(V_{GS},V_{DS}) = I_A(V_{GS}) \cdot I_B(V_{DS}) . \tag{2.7}$$

The nonquasi-static effects are finally taken into account by adding a correction term to the current (2.6), i.e.:

$$I(V_{23},V_{13}) - \tau \cdot \frac{dI(V_{23},V_{13})}{dt}, \tag{2.8}$$

where τ is the transit time under the gate and $\frac{dI(V_{23},V_{13})}{dt} = \left|\frac{\partial I(V_{23},V_{13})}{\partial V_{23}}\right|_{V_{13}} \cdot \frac{dV_{23}}{dt}$. The correction term derives by the first order expansion of $I(t-\tau)$ in time.

An other example is provided by the Materka model, whose topology is plotted in Fig. 2.3.

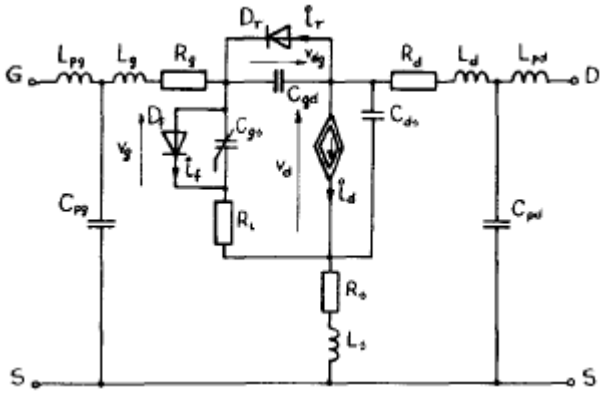


Fig. 2.3: Materka FET model [5]

In this model a more complex network is adopted for parasitic modelling, accounting also for inductive and coupling effects of the metallization. As far as the intrinsic device model is concerned, the same expression (5) is adopted for the gate-source capacitance Cgs and, analogously to Curtice model, Cgd and Cds are linear. The analytical function for the voltage-controlled drain-current source is instead:

$$i_d(v_g, v_d) = I_{dss} \cdot \left(1 - \frac{v_g}{V_p}\right)^2 \cdot \tanh\left(\frac{\alpha v_d}{v_g - V_p}\right). \tag{2.9}$$

with $V_p = V_{p0} + \gamma v_d$ and where I_{dss}, V_{p0}, α and γ are the model parameters. In order to take into account the memory effects, the instantaneous current (2.9) is calculated with $v_g = v_g(t - \tau)$ and $v_d = v_d(t)$, where τ is a model parameters. A series resistance R_i is also added. In addition, the Materka model also has two diodes, D_f modelling the current in the gate-channel junction and D_r to model the gate-drain breakdown.

Angelov *et al*. proposed in [6] a FET model for the prediction of the I/V characteristic and its derivatives, derivable in a simple manner from inspection of the experimental $I_{ds}(V_{gs},V_{ds})$ and $g_m(V_{gs})$ (Fig 2.4). The authors adopt (2.7) for describing the voltage-dependent drain current, with the same expression for $I_B(V_{DS})$. On the contrary, a more complex expression is used for the gate-source voltage dependence:

$$I_{ds}(V_{gs}, V_{ds}) = I_{pk} \cdot (1 + \tanh(\psi)) \cdot (1 + \lambda V_{ds}) \cdot \tanh(\alpha V_{ds}) \tag{2.10}$$

The hyperbolic tangent is chosen because of the bell-shaped structure of its first order derivative, the same shape of the device transconductance. In fact, not only the current-voltage characteristics, but also their derivatives have to be well modelled, especially when the model is aimed to intermodulation distortion analysis. In (2.10) I_{pk} is the drain current at which we have the maximum transconductance. The parameters λ and α have the same meaning as in Curtice model [4], while for ψ it holds:

$$\psi = P_1(V_{gs} - V_{pk}) + P_2(V_{gs} - V_{pk})^2 + P_3(V_{gs} - V_{pk})^3 + \ldots, \tag{2.11}$$

where V_{pk} is the gate voltage for having the maximum transconductance.

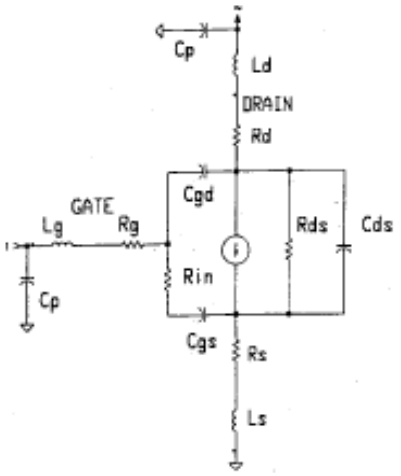


Fig. 2.3: FET model by Angelov et al. [6]

As far as the gate capacitances are concerned, both the gate-source and the gate-drain capacitances were considered nonlinear. The same type of modelling function was thus chosen for their modelling:

$$\begin{aligned} C_{gs}(V_{gs},V_{ds}) &= C_{gs0}\cdot\left(1+\tanh\left(\psi_1\right)\right)\cdot\left(1+\tanh\left(\psi_1\right)\right) \\ C_{gd}(V_{gs},V_{ds}) &= C_{gd0}\cdot\left(1+\tanh\left(\psi_3\right)\right)\cdot\left(1-\tanh\left(\psi_4\right)\right) \end{aligned} \quad (2.12)$$

where ψ_i (i=1,…,4) are again power series function of gate-source (ψ_1 and ψ_3) and drain-source voltages (ψ_2 and ψ_4):

$$\begin{aligned} \psi_1 &= P_{0gsg}+P_{1gsg}V_{gs}+P_{2gsg}V_{gs}^2+P_{3gsg}V_{gs}^3+\ldots \\ \psi_2 &= P_{0gsd}+P_{1gsd}V_{ds}+P_{2gsd}V_{ds}^2+P_{3gsd}V_{gd}^3+\ldots \\ \psi_3 &= P_{0gdg}+P_{1gdg}V_{gs}+P_{2gdg}V_{gs}^2+P_{3gdg}V_{gs}^3+\ldots \\ \psi_4 &= P_{0gdd}+\left(P_{1gdd}+P_{1cc}V_{gs}\right)V_{ds}+P_{2gdd}V_{ds}^2+P_{3gdd}V_{ds}^3+\ldots \end{aligned} \quad (2.13)$$

Equations (2.12)-(2.13) also account for the cross-coupling of V_{gs} and V_{ds} on C_{gd} by means of the $P_{1cc}V_{gs}$ term. When an accuracy of 5-10% can be sufficient and the cross-coupling effects can be neglected, the simplified forms can be adopted:

$$\begin{aligned} C_{gs}(V_{gs},V_{ds}) &= C_{gs0}\cdot\left(1+\tanh\left(P_{1gsg}V_{gs}\right)\right)\cdot\left(1+\tanh\left(P_{1gsd}V_{ds}\right)\right) \\ C_{gd}(V_{gs},V_{ds}) &= C_{gd0}\cdot\left(1+\tanh\left(P_{1gdg}V_{gs}\right)\right)\cdot\left(1-\tanh\left(P_{1gdd}V_{ds}\right)\right) \end{aligned} \quad (2.14)$$

All the so far described models do not consider low-frequency dispersive effects. However, the dispersion in the I/V characteristics can be separately modelled, again adopting an equivalent-

circuit approach [7]-[12]: the circuit accounting for the dispersion can be after embedded in the nonquasi-static model. For instance, an extension of the Chalmers model by Angelov has been presented, in which dispersion due to trapping and thermal effects are dealt with by means of an analytical and an equivalent circuit approach. The analytical approach consists in modifying the current expression (2.10) by introducing a frequency dependence in the P_1 parameter of (2.11):

$$P_1 = P_{1d} P_{1,DC}$$
$$P_{1d} = \frac{P_{1srf}}{P_{1sDC}} + \frac{P_{1sDC} - P_{1srf}}{P_{1sDC}} \sum_{n=1}^{N} \frac{k_n}{1 + \left(\frac{f}{f_{tr,n}} \right)^2} . \tag{2.15}$$

where $P_{1,DC}$ and P_{1srf} are the P_1 values extracted from DC and RF measurements, respectively, while $f_{tr,n}$ represent the corner frequencies for the dispersion effects.

The equivalent circuit approach models the output conductance frequency dependence by means of an RC series circuit, suggesting for R a gate-bias-dependent equation. The decrease of transconductance is also described by adding a parallel branch, series RC, between the intrinsic gate and source terminals. Thermal effects are accounted by authors considering a linear dependence of the generic circuit parameters P on the temperature T, $P(T) = P_0 + A_1 (T - T_0)$, being P_0 the considered parameter at the ambient temperature T_0.

The equivalent-circuit models are widely used in the microwave component design: they are rapidly convergent in CAD analysis, provide a globally good fit and are often readily available as foundry models. Nevertheless, an high accuracy needs high complexity and a significant number of model parameters, whose identification requires nonlinear optimization procedures with related problems of convergence and initial-guess best-choice. In addition, lumped components are not always adequate for describing the distributed effects arising at very high frequencies. Due to these limits, other kinds of models are sometimes preferred.

2.1.2 Black-box Models

The black-box modelling approach considers the electron device in an almost purely behavioural perspective. This kind of models are based on mathematical formulations for the device description, derived from totally general physical considerations (like charge- or voltage-controlled equations) or from purely mathematical tools (state-space nonlinear equations or Volterra Series expansions). The black-box model is so called because there is no view on the physical device structure, thus it is technology-independent. The black-box modelling approach can be applied to the whole device or

even to complex circuits (mixers, amplifiers, etc.): this is the case of totally behavioural models, which, in correspondence to input stimulus (e. g., external device port voltages) provide in output the device/circuit response (e. g., the extrinsic device currents). However, it is also possible to choose a black-box for modelling the intrinsic device, or just a particular phenomena: a parasitic network with lumped-components can be, for instance, chosen and different models can be adopted for dealing with the long and fast device dynamics separately. In general, black-box models are directly implemented in the CAD tool by means of analytical or, more often, table-based functions; recently, also Artificial Neural Networks (ANN) are exploited.

We start to consider black-box models based on the charge-controlled description (2.1)-(2.2) for the modelling of the intrinsic device: if a quasi-static description is adequate, the $\mathbf{\Phi}\{\mathbf{q}(t),\mathbf{v}(t)\}$ functions are identified with the measured static currents, while the gate charges are usually extracted from measured differential parameters by means of capacitance integration. Both the currents and the charges are directly stored into Look-Up Tables.

When high frequencies are involved, a nonquasi-static model is required, accounting for the charge-carriers delay in rearranging the channel status. This delay leads to a dependence of charges on actual and past values of applied voltages:

$$\begin{aligned}\mathbf{i}(t) &= \mathbf{\Phi}\left\{\mathbf{q}^{NQS}(t),\mathbf{v}(t)\right\} + \frac{d\mathbf{q}^{NQS}(t)}{dt} \\ \mathbf{q}^{NQS}(t) &= \mathbf{\Psi}^{NQS}\left|\mathbf{v}(t-\tau)\right|_{\tau=0}^{T_M},\end{aligned} \tag{2.16}$$

where T_M is the device memory time.

Remaining in the framework of the charge-controlled description, the memory effects can be modelled by choosing a charge-perturbation. Daniels *et al*., for instance, proposed in [13] to represent the nonquasi-static charge by means of a quasi-static charge $\mathbf{q}^{QS}(t)$ modified by a nonquasi-static term $\mathbf{\Delta q}(t)$:

$$\mathbf{q}^{NQS}(t) \doteq \mathbf{q}^{QS}(t) + \mathbf{\Delta q}(t) = \mathbf{q}^{QS}\left\{\mathbf{v}(t)\right\} - \boldsymbol{\tau}\left\{\mathbf{v}(t)\right\}\cdot\frac{d\mathbf{q}^{NQS}(t)}{dt}. \tag{2.17}$$

This charge-perturbation term is described by nonlinearly delayed functions, by means of voltage dependent charge redistribution times $\boldsymbol{\tau}$. In addition, Daniels assumed high frequency phenomena to affect only the displacement currents while the quasi-static conductive currents remain unchanged, that is:

$$\mathbf{i}(t) = \mathbf{\Phi}\left\{\mathbf{q}^{QS}(t), \mathbf{v}(t)\right\} + \frac{d\mathbf{q}^{NQS}(t)}{dt} = \mathbf{F}\left\{\mathbf{v}(t)\right\} + \frac{d\mathbf{q}^{NQS}(t)}{dt} = \mathbf{i}_c\left\{\mathbf{v}(t)\right\} + \frac{d\mathbf{q}^{NQS}(t)}{dt}. \tag{2.18}$$

Daniels adopted bi-cubic B-spline functions to describe the **q** functions and identified them by fitting the function derivatives on the small-signal measurements.

Afterwards, Fernandez-Barciela *et al.* [14] simplified Daniels' approach by choosing linearly delayed functions, and completed it by adopting the low-frequency dispersion model proposed by Root for the conductive currents:

$$\begin{aligned} &\mathbf{i}(t) = \mathbf{i}_{LF}(t, \tau_x) + \frac{d\mathbf{q}^{NQS}(t)}{dt} \\ &\mathbf{q}^{NQS}(t) = \mathbf{q}^{QS}\left\{\mathbf{v}(t)\right\} - \boldsymbol{\tau} \cdot \frac{d\mathbf{q}^{QS}\left\{\mathbf{v}(t)\right\}}{dt}, \end{aligned} \tag{2.19}$$

where τ_x accounts for the slow dynamics of charge-trapping and self-heating effects: it determines the cut-off frequency of a filtering function which realizes the transition between the dc currents and the dynamic ones (see Root's model, below).

A charge-controlled description is also adopted by Root *et al.* in [15], but here the authors described the intrinsic device by means of nonlinear state functions directly extracted from small-signal differential parameters. To this aim, the large-signal equation for the drain current is formulated in the frequency domain as:

$$I_D = H(\omega) I_D^{DC}(V_{GS}, V_{DS}) + j\Omega Q_D(V_{GS}, V_{DS}) + (1 - H(\omega)) I_D^{high}(V_{GS}, V_{DS}). \tag{2.20}$$

Equation (2.20) takes into account low-frequency dispersive effects by means of the nonlinear functions I_D^{DC} and I_D^{high}, which represent the device currents in static conditions and above the dispersion cut-off frequency, respectively. The transition between the dc and the "high" frequency current is modelled by the low-pass-filter function $h(\omega)$, described in the frequency domain by the diagonal matrix *H*, whose elements are $h(n\omega_0)$ (*n*=0,1,2,…), being ω_0 the fundamental frequency. The term $j\Omega Q_D$ corresponds, instead, to the time derivative of the nonquasi-static charge, where Ω is a diagonal matrix with elements $n\omega_0$, *n*=0,1,2, etc. In this model, the nonquasi-static charges are identified by numerical integration of the intrinsic differential parameters, as well as the above-cut-off drain current, that is:

$$\begin{aligned}
\nabla Q_G\left(V_{GS},V_{DS}\right) &= \frac{\operatorname{Im} Y_{11}\left(V_{GS},V_{DS},\omega\right)}{\omega}\hat{V}_{GS} + \frac{\operatorname{Im} Y_{12}\left(V_{GS},V_{DS},\omega\right)}{\omega}\hat{V}_{DS} \\
\nabla Q_D\left(V_{GS},V_{DS}\right) &= \frac{\operatorname{Im} Y_{21}\left(V_{GS},V_{DS},\omega\right)}{\omega}\hat{V}_{GS} + \frac{\operatorname{Im} Y_{22}\left(V_{GS},V_{DS},\omega\right)}{\omega}\hat{V}_{DS} \\
\nabla I_D^{high}\left(V_{GS},V_{DS}\right) &= \frac{\operatorname{Re} Y_{21}\left(V_{GS},V_{DS},\omega\right)}{\omega}\hat{V}_{GS} + \frac{\operatorname{Re} Y_{22}\left(V_{GS},V_{DS},\omega\right)}{\omega}\hat{V}_{DS}
\end{aligned} \tag{2.21}$$

where $\nabla = \frac{\partial}{\partial V_{GS}}\hat{V}_{GS} + \frac{\partial}{\partial V_{DS}}\hat{V}_{DS}$ and $\hat{V}_{GS}$, $\hat{V}_{DS}$ are unit vectors along the orthogonal intrinsic voltage axes. All the model nonlinear functions were then stored into tables.

This model has the advantages of being fully compatible with harmonic balance simulations, fast and unambiguously identifiable and charge-conservative. The drawback is that problems can arise with the parameters integration, like an eventual dependence on the integration path.

Nahri obtained in [16] a more accurate representation of the frequency device behaviour by *extending* the Root's approach. He started from the assumption that the quasi-static charge-controlled formulation (2.1) can be seen as the truncated form of the most general expansion:

$$\mathbf{i}(t) = \mathbf{F}\left[\mathbf{v}\right] + \frac{d}{dt}\mathbf{q}^{(1)}[\mathbf{v}] + \frac{d^2}{dt^2}\mathbf{q}^{(2)}[\mathbf{v}] + \frac{d^3}{dt^3}\mathbf{q}^{(3)}[\mathbf{v}] + \ldots . \tag{2.22}$$

The higher order terms accounts for the memory effects, thus allowing to obtain a an accurate description of frequency-dependent small-signal parameters. Even though (2.22) could be used for directly modelling the external device currents, Nahri applied it to the intrinsic device only, because the frequency-dependence of the intrinsic y parameters is less severe and allows to use a lower order series.

Equation (2.22) is equivalent to

$$\mathbf{i}(t) \cong \mathbf{h}_0(\mathbf{v})\cdot\mathbf{v} + \mathbf{h}_1(\mathbf{v})\cdot\frac{d\mathbf{v}}{dt} + \mathbf{h}_2(\mathbf{v})\cdot\frac{d^2\mathbf{v}}{dt^2} + \mathbf{h}_3(\mathbf{v})\cdot\frac{d^3\mathbf{v}}{dt^3} + \ldots, \tag{2.23}$$

which is obtained by linearizing the functions

$$\mathbf{i}(t) = \mathbf{f}\left(\mathbf{v}(t), \dot{\mathbf{v}}(t), \ddot{\mathbf{v}}(t), \dddot{\mathbf{v}}(t), \ldots\right) \tag{2.24}$$

with respect to voltage derivatives $\dot{\mathbf{v}}(t), \ddot{\mathbf{v}}(t), \dddot{\mathbf{v}}(t)\ldots .$

On the other hand, if we consider the state space equations:

$$\begin{aligned}\dot{\mathbf{X}}(t) &= \mathbf{F}_a\left(\mathbf{X}(t), \mathbf{V}(t)\right) \\ \mathbf{I}(t) &= \mathbf{F}_b\left(\mathbf{X}(t), \mathbf{V}(t)\right),\end{aligned} \tag{2.25}$$

where the terminal voltages **V** are the input, the terminal currents **I** are the output and **X** is the vector of the internal state variables, it is clear how (2.24) represents equations (2.25) reformulated in terms of the device external variables. In fact, in this case we would have:

$$\mathbf{I}(t) = \mathbf{f}\left(\mathbf{V}(t), \dot{\mathbf{V}}(t), \ddot{\mathbf{V}}(t), ..., \dot{\mathbf{I}}(t), \ddot{\mathbf{I}}(t), ...\right), \tag{2.26}$$

but in microwave transistors the feedback components can become important only in the case of nonlinear inductive effects, which are quite rare, thus the device currents can be represented as nonlinear functions of applied voltages and their derivatives, just as in (2.24).

The state-space behavioural approach (2.26) was adopted by Schreurs *et al*. in [17]: in this case, the identification of the **f** functions is carried out by means of Artificial Neural Networks, through the fitting of large signal experimental data at various bias and input power levels (measurement obtained by exploiting a LSNA). The first step in the model construction is to determine the order of the state variables, also considering that a trade-off is required between model accuracy and complexity. Schreurs found that state variables up to the second order derivatives must be included for modelling the HEMT device under test. Thus, an artificial neural network (ANN) with six input (the applied voltages and their first and second derivatives) and two output (the gate and drain currents) is used to fit the measured time-domain currents **I** to the measured independent variables $\mathbf{V}(t), \dot{\mathbf{V}}(t), \ddot{\mathbf{V}}(t)$.

All the so far introduced approaches can be also described by a current versus voltage relationship nonlinear with memory, that is:

$$\mathbf{i}(t) = \mathbf{\Psi}\left\|\left[\mathbf{v}(t-\tau)\right]\right\|_{\tau=0}^{T_M}. \tag{2.27}$$

where T_M is the virtually infinite memory time of the device. This relationship can be represented also by the Volterra series:

$$\begin{aligned}\mathbf{i}(t) = &\int_0^{T_M} \mathbf{h}_1(\tau_1)\mathbf{v}(t-\tau_1)d\tau_1 + \iint \mathbf{h}_2(\tau_1,\tau_2)\mathbf{v}(t-\tau_1)\mathbf{v}(t-\tau_2)d\tau_1 d\tau_2 + \\ &+\iiint \mathbf{h}_3(\tau_1,\tau_2,\tau_3)\mathbf{v}(t-\tau_1)\mathbf{v}(t-\tau_2)\mathbf{v}(t-\tau_3)d\tau_1 d\tau_2 d\tau_3 + \ldots\end{aligned} \tag{2.28}$$

Volterra kernels completely characterize the amplifier nonlinear dynamic response, so they provide a general and rigorous device description. Unfortunately, kernel measurements at microwave frequencies are rather difficult and Volterra series can be practically used only for weakly nonlinear systems: for strong nonlinearities some different approximations must be introduced.

Filicori and Vannini [18], for instance, separated memory from nonlinearity by introducing the dynamic voltage deviations $\mathbf{e}(t,\tau) \doteq \mathbf{v}(t-\tau) - \mathbf{v}(t)$:

$$\mathbf{i}(t) = \boldsymbol{\Psi}\left|\mathbf{v}(t-\tau)\right|_{\tau=0}^{T_M} = \boldsymbol{\Psi}\left|\mathbf{v}(t) + \mathbf{v}(t-\tau) - \mathbf{v}(t)\right|_{\tau=0}^{T_M} = \tilde{\boldsymbol{\Psi}}\left|\mathbf{v}(t), \mathbf{e}(t,\tau)\right|_{\tau=0}^{T_M}. \tag{2.29}$$

It is worth noting that by expanded the dynamic voltage deviations in Taylor series at $\tau = 0$, we obtain $\mathbf{v}(t-\tau) = \mathbf{v}(t) - \frac{d\mathbf{v}}{dt}\tau + \frac{d^2\mathbf{v}}{dt^2}\tau^2 - \ldots$, which, substituted in (2.29), leads to:

$$\mathbf{i}(t) = \tilde{\boldsymbol{\Psi}}\left|\mathbf{v}(t), -\frac{d\mathbf{v}}{dt}\tau + \frac{d^2\mathbf{v}}{dt^2}\tau^2 - \ldots\right|_{\tau=0}^{T_M} = \mathbf{f}\left(\mathbf{v}(t), \dot{\mathbf{v}}(t), \ddot{\mathbf{v}}(t), \ldots\right). \tag{2.30}$$

This leads to conclude that equation (2.29) is substantially equivalent to the approaches adopted by Nahri and Schreurs.

On the basis of (2.29), Filicori *et al.* developed the Finite Memory Model (FMM, [19]). The basic assumption of FMM is that actual electron devices behave according to a short duration of memory effects, as it can be found by experiments and simulations. In particular, when signal frequencies involved are small with respect to the inverse of the device memory duration (property well verified in the typical frequency operation range) the voltage dynamic deviation can be assumed as small even under large-signal operations. Therefore, the voltage-controlled functional can be linearized with respect to vanishingly small dynamic deviation, obtaining the nonlinear finite memory model formulation:

$$\mathbf{i}(t) = \mathbf{F}\left[\mathbf{v}(t)\right] + \int_0^{T_M} \mathbf{g}\left[\mathbf{v}(t), \tau\right] \mathbf{e}(t,\tau)\, d\tau, \tag{2.31}$$

where, $\mathbf{F}\left[\mathbf{v}(t)\right]$ are the static current characteristics and $\mathbf{g}\left[\mathbf{v}(t), \tau\right]$ are the nonlinearly voltage-controlled impulse responses. The nonlinear convolution integral represents a purely dynamic contribution, which takes into account reactive effects in the presence of fast-varying signals: it describes all the nonquasi-static memory effects.

It is possible to show (see [20]) that the nonlinear finite-memory formulation (2.31) becomes the conventional quasi-static voltage-controlled model (2.3) when relatively low frequencies are considered:

$$\lim_{\omega T_M \to 0} \left\{ \int_0^{T_M} \mathbf{g}\left[\mathbf{v}(t),\tau\right]\mathbf{e}(t,\tau)\, d\tau \right\} = \mathbf{C}\left[\mathbf{v}\right]\frac{d\mathbf{v}}{dt}; \tag{2.32}$$

instead, for higher frequencies (2.31) provides a mildly nonquasi-static model, where electron device memory time is compatible with a convolution-based linearization without memory truncation errors.

The finite memory model can be simplified for a better implementation in CAD tools by discretizing the T_M memory time into N_D time slots $\Delta\tau$. In such a way, we obtain the Nonlinear Discrete Convolution model (NDC, [20]):

$$\mathbf{i}(t) \cong \mathbf{F}_{LF}\left[\mathbf{v}(t)\right] + \sum_{p=1}^{N_D} \mathbf{g}_p\left[\mathbf{v}(t)\right] \cdot \left[\mathbf{v}(t - p\Delta\tau) - \mathbf{v}(t)\right]. \tag{2.33}$$

The model functions $\mathbf{g}_p[\mathbf{v}]$ can be identified from small-signal, bias-dependent S-parameter measurements by means of linear least-squares fitting at each bias point $v = V_{BIAS}$. Nonlinear optimization algorithms and related convergence problems are avoided, obtaining a robust and accurate model which can be implemented into commercial CAD tools with minor approximations. In addition, the NDC model can also be identified from LSNA measurements.

In order to have a more complete and consistent model, low-frequency dispersive effects are taken into account by replacing the DC device currents with a suitable low-frequency model $\mathbf{F}_{LF}[\mathbf{v}(t)]$. Due to characteristics dispersion, the voltage-controlled nonlinear currents depend also on additional state variables:

$$\mathbf{F}_{LF}\left[\mathbf{v}(t), T_j(t), \mathbf{x}(t)\right], \tag{2.34}$$

where T_j is the junction temperature and $\mathbf{x}(t)$ the trap filling status. These state variables feature a very long memory. However, the device thermal impedance and the trap filling dynamics act as low-pass-filters on the state variables, so that the current value in operation above cut-off is determined by the average component T_{j0} and $\mathbf{X}_0$. In addition, a proportionality law can be assumed between the average junction temperature and the DC component of the dissipated power, as also

between the average trap-filling state and the mean values of applied voltages, so the following equation can be adopted for the description of the channel current [20]-[21]:

$$i_D \cong F_{D,LF}\left[\mathbf{v}(t),\mathbf{V}_0,P_0\right] = F_{DC}\left[v_g,v_d\right] + f_g\left[v_g,v_d\right]\left(v_g - V_{g0}\right) + f_d\left[v_g,v_d\right]\left(v_d - V_{d0}\right) + \\ + f_p\left[v_g,v_d\right]\left(p_s(t) - P_0\right), \tag{2.35}$$

where f_g, f_d and f_p are the nonlinear model functions to be identified and $p_s(t) = v_d * F_{DC}[v_g, v_d]$ is the purely-quasi-static instantaneous power. In (2.35) the current deviations due to charge-trapping are accounted for by means of the currents dependence on voltage mean values and the deviations due to self-heating by means of the average dissipated power.

2.2 Conclusion

The main approaches to empirical device modelling have been discussed in this chapter. In particular, some well-known models presented in the literature have been illustrated as practical examples: the equivalent-circuit-based models of Curtice, Materka and Angelov, but also black-box models based on charge-controlled description of the electron device behaviour (Daniels, Fernandez-Barciela, Root), on the state-space equations (Nahri, Schreurs) or on the Volterra series approach (Filicori). All this models can be traced back to common physical considerations or system-theory-based equations.

In the next chapter, a new, empirical and simple, modelling approach developed during the PhD course will be described in details.

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Chapter 3

A New Modelling Approach: The Equivalent Voltages

Nonquasi-static phenomena arising in high frequency applications introduce practically finite memory effects in the dynamics of the electron devices. As discussed in Chapter 2, these effects may be taken into account in the framework of conventional equivalent-circuit modelling approaches for frequency-domain analyses, by adding series parasitic resistors and/or series resistive elements to the input capacitor (e.g. [1]-[7]). Some authors also introduce suitable delays in the voltage-controlled drain current source (e.g. [8] -[11]). If a mathematical approach is instead adopted, a voltage-controlled functional description based on a Volterra-like formulation has been proven to be adequate [12].

Nonquasi-static phenomena can be also taken into account in charge-based device descriptions, by adopting a perturbation-like approach (e.g. [13]-[15]). For instance, Daniels et al. [13] propose the use of a quasi-static charge, which is modified by means of a nonquasi-static term described by nonlinearly voltage-controlled delayed functions.

A similar charge-perturbation approach has been adopted in order to develop a new, original model, but significant simplifications have been achieved by modelling the nonquasi-static perturbations by means of an *equivalent-voltage approach*. The developed nonlinear device model accounts for nonquasi-static phenomena by means of linear, frequency-dependent voltage sources applied to an ideal *associated quasi-static device* [16]: the NonQuasi-Static Equivalent Voltage Model (NQS-EVM) will be described in details and empirically validated in the present chapter.

The equivalent voltage approach, already successfully adopted in different contexts (e.g., [20]), was originally introduced in [17] for the modelling of nonquasi-static phenomena in electron devices. In [17], the nonquasi-static phenomena are taken into account by controlling any existing quasi-static device model by means of equivalent, instead of actual, gate-source and drain-source port voltages. In the updated version [16], through a more accurate analytical derivation process, we presented a new model where different equivalent controlling port voltages were introduced for the conductive and the displacement current components. This, apparently trivial, modification is fully

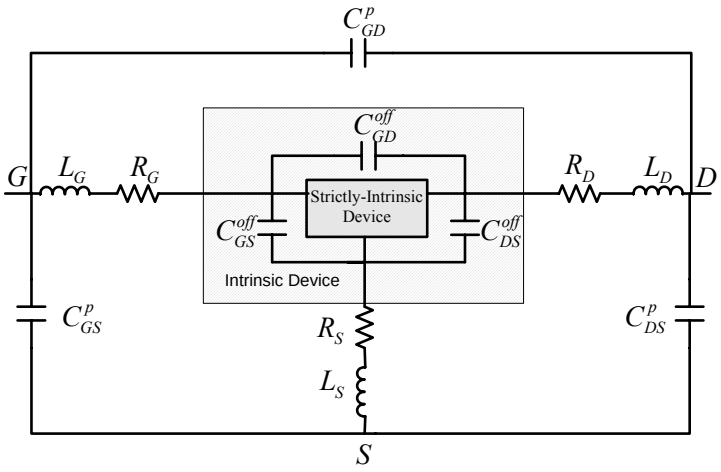


Fig. 3.1. Circuit topology for the identification of the strictly intrinsic device.

justified by theoretical analysis and leads to important improvements in the model predictive capabilities. In comparison with other classical modelling approaches, the proposed model proves to be accurate under both small- and large-signal operation in a much more extended range of bias conditions.

The proposed model is technology-independent, since it can be adopted for either bipolar devices and FETs. It can be easily identified from conventional measurements and directly implemented in the framework of time- or frequency-domain oriented CAD tools.

This chapter is organized as follows. In Section 3.1 the theory of the new model is presented by adopting a charge-controlled approach. The model identification procedure and CAD implementation is outlined in Section 3.2 and, finally, in Section 3.3, the experimental results are discussed by using a 0.25 μm GaAs PHEMT.

3.1 The New Nonquasi-Static Model

We proposed in [16] a new empirical, black-box model, which is simple and accurate at the same time. Although the proposed approach is technology-independent, the following discussion is focused for reference on field effect transistors. However, an analogous approach can be applied to bipolar devices.

3.1.1 The Strictly-Intrinsic Device

We define as a *strictly-intrinsic* device the one obtained after de-embedding not only from extrinsic parasitic elements, but also from the components of a purely-capacitive parallel π-network, which describes the behaviour of the intrinsic device in the off-state (i.e. $v_{GS} < V_T$), according for

instance to the circuit topology sketched in Fig. 3.1. In particular, the C_{GS}^{off}, C_{GD}^{off} and C_{DS}^{off} capacitors are assumed here to be linear and identified in a deep pinched-off channel condition with zero drain-source voltage (cold-FET).

The strictly-intrinsic transistor has the property of becoming practically an open circuit in the pinched-off region. This will lead to great model simplification, as it will be pointed out in the following.

3.1.2 Equivalent Controlling Voltages

As outlined in Chapter 2, quasi-static charge-controlled device equations may be seen as a particular case of system theory-based input-output relationships applied to the electron device. In particular, we assume here applied voltages, port currents and internal charge distributions as input, output and state variables, respectively. In such a way, vector quasi-static model equations for the strictly-intrinsic device may be written as:

$$\mathbf{i}(t) = \mathbf{\Phi}\left\{\mathbf{q}(t), \mathbf{v}(t)\right\} + \frac{d\mathbf{q}(t)}{dt} \tag{3.1}$$

$$\mathbf{q}(t) = \mathbf{\Psi}\left\{\mathbf{v}(t)\right\}, \tag{3.2}$$

where $\mathbf{i} = \left[i_1\ i_2\right]^T$, $\mathbf{q} = \left[q_1\ q_2\right]^T$ and $\mathbf{v} = \left[v_1\ v_2\right]^T$. For instance, in a common gate configuration, these quantities correspond with source and drain currents, gate-source and gate-drain charges, gate-source and gate-drain voltages, respectively. Moreover, $\mathbf{\Phi}(\cdot) = \left[\Phi_1(\cdot)\ \Phi_2(\cdot)\right]^T$ and $\mathbf{\Psi}(\cdot) = \left[\Psi_1(\cdot)\ \Psi_2(\cdot)\right]^T$ represent the relationships between source/drain conductive currents versus voltage, and gate-source/gate-drain charges versus voltage, respectively. Both, $\mathbf{\Phi}$ and $\mathbf{\Psi}$ are vectors of purely algebraic nonlinear functions.

The charge-controlled model (3.1)-(3.2) is suitable to describe the device behaviour under quasi-static operation and it can be alternatively expressed in a voltage-controlled form, by simply substituting (3.2) into (3.1), i.e.:

$$\mathbf{i}(t) = \mathbf{\Phi}\left\{\mathbf{\Psi}\left\{\mathbf{v}(t)\right\}, \mathbf{v}(t)\right\} + \frac{d\mathbf{\Psi}\left\{\mathbf{v}(t)\right\}}{d\mathbf{v}} \cdot \frac{d\mathbf{v}(t)}{dt} \doteq \mathbf{F}\left\{\mathbf{v}(t)\right\} + \mathbf{C}\left\{\mathbf{v}(t)\right\} \cdot \frac{d\mathbf{v}(t)}{dt} \quad , \tag{3.3}$$

where $\mathbf{F}$ is the vector of the dc currents and $\mathbf{C}$ is a capacitive matrix describing the device dynamics, whenever the charge response to the voltage excitation may be considered almost instantaneous, i.e., when memory effects have vanishing small durations. Current-voltage

relationship (3.3) is coherent with the finite memory model (2.30) in Chapter 2, when the integral term is replaced by (2.31).

It is worth considering that (3.3) could have been obtained also by neglecting in (3.1) the explicit dependence of the functions $\mathbf{\Phi}$ either on the voltages $\mathbf{v}$ (also affecting the internal electric field distribution) or on the charges $\mathbf{q}$. Such a choice was actually made in [17], where the function $\mathbf{\Phi}$ was assumed to be only dependent on $\mathbf{q}$. This is a quite common assumption involving no loss of generality in the quasi-static operation mode associated with the charge-control equations. Unfortunately, this is not fully justified when a charge-perturbation-based approach is adopted, as in this case. Thus, both dependencies must necessarily be taken into account here.

At very high-frequencies charges respond with finite memory times, which cannot be neglected anymore. Under this operation, (3.2) must be replaced by a modified internal charge distribution, which may be generally described as:

$$\mathbf{q}^{NQS}(t) = \mathbf{\Psi}^{NQS}\left|\mathbf{v}(t-\tau)\right|_{\tau=0}^{T_M}, \tag{3.4}$$

or, equivalently:

$$\mathbf{q}^{NQS}(t) = \tilde{\mathbf{\Psi}}^{NQS}\left|\mathbf{v}(t), \mathbf{v}(t-\tau)-\mathbf{v}(t)\right|_{\tau=0}^{T_M}, \tag{3.5}$$

where the nonquasi-static charges $\mathbf{q}^{NQS} = \left[\, q_1^{NQS} \; q_2^{NQS} \,\right]^T$ have been defined through a functional $\mathbf{\Psi}^{NQS}$ (or $\tilde{\mathbf{\Psi}}^{NQS}$) of the voltages $\mathbf{v}(\cdot)$ evaluated at both present (t) and past times ($t-\tau$), with τ ranging from zero to a memory time T_M, which assumes practically finite values. Thus, (3.1) is replaced by:

$$\mathbf{i}(t) = \mathbf{\Phi}\left\{\mathbf{q}^{NQS}(t), \mathbf{v}(t)\right\} + \frac{d\mathbf{q}^{NQS}(t)}{dt}. \tag{3.6}$$

Now we describe the nonquasi-static charge $\mathbf{q}^{NQS}$ in terms of the quasi-static charge $\mathbf{q}$ given in (3.2), perturbed by an additional charge deviation $\Delta\mathbf{q} = \left[\Delta q_1 \; \Delta q_2\right]^T$, which takes into account the actual nonstationary effects, i.e.:

$$\mathbf{q}^{NQS}(t) \doteq \mathbf{q}(t) + \Delta\mathbf{q}(t). \tag{3.7}$$

The quasi-static charge $\mathbf{q}$ in (3.7) is such that, when considering signal spectral components at frequencies much lower than $1/T_M$ ($\omega \ll 1/T_M$), it holds:

$$\mathbf{q}(t) = \tilde{\mathbf{\Psi}}^{NQS}\left\{\mathbf{v}(t), 0\right\} \doteq \mathbf{\Psi}\left\{\mathbf{v}(t)\right\}, \tag{3.8}$$

since, under this operation, the voltage dynamic deviations $\mathbf{v}(t-\tau) - \mathbf{v}(t)$ are vanishingly small.

According to (3.7)-(3.8), all of the memory effects related to the nonquasi-static device behaviour are now due to the charge perturbation term $\Delta\mathbf{q}$. Thus, charge-voltage relationship (3.5) becomes now:

$$\mathbf{q}^{NQS}(t) = \mathbf{\Psi}\left\{\mathbf{v}(t)\right\} + \Delta\mathbf{q}(t). \tag{3.9}$$

Unfortunately, the charge perturbation $\Delta\mathbf{q}$ is expected to be strongly nonlinearly dependent on voltages. In fact, it must provide non-negligible correction under *on* conditions, while it must be vanishingly small under *off* device conditions since, according to empirical evidence, the off-state behaviour is practically quasi-static.

To overcome this drawback, the same result expressed by (3.9) can be more conveniently obtained by introducing suitable *equivalent voltages* $\hat{\mathbf{v}}_d \doteq \left[\hat{v}_{d1}\ \hat{v}_{d2}\right]^T$, according to:

$$\hat{\mathbf{v}}_d(t) \doteq \mathbf{\Psi}^{-1}\left\{\mathbf{q}^{NQS}(t)\right\} \doteq \mathbf{v}(t) + \Delta\mathbf{v}_d(t), \tag{3.10}$$

with $\Delta\mathbf{v}_d \doteq \left[\Delta v_{d1}\ \Delta v_{d2}\right]^T$ and where (3.7) and (3.8) have been taken into account. The equivalent voltages (3.10) satisfy the feature of providing the same charge distribution $\mathbf{q}^{NQS}$ (i.e., the same displacement current) in a virtually quasi-static device described by (3.1)-(3.2). Thus, (3.6) can be equivalently written as:

$$\mathbf{i}(t) = \mathbf{\Phi}\left\{\mathbf{q}^{NQS}(t), \mathbf{v}(t)\right\} + \mathbf{C}\left\{\hat{\mathbf{v}}_d(t)\right\} \cdot \frac{d\hat{\mathbf{v}}_d(t)}{dt}, \tag{3.11}$$

where (3.10) is taken into account. This shows that the displacement current ($d\mathbf{q}^{NQS}/dt$) of the nonquasi-static device may be equivalently evaluated through the corresponding term of *an associated purely quasi-static device,* where the actual controlling voltages $\mathbf{v}$ are replaced by suitably defined equivalent voltages $\hat{\mathbf{v}}_d$. The same consideration does not apply for the conductive current contribution, since the explicit dependence of the function $\mathbf{\Phi}$ on the voltage $\mathbf{v}$ has been not

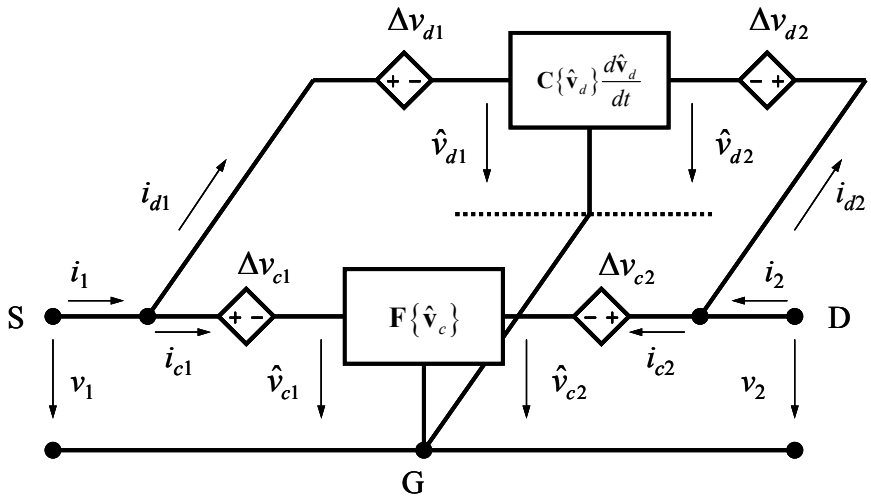


Fig. 3.2. Circuit schematic of the proposed non-quasi-static modeling approach for the strictly-intrinsic device in common-gate configuration.

initially neglected in (3.1), as in [17]. Thus, by considering the conductive term only, as expressed in (3.6), we have:

$$\mathbf{\Phi}\left\{\mathbf{q}^{NQS}(t),\mathbf{v}(t)\right\}=\mathbf{\Phi}\left\{\mathbf{\Psi}\left\{\mathbf{v}(t)\right\}+\Delta\mathbf{q}(t),\mathbf{v}(t)\right\}. \tag{3.12}$$

This shows how the term $\Delta\mathbf{q}$ gives rise to a perturbation in the conductive current, which is also expected to have a strong nonlinear dependence on voltages. In accordance with the equivalent voltage approach adopted for the charge-voltage relationship (3.10), also in this case it is convenient to define suitable equivalent voltages $\hat{\mathbf{v}}_c \doteq \left[\hat{v}_{c1}\ \hat{v}_{c2}\right]^T$:

$$\hat{\mathbf{v}}_c(t)\doteq\mathbf{F}^{-1}\left\{\mathbf{\Phi}\left\{\mathbf{q}^{NQS}(t),\mathbf{v}(t)\right\}\right\}\doteq\mathbf{v}(t)+\Delta\mathbf{v}_c(t), \tag{3.13}$$

with $\Delta\mathbf{v}_c=\left[\Delta v_{c1}\ \Delta v_{c2}\right]^T$. The equivalent voltages (3.13) provide the same conductive current into a virtually quasi-static device described by (3.1)-(3.2), or equivalently by (3.3). Then, by substituting (3.13) into (3.11), we get:

$$\mathbf{i}(t)=\mathbf{F}\left\{\hat{\mathbf{v}}_c(t)\right\}+\mathbf{C}\left\{\hat{\mathbf{v}}_d(t)\right\}\cdot\frac{d\hat{\mathbf{v}}_d(t)}{dt}, \tag{3.14}$$

which gives the total nonquasi-static current of the actual device in an equivalent voltage-controlled form through equations which are analogous to the quasi-static model (3.3). Model equations (3.14) are coherent with the circuit schematic shown in Fig. 3.2.

According to (3.14), a nonlinear nonquasi-static model is obtained by considering an *associated virtual quasi-static device* described by the nonlinear algebraic functions $\mathbf{F}$, $\mathbf{C}$ defined in (3.3), where $\mathbf{F}$ and $\mathbf{C}$ are controlled by *equivalent,* instead of actual, port voltages ($\hat{\mathbf{v}}_c$ and $\hat{\mathbf{v}}_d$, respectively). This formulation is convenient since, in order to guarantee that no charge perturbation is introduced in the off-state (where the device behaviour is practically quasi-static), the $\Delta\mathbf{v}_d$ and $\Delta\mathbf{v}_c$ voltage deviations do not need to become vanishingly small when applied to the *strictly-intrinsic* device (which acts as an open circuit in the off-state). This suggests that, unlike $\Delta\mathbf{q}$, the $\Delta\mathbf{v}_d$ and $\Delta\mathbf{v}_c$ corrections can be not so strongly nonlinearly dependent on the applied voltages. Actually, empirical evidence provided in Sec. 3.3 shows that a linear dependence of the $\Delta\mathbf{v}_d$ and $\Delta\mathbf{v}_c$ terms on the voltages $\mathbf{v}$ can be considered to be sufficiently adequate to achieve very good accuracy.

The two voltage deviations terms, $\Delta\mathbf{v}_d$ and $\Delta\mathbf{v}_c$, are not independent one of each other. Their relationship is investigated in Appendix A. In particular, under the hypothesis of small voltage deviations, it is proven that:

$$\mathbf{G}\{\mathbf{v}(t)\}\cdot\Delta\mathbf{v}_c(t)=\left.\frac{\partial\boldsymbol{\Phi}\{\mathbf{q}^{NQS}(t),\mathbf{v}(t)\}}{\partial\Delta\mathbf{q}}\right|_{\Delta\mathbf{q}=0}\cdot\mathbf{C}\{\mathbf{v}(t)\}\cdot\Delta\mathbf{v}_d(t)\,, \tag{3.15}$$

where $\mathbf{G}\{\mathbf{v}(t)\}$ represents the voltage dependent, differential conductance matrix of the resistive part $\mathbf{F}$ of the associated quasi-static device.

Equation (3.15) will be considered in the model identification presented in Sec. 3.2.

3.1.3 Modelling of Voltage Deviations

The memory effects due to nonquasi-static phenomena, are taken into account by means of the voltage deviations $\Delta\mathbf{v}_c$, $\Delta\mathbf{v}_d$. The two of them can be written as:

$$\Delta\mathbf{v}_x(t)=\boldsymbol{\Gamma}_x\left|\mathbf{v}(t-\tau)\right|_{\tau=0}^{T_M}, \tag{3.16}$$

where the subscript x stands here for either c or d and $\boldsymbol{\Gamma}_x$ is a functional of present and past voltages. Since microwave devices usually behave with very short memory time dynamics, a finite memory time T_M has been adopted in (3.16) without practical loss in accuracy. By adopting a

similar approach as in Sec. 3.1, we describe the voltage deviations (3.16) through a convolution integral as:

$$\Delta\mathbf{v}_x(t) = \int_0^{T_M} \mathbf{a}_x\left\{\mathbf{v}(t),\tau\right\}\cdot\left[\mathbf{v}(t-\tau)-\mathbf{v}(t)\right]d\tau\,, \tag{3.17}$$

where $\mathbf{a}_x$ is a suitable matrix of functions nonlinearly dependent on $\mathbf{v}$ in the most general case. The dependence on the dynamic voltage deviations $\mathbf{v}(t-\tau)-\mathbf{v}(t)$ allows for a vanishing contribution of (3.17) when the signal frequencies involved are not high enough to generate a nonquasi-static behaviour.

Expression (3.17) could be directly implemented into modelling CAD environments as a nonlinearly-controlled voltage-source, for instance by storing the functions $\mathbf{a}_x$ as look-up tables. However, in the present work a simple linear dependence of $\Delta\mathbf{v}_x$ on port voltages is assumed (i.e. $\mathbf{a}_x$ independent of $\mathbf{v}$), leading to an extremely compact and computationally efficient model. In fact, most of the nonlinear dependence of the device nonquasi-static behaviour is implicitly taken into account by the characterizing feature of the strictly-intrinsic device. The latter, actually, becomes an open circuit in the off-state, so it is implicitly guaranteed that the equivalent voltage generators will introduce nonquasi-static corrections in the on-state device operation only. The validity of this hypothesis will be empirically proven by the model predictive accuracy shown, in Sec. V, under linear and nonlinear nonquasi-static device operation.

In order to further simplify both the identification procedure of the model and its implementation into CAD tools for microwave circuit analysis, the integral convolution (3.17) is eventually approximated with a finite summation, after having divided the memory time TM into ND elementary time slots $\Delta\tau$ (i.e. $T_M = N_D\Delta\tau$). Thus:

$$\Delta\mathbf{v}_x(t) \cong \sum_{p=1}^{N_D} \mathbf{a}_{x,p}\cdot\left[\mathbf{v}(t-p\Delta\tau)-\mathbf{v}(t)\right] \tag{3.18}$$

where $\mathbf{a}_{x,p}$, with p=1,…,N_D, are now matrices of real parameters to be identified. The extraction procedure will be described in Sec. 3.2.

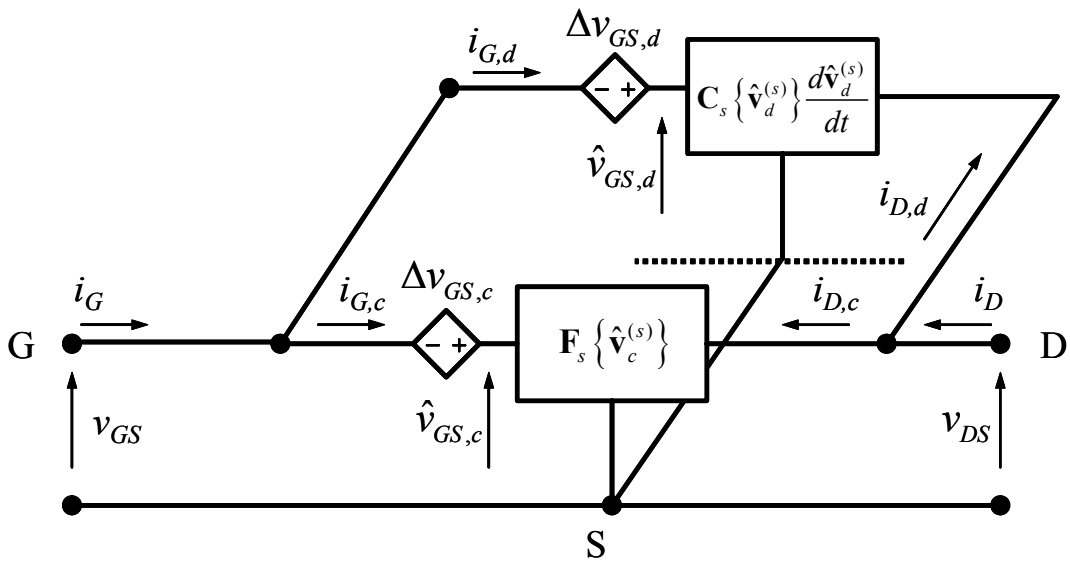


Fig. 3.3. Circuit schematic of the proposed non-quasi-static modeling approach for the strictly-intrinsic device in common-source configuration.

3.1.4 Common-Source Model Equations

According to the previously-introduced linearity assumption of the voltage deviations $\Delta\mathbf{v}_c$, $\Delta\mathbf{v}_d$ with respect to the port voltages $\mathbf{v}$, additional model simplification can be achieved.

To this aim, we consider a FET device, cold-biased at V_{DS}=0 V. Under this operating condition the intrinsic device (identified as the region strictly beneath the gate electrode) is, in many cases, perfectly symmetrical from both the geometrical and electrical point of view. Nonquasi-static effects can still be taken into account by the proposed equivalent voltage approach, but symmetrical voltage deviations should be considered in a common-gate device description, i.e.:

$$\Delta v_{x1} = \Delta v_{x2}\,, \tag{3.19}$$

where the subscript x stands for either c or d.

However, since the voltage deviations are assumed here to be bias-independent, relationship (3.19) must hold at each bias condition. This allows to greatly simplify the modeling approach, especially if applied to a common-source device configuration: in fact, the voltage deviations in a common-source device (denoted by 's') are related to the corresponding quantities in the common-gate case (denoted here for the sake of clearness by 'g') as:

$$\Delta v_{x1}^{(s)} = \Delta v_{x1}^{(g)} \tag{3.20}$$

$$\Delta v_{x2}^{(s)} = \Delta v_{x1}^{(g)} - \Delta v_{x2}^{(g)}\,, \tag{3.21}$$

which, taking into account (3.19), lead to neglecting the voltage deviation applied at the drain electrode, i.e.:

$$\Delta v_{x2}^{(s)} = 0\,. \tag{3.22}$$

The model topology obtained so far is in accordance with Fig. 3.3, where a more conventional notation has been adopted, i.e. $v_1^{(s)} \equiv v_{GS}$, $v_2^{(s)} \equiv v_{DS}$, $\Delta v_{x1}^{(s)} \equiv \Delta v_{GS,x}$, and $\mathbf{F}_s$, $\mathbf{C}_s$ are vector quantities corresponding in the common-source-domain to $\mathbf{F}$, $\mathbf{C}$, respectively. The only two scalar voltage deviations $\Delta v_{GS,c}$, $\Delta v_{GS,d}$ are, therefore, adequate to model all of nonquasi-static phenomena. As shown in Appendix A, the relationship (3.15) between them simply becomes:

$$\Delta v_{GS,c} = \rho \cdot \Delta v_{GS,d}\,, \tag{3.23}$$

where ρ is a scalar model coefficient. The hypothesis of linearity for the voltage deviations $\Delta v_{GS,c}$ and $\Delta v_{GS,d}$ leads to consider the parameter ρ bias-independent. Actually, the experimental validation described in Section 3.3 for a GaAs PHEMT leads to an almost zero ρ value.

According to (3.18), $\Delta v_{GS,d}$ may be expressed as:

$$\Delta v_{GS,d}(t) \cong \sum_{p=1}^{N_D} a_{1p}^{(s)} \cdot \left[v_{GS}(t - p\Delta\tau) - v_{GS}(t) \right] + \sum_{p=1}^{N_D} a_{2p}^{(s)} \cdot \left[v_{DS}(t - p\Delta\tau) - v_{DS}(t) \right], \tag{3.24}$$

where $a_{1p}^{(s)}$ and $a_{2p}^{(s)}$ ($p=1,...,N_D$) are scalar coefficients to be identified.

3.2 Model Identification and CAD Implementation

Model identification is easily carried out on the basis of small-signal, bias-dependent, S-parameters device measurements. In particular, under small signal regime around a bias condition $\mathbf{V}^B \doteq \left[V_{GS}^B \; V_{DS}^B \right]^T$, according to Fig. 3.3, we have:

$$\mathbf{I}(\omega) = \mathbf{Y}(\mathbf{V}^B, \omega) \cdot \mathbf{V}(\omega) = \mathbf{I}_c(\omega) + \mathbf{I}_d(\omega) = \mathbf{G}_s(\hat{\mathbf{V}}_c^B) \cdot \hat{\mathbf{V}}_c(\omega) + j\omega \mathbf{C}_s(\hat{\mathbf{V}}_d^B) \cdot \hat{\mathbf{V}}_c(\omega), \tag{3.25}$$

where $\mathbf{I} \doteq \left[I_G \; I_D \right]^T$, $\mathbf{I}_c \doteq \left[I_{G,c} \; I_{D,c} \right]^T$, $\mathbf{I}_d \doteq \left[I_{G,d} \; I_{D,d} \right]^T$ are the vector of total, conductive and displacement phasors of currents in the frequency domain; $\mathbf{Y}$ is the bias- and frequency-dependent admittance matrix of the strictly-intrinsic device; $\mathbf{G}_s$ is a differential conductance matrix which will

be better defined later; $\mathbf{V} \doteq \left[V_{GS}\ V_{DS}\right]^T$, $\hat{\mathbf{V}}_c \doteq \left[\hat{V}_{GS,c}\ V_{DS}\right]^T$, $\hat{\mathbf{V}}_d \doteq \left[\hat{V}_{GS,d}\ V_{DS}\right]^T$ are the actual and the equivalent phasors of voltages and $\hat{\mathbf{V}}_c^B \doteq \left[\hat{V}_{GS,c}^B\ V_{DS}^B\right]^T$, $\hat{\mathbf{V}}_d^B \doteq \left[\hat{V}_{GS,d}^B\ V_{DS}^B\right]^T$. According to (3.10) and (3.13) we have $\hat{\mathbf{V}}_c(\omega) = \mathbf{V}(\omega) + \Delta\mathbf{V}_c(\omega)$ and $\hat{\mathbf{V}}_d(\omega) = \mathbf{V}(\omega) + \Delta\mathbf{V}_d(\omega)$, where $\Delta\mathbf{V}_c \doteq \left[\Delta V_{GS,c}\ 0\right]^T$ and $\Delta\mathbf{V}_d \doteq \left[\Delta V_{GS,d}\ 0\right]^T$. Moreover, by taking into account (3.42) and (3.24), we have:

$$\Delta\mathbf{V}_c(\omega) = \rho \cdot \Delta\mathbf{V}_d(\omega) \tag{3.26}$$

$$\Delta\mathbf{V}_d(\omega) = \sum_{p=1}^{N_D} \mathbf{a}_p^{(s)} \cdot (e^{-j\omega p\Delta\tau} - 1) \cdot \mathbf{V}(\omega), \tag{3.27}$$

where $\mathbf{a}_p^{(s)} \doteq \begin{bmatrix} a_{1p}^{(s)} & a_{2p}^{(s)} \\ 0 & 0 \end{bmatrix}$ with ($p=1,...,N_D$). By substituting (3.26) and (3.27) into (3.25), after simple algebraic manipulation, we obtain:

$$\mathbf{Y}(\mathbf{V}^B, \omega) = \mathbf{G}_s(\hat{\mathbf{V}}_c^B) \cdot \left[\mathbf{1} + \rho \cdot \sum_{p=1}^{N_D} \mathbf{a}_p^{(s)} \cdot (e^{-j\omega p\Delta\tau} - 1)\right] + j\omega\mathbf{C}_s(\hat{\mathbf{V}}_d^B) \cdot \left[\mathbf{1} + \sum_{p=1}^{N_D} \mathbf{a}_p^{(s)} \cdot (e^{-j\omega p\Delta\tau} - 1)\right]. \tag{3.28}$$

In order to use (3.28) for the identification of the model parameters $\mathbf{a}_p^{(s)}$ and ρ, the matrices $\mathbf{G}_s$ and $\mathbf{C}_s$ are preliminary evaluated. To this aim, (3.28) is first considered at sufficiently-low frequencies such that nonquasi-static effects are still negligible. In fact, in this condition we can write $\mathbf{Y}\left(\mathbf{V}^B, \omega\right) = \mathbf{G}_s\left(\mathbf{V}^B\right) + j\omega\mathbf{C}_s\left(\mathbf{V}^B\right)$, allowing for an easy multi-bias identification of the $\mathbf{G}_s$ and $\mathbf{C}_s$ matrices. After this, a closed-form least-square best fit procedure based on (3.28) can be used for the evaluation of the coefficients $\mathbf{a}_p^{(s)}$, ρ on a suitable frequency range in the region where non-quasi-static phenomena occur. To this aim, either a multi- or single-bias optimization procedure can be adopted. By considering N_f different frequencies and N_b biases, the resulting identification problem consists in the solution of an over-determined system of $8 \cdot N_f \cdot N_b$ equations in the $2 \cdot N_D + 1$ unknowns ρ, $a_{1p}^{(s)}$ and $a_{2p}^{(s)}$ ($p=1,...,N_D$). In this work, a simplified identification procedure based on a single bias point, chosen for class-A large signal operation, provided very good model prediction capabilities.

The above outlined flexibility in choosing the number of model parameters and their closed form identification procedure represent a great advantage of this model over more classical approaches. In fact, parameters like R_i or τ in typical equivalent-circuit-based models provide limited multi-bias

flexibility and are normally identified in the framework of a strongly nonlinear optimization procedure.

The nonquasi-static device model can be easily implemented in commercially available CAD tools. For the conductive currents, the PHEMT low-frequency dispersive I/V model proposed in [21] is adopted here. The corresponding CAD implementation may be also found in [21]. This model is capable of accurate predictions in the presence of signals having spectral components at frequencies above the cut-off of dispersive phenomena but low enough to consider the device reactive effects still negligible. The quasi-static displacement currents of the strictly-intrinsic device can be modelled by using look-up-table-based bias-dependent capacitive elements. Then, each voltage deviation is modelled by means of two series-connected voltage-sources, controlled by the actual intrinsic voltages, according to Fig.3.3. Finally, in agreement with Fig. 3.1, the extrinsic device model is obtained by embedding the purely capacitive π-network (i.e. C_{GS}^{off} , C_{GD}^{off} and C_{DS}^{off}) and the linear network of extrinsic parasitic elements.

The schematic implementation in Agilent ADS is, for instance, reported in Fig. 3.4.

3.3 Experimental Validation

In order to experimentally validate the proposed model, a GaAs PHEMT (L=0.25 μm, W=600 μm) was characterized under static and small-signal dynamic regime, up to 70 GHz. Well known cold-FET procedures [10] were used for the identification of extrinsic parasitic elements according to the circuit topology shown in Fig. 3.1.The parallel network of linear capacitors introduced in Section 3.1.1 was identified in a deep pinched-off, cold-FET condition ($V_{GS} = -1.5$ V , $V_{DS} = 0$ V), leading to: $C_{GS}^{off} = 162$ fF , $C_{GD}^{off} = 148$ fF and $C_{DS}^{off} = 130$ fF . The strictly-intrinsic small-signal device description was finally obtained by de-embedding the measurements from these elements.

In order to identify the voltage-controlled voltage-sources (3.26), (3.27), the matrices $\mathbf{G}_s$ and $\mathbf{C}_s$ were preliminary identified. According to the procedure outlined in Sec. 3.2, a least square "best fit" numerical procedure was carried out between (3.28) and the corresponding strictly intrinsic device admittances obtained from de-embedded measurements. To this aim, a single bias point (V_{GS}=-0.55 V, V_{DS}=6.5 V) and N_f =9 frequencies between 2 GHz and 10 GHz (1 GHz step) were considered. In this range the device behaviour was found to be nearly quasi-static.

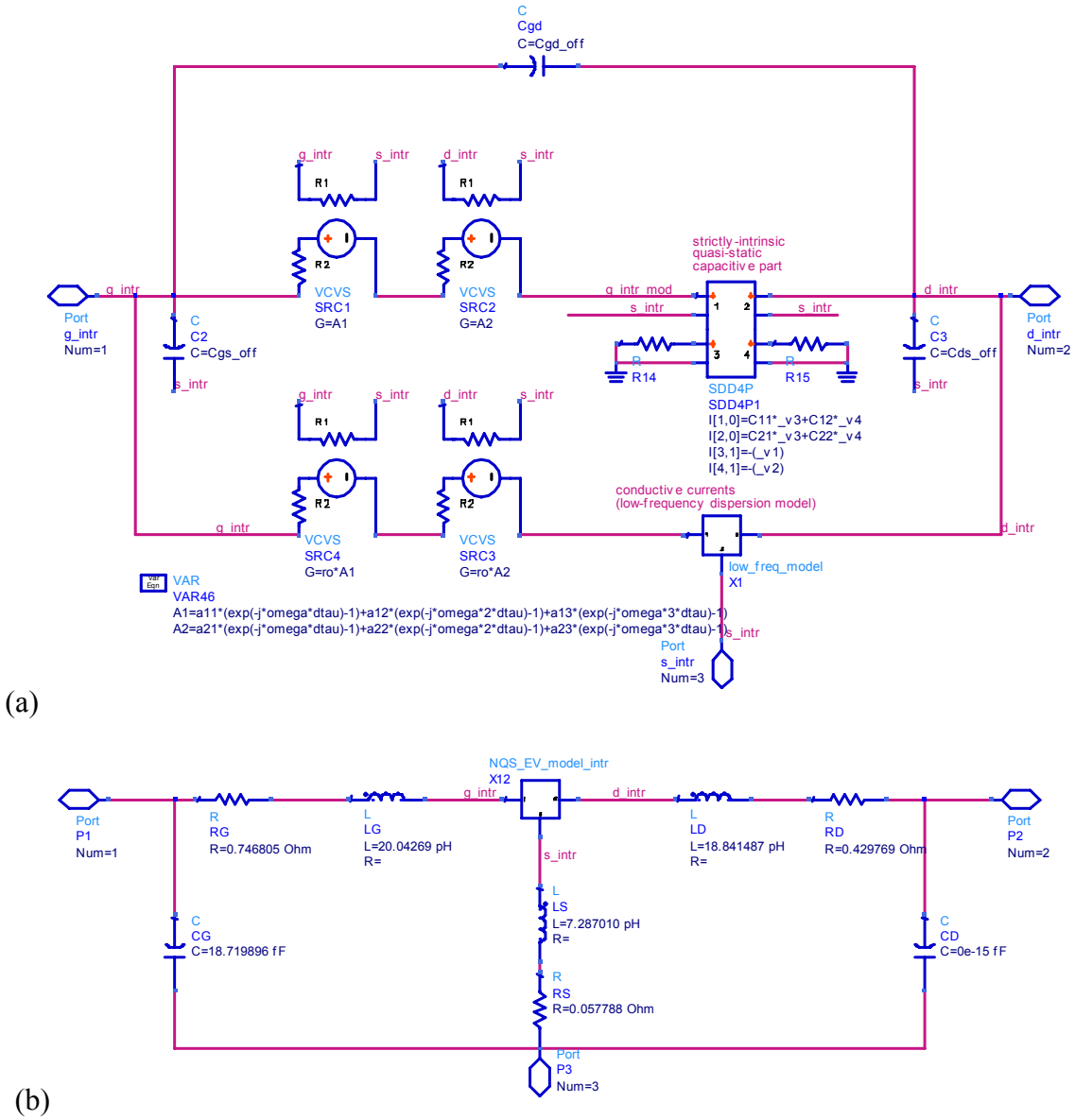


Fig. 3.4: The ADS schematic of the NQS-EV model: The intrinsic model implementation (a) and the extrinsic parasitic network (b).

Finally, the complete identification of the model parameters ρ, $a_{1p}^{(s)}$, $a_{2p}^{(s)}$ was based on the evaluation of (3.28) in a much more extended frequency range, namely from 2 GHz to 70 GHz. For the device under test, a memory time T_M=1.8 ps with $N_D = 3$ was chosen[1]. In such a way, only seven scalar coefficients are needed. Closed-form minimization of squared deviations between (3.28) and de-embedded measurements provided the optimal parameters: $a_{11}^{(s)} = -4.054$, $a_{12}^{(s)} = 5.1033$, $a_{13}^{(s)} = -3.1458$, $a_{21}^{(s)} = -1.1464$, $a_{22}^{(s)} = 0.9255$, $a_{23}^{(s)} = -0.2796$ and $\rho = 1.3\text{e}-6$. It is worth noting that a near zero value was found for the parameter ρ: this means that, for the actual PHEMT, the

[1] Considerations discussed in [11] for the most appropriate choice of T_M and N_D parameters, may be still applied here.

charge perturbation due to nonquasi-static phenomena mainly affects the displacement current while its effect on the conductive current is almost negligible. In this case (3.14) would become:

$$\mathbf{i}(t) = \mathbf{F}\left\{\mathbf{v}(t)\right\} + \frac{d\mathbf{q}^{NQS}(t)}{dt}, \tag{3.29}$$

where the displacement term is here an approximation of the integral term in the functional approach (2.30) described in Chapter 2. The same conclusion has been adopted by several authors which have modelled high frequency, nonquasi-static phenomena in electron devices (e.g. Daniels [13]-[14], as discussed in Section 2.1.2).

Once the $\Delta V_{GS,c}$, $\Delta V_{GS,d}$ voltage deviations are identified, nonquasi-static device modelling can be based on the circuit topology shown in Fig.3.3, where $\mathbf{F}_s$, $\mathbf{C}_s$ may be provided by any nonlinear purely quasi-static model.

The empirical model proposed in [21] was used for the drain conductive current, in order to take also into account low frequency dispersive effects due to device self-heating and charge-trapping phenomena. According to the procedures described in [21], the involved parameter functions were identified on the voltage grid defined by V_{GS} ranging from -1.5 V to 0 V (step 0.1 V) and V_{DS} between 0 V and 10 V (step 1 V) and stored into look-up-tables in the framework of the CAD tool.

The displacement currents were described directly in accordance with the schematic shown in Fig. 3.3. To this aim, the matrix $\mathbf{C}_s$ was identified on the same bias grid used for the low frequency conductive model. A look-up-table-based approach was also adopted for CAD implementation.

The nonquasi-static model was initially validated under small-signal dynamic operation. In Fig. 3.5, the predicted intrinsic admittance parameters Y_{11} and Y_{21} (the two most affected by nonquasi-static phenomena, as it can be drawn from Sec. 1.2.2) are plotted versus frequency and compared with measurements under two bias conditions, different from that used for the identification. The first bias point (Figs. 3.5-a and 3.5-b) corresponds to on-state device operation: as it can be seen, a very good agreement with measured data is achieved up to 70 GHz. The virtual quasi-static behaviour is also plotted here as a reference, showing that important corrections are applied by the voltage-controlled voltage-sources. However, in off-state condition (Figs. 3.5-c and 3.5-d), where nonquasi-static effects should be found negligible, the model behaves quasi-statically, thanks to the suitable definition of the strictly-intrinsic device, which provides an almost open-circuit in the pinched-off region.

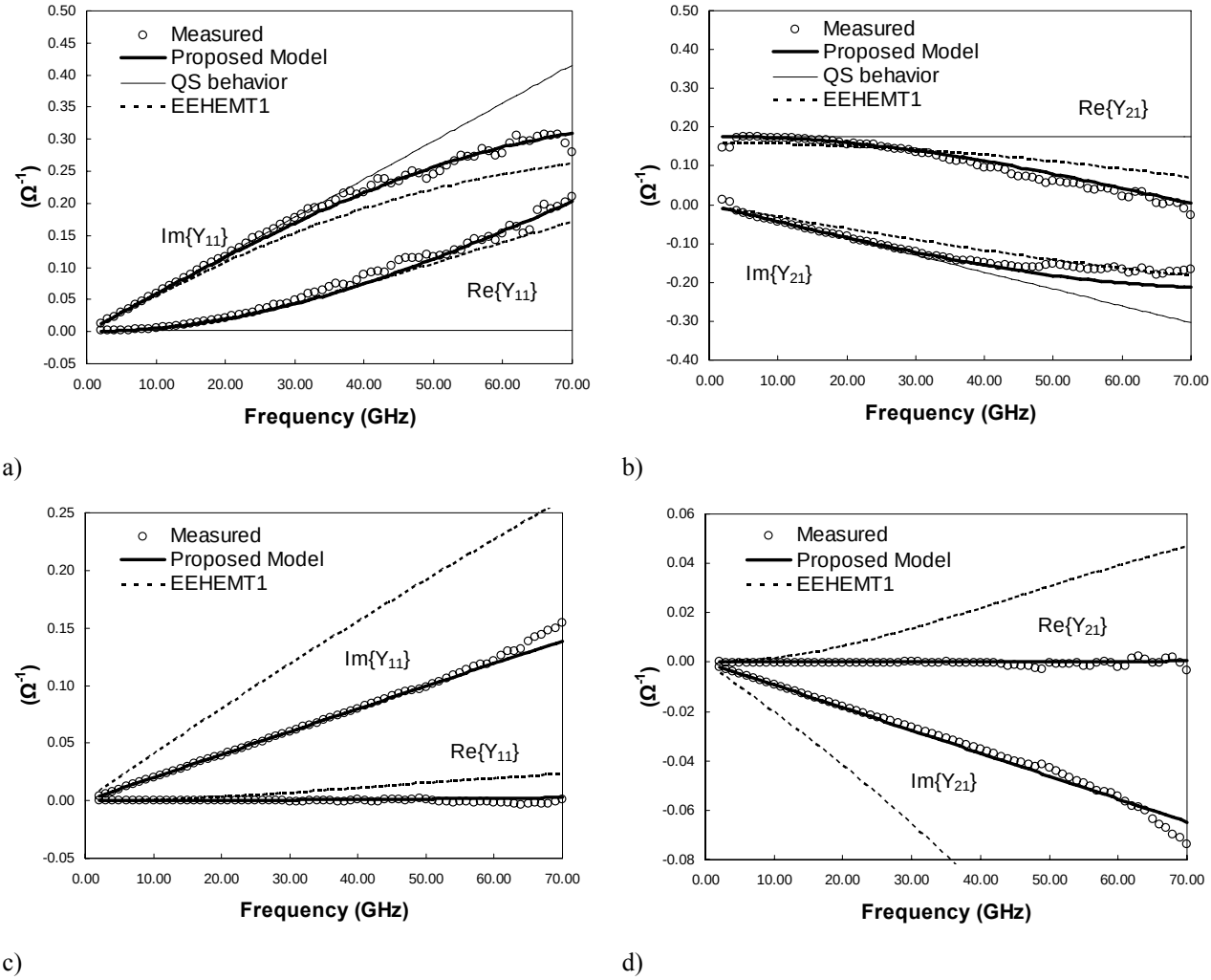
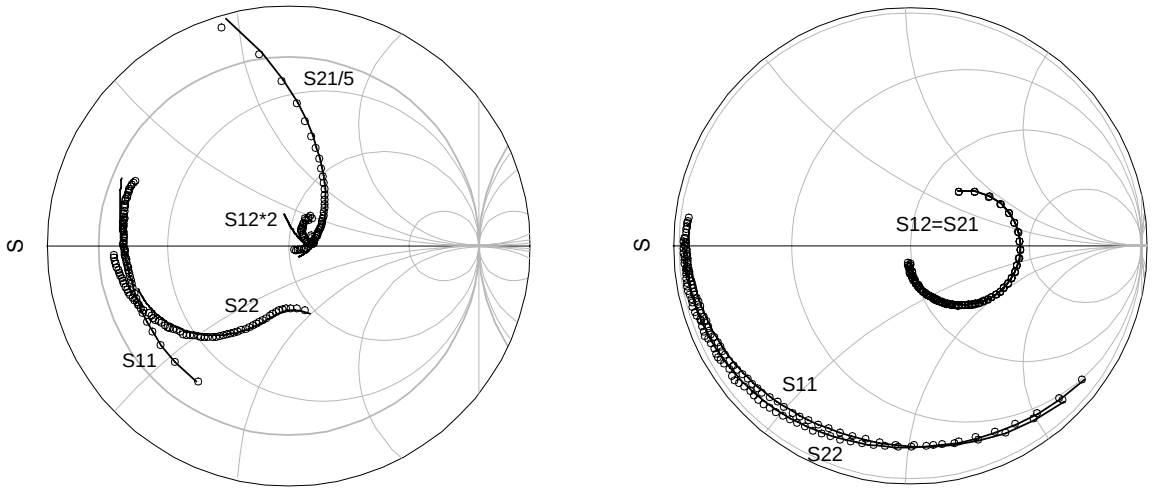


Fig. 3.5: Intrinsic admittance parameters Y_{11} and Y_{21} versus frequency of the 0.25 μm GaAs PHEMT: measurements (o), proposed nonquasi-static model (continuous line), EEHEMT1 model (dashed line). Ideal quasi-static behavior (thin continuous line) is also plotted for reference. Two different bias conditions are shown: V_{GS}=-0.75 V, V_{DS}=7.5 V (on-state, a, b), V_{GS}=-1.2 V, V_{DS}=0 V (off-state, c, d). Analogous results were obtained also for the Y_{12}, Y_{22} parameters and for different biases.

Conventional nonquasi-static approaches based on equivalent-circuits rarely provide such a good agreement both under off and on device conditions. For instance, an EEHEMT1 model [22] of the same PHEMT was extracted, by means of a commercial device characterization tool [23]. This model provides small-signal predictions with comparable accuracy in the proximity of the nominal bias as shown in Fig. 3.5-a and 3.5-b, but it becomes extremely inaccurate in the cold pinched-off FET condition shown in Fig. 3.5-c and 3.5-d.

Predicted and measured extrinsic S-parameters at the same bias conditions are shown in Fig.3.6.



a) b)

Fig. 3.6. Predictions based on the proposed model of extrinsic S-parameters (continuous line) compared with measured data (o) in on-state (a, V_{GS}=-0.75 V, V_{DS}=7.5 V) and off-state bias condition (b, V_{GS}=-1.2 V, V_{DS}=0 V).

Although the proposed model is very simple and can be characterized by only seven real scalar parameters, it provides good predictions also strongly varying the device bias, as it can be seen in Fig. 3.7, where, predicted intrinsic admittance parameters at the frequency of 40 GHz are compared with measurements at values of V_{GS} ranging from off-state to on-state condition. It can be noted that the voltage generators $\Delta V_{GS,c}$, $\Delta V_{GS,d}$ allow to accurately model the important bias-dependent deviations existing between the actual device response and the ideally quasi-static behaviour, also shown in the figure. Instead, limited multi-bias fitting capability is obtained with the EEHEMT1 model. Probably, this is not exclusively due to nonquasi-static phenomena, but also to the approximation in the $C_{GS}(V_{GS})$ nonlinear analytical expressions of the EEHEMT1 model (the functions used in the EEHEMT1 are similar to the expression of the equivalent-circuit models discussed in Sec. 2.1.1).

An important improvement is also obtained with respect to the previous equivalent-voltage model [17], where a unique correction was used for both conductive and displacement part: the comparison between the old and the new model version is reported in Fig 3.8.

The accuracy in multi-bias small-signal operation represents an important requirement for providing good predictions also under large signal validation tests. Measurements of third order intermodulation distortion (IMD) were carried out on the device at the frequency of 37 GHz and with a two tone displacement of 10 MHz: different load and source impedances were used, at different bias points. Simulation results were then compared with measured data, exhibiting great accuracy in every condition: two typical examples are provided in Fig. 3.9 where the third order IM product is plotted versus output power. Very good accuracy is also obtained with the EEHEMT1

model when biasing the device at the nominal bias point and with reasonably small signal amplitudes, while accuracy dramatically decreases at different biases.

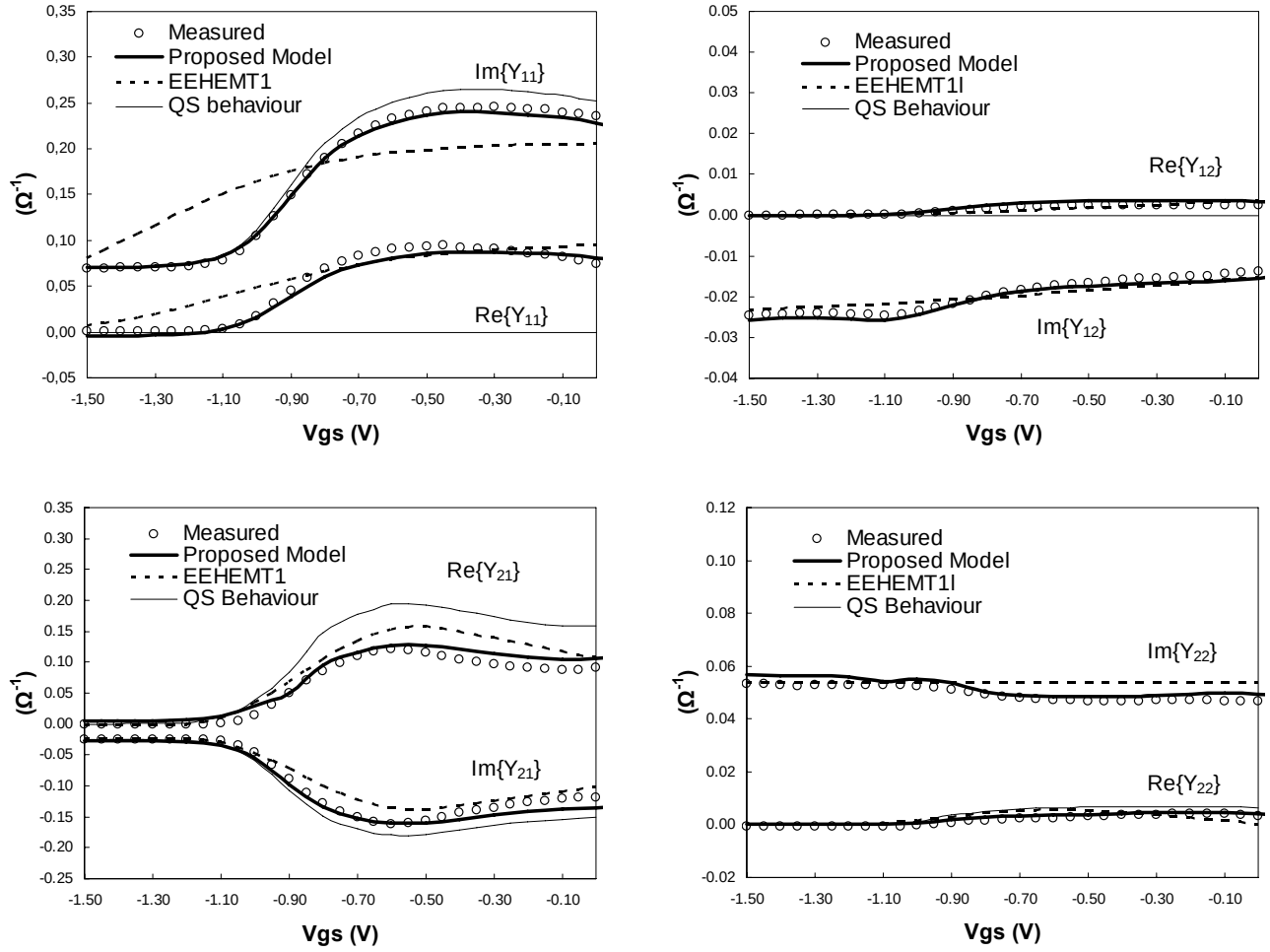


Fig. 3.7. Bias-dependent intrinsic admittance parameters versus the gate-source voltage at the frequency of 40 GHz: measurements (o), nonquasi-static model predictions (continuous line), EEHEMT1 predictions (dashed line), ideal quasi-static behavior (thin continuous line). The drain-source voltage is V_{DS}=6.5 V.

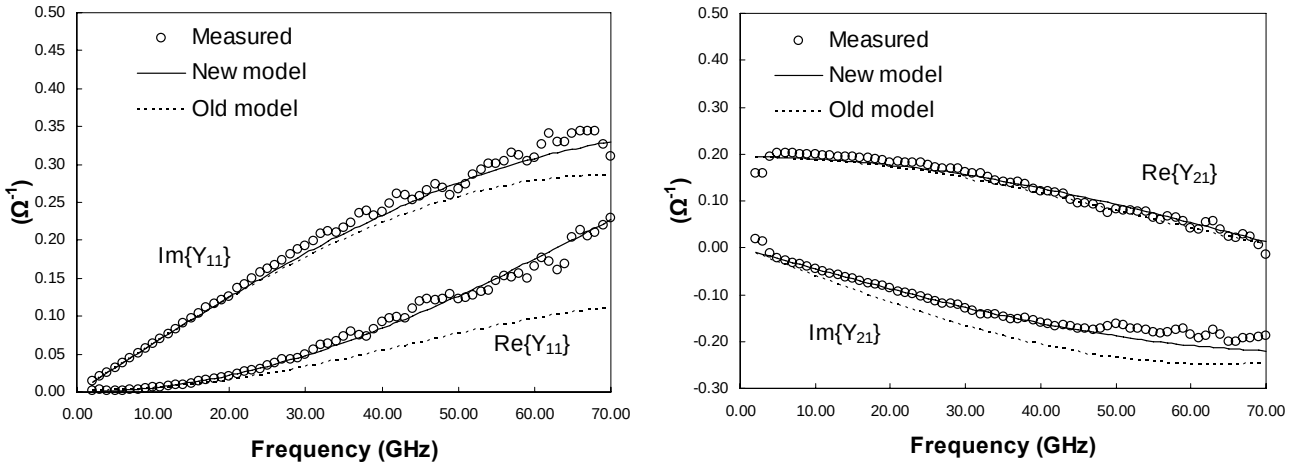
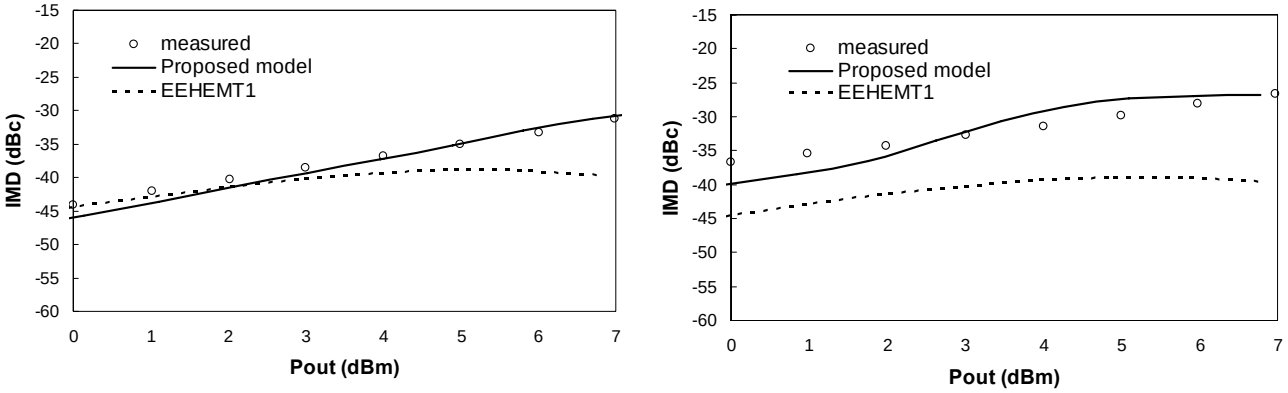


Fig. 3.8: : Intrinsic admittance parameters Y_{11} and Y_{21} versus frequency at V_{GS}=-0.55 V, V_{DS}=6.5 V: measurements (o), proposed nonquasi-static model (continuous line), old EV model version (dashed line).



a) b)

Fig.3.9. Third-order intermodulation product versus output power for the 0.25 μm GaAs PHEMT at 37GHz. (a): Bias I_D=60 mA, V_{DS}=6.5 V, Source Γ_S=(0,09∠-87°), Load Γ_L=(0,24∠-177°). (b): Bias I_D=15 mA, V_{DS}=5,5 V, Source Γ_S=(0,08∠-130°), Load Γ_L=(0,24∠-177°). Similar results were obtained also with different biases and termination impedances.

Finally, the prediction capability of the NQS-EV model is compared with that of a classic equivalent circuit model, readily available in the foundry libraries, and of a very accurate but more complex empirical model: the TriQuint's Own Model (TOM) [24] and the Nonlinear Discrete Convolution (NDC) model [12] discussed in Section 2.1.2. To this aim, the NDC model was identified for the same device: this model, based on the modified Volterra series approach described in Chapter 2, provides great accuracy, but its CAD implementation requires the use of several Symbolically Defined Device (SDD) components, which sensibly reduce the computational efficiency. This draw-back, however, could be avoided by implementing the NDC model in a User Compiled version. The NDC model was here implemented in its SDD version and in conjunction with the same low-frequency dispersion model [21], in order to guarantee a fair comparison with the EVM. In addition, the equivalent-circuit-based TOM [24], available in the foundry library and, thus, very often employed in MMIC design, was also used.

The three models were, initially, tested under small-signal operations, providing sufficiently good predictions: in Fig. 3.10 the predicted S parameters are compared with the measured ones, with frequency ranging from 4 GHz to 70 GHz, at V_{GS}= -0.55 V and V_{DS}= 6.5 V, corresponding to a class A large-signal operation bias for the device. In particular, while the three model predictions of the S_{11}, S_{12} and S_{22} parameters are quite similar, the predictions of the S_{21} parameter provided by the NDC and the NQS-EV models are slightly better than that provided by the TOM.

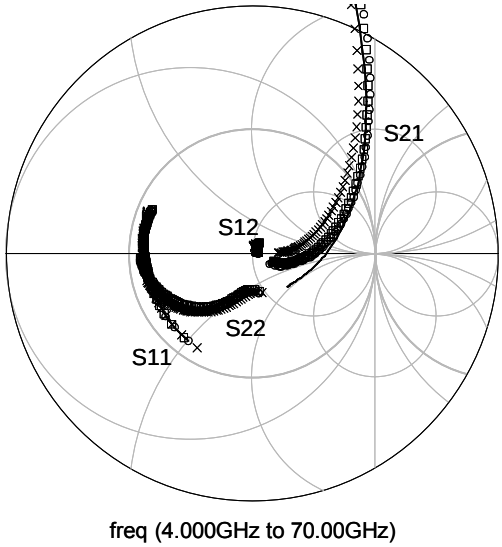


Fig. 3.10. Extrinsic S parameters corresponding to V_{GS}=-0.55V and V_{DS}=6.5V, at frequency ranging from 4 GHz to 70 GHz: measurements (o) compared with predictions of NQS-EV model (continuous line), NDC model (square) and foundry TOM (x).

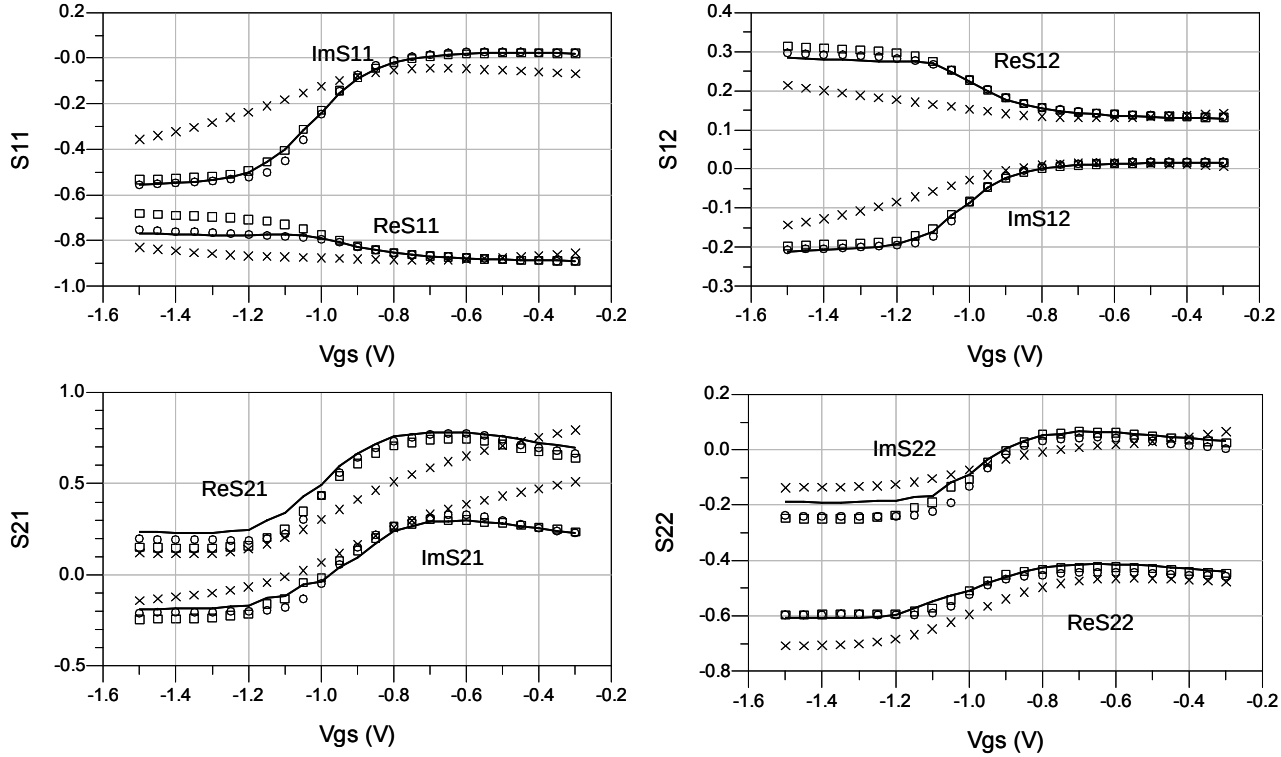


Fig. 3.11: Bias-dependent extrinsic scattering parameters, in real and imaginary part, versus the gate-source voltage at the frequency of 30 GHz: measurements (o) compared with predictions of NQS-EV model (continuous line), NDC model (square) and TOM (x). The drain-source voltage is V_{DS}= 6.5 V.

The NQS-EV model provides very accurate predictions of the extrinsic scattering parameters in a wide range of bias points: in Fig.3.11, at a frequency of 30 GHz, and with the gate-source voltage ranging from off-state to on-state condition for the device, NQS-EV predictions are compared with measurements and with the other two models, showing, for several bias conditions, a better

accuracy than the TOM and a general comparable quality with respect to the NDC model. Similar considerations can be drawn from Fig. 3.12, where, at the same frequency, the bias-dependent S parameters are plotted versus the drain-source voltage.

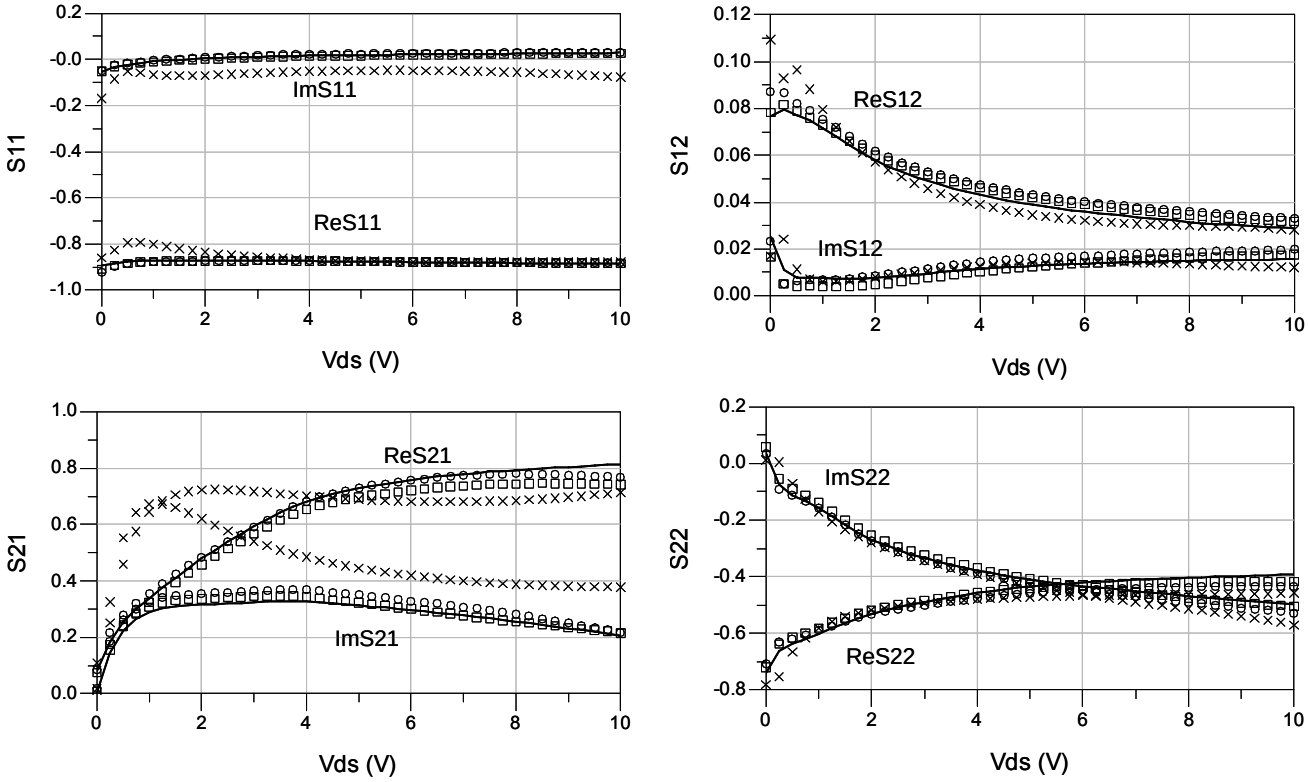
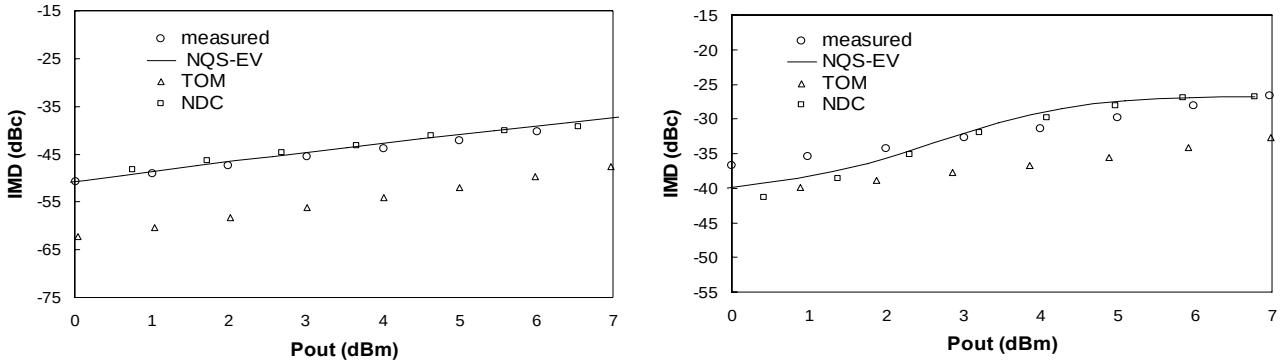


Fig. 3.12: Bias-dependent S parameters, in real and imaginary part, with the drain-source voltage ranging from 0 V to 10 V, at the frequency of 30 GHz: measurements (o), NQS-EV model (continuous line), NDC model (square) and TOM (x). The gate-source voltage is V_{GS}= -0.55 V.

The model prediction capabilities were, in addition, tested for intermodulation distortion: the results are plotted in Fig. 3.13. Two bias points were considered, corresponding to class A and class AB operation for the device, and different source and load impedances were used. Both the NQS-EV model and the NDC model provide very good performances, even if the first model is much simpler. On the contrary, the predictions provided by the TOM are quite inadequate: this is due to the worse multi-bias prediction capability, as previously shown, but probably also to a less adequate modelling of the low-frequency dispersive effects, as outlined in Section 1.2.1.

It is worth noting that the simple implementation of the NQS-EV model considerably reduces the computational time costs with respect to traditional black-box model based on SDD components: the NQS-EV model is, in fact, about fifty times faster in intermodulation analysis with respect to the NDC model implemented in the SDD version.



a) b)

Fig. 3.13: Third-order intermodulation product versus output power at 37 GHz, two tones displacement of 10 MHz. (a): Bias I_D=60 mA, V_{DS}=6.5 V, Source Γ_S = (0,09∠-87°), Load Γ_L = (0,56∠156°). (b): Bias I_D=15 mA, V_{DS}=5.5 V, Source Γ_S = (0,08∠-130°), Load Γ_L = (0,24∠-177°).

3.4 Conclusion

A simple, technology-independent, nonlinear modelling approach for microwave and millimetre wave applications has been described. The model takes into account nonquasi-static phenomena by means of suitable bias-independent voltage-controlled voltage-sources applied to an associated quasi-static device. The "nonquasi-static correction" can be associated to any nonlinear quasi-static model, in order to improve its predictive capability under high frequency operation. Quasi-static device models, either defined in the time- and frequency-domain, are suitable to be used in association with the proposed approach. The NQS-EV model is featured by a very simple identification procedure: the associated quasi-static device can be implemented by exploiting look-up-tables directly extracted from quasi-static measurements, while nonquasi-static phenomena are modelled by means of only six scalar parameters. These parameters can be identified in almost closed-form, avoiding nonlinear optimization procedures and related problems, such as convergence difficulty and dependence on initial condition. This is a great advantage on equivalent-circuit models: the circuit designer, in fact, can implement the NQS-EV model in commercial CAD tools, without great modelling knowledge and at very little time cost. In such a way, the designer can obtain much more accurate predictions than those provided by models available in foundry libraries and a comparable accuracy with, possibly, higher computational efficiency with respect to more elaborate behavioural models.

A large experimental validation has been reported in the chapter by considering a 0.25 μm GaAs PHEMT, in a wide range of frequencies, where nonquasi-static effects are important. Good predictive capabilities have been shown under both small- and large-signal operation and at different device bias conditions. Improved performance has been obtained with respect to more conventional, equivalent-circuit-based models.

It is worth noting that the NQS-EV model can be associated to any quasi-static model, both frequency- or time-domain oriented, and could be also applied to existing models in order to improve their prediction capabilities.

Finally, the simple and unambiguous identification procedure makes the proposed model a valuable tool and reduces the costs and effort required by the model development phase in MMIC design flow.

In the next chapter, the equivalent voltage approach will be applied to GaN-based device, in a double form: for modelling both nonquasi-static and dispersive effects.

Appendix A

The relationship between the two voltage deviations terms $\Delta\mathbf{v}_d$ and $\Delta\mathbf{v}_c$, defined in (3.10) and (3.13) respectively, is here investigated. To this aim, (3.14) is rewritten as:

$$\mathbf{i} = \mathbf{F}\left\{\hat{\mathbf{v}}_c\right\} + \frac{d\mathbf{q}^{NQS}}{dt} = \mathbf{F}\left\{\mathbf{v} + \Delta\mathbf{v}_c\right\} + \frac{d\boldsymbol{\Psi}\left\{\mathbf{v} + \Delta\mathbf{v}_d\right\}}{dt}. \tag{3.30}$$

Linearization of the nonquasi-static charge, under the hypothesis of small $\Delta\mathbf{v}_d(t)$ voltage variation, leads to:

$$\boldsymbol{\Psi}\left\{\mathbf{v}(t) + \Delta\mathbf{v}_d(t)\right\} \cong \boldsymbol{\Psi}\left\{\mathbf{v}(t)\right\} + \mathbf{C}\left\{\mathbf{v}(t)\right\} \cdot \Delta\mathbf{v}_d(t), \tag{3.31}$$

where:

$$\mathbf{C}\left\{\mathbf{v}(t)\right\} = \left.\frac{d\boldsymbol{\Psi}\left\{\hat{\mathbf{v}}_d(t)\right\}}{d\hat{\mathbf{v}}_d}\right|_{\hat{\mathbf{v}}_d = \mathbf{v}}. \tag{3.32}$$

By comparison with (3.9) we have:

$$\mathbf{C}\left\{\mathbf{v}(t)\right\} \cdot \Delta\mathbf{v}_d(t) \cong \Delta\mathbf{q}(t). \tag{3.33}$$

Moreover, linearization of the nonquasi-static conductive current, under the hypothesis of small $\Delta\mathbf{v}_c(t)$ voltage variation, leads to:

$$\mathbf{F}\left\{\mathbf{v}(t) + \Delta\mathbf{v}_c(t)\right\} \cong \mathbf{F}\left\{\mathbf{v}(t)\right\} + \mathbf{G}\left\{\mathbf{v}(t)\right\} \cdot \Delta\mathbf{v}_c(t), \tag{3.34}$$

where:

$$\mathbf{G}\left\{\mathbf{v}(t)\right\} = \left.\frac{d\mathbf{F}\left\{\hat{\mathbf{v}}_c(t)\right\}}{d\hat{\mathbf{v}}_c}\right|_{\hat{\mathbf{v}}_c=\mathbf{v}} \tag{3.35}$$

represents the voltage dependent, differential conductance matrix of the resistive part **F** of the associated quasi-static device.

On the other hand, by considering the conductive current as in (3.12), linearization with respect to $\Delta\mathbf{q}$, under the hypothesis of small charge perturbation, leads to:

$$\mathbf{\Phi}\left\{\mathbf{\Psi}\left\{\mathbf{v}(t)\right\} + \Delta\mathbf{q}(t), \mathbf{v}(t)\right\} \cong \mathbf{\Phi}\left\{\mathbf{\Psi}\left\{\mathbf{v}(t)\right\}, \mathbf{v}(t)\right\} + \Delta\mathbf{i}_c(t) = \mathbf{F}\left\{\mathbf{v}(t)\right\} + \Delta\mathbf{i}_c(t) \quad , \tag{3.36}$$

where $\Delta\mathbf{i}_c(t) \doteq \left[\Delta i_{c1}\ \Delta i_{c2}\right]^T$ are conductive current deviations satisfying:

$$\Delta\mathbf{i}_c(t) \doteq \left.\frac{\partial\mathbf{\Phi}\left\{\mathbf{q}^{NQS}(t), \mathbf{v}(t)\right\}}{\partial\mathbf{q}^{NQS}}\right|_{\mathbf{q}^{NQS}=\mathbf{q}} \cdot \Delta\mathbf{q}(t)\,. \tag{3.37}$$

By comparison with (3.34), we get:

$$\mathbf{G}\left\{\mathbf{v}(t)\right\} \cdot \Delta\mathbf{v}_c(t) = \Delta\mathbf{i}_c(t)\ . \tag{3.38}$$

or, by also taking into account (3.33):

$$\mathbf{G}\left\{\mathbf{v}(t)\right\} \cdot \Delta\mathbf{v}_c(t) = \left.\frac{\partial\mathbf{\Phi}\left\{\mathbf{q}^{NQS}(t), \mathbf{v}(t)\right\}}{\partial\mathbf{q}^{NQS}}\right|_{\mathbf{q}^{NQS}=\mathbf{q}} \cdot \mathbf{C}\left\{\mathbf{v}(t)\right\} \cdot \Delta\mathbf{v}_d(t)\,. \tag{3.39}$$

By adopting a common-source device configuration and considering electrical and geometrical symmetry properties of the device, (3.39) may be expressed by the scalar equations:

$$G_{s,11}\left\{\mathbf{v}^{(s)}\right\} \cdot \Delta v_{GS,c} = \left(\frac{\partial\Phi_{s,1}\left\{\mathbf{q}^{NQS}, \mathbf{v}^{(s)}\right\}}{\partial\Delta q_{GS}} C_{s,11}\left\{\mathbf{v}^{(s)}\right\} + \frac{\partial\Phi_{s,1}\left\{\mathbf{q}^{NQS}, \mathbf{v}^{(s)}\right\}}{\partial\Delta q_{DS}} C_{s,21}\left\{\mathbf{v}^{(s)}\right\}\right) \cdot \Delta v_{GS,d} \tag{3.40}$$

$$G_{s,21}\left\{\mathbf{v}^{(s)}\right\} \cdot \Delta v_{GS,c} = \left(\frac{\partial\Phi_{s,2}\left\{\mathbf{q}^{NQS}, \mathbf{v}^{(s)}\right\}}{\partial\Delta q_{GS}} C_{s,11}\left\{\mathbf{v}^{(s)}\right\} + \frac{\partial\Phi_{s,2}\left\{\mathbf{q}^{NQS}, \mathbf{v}^{(s)}\right\}}{\partial\Delta q_{DS}} C_{s,21}\left\{\mathbf{v}^{(s)}\right\}\right) \cdot \Delta v_{GS,d} \tag{3.41}$$

where (3.22) has been taken into account. In (3.40)-(3.41), we have: $\mathbf{v}^{(s)} \doteq \left[v_{GS}\, v_{DS} \right]^T$, $\mathbf{\Phi}_s(\cdot) \doteq \left[\Phi_{s,1}(\cdot)\, \Phi_{s,2}(\cdot) \right]^T$. $G_{s,ij}$, $C_{s,ij}$ (i, j = 1, 2) are the quasi-static, differential conductance and capacitance elements, respectively.

Both (3.40) and (3.41) describe a relationship between the two voltage deviations like:

$$\Delta v_{GS,c} = \rho \cdot \Delta v_{GS,d}\,, \tag{3.42}$$

where ρ is a scalar model coefficient defined either by (3.40) or (3.41).

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Chapter 4

Modelling of GaN-based Devices

GaN-based transistors feature higher breakdown voltage and higher operating temperatures than Si- and GaAs-based devices. These characteristics and the ability of growing epitaxial layers of GaN on different substrates, such as SiC and Si, are among the main reasons why this technology is nowadays considered as the most promising for high power and high efficiency amplifier design in the L, C and X bands. Great efforts are actually oriented towards this technology also by the European research community.

As it is well known, the design of monolithic integrated circuits at microwave frequencies always requires accurate device models [1]. This is especially true when dealing with GaN-based circuits, since important self-heating and trap states in the energy bands affect the low-frequency behaviour of this kind of devices [2]-[4]. In addition, by considering the increasing operating frequencies of many applications, the nonquasi-static effects related to charge-carriers delay (e.g. [5]-[8]) should be also accurately taken into account.

Existing GaN device models are typically based on standard S-parameter measurements and on dc or pulsed current characteristics (e.g. [7]-[8]). We proposed in [28] an empirical model for GaN-devices, based on the equivalent-voltage (EV) concept described in Chapter 3 ([9]-[10]) adopted for the very first time in a two-fold and innovative way to the description of the low-frequency dispersive phenomena and the high-frequency nonquasi-static effects. The GaN model is based on pulsed measurements of both drain current and S parameters, besides on conventional dc and CW differential parameters.

In Section 4.1, the model theory is described: in particular, the new low-frequency dispersion EV model is outlined in Section 4.1.1, while the nonquasi-static EV model is presented in 4.1.2. The proposed modelling approach is then applied to an AlGaN/GaN 8x50 μm PHEMT. Device characterization and model identification procedures are reported in 4.2 along with comments on practical model implementation into commercial CAD tools. Extensive experimental validation is provided at both multi-bias small-signal conditions up to 30 GHz and under large-signal operation in the framework of a 4-GHz power amplifier design for wireless applications.

4.1 The Equivalent-Voltage approach applied to GaN devices

The proposed model topology is plotted in Fig. 4.1. The model has been derived by doubly adopting an equivalent-voltage approach for taking into account both low-frequency dispersive phenomena, due to device self-heating and charge-trapping [9], and high-frequency nonquasi-static effects, related to charge-carriers delay in rearranging the channel status [10]. Thanks to this approach, the two-port device currents may be described by:

$$\mathbf{i}(t) = \mathbf{F}\left[\tilde{\mathbf{v}}_c(t)\right] + \mathbf{C}\left[\tilde{\mathbf{v}}_d(t)\right]\frac{d\tilde{\mathbf{v}}_d(t)}{dt}, \tag{4.1}$$

where **F** is a vector of purely algebraic nonlinear functions representing nondispersive I/V device characteristics, for instance gate and drain currents pulsed from a nominal quiescent condition[1], and **C** is a quasi-static capacitance matrix. The nonlinear functions in **F** and **C** are controlled by equivalent voltages $\tilde{\mathbf{v}}_c, \tilde{\mathbf{v}}_d$, related to the conductive and displacement branches of the model, respectively, as shown in Fig. 4.1. The equivalent voltages are defined as:

$$\tilde{\mathbf{v}}_c(t) \doteq \mathbf{v}(t) + \Delta\mathbf{v}_c(t) \tag{4.2}$$

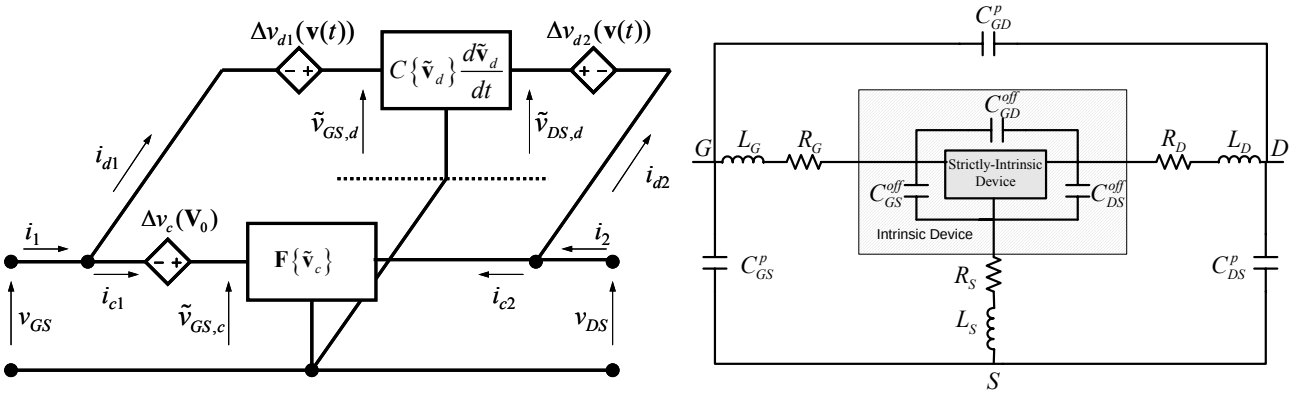
$$\tilde{\mathbf{v}}_d(t) \doteq \mathbf{v}(t) + \Delta\mathbf{v}_d(t) \tag{4.3}$$

where **v** are the actual applied voltages at the intrinsic device ports, while $\Delta\mathbf{v}_c$ and $\Delta\mathbf{v}_d$ are voltage deviation terms to be identified. These deviations account for both the long-term dynamics due to low-frequency dispersion and the short, yet finite, memory associated to nonquasi-static phenomena. Consistently with the EV approach, the desired modelling effect is obtained by modifying the controlling voltages of the conductive I/V and displacement C/V functions of a quasi-static nondispersive device model.

According to quite a commonly accepted assumption in the literature (e.g. [2]-[4]), low-frequency dispersive phenomena are here considered as affecting the conductive current only in the electron device. If present, dispersive effects on the displacement current are assumed to be negligible. On the other hand, nonquasi-static effects at high-frequencies are here neglected on the purely conductive device current, as also widely accepted by many authors (e.g. [5]-[6]). Since dynamic effects due to dispersive (long-term memory) and nonquasi-static phenomena (short-term memory) are associated to separate current contributions (conductive and displacement, respectively), each of

[1] Gate current is not usually affected by low-frequency dispersion [2], so that the first element of the **F** vector can be simply thought of as the static bias-dependent gate current characteristic.

the voltage deviations $\Delta\mathbf{v}_c$, $\Delta\mathbf{v}_d$ may be simply associated in our approach with the modelling of a single kind of dynamics. In particular, short memory nonquasi-static effects are taken into account here by considering voltage deviations $\Delta\mathbf{v}_d$ into the displacement part of the model, while long-memory dispersive effects are dealt with by $\Delta\mathbf{v}_c$ voltage deviations in the conductive branch.



(a) (b)

Fig. 4.1: Strictly-intrinsic (a) and complete (b) topology of the Equivalent-Voltage model for GaN-based devices.

4.1.1 Equivalent Voltages applied to Low-Frequency Device Modelling

Similarly to the equivalent-voltage modelling approach described in [9], the dependence of the I/V low-frequency characteristics on the quiescent condition is taken into account by means of a nondispersive intrinsic device controlled by modified voltages.

However, unlike the approach followed in [9], we propose here a much simpler choice. We adopt a particular pulsed drain current characteristic to describe the nondispersive device. This can be a good choice, especially when the chosen quiescent condition is a typical bias point of the actual application considered, such as, for instance, the class A/AB bias in a microwave power amplifier. Unfortunately, even in the theoretical case of a FET biased at particular gate-source and drain-source voltages through ideal bias networks (no self-biasing), the thermal device status changes due to self-heating during actual RF operation, especially when a strong nonlinear regime is considered. Corresponding drain current deviations must therefore be modelled. When self-biasing is also an issue, and/or the ability of choosing the best bias condition must be guaranteed to the designer, the dependence of the dynamic I/V characteristics on the actual quiescent condition must also be considered. Both corrections are here implemented.

To this aim, we propose to modify the reference characteristic, pulsed from the bias V_{GS0}^*, V_{DS0}^*, through a single Δv_c voltage deviation on the gate side, defined like:

$$\Delta v_c = B_1(V_{GS0} - V_{GS0}^*) + B_2(V_{DS0} - V_{DS0}^*) + D(P_0 - P_0^*) \tag{4.4}$$

which is assumed to be linear in practical applications. B_1, B_2 and D are bias-independent model parameters to be identified[2]. The term $B_1(V_{GS0} - V_{GS0}^*) + B_2(V_{DS0} - V_{DS0}^*)$ in (4.4) takes into account the dynamic drain current deviations due to charge trapping phenomena, depending on the actual quiescent condition V_{GS0}, V_{DS0}. Instead, the term $D(P_0 - P_0^*)$ accounts for thermal changes related to device self-heating. P_0 and P_0^* represent the average dissipated power in actual dynamic operation and in the reference quiescent condition, respectively.

Although a term similar to (4.4) could be applied on the drain side also, effective current corrections tend to be obtained through non-acceptably large voltage deviations due to relatively high output device conductance in the saturation region. Empirical evidence presented in 4.1.3 shows that the single correction on the gate side works properly.

4.1.2 Nonquasi-Static High-Frequency Modelling

Empirical modelling of the quasi-static displacement current contribution in electron devices is mostly accomplished by means of two approaches. In the first one, suitable charge-voltage nonlinear functions Q/V are evaluated by numerical integration of multi-bias differential parameters of the intrinsic device at sufficiently low-frequencies, where nonquasi-static phenomena are still negligible. Displacement current is then obtained by simple derivation of the charge-voltage relationships (e.g. [11]-[12]). This approach is physically consistent since it guarantees charge conservation [13]-[15], but problems may sometime arise due to non-exact integration capabilities of differential parameters leading to somehow inaccurate prediction of multi-bias small-signal parameters.

The second approach is, instead, simply based on the direct evaluation of capacitance-voltage relationships C/V from conventional multi-bias differential parameters of the intrinsic device (e.g. [16]-[18]). The displacement current is then obtained by simply adopting an expression like in (4.1). This method provides in general better accuracy in the prediction of the small-signal behaviour, but charge conservation is not necessarily guaranteed in the presence of capacitance terms depending on both gate-source and drain-source voltages [13]-[15].

The availability of pulsed RF differential measurements [19] offers nowadays interesting opportunities for experimenting new device models (e.g. [20]). Pulsed S parameters provides the

[2] In a more general modeling approach, the B_1, B_2 and D coefficients could be replaced by nonlinear algebraic functions depending on the instantaneous voltages of the intrinsic device.

important advantage of preserving the internal device temperature and the charge trapping status in the quiescent condition, making the device operating conditions much more similar to those in actual applications such as, for instance, in power amplifiers. This feature positively affects the device model extraction and makes theoretically equivalent the two above mentioned approaches to the description of the quasi-static displacement current. In fact, the nonlinear behaviour of the device functions Q/V, C/V obtained on the basis of pulsed S parameters is not altered by actual bias-conditions (corresponding to different thermal and trap status), as it happens when conventional small-signal CW measurements are used instead.

In this model, the bias-dependent capacitance matrix **C** was obtained directly from pulsed differential parameters after de-embedding from extrinsic parasitics.

As far as nonquasi-static phenomena modelling is concerned, an equivalent voltage approach is also adopted. According to (4.1), displacement current deviations due to nonquasi-static effects are modelled by means of the same quasi-static C/V relationships, described by the matrix **C**, after modification of the controlling voltages through voltage deviations $\mathbf{\Delta v}_d$, as also in Fig. 4.1. These voltage perturbation terms are here assumed linearly dependent on applied voltages as in Chapter 3. As it will be shown in the experimental Sec. 4.1.3, optimal predictions of the nonquasi-static device behaviour is obtained, with the GaN-based device considered, by applying voltage modifications at both the gate and drain intrinsic voltages, i.e.:

$$\Delta v_{d1} = \sum_{p=1}^{N_D} \left[a_{11,p} \cdot \left(v_{GS}(t - p\Delta\tau) - v_{GS}(t) \right) + a_{12,p} \cdot \left(v_{DS}(t - p\Delta\tau) - v_{DS}(t) \right) \right] \tag{4.5}$$

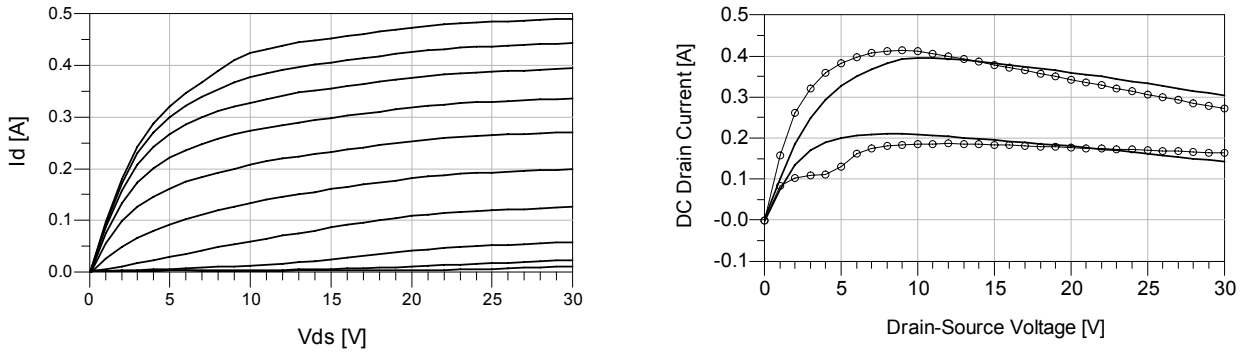
$$\Delta v_{d2} = \sum_{p=1}^{N_D} \left[a_{21,p} \cdot \left(v_{GS}(t - p\Delta\tau) - v_{GS}(t) \right) + a_{22,p} \cdot \left(v_{DS}(t - p\Delta\tau) - v_{DS}(t) \right) \right] , \tag{4.6}$$

where the $a_{ij,p}$ (with i, j=1,2 and p=1,..,N_D) are real, bias-independent model parameters to be identified [10]. The typical finite memory time T_M associated with nonquasi-static phenomena[3] is divided here into N_D elementary time slots $\Delta\tau$ (i.e. $T_M = N_D \Delta\tau$).

Due to limited upper frequency range extension of typical pulsed rf measurement systems we propose here to identify the model parameters $a_{ij,p}$ on the basis of linear best fit procedures of small-signal admittance parameters obtained from conventional CW differential measurements. In particular, model parameters $a_{ij,p}$ are easily obtainable as the solution of an over-determined linear system of equations imposing the model fitting on a high frequency range either based on a multi-

[3] Considerations discussed in [10] for the most appropriate choice of T_M and N_D parameters, may be still applied here.

or a single-bias procedure. This is partially justified by the linearity of the voltage deviations terms in (4.5)-(4.6) and empirically verified by experimental results presented in 4.1.3.



(a) (b)

Fig. 4.2: Reference pulsed I/V characteristic of the GaN-based PHEMT (a) from quiescent condition V_{GS0}=-5 V, V_{DS0}=20 V. Instantaneous voltages v_{GS} ranging from -9 to 0 V (step 1 V). Static drain currents at V_{GS}= -5 V and V_{GS}=0 V (b). Model (line) vs. measurement (circles).

4.1.3 Experimental Validation

The modelled samples were grown on 2-inch silicon carbide substrate by means of metal organic chemical vapour deposition. The epi-layers consist of (from the bottom) nucleation layer, 1.2-µm thick GaN buffer layer, 30-nm thick unintentionally doped AlGaN. The Al-content is 23%. The devices are obtained using Tiger standard AlGaN/GaN process.

Pulsed characterization of these devices are performed with specific pulsed equipment, which is described in [19]. For this study, a pulse duration of 500 ns is chosen, which is shorter than the time constant of most traps (observed in AlGaN) and the duty cycle is fixed to 10 µs. Static and high-frequency characterization of AlGaN/GaN HEMTs (W = 8x50 µm , L = 0.25 µm) is carried out on wafer. A maximum drain current density of 1.2 A/mm is observed at V_{GS} = 0 V and a threshold voltage of V_{th} = -8 V is obtained. The maximum transconductance g_m is about 230 mS/mm at V_{DS} = 10 V and V_{GS} = -6 V. An extrinsic current gain cut-off frequency (F_T) of 40 GHz and a maximum power gain cut-off frequency (F_{MAX}) of 80 GHz is achieved at V_{DS} = 12 V and V_{GS} = -6 V.

In order to identify the proposed Equivalent-Voltage model, the I/V characteristics and the S parameter measurements, both pulsed and CW, are preliminary de-embedded from the extrinsic parasitic network (see Fig. 4.1-b), which is identified by means of known cold-FET procedures [21] on the basis of pulsed differential parameters.

The measured drain current characteristic pulsed from $V_{10}^{*} = -5$ V , $V_{20}^{*} = 20$ V and shown in Fig. 4.2-a is chosen to model the nondispersive I/V device characteristic **F** in (4.1). The voltage deviation Δv_c in (4.4) is then identified, in closed form, as the solution of an over-determined linear

system of equations in the three unknowns B_1, B_2 and D: each equation is obtained by asking the Δv_c to provide the best fit of a quiescent drain current value in the corresponding V_{GS0}, V_{DS0} voltage pair. In this work, the minimum of three significant quiescent conditions are chosen. In particular, the three points are: (V_{GS0} = -5 V, V_{DS0} = 10 V), (V_{GS0} = 0 V, V_{DS0} = 10 V), (V_{GS0} = 0 V, V_{DS0} = 20 V). The values obtained for the low-frequency model parameters are: B_1=-0.19, B_2=-0.05 and D=-0.36.

The low-frequency model obtained is easily implemented into a commercial CAD tool by means of a look-up-table approach for the I/V characteristic **F**, where the controlling gate voltage is modified by the Δv_c deviation according to (4.2), (4.4). Average values V_{GS0}, V_{DS0} and P_0 are obtained through single-pole low-pass filters with frequency cut-off consistent with dispersion dynamics.

Predictions of the static output characteristics for a couple of V_{GS} values, chosen where self-heating effect is important, are compared with measurements in Fig. 4.2-b, showing a fairly good agreement in the voltage range of interest for typical application in power amplifiers. It is worth noting that this result is not obvious at all. It is mainly due to the ability of the voltage deviation Δv_c in (4.4) of appropriately modifying the gate controlling voltage of the reference pulsed I/V characteristic at each bias condition. Typical kink effects observed in measured static I/V characteristics, but not usually present in pulsed I/V curves, are obviously not modelled here. However, this is in our opinion not a major problem, since kinks occur in bias regions normally quite far from quiescent conditions in class-A/AB power amplifier design.

As far as the displacement current modelling is concerned, the quasi-static capacitance matrix **C** is obtained from pulsed measured differential parameters (V_{GS0}=-5 V, V_{DS0}=20 V) in a frequency range where nonquasi-static effects are still negligible over an instantaneous voltage grid: -9 V < v_{GS} < 1 V and 0 V < v_{DS} < 30 V.

Displacement current deviations due to nonquasi-static effects are then modelled by means of the $\mathbf{\Delta v}_d$ corrections as in Fig. 4.1-a. According to the approach described in [10], the small-signal device behaviour in off-state conditions (V_{GS}=-9 V, V_{DS}=0 V in the present work) is first modelled through a Π-network of linear capacitances and their values are de-embedded from the capacitance matrix **C.** The voltage deviations $\mathbf{\Delta v}_d$ are thus applied to the resulting *strictly intrinsic device* (see the complete device model in Fig. 4.1-b).

As discussed in 4.1.2, conventional CW S parameters are exploited in order to extract the voltage deviations $\mathbf{\Delta v}_d$ in (4.5), (4.6) on a large frequency range where nonquasi-static effects are important. In particular, measurements up to 30 GHz are used here. A memory time T_M = 4.5 ps,

divided into 3 time slot $\Delta\tau$, is chosen, and the model parameters $\mathbf{a}_p$ (p=1,…,3) are identified by means of a linear optimization procedure, based on the best fit between predictions and measurements in the nominal bias point V_{GS0}=-5 V, V_{DS0}=20 V. The intrinsic admittance parameters are compared in Fig. 4.3 with measured data, with the frequency ranging from 250 MHz to 30 GHz. Very good fitting of nonquasi-static effects is achieved thanks to the equivalent voltage approach adopted.

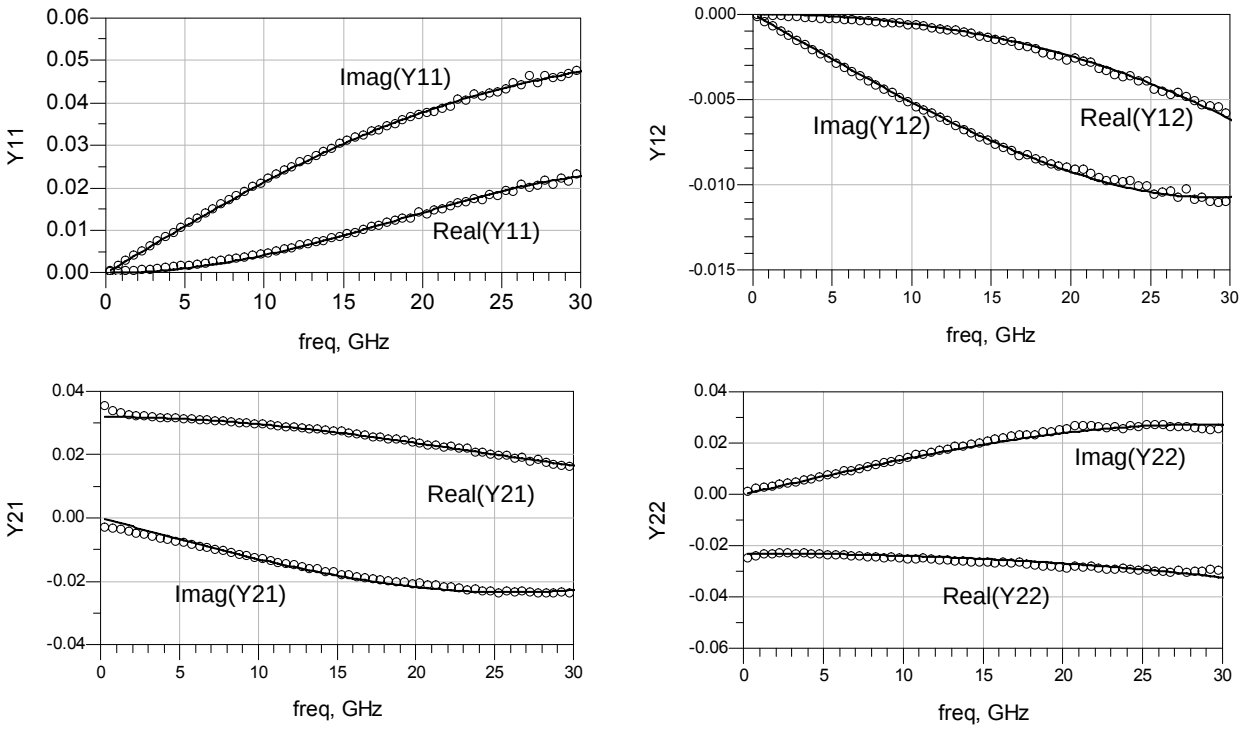
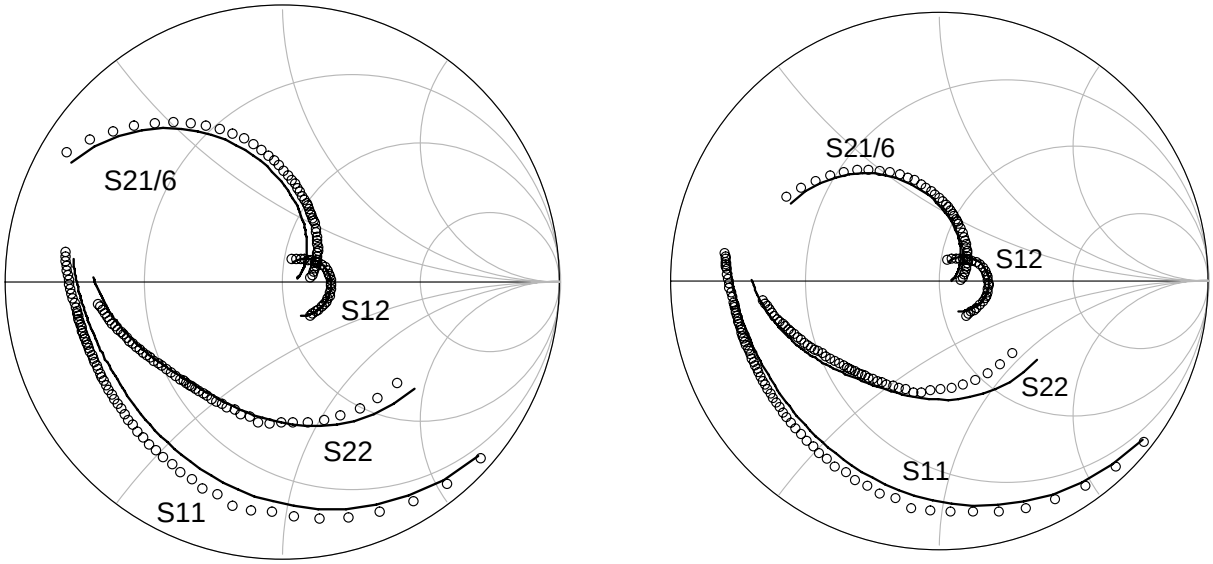


Fig. 4.3: Intrinsic admittances of the GaN-based PHEMT extracted from the measured CW S parameters (circles) in V_{GS}=-5 V and V_{DS}=20 V. The corresponding model fitting (line) is very good up to the highest frequency.



(a) (b)

Fig. 4.4: Predicted (line) and measured (circles) extrinsic S parameters of the GaN-based PHEMT *pulsed* from V_{GS0}= -5 V, V_{DS0}= 20 V. Instantaneous voltages: v_{GS}= -5 V, v_{DS}= 17 V (a) and v_{GS}= -3 V, v_{DS}= 10 V (b); the frequency sweeps between 1 GHz and 20 GHz.

The extracted voltage deviations $\Delta \mathbf{v}_d$ are then plugged into the device model shown in Fig. 4.1-a/b in the framework of the CAD tool. A look-up-table approach is also used for the implementation of the matrix **C**, while the voltage deviations $\Delta \mathbf{v}_d$ are implemented by means of voltage-controlled voltage-sources [10] on the gate and drain displacement branches.

The extrinsic frequency-dependent S parameters at different instantaneous voltages reached by pulsing from the quiescent condition V_{GS0} = -5 V, V_{DS0} = 20 V are plotted in Fig 4.4. Good agreement with measured data shows that the model is capable of good predictions in instantaneous voltage conditions both near and far the quiescent point. The slight disagreement at the lowest frequencies are due to little discrepancies observed between the transconductance extracted from pulsed I/V curves and from pulsed S parameters, as already reported by other authors, for instance in [22]. In addition, predicted pulsed S parameters versus v_{DS} at 4 GHz are compared in Fig. 4.5 with measurements in v_{GS}=-5 V, showing also a good multi-bias prediction capability.

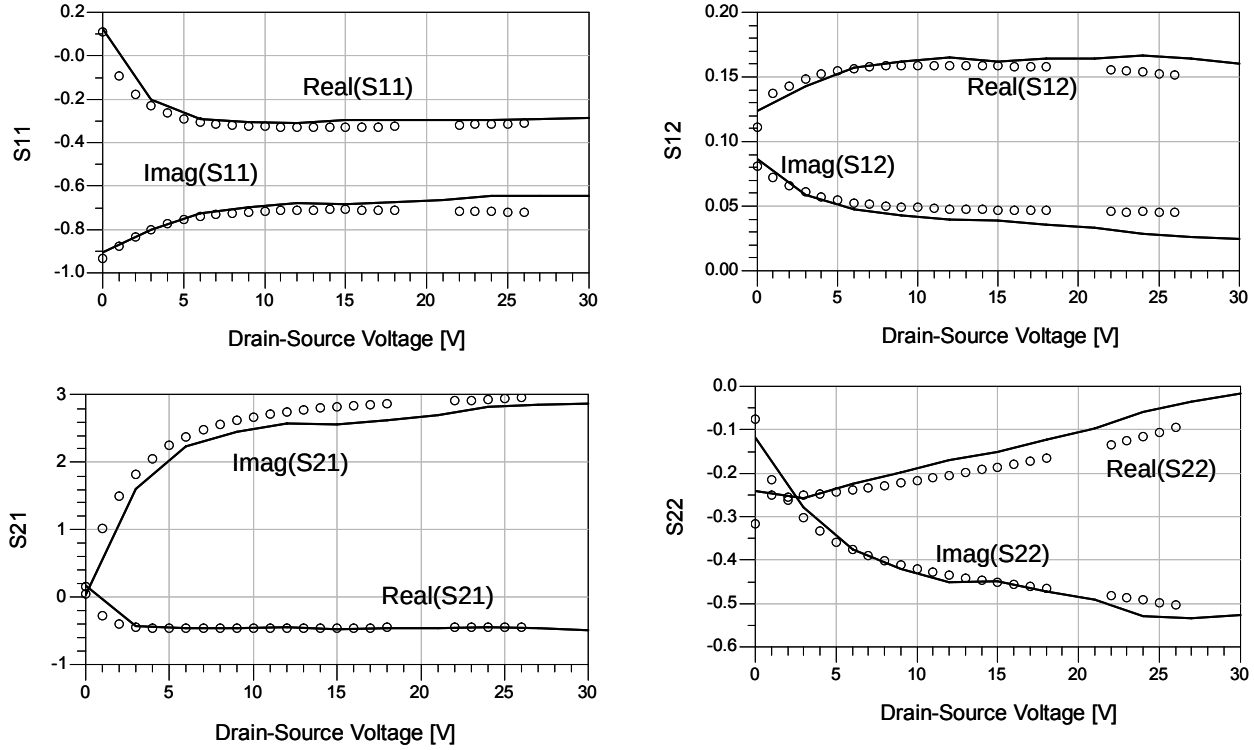
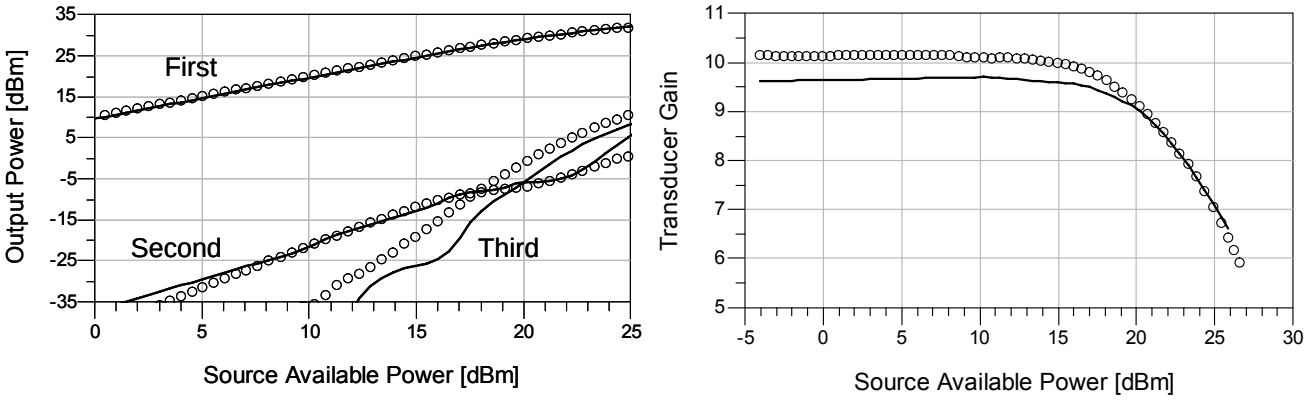


Fig. 4.5: S parameters of the GaN-based PHEMT at 4 GHz *pulsed* from V_{GS0}=-5 V, V_{DS0}=20 V. Instantaneous values of v_{DS} between 0 V and 30 V are dynamically reached (v_{GS}= V_{GS0}=-5 V). Predictions (line) are fairly close to measurements (circle).

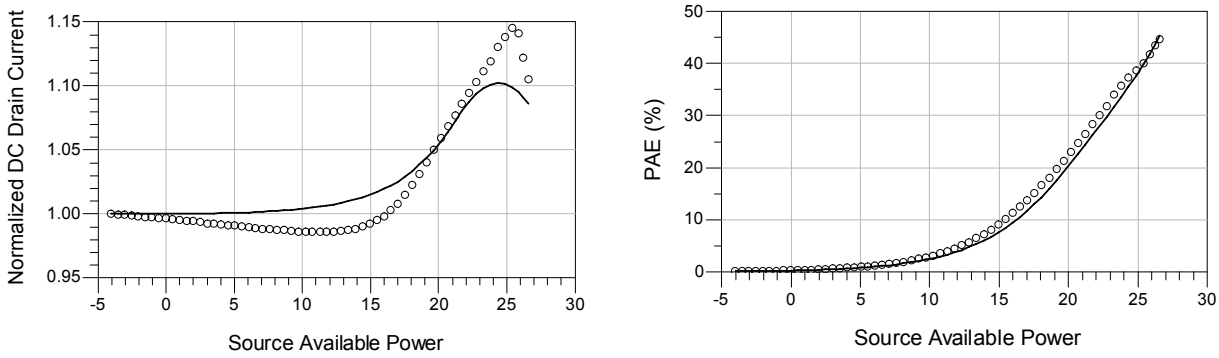
The proposed model is eventually validated under large-signal conditions in the framework of the design of a power amplifier for typical wireless applications. The device is biased in V_{GS0}=-5 V, V_{DS0}=20 V (class-A operation), and operated at the frequency of 4 GHz. Validation tests are carried out with a 50-Ω rf power source and with a load termination Γ_L=0.31∠89.6°. First, second and third harmonics of the predicted output power are compared with measurements in Fig. 4.6-a, showing a

very good agreement up to strongly saturated conditions. The transducer gain is also plotted in Fig. 4.6-b. Thanks to the low-frequency EV model, which takes into account thermal deviations due to device self-heating, a good prediction is achieved for the dc component of the drain current and the Power Added Efficiency, as outlined in Fig. 4.7 and as expected from the fairy good prediction of the static I/V characteristic in the region of interest (see Fig. 4.2-b).



(a) (b)

Fig. 4.6: Harmonic distortion test of a single-stage power amplifier based on the GaN PHEMT (V_{GS0}=-5 V, V_{DS0}=20 V, f_0= 4 GHz, Γ_S=0, Γ_L=0.31∠89.6°). Model (line) vs. measurement (circle).



(a) (b)

Fig. 4.7: Normalized dc drain current in the harmonic distortion test (a). Power Added Efficiency (b). Model (line) vs. measurement (circle).

4.2 Accurate Drain Current Prediction

In microwave power amplifiers the accurate prediction of the dynamic drain current dependence on signal amplitude and, in particular, of its DC component (i.e. AC to DC conversion), is extremely important since it is strictly related with the estimation of other critical quantities, such as Power Added Efficiency, dissipated power, associated internal device temperature and, consequently, circuit reliability.

Unfortunately, the good prediction of this parameter is not always easy to obtain with conventional dispersive models. In many modelling approaches dispersive phenomena are taken into account (e.g. [2]-[3],[27]-[28]) by simply using, in the drain current equivalent source identification, pulsed ([19],[25]), instead of purely static, I/V characteristics. These approaches implicitly assume that, in large signal operation at microwave frequencies, both the temperature and the charge trapping state are nearly constant and only depend on the selected quiescent/bias condition (i. e. DC voltage values), analogously to what happens in the case of short-duration, voltage-pulsed measurements. However, it should not be forgotten that the time-invariant internal temperature and trap filling status in strongly non-linear amplifier operation, where large rms values of the voltage AC components are involved, can be quite different from the case of short-duration, short-duty-cycle pulse operation, where the rms values of AC voltage components are clearly negligible. Thus, simple replacement of static I/V characteristics with pulsed ones may lead to fairly good performance predictions for power amplifiers only when considering a mild nonlinear regime. However, when more accurate modelling is needed and strongly non-linear operation is involved, suitable corrections must be introduced to account for the differences, in the internal device temperature and trap-filling status, between the pulsed measurements and the actual large-signal amplifier operating conditions. To this aim, not only self-heating but also trap-filling status dependence on AC voltage components must be taken into account.

Improvements have been obtained by involving only a thermal correction applied to the pulsed I/V characteristics of a GaN-based HEMT by means of the equivalent voltage approach [28], as shown in Fig. 4.7, but such a correction is not sufficient to provide accurate prediction of the average drain current.

Thus, an important model improvement is proposed in the following. This is based on the assumption, introduced here for the very first time, that the observed deviations in the dynamic drain current due to the dispersive phenomena are not only dependent on the specific quiescent voltage conditions, or, nearly equivalently, on the DC components, (as it is commonly believed, e.g. [2]-[3],[27]-[28]), but also on the whole AC waveform of the gate and drain voltages. A theoretically explanation is provided in this section along with the appropriate model development. Experimental model validation, based on a medium-power AlGaN-GaN HEMT, is also presented in this section. To this aim, the new low-frequency dynamic drain current source is here associated with the Equivalent Voltage model for GaN devices, identified on the basis of multi-bias pulsed S-parameters and already described and validated in the previous section: accurate predictions of all the critical PA characteristics at different loading conditions are experimentally verified.

We focus on the modelling of the drain current of the intrinsic FET under low-frequency dynamic operation, i.e. when the contribution of the displacement current component may be considered as negligible. As already said, the drain current is strongly affected by dispersive phenomena. These can be generally described in terms of a current dependence on a vector $\underline{x}$ of state variables, associated with the instantaneous internal charge trapping state, and on a variable ϑ, corresponding to the instantaneous channel temperature. However, the instantaneous values of $\underline{x}$ and ϑ are replaced with their mean values $\underline{X}_0$ and ϑ_0, when the involved signal spectral components lay well-above the upper cut-off frequency of dispersive phenomena (typically in the order of MHz), i.e:

$$i_D = F[v_G, v_D, \underline{X}_0, \vartheta_0]. \tag{4.7}$$

Conventional modelling approaches (e.g. [28]) are based on the assumption that $\underline{X}_0$ and ϑ_0 are only functionally dependent on the mean values of the applied voltages V_{G0}, V_{D0} (i.e.: $\underline{X}_0 = \underline{H}_x[V_{G0}, V_{D0}]$) and on the mean dissipated power P_0 (i.e. $\vartheta_0 = H_\vartheta[P_0]$), respectively. This intuitively suggests that a direct identification of (4.7) can be obtained through a pulsed I/V characterization, corresponding to selected quiescent voltage condition V_G^*, V_D^* (and $P^* = V_D^* \cdot F_{DC}[V_G^*, V_D^*]$, F_{DC} being the static I/V characteristics). This can be chosen, for instance, as coincident with the bias of the actual power amplifier under investigation. Thus, the drain current is often simply modelled by means of:

$$i_D = F_p[v_G, v_D] = F[v_G, v_D, \underline{X}^*, \vartheta^*]. \tag{4.8}$$

where $\underline{X}^* = \underline{H}_x(V_G^*, V_D^*)$ and $\vartheta^* = H_\vartheta(P^*)$.

However, even in the theoretical case of a FET biased through ideal bias networks imposing the selected bias voltages, also the internal device temperature variations, due to changes in self-heating under the actual amplifier operation, should be taken into account for a more accurate drain current prediction. To this aim, we consider here the only thermal part of the low-frequency model described in 4.1. The pulsed characteristic (4.8) is left unchanged, but it is controlled by an *equivalent gate voltage* $\tilde{v}_G$ obtained from the applied gate voltage v_G through a suitable voltage deviation Δv_G, i.e.:

$$i_D = F_p[\tilde{v}_G, v_D], \tag{4.9}$$

where $\tilde{v}_G = v_G + \Delta v_G$. The model is accordingly sketched in Fig. 4.8. We consider here the simple self-heating correction:

$$\Delta v_G = k_P \cdot \left(P_0 - P^*\right) \tag{4.10}$$

where k_P is a scalar coefficient to be identified.

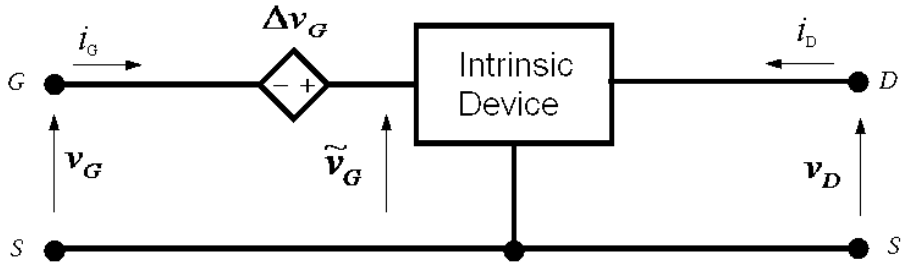


Fig. 4.8. Intrinsic device model schematic based on the Equivalent Voltage approach.

Models based on equations like (4.8) for the I/V characteristics usually can provide acceptable accuracy on output power and gain, especially when mild nonlinearities are involved. However, average drain current and power consumption accuracy may become poor with stronger nonlinearity (i.e. AC/DC conversion) in large-signal amplifier operation. Improvements can be obtained by suitably identifying the k_P coefficient in models based on (4.9)-(4.10), but results can be still not fully satisfactory, as shown in Fig. 4.9, where the average drain current predictions, obtained by means of models based on (4.8) or (4.9)-(4.10), are compared with measurements for two different load impedances. The two drain current models were extracted for an AlGaN-GaN PHEMT. The displacement currents were predicted by using the nonquasi-static electron device model and the identification procedures described in [10] and [28]; an optimal value for $k_P = -0.36$ was obtained, starting from a measured I/V characteristic pulsed from $V_G^* = -5$ V and $V_D^* = 20$ V.

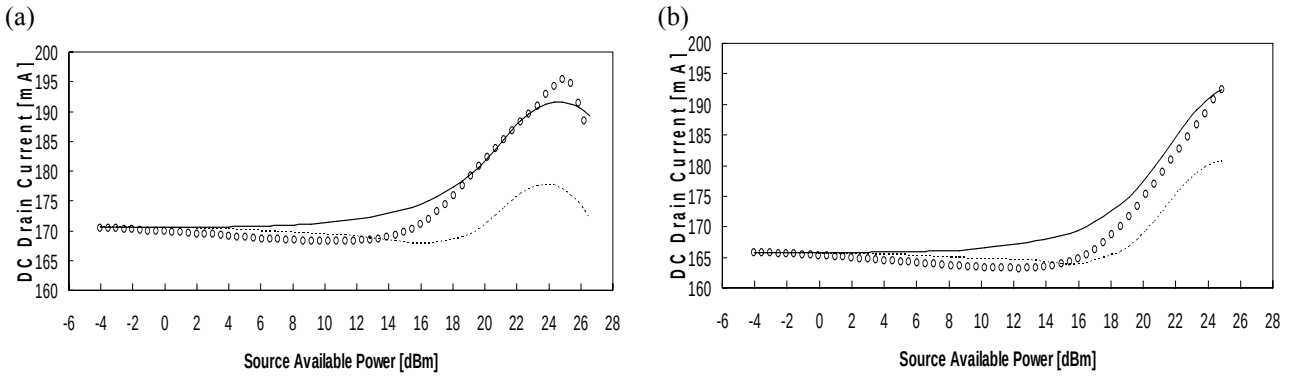


Fig. 4.9. Average drain current for ΓS=0 and two load impedances: ΓL=0.31∠89.6° (a) and ΓL=0.19∠68.8° (b). Measured (circles) versus prediction obtained with the model based on (2) (dashed line) and the one based on (3)-(4) (continuous line)

The results presented in Fig. 4.9 show that the simple correction due only to self-heating effects, introduced by (4.10) into the pulsed drain current characteristic (4.9), appears to be beneficial, yet not fully satisfactory. This suggests that also an additional correction term, related to different values of the trap-filling state, possibly due to the difference between the relatively large rms value of the AC voltage components in power amplifier operation in comparison with the nearly zero value in low-duty-cycle, pulsed operation, should be considered in (4.10). Thus, we start from the assumption that the state variables associated with charge trapping phenomena do not only depend on the bias/DC values of the gate and drain voltages but, instead, on the whole spectrum of the voltage waveforms. More precisely, by considering that the voltage waveforms normally considered in circuit analysis can be adequately described by a set of discrete spectral components, represented by a set of complex voltage phasors V_{Gp}, V_{Dp} corresponding to a generalized Fourier representation of the gate and drain voltage waveforms at the angular frequencies $\omega_p = p \cdot 2\pi/T$ (p=1,2,…), we assume that state variables $\underline{X}_0$ can be expressed in the form

$$\underline{X}_0 = \underline{H}_x \left[V_{G0}, V_{D0}, V_{G1}, V_{D1}, V_{G2}, V_{D2}, \ldots \right]. \tag{4.11}$$

This equation, which provides a generalized description of the dependence of the trap-filling state variables on the intrinsic device voltage waveforms, would be clearly quite difficult to use for empirical model identification, owing to the very wide space of independent variables considered. However, in order to make the model simple enough, the functional dependence in (4.11) can be practically limited to the first order harmonics. This simplification can be intuitively and empirically justified by considering that the capacitive part of the intrinsic device has a low-pass filtering effect on the intrinsic voltage waveforms, so that first harmonics can be in many cases considered, with acceptable loss of accuracy, as the dominating voltage spectral components. Thus,

by assuming without loss of generality $Im\{V_{G1}\}$=0 (in a time invariant system a phase can always be arbitrarily chosen), equation (4.11) becomes:

$$\underline{X}_0 = \underline{H}_x\left[V_{G0}, V_{D0}, Re\{V_{G1}\}, Re\{V_{D1}\}, Im\{V_{D1}\}\right]. \tag{4.12}$$

Moreover, to make both model identification ad implementation easier, a simple variable transformation can be adopted in terms of second order moments of the gate and drain AC voltage waveforms $v_{G,a} = v_G - V_{G0}$ and $v_{D,a} = v_D - V_{D0}$:

$$\overline{v_{G,a}^2} = \frac{1}{T}\int_{-T/2}^{+T/2} v_{G,a}^2(t)\cdot dt \ , \qquad \overline{v_{D,a}^2} = \frac{1}{T}\int_{-T/2}^{+T/2} v_{D,a}^2(t)\cdot dt \tag{4.13}$$

and:

$$\overline{v_{G,a}v_{D,a}} = \frac{1}{T}\int_{-T/2}^{+T/2} v_{G,a}(t)v_{D,a}(t)\cdot dt \ , \tag{4.14}$$

which are related to the first order voltage harmonics by:

$$\begin{aligned}
&\overline{v_{G,a}^2} \simeq \left(Re\{V_{G1}\}\right)^2 \Big/ 2 \\
&\overline{v_{D,a}^2} \simeq \left(\left(Re\{V_{D1}\}\right)^2 + \left(Im\{V_{D1}\}\right)^2\right) \Big/ 2 \\
&\overline{v_{G,a}v_{D,a}} \simeq \left(Re\{V_{G1}\}\cdot Re\{V_{D1}\}\right) \Big/ 2.
\end{aligned} \tag{4.15}$$

These equations show how the first order voltage harmonics can be easily computed in terms of the above defined second order moments; thus equation (4.12) can take the equivalent form:

$$\underline{X}_0 = \underline{H}_x\left[V_{G0}, V_{D0}, \overline{v_{G,a}^2}, \overline{v_{D,a}^2}, \overline{v_{G,a}v_{D,a}}\right]. \tag{4.16}$$

Finally, by still adopting the Equivalent Voltage Modelling approach and assuming a linear dependence of the voltage correction Δv_G on the second order moments of the voltages, we obtain the new equivalent voltage model equation:

$$\Delta v_G = k_P\cdot\left(P_0 - P^*\right) + k_{GG}\cdot\overline{v_{G,a}^2} + k_{DD}\cdot\overline{v_{D,a}^2} + k_{GD}\cdot\overline{v_{G,a}v_{D,a}} \tag{4.17}$$

where k_P accounts for the device self-heating, like in (4.9), and k_{GG}, k_{DD} and k_{GD} account for the dependence on the nonlinear dynamics of the charge-trapping. These are scalar model parameters to be identified.

It is worth noting that the voltage correction term (4.17) vanishes in small-signal conditions, but also under pulsed regime: in fact, in both cases P_0 is almost constant and the second order moments are negligible. This explains why the only pulsed measurements do not allow a full characterization of the dispersive effects on the device behaviour.

Theoretical considerations and empirical evidence show that the voltage correction (4.17) has a considerable impact on the average drain currents, but more limited effects on RF output power and gain prediction. For this reason, model identification can be carried out by simply fitting the average drain current measured for a set of different input power values and loading conditions, either at relatively low or high operating frequencies.

The model (4.17) was here extracted for the same AlGaN-GaN PHEMT of 4.1 and used again in conjunction with the nonquasi-static EV model. Four sets of load-pull measurements, corresponding to four different load impedances, were here considered for the identification, leading to an over-determined system of equations whose closed-form resolution resulted in $k_P = 0.375$, $k_{GG} = -0.048$, $k_{DD} = -0.002$ and $k_{GD} = -0.044$.

The equivalent voltage model equation (4.17) was implemented into the Agilent ADS CAD tool, by using the Symbolically Defined Device (SDD) facility for the direct implementation of the product operators needed, according to (4.13) and (4.14), for the computation of the second order moments of the gate and drain voltages and of the dissipated power; the associated averaging operators were approximated by simple, RC-like low-pass filters. Thus, the voltage correction (4.17) has been directly applied to the gate port of an SDD which implements, through a look-up-table containing the measured values of the pulsed I/V characteristic chosen as reference, the drain current source.

The overall good agreement shown in Figg. 4.10, 4.11 and 4.12 between measured and predicted average drain current, output power, gain and PAE confirms the validity of the gate voltage correction (4.17) for the modelling of dispersive effects.

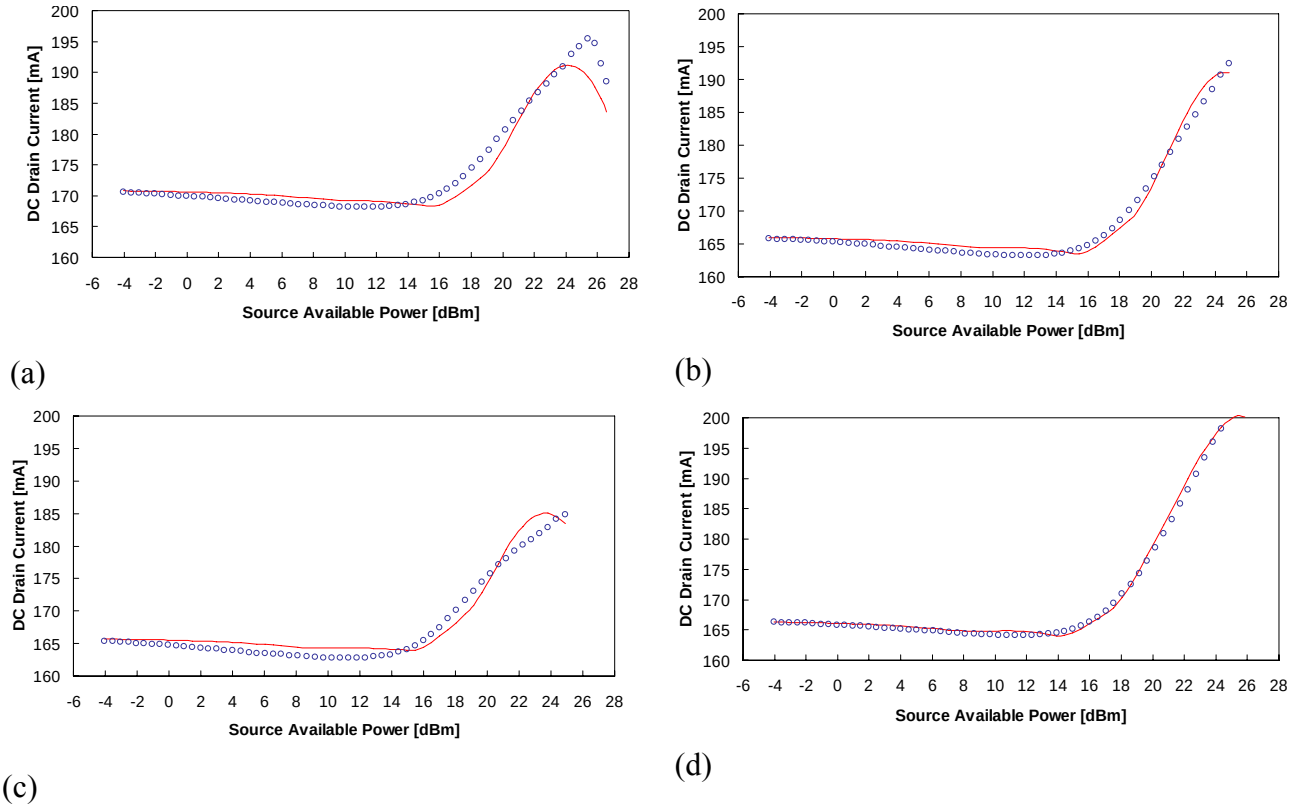


Fig. 4.10. New model predictions (line) versus measurements (circles) of average dc current for Γ_S=0 and four different load impedances. (a): Γ_L=0.31∠89.6°; (b): Γ_L=0.19∠68.8°; (c): Γ_L=0.43∠93.1°; (d): Γ_L=0.26∠142.8°.

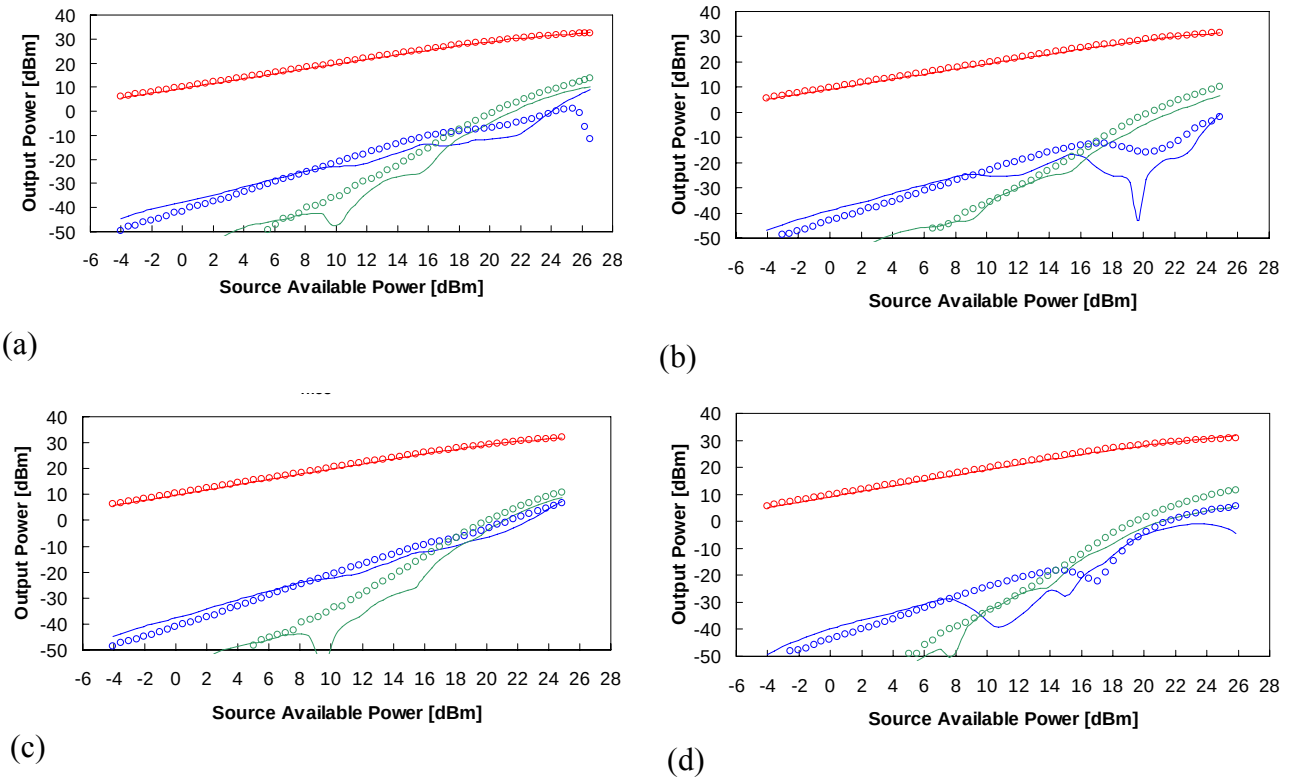


Fig. 4.11. New model predictions (line) versus measurements (circles) of output power up to the third harmonic for Γ_S=0 and four different load impedances. (a): Γ_L=0.31∠89.6°; (b): Γ_L=0.19∠68.8°; (c): Γ_L=0.43∠93.1°; (d): Γ_L=0.26∠142.8°.

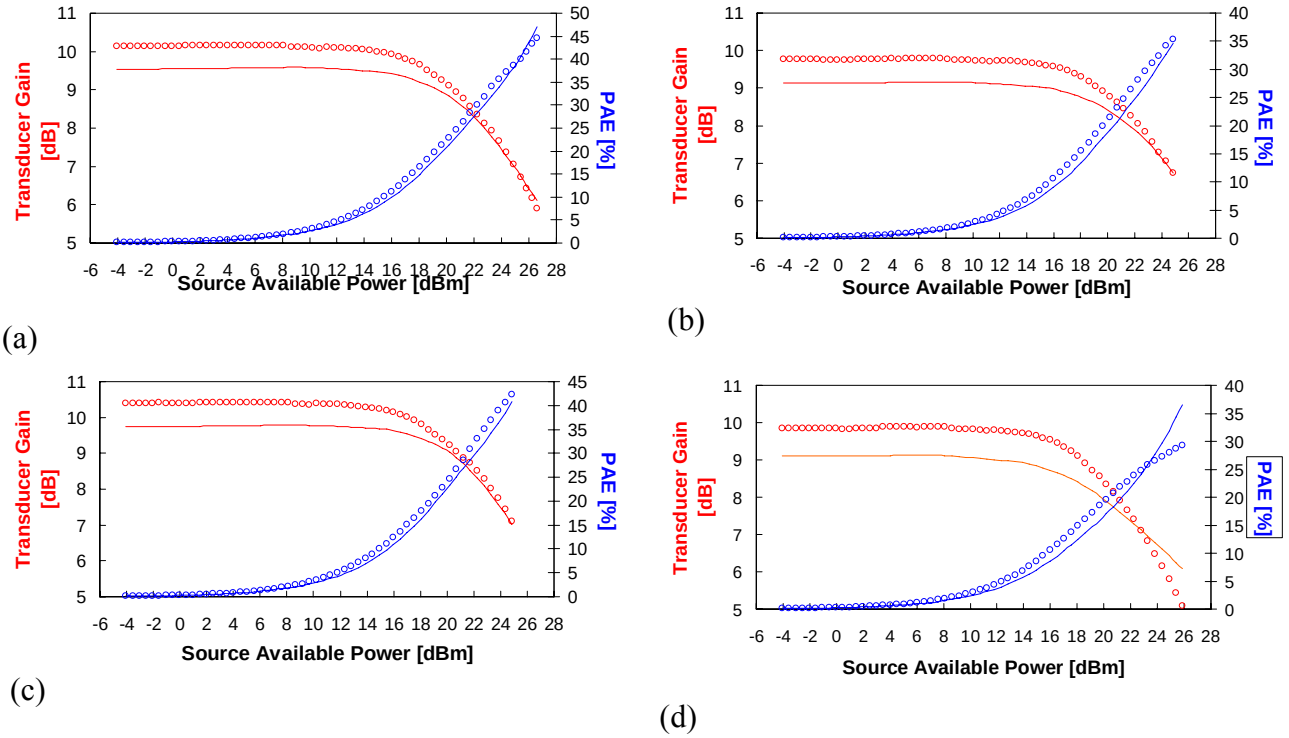


Fig. 4.12. New model predictions (line) versus measurements (circles) of transducer gain and PAE (from left to right, respectively) for Γ_S=0 and four different load impedances. (a): Γ_L=0.31∠89.6°; (b): Γ_L=0.19∠68.8°; (c): Γ_L=0.43∠93.1°; (d): Γ_L=0.26∠142.8°.

4.3 Alternative Modelling of Low-frequency Dispersive Effects

In this section a different approach to the modelling of LF dispersive phenomena in GaN-based devices is described, which provides accurate characterization of the effects due to self-heating and charge-trapping phenomena in the frequency range between the cut-off (e.g. 1MHz) and the typical RF region (e.g. GHz).

The proposed model is based on [24], developed for GaAs PHEMTs, but is for the first time applied to an AlGaN-GaN HEMT in a new form, where the identification procedure has been suitably modified in order to guarantee a better accuracy in dynamic drain current predictions. This model can be easily implemented in commercial CAD environments by means of look-up tables and, when adopted in conjunction with any high-frequency nonlinear model, can be a valuable tool for microwave circuit design.

The empirical large-signal model [24] has been already outlined in Chapter 2: it predicts the device drain I/V behaviour under dynamic operation above the cut-off frequencies of dispersive phenomena. In these conditions, charge-trapping effects and self-heating can be taken into account by means of a dependence of the I/V model characteristics on the average voltage values (V_{GS0},V_{DS0}) and on the average dissipated power (P_0), respectively. The approach is, thus, based on

the definition of a small set of purely algebraic model functions, f_G, f_D and f_P, accounting for the deviations between the static and dynamic drain current characteristics, according to:

$$\begin{aligned} i_D^{LF}(t) = {} & F_{DC}[v_{GS}(t), v_{DS}(t)] + f_G[v_{GS}(t), v_{DS}(t)] \cdot (v_{GS}(t) - V_{GS0}) + \\ & + f_D[v_{GS}(t), v_{DS}(t)] \cdot (v_{DS}(t) - V_{DS0}) + f_P[v_{GS}(t), v_{DS}(t)] \cdot (p_S(t) - P_0) \end{aligned} \tag{4.18}$$

where F_{DC} is the non-equithermal static drain current characteristic, $v_{GS}(t)$, $v_{DS}(t)$ are the instantaneous gate and drain voltages, respectively, and

$$p_S(t) \doteq F_{DC}\left[v_{GS}(t), v_{DS}(t)\right] \cdot v_{DS}(t) \tag{4.19}$$

is a "quasi-static" instantaneous power, i.e. the power that would be dissipated under purely quasi-static conditions in the presence of applied voltages $v_{GS}(t)$, $v_{DS}(t)$.

The model formulation (4.18) allows to directly use the measured DC I/V characteristic as the F_{DC} function and to identify the remaining three functions f_G, f_D and f_P by means of a linear optimization procedure over the voltage regions of interest, as indeed carried out in [24].

GaN devices are typically affected by important kink phenomena in the DC characteristics. Instead, the same kind of behaviour is not observed to such a large extent in pulsed measured data [25]. In addition, static I/V curves are usually carried out on a somehow limited region in the V_{GS}, V_{DS} domain, due to maximum rating on dissipated power. However, dynamic device operation in practical applications often involves instantaneous port voltages far beyond the static dissipation limits. Modelling approaches (either analytical or LUT-based) exploiting static I/V characterization data might then require critical 2D extrapolation. On this basis, the dispersive model (4.18) of the AlGaN-GaN HEMT, identified according to [24], has been found reasonably, yet not optimally accurate.

Thus, in order to have a better prediction of the dynamic drain currents, a new model identification has been adopted here. The F_{DC} term is considered now as a fourth unknown model function and identified on the basis of pulsed measurements only, together with f_G, f_D and f_P. It is expected that such a choice will lead to a trade-off between better pulsed I/V curves prediction and accurate determination of the device quiescent conditions. In fact, the kink behaviour of the static characteristics is expected not to be accurately predicted by the model. However, the kinks affect the DC characteristics in a region quite limited to low V_{DS} - low I_D values, thus, since quiescent conditions of electron devices in typical applications, such as power amplifiers, are not chosen in this area, this will not have practical impact on model exploitation.

According to the new model identification procedure proposed, the four unknown functions have been identified over a suitable grid of v_{GS}, v_{DS} couples, representing the instantaneous voltages, through a numerical optimization procedure, whose error function is the square deviation between pulsed measurements and corresponding predictions of (4.18).

Since the F_{DC} function is considered as unknown, the optimization is, here, nonlinear because of the thermal term. However, the weak nonlinearity of the product f_P*F_{DC} neither creates great problems of convergence and local minima, nor of dependence on initial solution choice. The algorithm convergence is anyway faster by adopting, at each change of voltage values of the grid, the optimum solution achieved for the previous voltage couple. The four model functions are, in such a way, identified over the chosen grid and stored into look-up tables, which can be easily implemented into commercial simulator for microwave circuit design based on harmonic-balance algorithms.

In order to guarantee better prediction accuracy and fast simulation time, the proposed model makes use of a dedicated algorithm of data approximation (see Chapter 5 and [26]). This algorithm allows to approximate nonlinear functions by using an approach similar to the well-known methods for reconstruction of continuous-time signals from a given sequence of samples. The adopted approximation algorithm guarantees, as a further advantage, to reduce possible inaccuracies of the pulsed measurement set-up, applying a sort of filtering (smoothing) action to the drain current characteristics.

The LF dispersion model was extracted for an AlGaN-GaN HEMT (L=0.25 μm, W=8*50 μm) processed and characterized by IEMN laboratories. To this aim, pulsed measurements were carried out between -9 V and 1 V for the gate voltage and between 0 V and 30 V for the drain voltage, while DC characterization ranges were upper limited to 0 V for V_{GS} and to 15 V for V_{DS}, due to maximum power dissipation constraints. The measurements were, then, de-embedded from the extrinsic parasitic elements, identified on the basis of known cold-FET procedures, and approximated by means of the above mentioned dedicated algorithm.

In the first model version, the measured DC drain currents were used after 2D extrapolation up to V_{DS}=30 V and the model functions f_G, f_D and f_P were identified by means of a least-square based, best-fit procedure between (4.18) and the four measured dynamic characteristics obtained by pulsing from different quiescent points: (V_{GS0}=-5 V, V_{DS0}=20 V), (V_{GS0}= 0 V, V_{DS0}=0 V), (V_{GS0}=-9 V, V_{DS0}=0 V) and (V_{GS0}=-9 V, V_{DS0}=20 V). With this kind of identification, the DC drain current is directly stored in a look-up table and its prediction is thus theoretically exact.

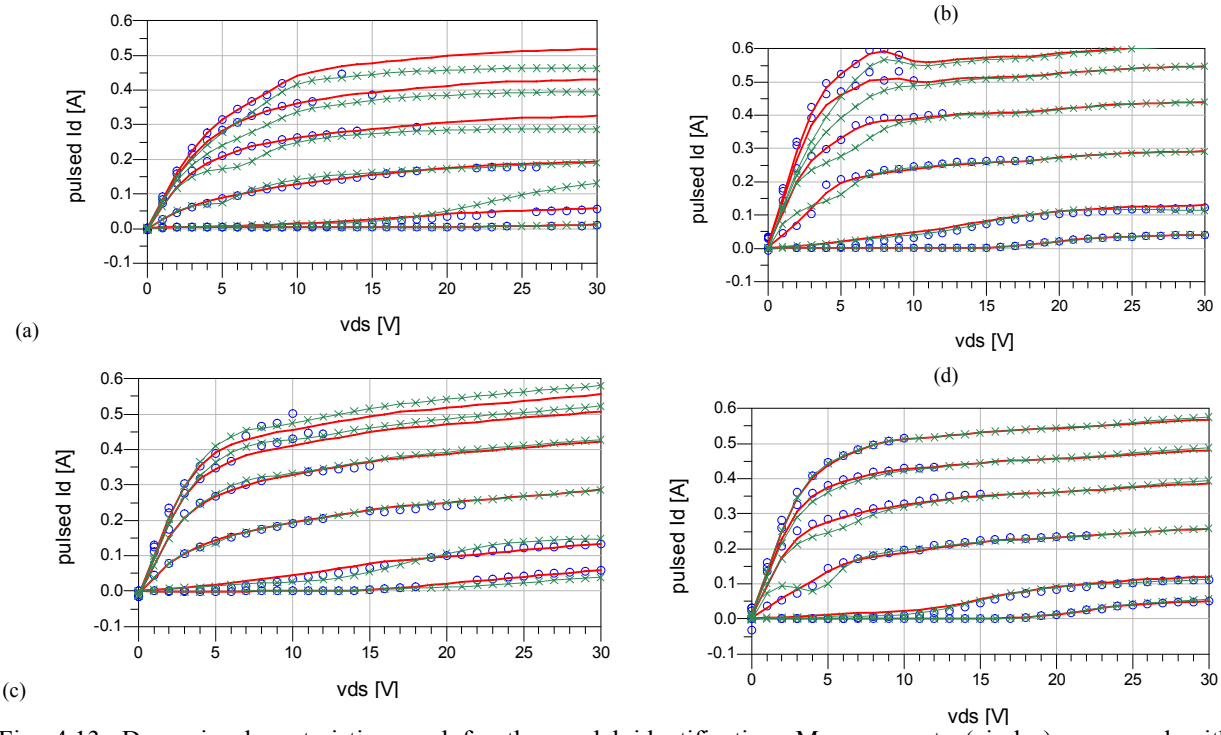


Fig. 4.13: Dynamic characteristics used for the model identification. Measurements (circles) compared with predictions: new identification procedure (continuous line), vs standard procedure using the DC measurements also (crossed line). The instantaneous gate voltage ranges between -9 V and 1 V (2-V step); quiescent points: (a): V_{GS0}=-5 V, V_{DS0}=20 V, (b):V_{GS0}= 0 V, V_{DS0}=0 V, (c):V_{GS0}=-9 V, V_{DS0}=20 V, (d): V_{GS0}=-9 V, V_{DS0}=0 V. The kink effect predicted by the classic model is well evident in (a), (b) and (d).

Instead, in the identification method proposed here the same four pulsed characteristics were used to identify the DC drain current also: in this case the model functions were extracted by solving a weakly nonlinear system of four equations in four unknowns for each couple of instantaneous voltages, v_{GS}, v_{DS}. This led to have a theoretically exact reproduction of the pulsed characteristics used for the model identification. In Fig. 4.13 the four measured pulsed characteristics are compared with model predictions. The slight difference between measured and simulated data is simply due to the filtering-like data approximation algorithm used. In addition, the predictions provided by the model identified in the conventional way are also plotted in Fig. 4.13. As expected, less accuracy is obtained in this case due to kink effects much more important with respect to those effectively present in dynamic measured characteristics and to the 2D- extrapolation of the DC characteristic beyond V_{DS} = 15 V.

In order to fully validate the model, two additional dynamic characteristics not used to extract the model functions were considered, obtained by pulsing from different quiescent conditions (V_{GS0}=-6 V, V_{DS0}=20 V and V_{GS0}=-9 V, V_{DS0}=15 V). Comparisons are provided in Fig. 4.14, showing the good accuracy achieved with both the models tested.

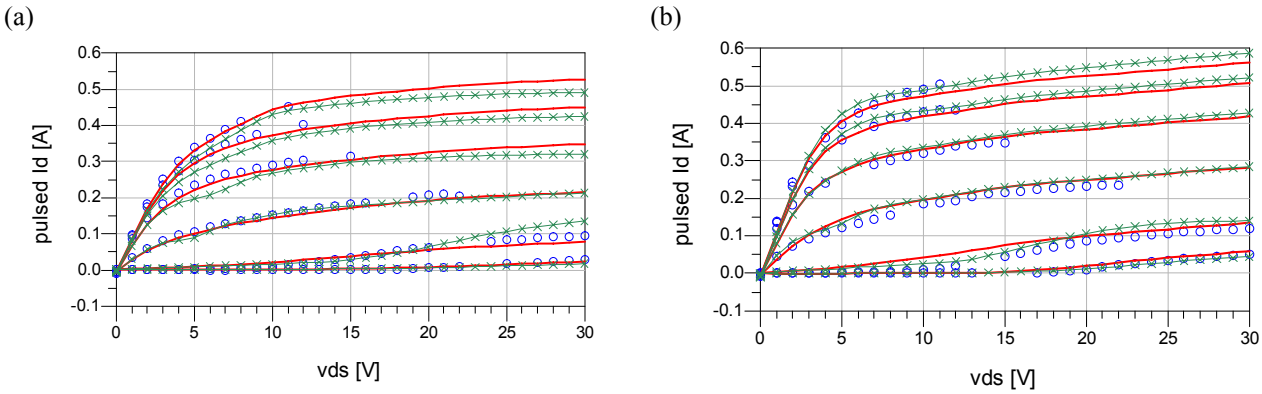


Fig. 4.14: Dynamic drain currents pulsed from V_{GS0}=-6 V, V_{DS0}=20 V (a), and V_{GS0}= -9 V, V_{DS0}=15 V (b): measurements (circles), predictions of the new model (line) and of the conventional model (x).

The static characteristics are shown in Fig. 4.15: as expected, the prediction is fairly good in the typical bias region for class A/AB device operations.

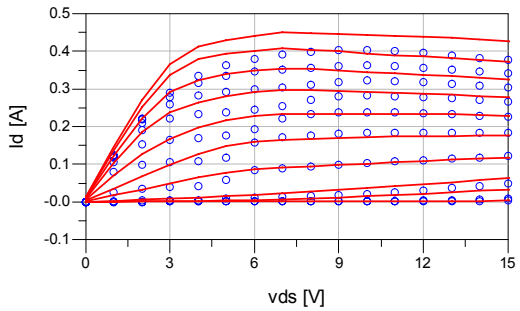


Fig. 4.15: Static drain currents for gate voltage ranging between -9 V and 0 V (1-V step): measurements (circles), predictions of the new model (line).

In addition, in order to better quantify the results achieved with the two models, the predictive errors are defined as the normalized mean square deviation between predicted and measured drain currents:

$$\varepsilon = \frac{\sum_{m,n} (I_{m,n}^{\mathrm{mod}} - I_{m,n}^{\mathrm{meas}})^2}{\sum_{m,n} (I_{m,n}^{\mathrm{meas}})^2} \tag{4.20}$$

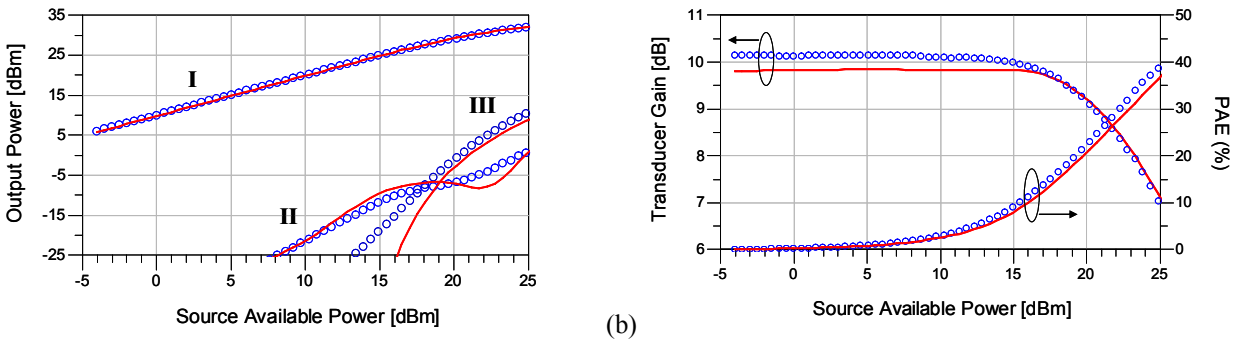
where m, n represents indexes ranging over the voltage values v_{GS}, v_{DS} within the identification grid. In Table 4.1 the average errors in predicting the pulsed measurements are plotted, as indicators of the general model accuracy.

TABLE 4.1

Average Errors on I/V Curves Prediction

Quiescent point (V_{GS0}; V_{DS0})	**Std. Model** (using meas. DC I/V) (%)	**New Model** (without using meas. DC I/V) (%)
(-5; 20)	0.83	0.01
(0; 0)	0.39	0.01
(-9; 0)	0.09	0.01
(-9; 20)	0.32	0.03
(-6; 20)	0.53	0.15
(-9; 15)	13.21	10.89
static I/V	0.01	1.62

The proposed low-frequency dispersion model was tested in conjunction with the Equivalent-Voltage nonquasi-static model [10] in a microwave application. The AlGaN-GaN PHEMT model was extracted for the design of a class A power amplifier at 4 GHz. Harmonic distortion tests were carried out with a 50-Ω rf power source, a load termination Γ_L=0.31∠89.6° and biasing the device at V_{GS0}=-5 V, V_{DS0}=20 V. First, second and third harmonics of the predicted output power are compared with measurements in Fig. 4.16-a, showing a very good agreement up to strongly saturated conditions. The transducer gain and the Power Added Efficiency are also plotted in Fig. 4.16-b.



(a) (b)

Fig. 4.16: Harmonic distortion test: V_{GS0}=-5 V, V_{DS0}=20 V, f_0= 4 GHz, Γ_S=0, Γ_L=0.31∠89.6°. Model (line) vs. measurement (circle).

4.4 Conclusion

A new empirical nonlinear model suitable for GaN-based PHEMTs has been extracted and experimentally validated. The model is based on the same equivalent voltage approach described in Chapter 3, but applied here for the first time in a two-fold way for describing both long-term dynamics associated to dispersive phenomena and short, yet finite, nonquasi-static memory effects. In addition, pulsed rf S-parameter measurements have been used in the identification phase leading to good prediction capabilities both in small- and large-signal operating conditions. Nonlinear device characteristics have been implemented here through a look-up-table approach, but analytical functions or approximations based on artificial neural network are also possible.

In GaN-based HEMT the dispersive effects are a significant impact on the device performances, so particular attention has been paid to the modelling of this phenomena. A correction for a better prediction of the dynamic drain current is introduced in the LF-EV model, where the effects of low-frequency dispersive phenomena on the drain current waveform are considered to be dependent not only on voltage bias but also on the second order moments of the AC components of the gate and drain voltages. considerable improvements, with respect to conventional modelling approaches strictly based on bias-dependent, pulsed I/V measurements only, can be achieved in terms of prediction accuracy of average drain current and, consequently, power consumption.

Finally, another modelling approach, developed for GaAs transistors, has been applied to AlGaN-GaN HEMTs, but a new model identification procedure has been here developed, by taking into account the specific properties of the GaN-based devices, such as the presence of strong kink effects in the DC characteristics.

In the next chapter a particular device modelling will be faced, for both Gallium Arsenide and Gallium Nitride technologies: the modelling of cold-FET behaviours.

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Chapter 5

Cold FET Modelling

Microwave communication systems require a higher and higher integration level: all the functional blocks tend to be embedded on the same MMIC. This leads to an increasing interest in FET-based mixers, which, unlike diodes, are fully technological compatible with the other system components, besides providing good performances. In this context, particular attention is paid to cold FET mixers, due to their high linearity and low phase-noise [1].

This kind of application requires nonlinear electron device models capable of accurately predicting the weak, local non linearity around the V_{DS} = 0 V bias condition, while the LO signal swings within the maximum rating range of the gate voltage. For this reason, readily available foundry models, mostly thought for "hot" operating conditions, are unsuitable. Unfortunately, also in the literature few models can be found satisfying these requirements [2]-[4]. Conventional equivalent circuit models, in fact, usually do not suit well this kind of applications, since the analytical functions they are based on, depending on a relatively small number of parameters, provide reasonably good global fitting of the nonlinear behaviour at the cost of local prediction accuracy. Therefore, Look-Up-Table-based models can be a good choice, since they can be tailored to an optimal description of the local nonlinearities: in such a way, their extraction can be carried out to a limited extent in the device operating region of interest, in order to optimize the model performances for the specific application.

5.1 Device Modelling for Cold-FET Mixer in GaAs technology

In this chapter, the empirical, purely mathematical, Nonlinear Discrete Convolution (NDC) model [5], already outlined in Chapter 2, is validated for electron devices in cold FET configuration, in the framework of a resistive mixer application with f_{LO} = 4.8 GHz, f_{RF} = 4.2 GHz, down-converting at f_{IF} = 600 MHz. The model is suitably identified in the particular region of interest, providing very good accuracy in both predictions of current and voltage waveforms and estimation of output power at the IF frequency for several levels of the LO power.

5.1.1 Model Description and Identification

The NDC model [5] describes the device dynamics (including nonquasi-static effects) in terms of elementary delay operators through a non-linearly controlled discrete-time convolution. The model can be derived, without any constrictions on the physical device structure, by considering that the instantaneous device currents depend on both present and past voltage values, and by adopting a purely mathematical functional description for the current/voltage relationship, i. e. for a single-port device:

$$i(t) = \Psi\left|v(t-\tau), \vartheta_C\right|_{\tau=0}^{\infty}, \tag{5.1}$$

where Ψ is a nonlinear functional, ϑ_C is the device case temperature and $i(t)$ and $v(t)$ are the current and voltage at the device port, respectively. By separately dealing with parasitic and low-frequency dispersive effects, which feature a slow-dynamics, a short duration of the memory effects with respect to the typical operating frequencies of the device can be assumed. The hypothesis is well verified by means of both numerical simulations and experimental validation. A finite memory time T_M, suitably chosen, can be thus adopted for the electron device, leading to:

$$i(t) = \tilde{\Psi}\left|v(t-\tau), P_0, V_0, \vartheta_C\right|_{\tau=0}^{T_M} = \tilde{\Psi}\left|v(t), v(t-\tau)-v(t), P_0, V_0, \vartheta_C\right|_{\tau=0}^{T_M}, \tag{5.2}$$

where V_0 and P_0 are the mean voltage values and the dissipated power, respectively, explicitly introduced in order to account for dispersive effects. Equation (5.2), in fact, allows great model simplification: the current-voltage functional description can be linearized with respect to purely dynamic voltage deviations between present and past voltages ($v(t-\tau)-v(t)$), leading to a convolution integral between voltage deviations and an impulse response function nonlinearly controlled by the instantaneous port voltages. By approximating the integral with a discrete summation of delayed terms, the final model equation is:

$$i(t) = F_{LF}[v(t), V_0, P_0, \vartheta_C] + \sum_{p=1}^{N_D} g_p[v(t)] \cdot [v(t-p\Delta\tau) - v(t)] \tag{5.3}$$

where the g_p functions are voltage-controlled impulse responses and N_D is a suitable number of intervals in which the memory time is divided ($T_M = N_D \cdot \Delta\tau$). The linear dependence on the voltage dynamic deviations is justified by considering that under short-memory conditions the dynamic deviations are small also in the presence of large voltage signals.

The F_{LF} function in (5.3) represents the low frequency device behaviour: a suitable dispersive model should be adopted in conjunction to the NDC model, accounting dispersive phenomena due to traps and thermal effects, by means of the current dependence on mean voltage values (V_0) and dissipated power (P_0), respectively [5]. However, dispersive phenomena affect cold-biased devices to a negligible extent, thus the F_{LF} function is here replaced by the simple DC I/V characteristics.

The nonlinear model (5.3) is directly identifiable on the basis of DC I/V characteristics and small-signal S parameters and can be easily implemented in commercial circuit simulators by simply using the tools normally available for the construction of user-defined models (i.e., non-linear purely algebraic functions and delay operators).

The F_{LF} and the g_p functions can be suitably identified starting from empirical data, according to the procedure outlined in [5], which allows a systematic and unambiguous link between conventional measurements and prediction of the large-signal electron device behaviour. In particular, the model has been here extracted on the basis of DC and S-parameter data, measured in the operating region of interest for resistive mixer device configuration: V_{GS} ranging from off-state to forward condition and V_{DS} in the neighbourhood of the cold FET bias.

5.1.2 Experimental Validation

The NDC model has been extracted for a GaAs 0.25-µm PHEMT with 140-µm width. To this aim, DC and S-parameter measurements were carried out for V_{GS} ranging from -3 V to 0.6 V (step 0.1 V) and V_{DS} between -0.8 V and 0.8 V (step 0.05 V); the S parameters were measured from 4 GHz up to 46 GHz exploiting an on-wafer TRL calibration. A memory time T_M=2.7 ps, divided into N_D=3 time slots, was chosen, according to the considerations reported in [5]. The static trans- and output I/V characteristics of the electron device are reported in Fig. 5.1, where the chosen quiescent condition for the current application, V_{GS}=-1.2 V and V_{DS}=0 V, is also outlined for reference.

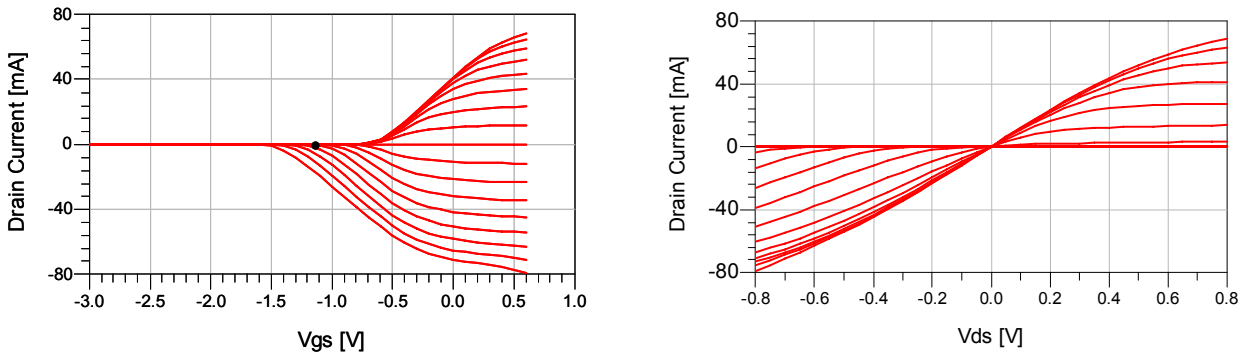

Fig. 5.1: PHEMT DC I/V characteristics. The black point on the trans-characteristic marks the nominal bias condition chosen for the cold FET model validation: V_{GS}=-1.2 V, V_{DS}=0 V

A first model validation was conducted in small signal conditions: the S parameters in the nominal bias point are plotted in Fig. 5.2, showing a very good model prediction.

In order to fully validate the model, a large-signal characterization was carried out on the device in cold FET configuration, by means of on-wafer waveform measurements under two-tone excitation, [6]. The measurement setup, Fig. 5.3, exploits a large-signal VNA, which acquires the spectral components in phase and amplitude (up to 20 GHz) of the incident and scattered voltage waves at the DUT ports. Two 50-Ω sources apply the signals at the gate port (LO signal) and at the drain port (RF signal). The measurement setup configuration adopted does not allow to tune source and load impedances, thus the device characterization has been carried out with termination impedances quite far from the real ones in mixer applications. This characterization is however significant in order to estimate the model prediction capabilities for cold FETs in large-signal operations.

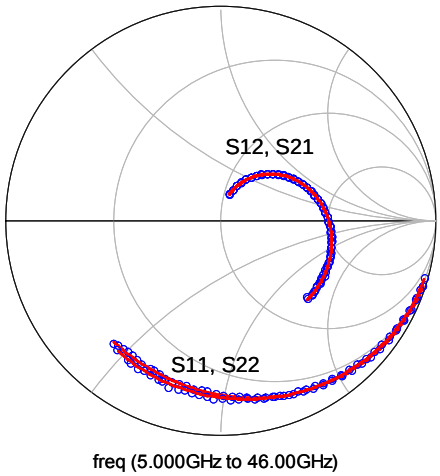

Fig. 5.2: PHEMT S parameters in V_{GS}=-1.2 V, V_{DS}=0 V, for frequency ranging between 5 and 46 GHz. Model predictions (red line) compared with measured data (blue circles).

In our test, the device is biased at V_{GS}=-1.2 V and V_{DS}=0 V and the input signal frequencies are 4.8 GHz for the LO generator and 4.2 GHz for the RF one. Different power levels are provided by the LO source, while the RF source power is constant.

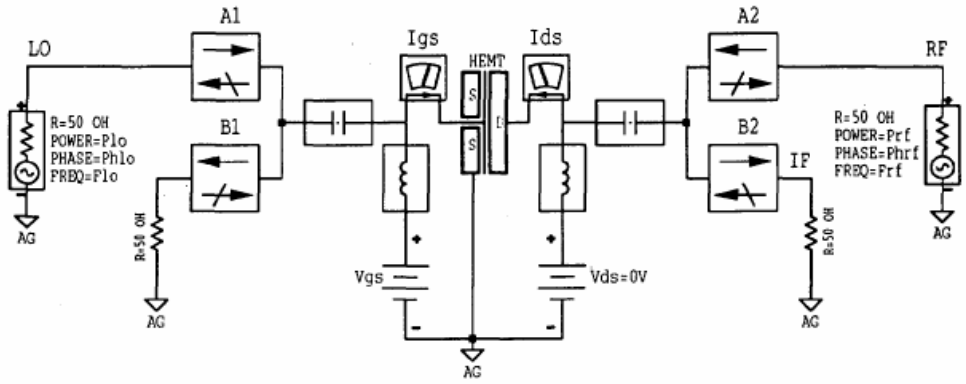

Fig. 5.3: Measurement setup configuration adopted for the large-signal characterization of the cold FET

The predicted and measured output power at the conversion IF frequency, i.e., 600 MHz, is plotted in Fig. 5.4-a, for the different levels of the LO input power, showing a very good model performance for the specific application. The conversion loss, obtained as the ratio between the IF output power and the RF input power, is plotted in Fig. 5.4-b: good agreement is achieved also in this test. An important requirement in mixer design is often the rejection of the LO and RF components at the output port (single or double balance): to this aim, it is important for the model at disposal to well predict also the unwanted output components. The predicted and measured output powers at the LO frequency is reported in Fig. 5.4-c and the globally good model performance can be evaluated from Fig. 5.4-d, where the whole spectrum of the reflected output waveform is displayed in correspondence of the maximum input power level.

Finally, the model performances are evaluated in the time domain by comparing predictions and measurements of the output voltages and currents in Fig. 5.5, again for the maximum LO source power level: the whole waveforms are well predicted, even though high nonlinearity is here involved.

The presented large signal validation outlines the very good capabilities of the NDC model in predicting the electrical FET behaviour under cold operation. This makes the model a good candidate for the design of a resistive mixer.

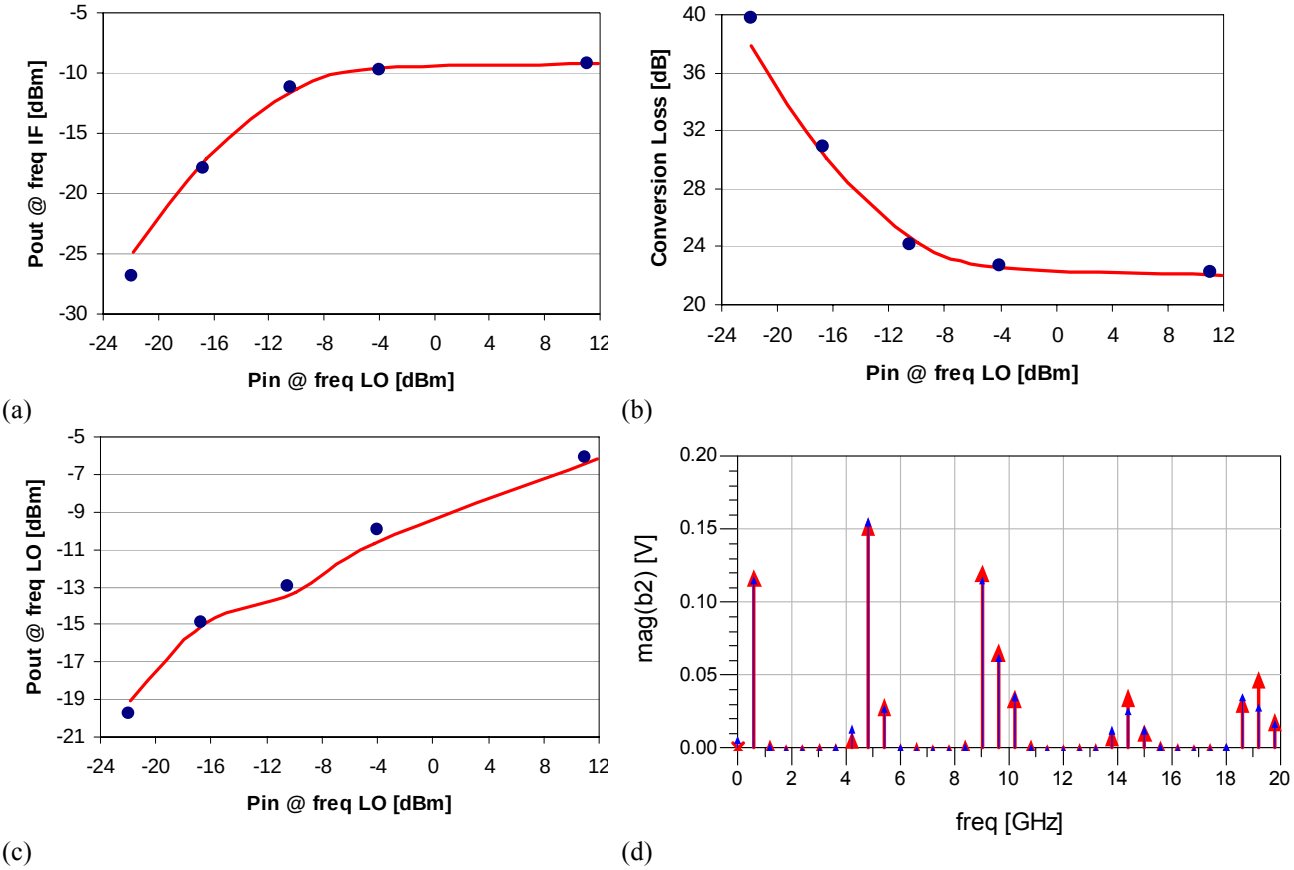

Fig. 5.4: LS validation (source and load terminations equal to 50Ω). (a): Output power at the conversion IF frequency (600 MHz) versus LO input power. (b): Conversion Loss. (c): Output power at the LO frequency (4.8 GHz). Model predictions (red line) and measurements (blue circles). (d): Spectrum of the output reflected waveform. Predictions (red bold line) and measurements (blue thin line).

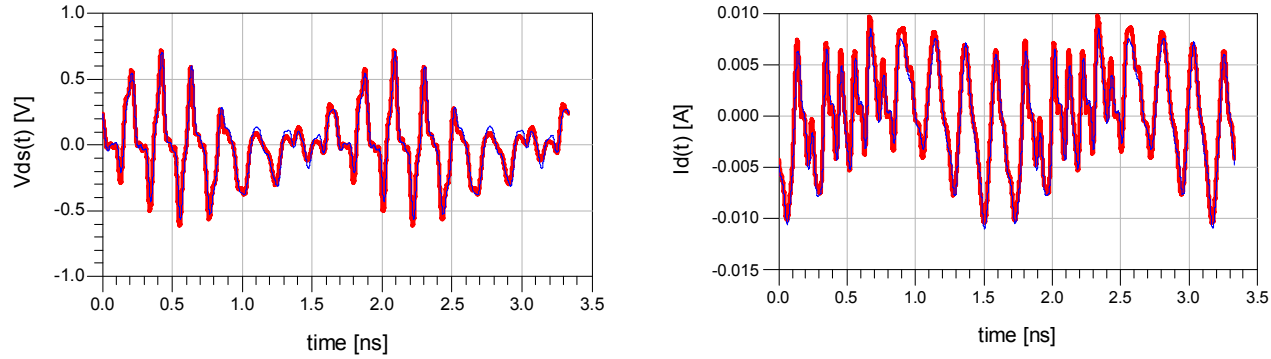

Fig. 5.5: Voltage and current waveforms at the output device port for the maximum level of input power. Model predictions (red bold line) and measurements (blue thin line). Source and load terminations equal to 50Ω.

A double balanced cold FET mixer has been designed by adopting a single device topology with a circulator connected at the drain port in order to separate the input RF from the output IF signal. The FET has been biased under almost pinched-off channel bias conditions (V_{GS}=-1.2 V). Two matching networks were synthesized in order to maximize the output power at the IF and to have

conjugate match at the gate port (LO input). Finally, a low-pass filter guarantees the mixer balance. The obtained performances are reported in Table 5.1.

TABLE 5.1
MAIN MIXER FIGURE OF MERIT

f_{LO} = 4.8 GHz f_{RF} = 4.2 GHz f_{IF} = 600 MHz P_{av}^{LO} = 24 dBm P_{av}^{RF} = −10 dBm	Conv. Loss ($P_{in}^{RF} / P_{out}^{IF}$)	LO Rejection ($P_{out}^{IF} / P_{out}^{LO}$)	RF Rejection ($P_{out}^{IF} / P_{out}^{RF}$)
	4.45 dB	18 dB	32 dB

5.2 Device Modelling for Cold-FET Mixer in GaN technology

Thanks to its capability of managing high powers and to its good linearity properties, GaN technology is emerging as a strong candidate for the receiver chain. However, according to our knowledge, very few GaN-based mixers have been achieved at the present [7]-[9], and, among these, just one is for wideband applications, that is an AlGaN/GaN HEMT MMIC resistive mixer for the X-Band, featuring a 2-GHz bandwidth for the IF signal and a conversion loss lower than 8 dB [9].

The target of this joint work with the IEMN Institute of Lille (FR) is, thus, to design a single-ended, wideband, down-converter mixer, by using an AlGaN/GaN HEMT: the RF and LO bandwidth are between 6 and 18 GHz, while, correspondingly, the IF signal is in the bandwidth DC-6 GHz. To this aim, an accurate LUT-based model for GaN devices is suitably extracted for the cold-FET application: the model chosen for this application has been the Equivalent-Voltage model [10].

The theory of the adopted AlGaN/GaN HEMT model, tailored on the cold-FET condition, is briefly recalled in the following, together with a preliminary, small- and large-signal model validation. The wideband mixer design, carried out by the IEMN team, is also reported: the preliminary results, obtained by means of electric and electromagnetic simulations, show a very good linearity and an adequately low conversion loss for a wideband, hybrid, GaN-based mixer.

5.2.1 Model Description and Validation

The GaN device model proposed in [10] and described in Chapter 4 is here adopted and suitably tailored on the cold-FET application. In resistive mixers, the devices are biased in V_{DS}=0 V and V_{GS}

near the threshold voltage, in order to obtain a switch-like behaviour when driving the FET with the LO signal applied to the gate. In this particular polarization, the device is almost not affected by either dispersive or nonquasi-static phenomena. Nevertheless, a quasi-static, nondispersive model cannot be adequate, since the device, during its final operation, will dynamically move in regions where these effects are no longer negligible.

We chose, thus, to account for the low-frequency dispersive effects by means of current sources directly obtained from the measured I/V characteristic, pulsed from the bias condition of the mixer design. As far as the nonquasi-static effects are concerned, the model accounts for them by adopting an equivalent-voltage approach, like in [10]. Thus, the model can be formulated as:

$$\mathbf{i}(t) = \mathbf{F}\left[\mathbf{v}(t)\right] + \mathbf{C}\left[\tilde{\mathbf{v}}_d(t)\right]\frac{d\tilde{\mathbf{v}}_d(t)}{dt}, \tag{5.4}$$

where **F** is a vector of purely algebraic nonlinear functions representing nondispersive I/V device characteristics, namely here gate and drain currents pulsed from the nominal quiescent condition, and **C** is a quasi-static capacitance matrix. The nonlinear functions in **C** are controlled by equivalent voltages $\tilde{\mathbf{v}}_d$:

$$\tilde{\mathbf{v}}_d(t) \doteq \mathbf{v}(t) + \Delta\mathbf{v}_d(t) \ , \tag{5.5}$$

where **v** are the actual applied voltages at the intrinsic device ports, while $\Delta\mathbf{v}_d$ are voltage deviation terms to be identified. These voltage perturbations are assumed linearly dependent on applied voltages and described by means of:

$$\Delta\mathbf{v}_d = \sum_{p=1}^{N_D}\left[\mathbf{a}_p \cdot \left(\mathbf{v}(t - p\Delta\tau) - \mathbf{v}(t)\right)\right] \ . \tag{5.6}$$

where $\mathbf{a}_p$ (with p=1,..,N_D) is a matrix of real, bias-independent model parameters to be identified. The typical finite memory time T_M associated with nonquasi-static phenomena is divided into N_D elementary time slots $\Delta\tau$, in order to easily implement the model in commercial CAD tools.

The model was extracted for an AlGaN/GaN HEMT, with gate length of 0.25 μm and width of 2*100 μm. To this aim, the device characterization was carried out by means of standard CW measurements of S parameters up to 110 GHz and I/V characteristics pulsed from V_{GS0}=-9 V (threshold voltage) and V_{DS0}=0 V. Both kind of measurements were carried out on the typical bias grid for cold-FET mixer applications: V_{GS} ranging between -14 V (deeply off-state) and 0 V and V_{DS} between -6 V and 8 V. The current sources were implemented by directly storing the DC gate

current[1] and the pulsed drain current into look-up-tables. The capacitance matrix **C** was, instead, extracted from the imaginary part of the intrinsic, admittance parameters in a frequency range high enough to observe reactive effects, but where nonquasi-static effects are still negligible (namely, here, between 1 and 5 GHz). The so-obtained nonlinear capacitances were also stored into look-up-tables.

As far as the identification of the voltage corrections is concerned, a memory time T_M=4.5 ps is adopted and divided into N_D=3 slots. A single bias point is then chosen for the $\mathbf{a}_p$ parameters extraction, that is the on-state condition, V_{GS}=0 V and V_{DS}=1 V. Alternatively, a multi-bias identification is also possible, on the whole region of interest and by means of least-square-based procedures. It is worth noting that the point chosen here for the identification is different from the quiescent condition adopted for the pulsed IV characterization, since the latter corresponds to a cold condition, practically unaffected by nonquasi-stationarity.

In order to avoid undesired corrections, due to the $\Delta\mathbf{v}_d$ terms, under off-state or cold-FET conditions, the device behaviour in off-state is first modelled through a Π-network of linear capacitances and their values are de-embedded from the capacitance matrix **C.** The voltage deviations $\Delta\mathbf{v}_d$ are thus applied to the resulting device (the *strictly intrinsic device*) de-embedded from both the off-state capacitances and the classic parasitic network [10]. The voltage corrections are thus implemented by means of two voltage-controlled voltage-sources, on the gate and drain displacement current branch of the strictly intrinsic device.

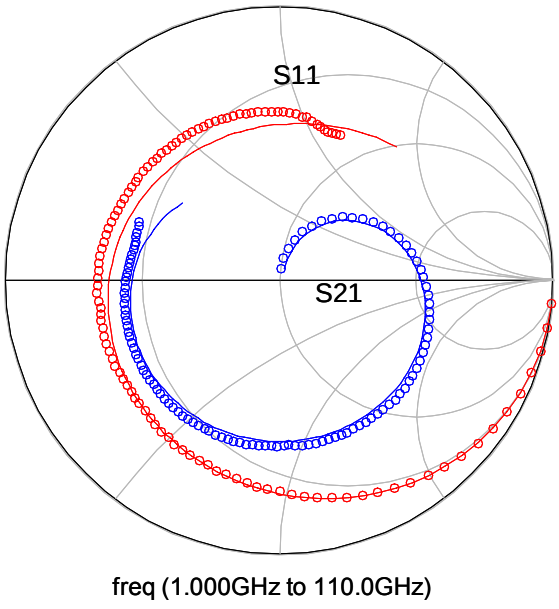

Fig. 5.6 Extrinsic S_{11} and S_{21} parameters: measurements (circles) versus model predictions (line)

[1] Gate current is not usually affected by low-frequency dispersion, so that the static bias-dependent gate current characteristic can be adequately used.

The prediction of the extrinsic S_{11} and S_{21} parameters is compared with measurements in Fig. 5.6, for V_{GS0}=-9 V and V_{DS0}=0 V, showing a very good agreement. Similar accuracy is obtained for S_{12} and S_{22}, which are almost equal to the others because of the electrical symmetry of the device condition.

The good multi-bias prediction capability of the model can be, instead, appreciated in Fig. 5.7, where the intrinsic trans- and output conductances at 18 GHz are shown for V_{DS}=0 V and V_{GS} sweeping.

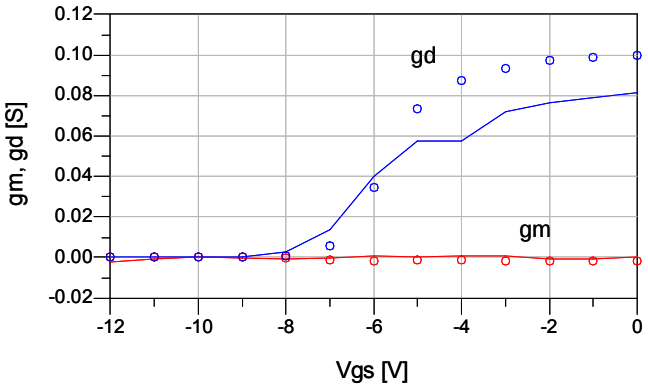

Fig. 5.7 Intrinsic g_m and g_d parameters versus V_{GS} at V_{DS} = 0V and 18 GHz. Model predictions (line) and measurements (circles). The minor accuracy for high values of V_{GS} is mainly due to slight discrepancies between the conductances obtained from pulsed I/V characteristics and the cw differential parameter measurements.

Finally, the cold-FET model was validated in large-signal conditions by means of load-pull measurements at 10 GHz, the device biased in V_{GS0}=-9 V and V_{DS0}=0 V. The power gain for a load impedance corresponding to conjugate matching is shown in Fig. 5.8.

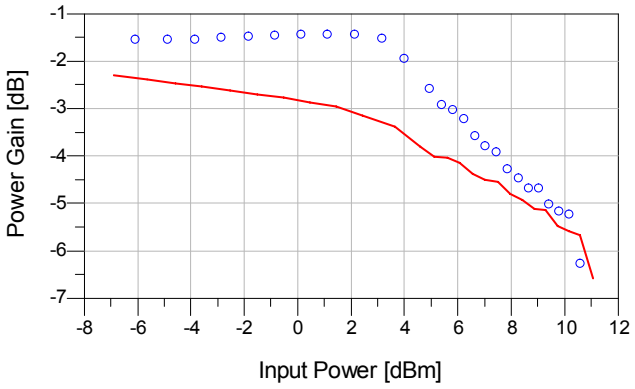

Fig. 5.8 Predicted (line) and measured (circle) power gain versus input power at 10 GHz. V_{GS0}=-9 V, V_{DS0}=0 V , Z_S =50 Ω, Z_L =0.722+j*0.624.

5.2.2 Wideband Mixer Design

The mixing function is here realized by means of a GaN transistor in cold configuration. To this aim, the drain is not biased (V_{DS} = 0 V) and the gate is pinched off (here, $V_{GS} = V_p$ = -9 V), in order to generate the maximum conversion.

In this configuration, the RF signal is applied to the drain whereas the LO signal is applied to the gate. The IF signal is obtained on the drain (Fig. 5.9).

In this area of polarization, the drain current characteristic is linear with respect to the drain voltage, so the device is equivalent to a variable resistance, controlled by the gate voltage. The LO modulation permits to modify the value of this resistance, which is low when V_{GS} is above pinch-off and high (virtually infinite) when $V_{GS} < V_p$. The magnitude of the resistance variation permits to obtain good mixer performances from resistive mixers.

The final circuit is a hybrid resistive mixer: the schematic is presented in Fig. 5.9. The design is composed by :

- Two bias tees: one on the gate to set the V_{GS} value (near the pinch-off voltage) and one on the drain in order to avoid self-polarization: the drain is linked down to the ground. These two bias tees are similar and include an 82-pF MIM capacitance and an 8-µH conical inductor.
- Two matching circuits at input and output of the transistor, in order to improve the gain conversion and compensate the bonding effect due to the connection between the circuit and the AlGaN/GaN HEMT.
- A Lange coupler to split the RF and IF signals. The simulation results show an RF/IF insulation higher than 20 dB and losses lower than 3 dB for the IF path (DC-6 GHz) and lower than 6 dB for the RF path (6-18 GHz).

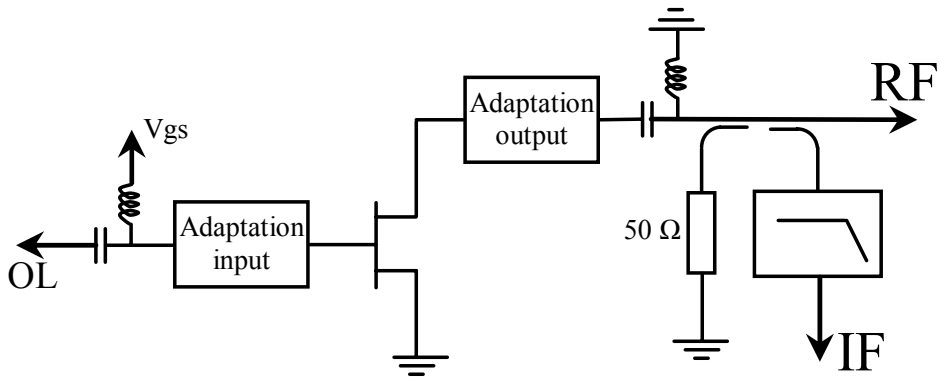

Fig. 5.9 Schematic of the resistive mixer**.**

A hybrid circuit requires the use of bonding between the transistor and the others components processed on alumina. The difficulty consists in predicting the length of bonding, which has, indeed, a direct influence on the mixer bandwidth. The adaptation circuit permits to limit this influence but in any case the bonding decreases frequency and gain conversion. The bonding length is fixed here at 750 µm.

The IF filter has been designed in order to cover the bandwidth DC - 6 GHz. His presence closes the IF bandwidth at 6 GHz but permits to considerably improve the insulation LO/IF and RF/IF (up to 40 dB in some area for RF/IF and up to 5 dB in some area for LO/IF).

For each element of the design, two types of simulation have been carried out: electric simulation with ADS for designing the mixer and electromagnetic simulation with Empire, to validate the simulations by also taking into account the coupling effects. A good agreement has been obtained with less than 1dB of error in the bandwidth DC - 20 GHz. In particular, conversion losses, insulation and linearity have been analysed for F_{RF} and F_{LO} sweeping on the whole bandwidth of interest. The three-dimensional results are reported in this paper by exploiting, for clarity, 2D plots in colour scale (e.g., Fig. 5.10). The simulations were performed for both F_{RF} and F_{LO} frequencies in the bandwidth 3 – 23 GHz, so, in each figure, the area of interest is pointed out in emphasized colours. This area corresponds to the LO and RF frequencies in the bandwidth 6 – 18 GHz that provide an IF frequency between DC and 6 GHz. For instance, by considering an F_{LO} = 10 GHz, the F_{RF} of interest is between 6 GHz and 16 GHz.

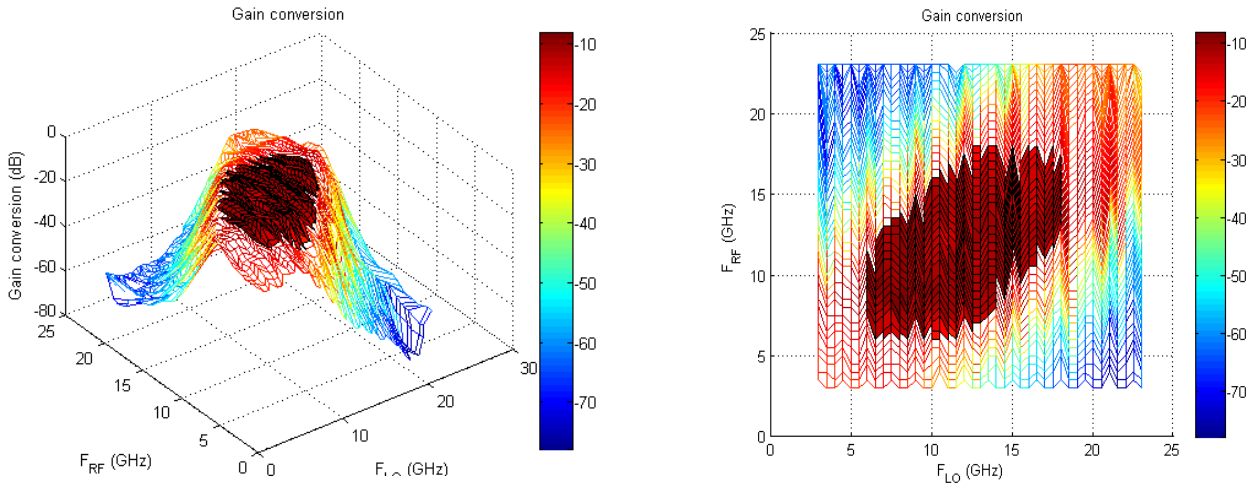

Fig. 5.10: Conversion gain versus F_{LO} and F_{RF} frequencies in 3D and 2D view. The more coloured area highlights the frequency points of interest.

The effects of the IF filter are evident from Fig. 5.10: a band of 6 GHz is, in fact, described when we sweep in F_{LO} and F_{RF}. The decrease of the gain conversion out of the 6-GHz band is clearly

related to the insertion losses of the filter, and the same considerations can be drawn for the insulation RF/IF in Fig.5.11. Nevertheless, the conversion losses are better than 16 dB in the bandwidth of interest.

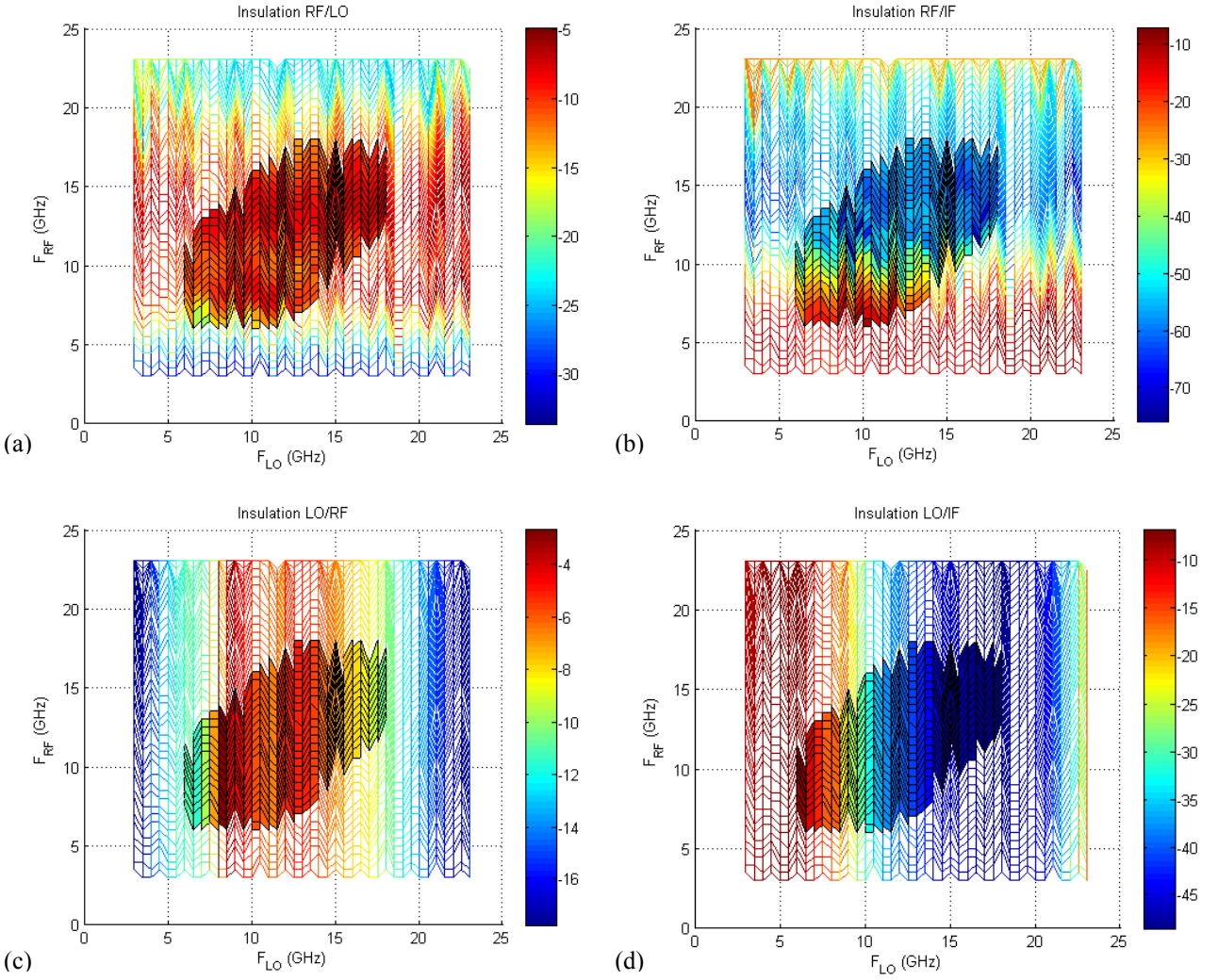

Fig. 5.11 Insulation RF/LO (a), RF/IF (b), LO/RF (c) LO/IF (d) versus F_{LO} and F_{RF} frequencies.

The insulations RF/LO and LO/RF, shown in Fig 5.11, present a variation area of [7 dB; 18 dB] and [3 dB; 11 dB], respectively. These insulations are not very high because the LO and RF frequencies are in the same range, so it is not possible to use filters to improve these parameters.

As far as the study of linearity is concerned, two signals, RF1 and RF2, are injected in the RF path. The F_{RF1} and F_{RF2} are separated by a spacing frequency ΔF equal once to 100 kHz and after to 1 MHz. The $F_{IF1} = |F_{LO}-F_{RF1}|$ and $F_{IF2}=|F_{LO}-F_{RF2}|$ are generated on the IF path with all the intermodulation harmonics. The gain conversion for F_{RF1} or F_{RF2} results strictly the same for each ΔF (Fig. 5.12), thus the mixer has a good stability of its conversion gain in the bandwidth of interest.

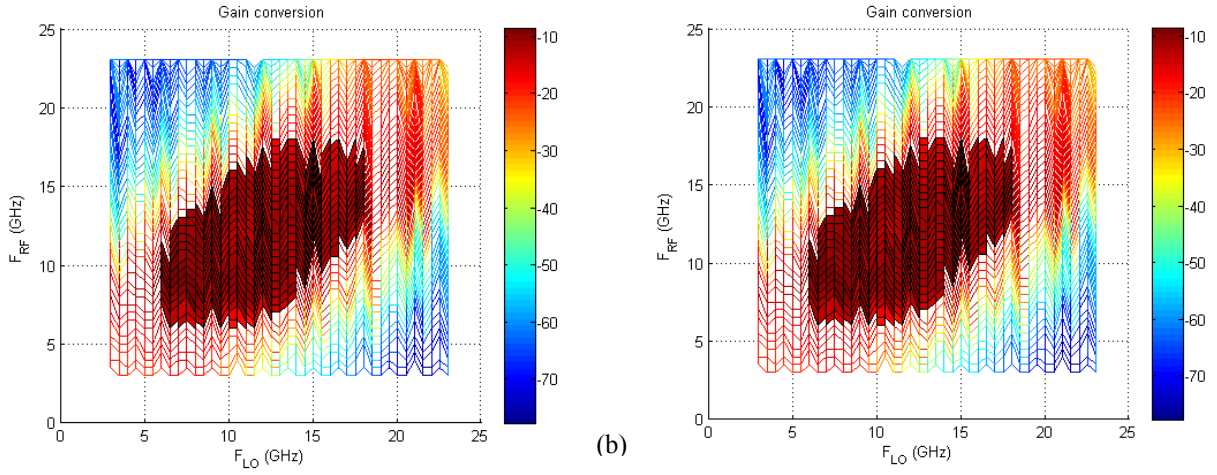

Fig. 5.12 Gain conversion for $\Delta F = |F_{RF1}-F_{RF2}| = 100kHz$ (a) and 1MHz (b).

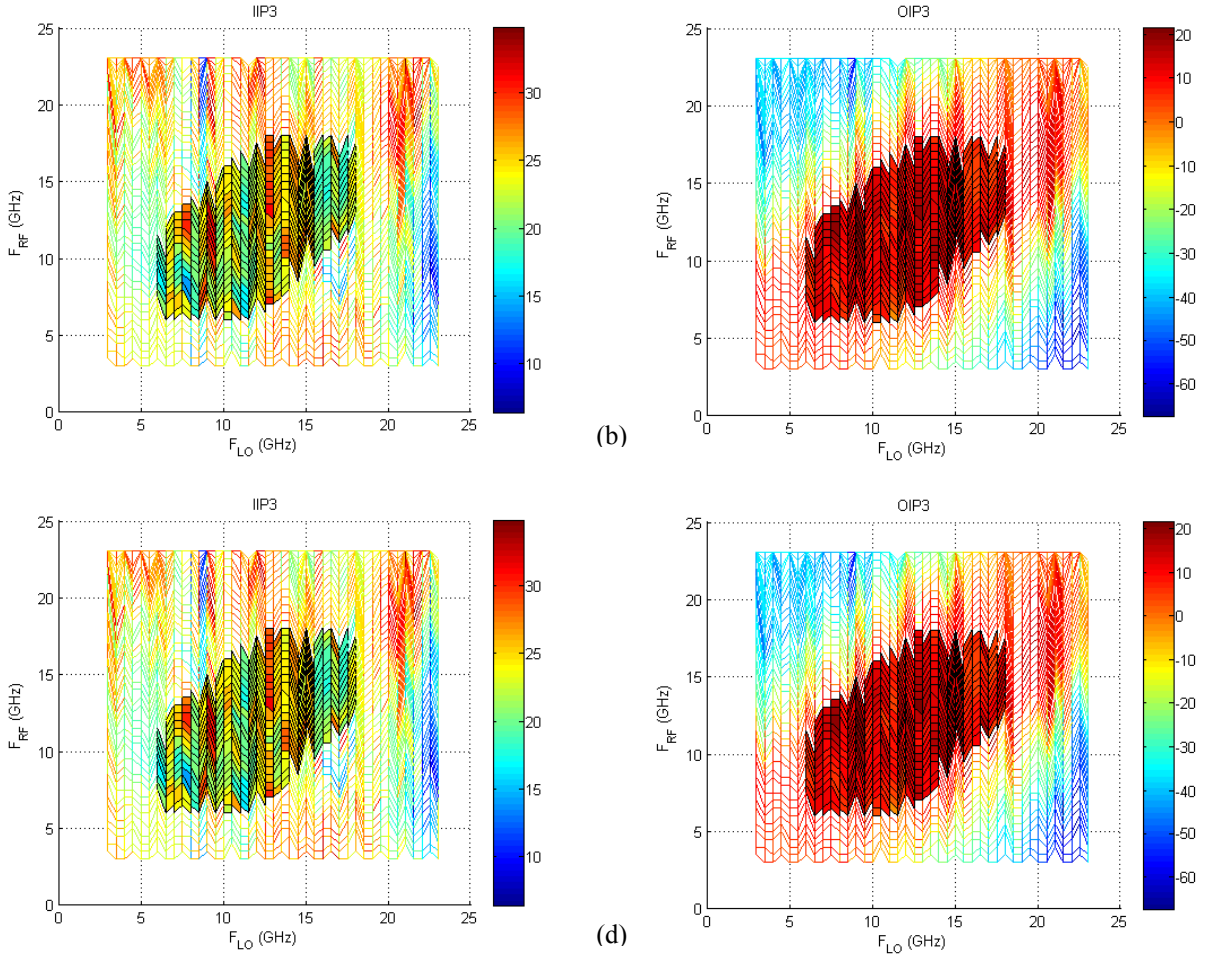

Fig. 5.13 : Third order input and output interception points. (a) IIP3, ΔF=100kHz. (b) OIP3, ΔF=100kHz. (c) IIP3, ΔF=1MHz. (d) OIP3, ΔF=1MHz.

The good linearity properties of the designed mixer are also pointed out by the output and input interception points obtained for either ΔF (Fig. 5.13). The interception points are related by the relationship:

OIP3 = IIP3 + Gc,

and represent the high potentiality of resistive mixers to naturally eliminate the harmonic intermodulation products, which can be here considered. Thanks to this behaviour the products of intermodulation can be considered negligible.

The Table 5.2 summarizes all the characteristics we obtained by simulation for our hybrid, GaN-based, resistive mixer.

TABLE 5.2 :
SUMMARY TABLE OF RESULT FOR SIMULATION OF MIXER
ONE AND TWO TONES

	Simulation Results
Bandwidth F_{RF} (GHz)	6 → 18
Bandwidth F_{LO} (GHz)	6 → 18
Bandwidth F_{IF} (GHz)	DC → 6
Conversion gain (dB)	-10.5 → -16
Insulation LO/RF (dB)	2.7 → 11.4
Insulation RF/LO (dB)	7 → 18
Insulation LO/IF (dB)	6.8 → 48
Insulation RF/IF (dB)	12 → 67
OIP3 (dBm)	5 → 20

5.3 Conclusion

In this chapter, the problem of accurately predicting the cold FET behaviour has been faced. Two models have been extracted for this application.

The empirical, behavioural NDC model has been adopted to model the cold-FET behaviour of a GaAs PHEMT: it has been validated in large-signal conditions, by exploiting LS measurements carried out at the University of Leuven, and it has shown very good performances in predicting some of the main figures of merit in mixer applications.

The EV model has been, instead adopted for an AlGaN/GaN HEMT and a wideband, single-ended, resistive mixer has been designed by means of this model. Electric and electromagnetic CAD simulations show very good performances in terms of band and linearity, with conversion

losses smaller than 16 dB over all the band. The mixer will be realized at the IEMN laboratories in hybrid technology.

The so far described modelling approaches are table-based, thus great importance is covered by the data interpolation algorithm, especially when high-linearity operation are involved and/or measurements on a dense voltage grid are not available. In Chapter 6, the original data approximation/interpolation algorithm, used in almost all our models, is described.

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Chapter 6

Interpolation Methods for LUT-based Models

The modelling of electron devices oriented to microwave circuits design must often face up the problem of device behaviour reconstruction from measured data. Accurate predictions under high-frequency large-signal operating conditions can be, in fact, obtained only provided that the model is able to approximate, through continuous and differentiable functions, the device nonlinear characteristics, such as static/pulsed I/V, C/V and Q/V relationships, which are necessarily known over a discrete grid of bias conditions.

Analogous problems are encountered in the behavioural modelling of communication system building blocks, such as, for instance, in power amplifiers, where AM/AM, AM/PM curves must be accurately reconstructed from sampled values.

The approximation can be obtained by means of analytic functions [1], or by using look-up-tables (LUT), [2]-[4]. Analytic functions, typically dependent on a limited number of scalar parameters, are widely adopted by many empirical modelling approaches: they usually provide fast numerical evaluation and reasonably good predictive accuracy, especially under saturated power operation. However, this kind of model can be, often, inadequate when accurate prediction of *local* nonlinearity, e.g. inter-modulation distortion (IMD), is needed, such as in the case of highly-linear Power Amplifier (PA) design [5]. In this latter kind of applications, many advantages can be obtained by exploiting nonlinear, empirical, LUT-based models, but a good and reliable interpolator is required.

To this aim, an original data approximation algorithm, here described, is used in our models:it is based on the strong analogy between time-domain signal reconstruction from a set of samples and the continuous approximation of device nonlinear characteristics on the basis of a finite grid of measurements. According to this criterion, nonlinear empirical device modelling can be carried out by using, in the sampled voltage domain, typical methods of the time-domain sampled-signal theory.

The full analytical development is provided in the following. In particular, besides the description of the approximating algorithm, we also provide a simple method for evaluating the *equivalent bandwidth* of the function to be approximated, that actually corresponds to “function nonlinearity”:

we assume, in fact, that the function $f(v)$ presents a sufficiently *smooth nonlinearity* (nearly band-limited function).

Experimental validation is also provided, by means of a 0.25-μm GaAs PHEMT: the developed approach is applied to its measured transcharacteristics, in order to evaluate the optimum discretization step and to outline the good reconstruction properties of the proposed approximator in comparison with classical Piece-Wise Cubic Splines and Piece-Wise-Linear interpolators. In addition, the approximating function is used with a LUT-based nonlinear model extracted for the same device, in order to provide a practical example of the good accuracy achievable in IMD prediction for high linearity power amplifiers.

6.1 A New Data Interpolation/Approximation Algorithm

6.1.1 Data Approximation

We first consider the problem of the continuous approximation of a generic nonlinear characteristic $f(v)$ of a single port electron device through a general-purpose function $\tilde{f}(v;\underline{P}) \cong f(v)$, where $\underline{P}$ represents a set of scalar parameters. In order to improve reliability and robustness in the parameter extraction phase, general-purpose approximating functions having a linear dependence on parameters (P_k) can be conveniently adopted, i.e.:

$$\tilde{f}(v;\underline{P}) = \sum_k P_k h_k(v) \tag{6.1}$$

where the $h_k(v)$ in (6.1) are a suitable set of *base functions*. This is a convenient choice since robust (i.e., unambiguous) parameter extraction can be carried out by means of linear regression procedures, provided that a sufficiently large set of measurements is used. The explicit dependence of the approximating function $\tilde{f}$ on the parameters P_k will be omitted in the following for the sake of notation simplicity.

Starting from this very general approach, a new method is proposed on the basis of the strict analogy between the approximation of nonlinear characteristics measured over a discrete voltage grid and the reconstruction of band-limited time-domain waveforms from sampled data. In particular, according to this analogy:

- voltage-domain corresponds to a virtual time-domain,

- measurements represent samples of the actual characteristic in the voltage space (analogously to the time-domain samples of a signal)
- function reconstruction (i.e., interpolation of samples) is carried out by low-pass filtering (LPF) the sampled function.

More precisely, let the samples of the function $f(v)$ be known over a uniform grid of voltages $v_k = k\,\Delta v$ in the measurement range $[v_{inf}, v_{sup}]$. In order to deal with the Fourier transform of $f(v)$, a very smooth extrapolation can be imagined outside the characterization interval. This extrapolation should satisfy two constraints:

1) the extended function should be absolutely integrable, i.e.:

$$\int_{-\infty}^{+\infty} \left| f(v) \right| dv < \infty, \tag{6.2}$$

so that the integral defining the Fourier-transform $\mathcal{F}\{f(v)\}$ is well defined;

2) the function behaviour in the extrapolated voltage region should correspond to an extremely smooth transition to zero values, in such a way that an almost linear extrapolation in the strict neighbourhoods of the measurement interval $[v_{inf}, v_{sup}]$ can be thought of to practical purposes.

Let $f_S(v)$ be the *voltage-domain sampled function*:

$$f_S(v) = \sum_k P_k \delta(v - k\Delta v), \tag{6.3}$$

where $P_k = f(k\Delta v)$, and $\delta(\cdot)$ is the Dirac delta function. According to the outlined analogy with the signal sampling theory, the approximating function $\tilde{f}(v)$ can be obtained through the linear convolution of a nearly-ideal Low-Pass-Filter (LPF) pulse response $h(v)$ and $f_S(v)$:

$$\tilde{f}(v) \doteq f_S(v) * h(v) = \sum_k P_k h(v - k\Delta v). \tag{6.4}$$

A special purpose choice of the LPF pulse response function $h(v)$, according to the behaviour of actual electron device characteristics ($f(v)$) is given in Section 6.1.2.

The generalization of the above approach to the reconstruction of device characteristics $f(v_1, v_2)$, defined on a bi-dimensional voltage domain, can be easily carried out by considering the pulse response $h_{2D}(v_1, v_2)$ of a nearly-ideal 2D-LPF. In the present work we assume:

$$h_{2D}(v_1, v_2) = \Delta v_1 \Delta v_2 \sum_k h_1(v_1) h_2(v_2), \tag{6.5}$$

where $h_1(\cdot)$ and $h_2(\cdot)$ are the pulse responses of 1D-LPF's defined accordingly to the behaviour of $f(v_1, v_2)$ with respect to the variables v_1, v_2, respectively under suitable function sections (see Section 6.1.5).

Thus, if $P_{k,r} = f(k\Delta v_1, r\Delta v_2)$ are the 2D samples over the v_1, v_2 voltage grid, the bi-dimensional reconstructing formula for *F* becomes:

$$\tilde{f}(v_1, v_2; \underline{P}) = \Delta v_1 \Delta v_2 \sum_{k,r} P_{k,r} h_1(v_1 - k\Delta v_1) h_2(v_2 - r\Delta v_2) \ . \tag{6.6}$$

Due to this straightforward generalization based on variables separation, the approximating procedure will be dealt with by considering the simple mono-dimensional case in the following section.

Two main issues must be faced off in order to make the proposed approach feasible. First, a reasonable approximation of a nearly-ideal FIR filter must be analytically defined, by satisfying specific requirements for the application to empirical electron device modelling. Second, an estimation of the *equivalent bandwidth* associated with the function $f(v)$ must be provided in order to chose the appropriate LPF bandwidth.

6.1.2 Nearly-ideal FIR filtering

A *frequency-equivalent* domain is first introduced by considering two new variables: $\varphi = 1/v$ [V^{-1}] and $\Omega = 2\pi\varphi = 2\pi/\Delta v$ [rad V^{-1}], equivalent to frequency and angular frequency, respectively. Then, let $F[\Omega] = \mathcal{F}\{f(v)\}$ and $H[\Omega] = \mathcal{F}\{h(v)\}$ be the Fourier-transforms of the function $f(v)$ and the LPF pulse response $h(v)$, respectively.

As it is well known, an ideal band-limited filter in the Ω-domain would involve an infinitely long pulse response in the voltage domain *v*. Since this cannot be practically implemented, a nearly-ideal Finite Impulse Response (FIR) filter must be adopted, which involves some approximations in the function reconstruction. However, the FIR-LPF filter has also the advantage of providing a smoothing effect on the noise-like measurement errors.

The shape of the 1D pulse responses $h_i(v_i)$ (*i*=1,2) in (6.5) must be chosen for a smooth function approximation, by taking also into account specific requirements of nonlinear electron device

modelling, i.e.: linear exactness (i.e., linear $f(v)$ with linear sequence of P_k's), monotonic correctness (i.e., monotonic $f(v)$ with monotonic sequence of P_k's), fast asymptotic convergence (e.g., approximation error decreasing at least quadratic for $\Delta v \to 0$). Finally, the approximating function $\tilde{f}(v)$ should be at least once differentiable in order to guarantee convergence of the HB algorithms. However, *n*-times differentiability (with *n* as high as possible) and compatibility with accurate representations of higher order derivatives are also of primary importance in the accurate prediction of intermodulation distortion [6].

A pure Piece-Wise Linear (PWL) interpolation of the function samples $f(k\Delta v)$ corresponds to a triangular LPF pulse response $h_T(v)$ and to a squared *sinc* filter shape in the equivalent angular frequency domain: $H_T[\Omega] = \Delta v \cdot \mathrm{sinc}^2(\Omega \Delta v / 2\pi)$. This choice satisfies linear exactness, monotonic correctness and fast asymptotical convergence, but unfortunately it is not differentiable. Another very common choice in the framework of LUT-based modelling consists in adopting a cubic spline base function $h_{SP}(v)$ [7]. This choice provides computationally efficient interpolations, which are three-times differentiable. Unfortunately, it does not necessarily satisfies linear exactness introducing the risk of a spurious oscillating behaviour on the function and its derivatives.

We propose an "hybrid" filter, whose impulse response $h(v)$ can be analytically expressed in the voltage domain as the convolution of a triangular and a Gaussian function:

$$h(v) = h_T(v) * h_G(v) \tag{6.7}$$

where:

$$h_T(v) = \begin{cases} 1 - \dfrac{|v|}{\Delta v} & 0 \le |v| \le \Delta v \\ 0 & \text{otherwise} \end{cases} \tag{6.8}$$

and:

$$h_G(v) = \frac{1}{\sqrt{2\pi\sigma^2}} \exp\left(\frac{-v^2}{2\sigma^2}\right). \tag{6.9}$$

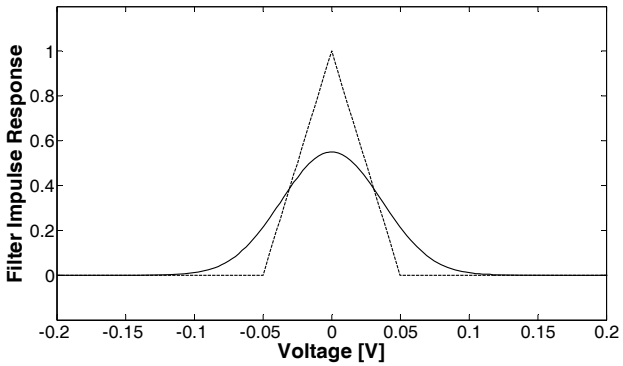

Fig. 6.1. LPF impulse response in the voltage domain, in the case of the proposed hybrid LPF (continuous line) and in the case of a *sinc*^{2} LPF which correspond to PWL interpolation (dashed line).

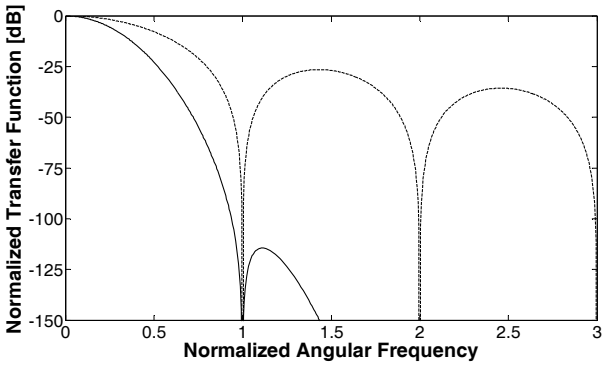

Fig. 6.2. LPF response in the normalized angular frequency domain, in the case of the proposed hybrid LPF (continuous line) and in the case of a *sinc*^{2} LPF which correspond to PWL interpolation (dashed line). Angular frequency axis normalized to $2\pi/\Delta v$.

The corresponding $H[\Omega]$ consists in the cascade of a *sinc*^{2} and a Gaussian-like transfer function in the Ω-domain, i.e.:

$$H(\Omega) = \Delta v \cdot \exp\left(\frac{-\sigma^2\Omega^2}{2}\right) \cdot \mathrm{sinc}^2\left(\frac{\Omega \Delta v}{2\pi}\right) \doteq \Delta v \cdot \bar{H}(\Omega). \tag{6.10}$$

where $\bar{H}[\Omega] \doteq H[\Omega]/\Delta v$ is here defined for the sake of subsequent notation simplicity.

This leads to a smooth and non-oscillating data approximation, which can also be interpreted as the Gaussian filtering of a PWL interpolator. The LPF pulse response (6.7) and the corresponding Fourier transform (6.10) are plotted in Fig. 6.1 and Fig. 6.2, respectively.

In practice, PWL interpolation gives linear exactness, no spurious oscillations and fast decreasing errors, while the highly effective smoothing of Gaussian filtering (besides preserving these features) provides both differentiability and measurement noise reduction. With exact (i.e., non-truncated) Gaussian filtering, the approximating function would be infinitely differentiable, while only first-

order differentiability is achieved after Gaussian-pulse-response truncation. However, reasonable truncation criteria easily lead to practically negligible discontinuities in higher-order derivatives.

6.1.3 Function reconstruction in the equivalent frequency domain

Let $F_S[\Omega]=\mathcal{F}\{f_S(v)\}$ be the F-transform of the sampled function (6.3). It is well known [8] that:

$$F_S[\Omega]=\frac{1}{\Delta v}\sum_{m=-\infty}^{+\infty}F\left[\Omega+m\frac{2\pi}{\Delta v}\right]. \tag{6.11}$$

Thus, the F-transform $\tilde{F}[\Omega]=\mathcal{F}\left\{\tilde{f}(v)\right\}$ of the approximated function (6.4), is easily evaluated by taking into account (6.10) and (6.11), as:

$$\tilde{F}[\Omega]=F_S[\Omega]\cdot H[\Omega]. \tag{6.12}$$

Thus, the proposed function approximation based on (6.4), or similarly on (6.12), is equivalent to the well-known signal reconstruction procedure from sampled data.

It is worth noting that the approximation of the n$^{\text{th}}$-order derivative $\tilde{f}^{(n)}(v)$ and its F-transform $\tilde{F}^{(n)}[\Omega]=\mathcal{F}\left\{\tilde{f}^{(n)}(v)\right\}$ are also easily expressed by using known differentiation properties of F-transforms, as:

$$\tilde{f}_S^{(n)}(v)\doteq f_S^{(n)}(v)*h(v) \tag{6.13}$$

$$\tilde{F}^{(n)}[\Omega]=F_S^{(n)}[\Omega]\cdot H[\Omega]. \tag{6.14}$$

with:

$$F_S^{(n)}[\Omega]=\frac{1}{\Delta v}\sum_{m=-\infty}^{+\infty}F^{(n)}\left[\Omega+m\frac{2\pi}{\Delta v}\right]=\frac{1}{\Delta v}\sum_{m=-\infty}^{+\infty}\left[j\left(\Omega+m\frac{2\pi}{\Delta v}\right)\right]^n F\left[\Omega+m\frac{2\pi}{\Delta v}\right]. \tag{6.15}$$

6.1.4 Equivalent Bandwidth

In our analogy, “signal bandwidth” actually corresponds to “function nonlinearity”, so that we assume that the function $f(v)$ presents a sufficiently *smooth nonlinearity* (nearly band-limited function).

A particularly intuitive indicator of the equivalent bandwidth of $f(v)$ is related to the second-order derivative $f^{(2)}(v)$. In fact, nonlinearity of the function $f(v)$ mainly occurs where the $f^{(2)}(v)$ is sensibly different from zero. Since an extremely smooth extrapolation of the function $f(v)$ is assumed outside the measurement interval, almost negligible values of $f^{(2)}(v)$ are obtained in these regions. However, the bandwidth can be evaluated equivalently by considering a generic nth-order derivative of $f(v)$, with n=0, 1, 2,…

To this aim, we consider the quadratic deviation error between the nth-order function derivative $f^{(n)}(v)$ and its approximation $\tilde{f}^{(n)}(v)$, with n=0, 1, 2, 3,… (where: $f^{(0)} \equiv f$ and $\tilde{f}^{(0)} \equiv \tilde{f}$):

$$\varepsilon_n^2 = \int_{-\infty}^{+\infty} \left| f^{(n)}(v) - \tilde{f}^{(n)}(v) \right|^2 dv \,. \tag{6.16}$$

This error can be evaluated, for an assigned function $f(v)$, in correspondence with each particular choice of a sampling voltage step Δv and a standard deviation value σ. In addition, according to Bessel's equality [8] the squared error (6.16) can be also evaluated as:

$$\varepsilon_n^2 = \frac{1}{2\pi} \int_{-\infty}^{+\infty} \left| F^{(n)}[\Omega] - \tilde{F}^{(n)}[\Omega] \right|^2 d\Omega \,, \tag{6.17}$$

being $F^{(n)}[\Omega] = \mathcal{F}\left\{ f^{(n)}(v) \right\}$.

By assuming that $f(v)$ is a nearly band-limited function, an *Equivalent Effective Bandwidth* B can be defined, such as:

$$\left| F^{(n)}[\Omega] - \tilde{F}^{(n)}[\Omega] \right| = \begin{cases} \bullet \ \left| 1 - \bar{H}[\Omega] \right| \cdot |\Omega|^n \cdot |F[\Omega]| & \text{with: } |\Omega| \le B; \\ \bullet \ \left| \bar{H}[\Omega] \right| \cdot \left| m\frac{2\pi}{\Delta v} + \Omega \right|^n \cdot \left| F\left[m\frac{2\pi}{\Delta v} + \Omega \right] \right| & \text{with:} \\ m\frac{2\pi}{\Delta v} - B \le |\Omega| \le m\frac{2\pi}{\Delta v} + B \quad (m = \pm 1, \pm 2, ...); & \\ \bullet \ 0 \qquad \text{elsewhere;} & \end{cases} \tag{6.18}$$

where the term valid for $|\Omega| \le B$ takes into account the in-band error contributions, while the other terms account for the out-of-band error components related to translated spectra.

According to (6.18), the squared error (6.17) may be evaluated after simple algebraic manipulation, as:

$$\varepsilon_n^2 = \frac{1}{\pi}\int_0^B D^2[\Omega]\cdot|\Omega|^{2n}\cdot|F[\Omega]|^2\, d\Omega\,, \tag{6.19}$$

where

$$D^2[\Omega] = |1-\bar{H}[\Omega]|^2 + \sum_{m=1}^{\infty}\left\{\left|\bar{H}\left[m\frac{2\pi}{\Delta v}-\Omega\right]\right|^2 + \left|\bar{H}\left[m\frac{2\pi}{\Delta v}+\Omega\right]\right|^2\right\}. \tag{6.20}$$

Thus, the equivalent bandwidth can be identified through a simple search over the one-dimensional space of the B values, in such a way to simultaneously satisfy (6.16) and (6.19) for any particular choice of Δv and σ.

6.1.5 Experimental Validation

Experimental validation is carried out by means of a 0.25 μm GaAs PHEMT device (W=600 μm). Static characteristics of the Device Under Test (DUT) are first measured on a dense grid of voltages, namely Δv_{GS} = 50 mV, Δv_{DS} =125 mV, and the trans-characteristic approximation is considered as a first practical application of the outlined theory. The considered I/V curve ($f(v)$) is plotted in Fig. 6.3 at V_{DS} = 5 V over the characterization range [-1.5 V ÷ 0.5 V]. The adopted grid is dense enough to provide a sufficiently accurate evaluation of the device characteristics and their derivatives up to the 5th-order through standard numerical differentiation algorithms [7].

According to the procedure outlined in Section 6.1.1, the measured function is extrapolated outside the characterization interval by using standard Blackman-Harris windowing functions. This should guarantee an extremely smooth transition to zero. Two possible examples (a, b) are plotted in Fig. 6.3. Corresponding F-transforms $F^{(2)}[\Omega]$ of the second order function derivative are plotted in Fig. 6.4. When the transition to zero provides a sufficiently smooth extrapolation (a-case in Fig. 6.3), any further softening of $f(v)$ (b-case) causes only minor changes in $F^{(2)}[\Omega]$, as it can be seen in Fig. 6.4.

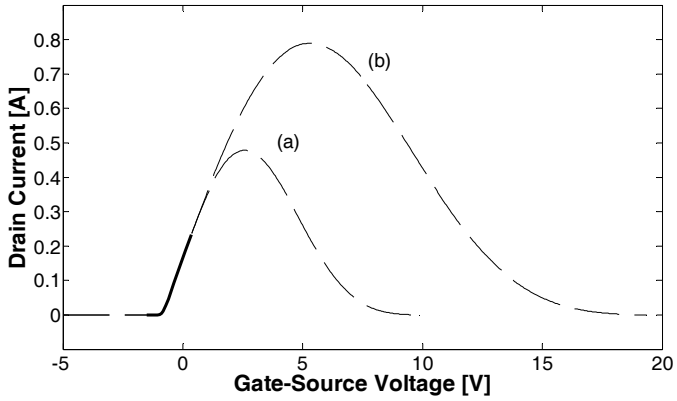

Fig. 6.3. Extended device trans-characteristic at V_{DS}=5V. Two different extrapolation cases (a) and (b) are considered (see text).

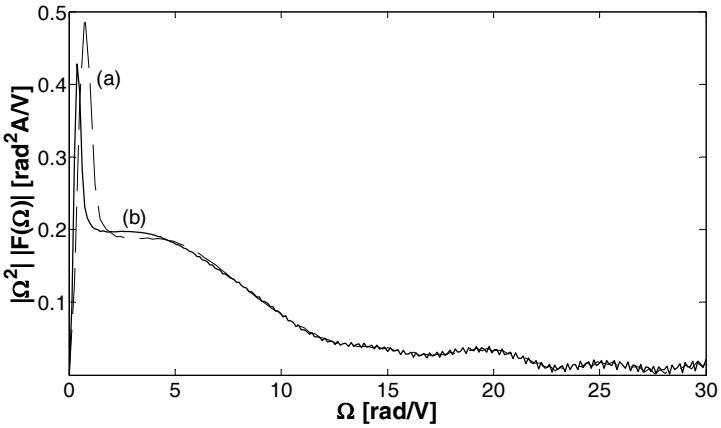

Fig. 6.4. Fourier transforms of the 2nd-order derivative of the extended trans-characteristic. The two different plots refer to the extrapolations (a) and (b) in Fig. 6.3.

In order to completely define the base function $h(v)$ described in (6.7)-(6.9), a proper value of the standard deviation σ must be specified. To this aim, we consider, as a first guess, the value providing a given attenuation (A) of the Gaussian filter (6.9) at the angular frequency $2\pi/\Delta v$ in the equivalent Ω-domain, i.e.:

$$H_G\left[\frac{2\pi}{\Delta v}\right] = A^{-1} \tag{6.21}$$

where: $H_G[\Omega] = \mathcal{F}\{h_G(v)\}$ and A=10^3 in our example. The frequency $2\pi/\Delta v$ corresponds to the central value of the first repetition of the $F[\Omega]$ spectral components in (6.11). By considering (6.9) and (6.21), we obtain:

$$\sigma = \frac{\Delta v}{2\pi}\sqrt{2\ln A}\,. \tag{6.22}$$

In our example, by also taking into account that $\Delta v \equiv \Delta v_{GS}$=50 mV, a first guess σ value of about 0.029 is calculated through (6.22).

The squared error deviations described in (6.16) are now evaluated in the voltage domain. In particular, the approximated trans-characteristic function and its nth-order derivatives $\tilde{f}^{(n)}(v)$ (for each n=0,1,2,3) are evaluated through (6.4) by letting $P_k = f^{(n)}(k\Delta v)$ for each *n*-value. To this aim, standard numerical differentiation techniques are used for the evaluation of the P_k coefficients when $n \geq 1$. The obtained squared errors are reported in Table 6.1. It is worth noting that only slightly different error values are obtained by extending the evaluation range to the whole voltage axis or by limiting the calculation to the strict measurement range. In fact, the approximation error outside this range is almost negligible due to the extremely smooth extrapolation of $f(v)$.

As outlined in Section 6.1.4, the same deviation errors (6.16) are obtainable through (6.17) after evaluations of the F-transforms $F^{(n)}[\Omega]$ (through standard FFT routines) and $\tilde{F}^{(n)}[\Omega]$ (through (6.14)).

TABLE 6.1
SQUARED DEVIATION ERRORS
(STANDARD UNITS)

	Measured Voltage Domain	Extended Voltage Domain
ε_0^2	3.9051 x 10^{-8}	4.4671 x 10^{-8}
ε_1^2	1.1846 x 10^{-6}	1.1855 x 10^{-6}
ε_2^2	1.2035 x 10^{-4}	1.2059 x 10^{-4}
ε_3^2	2.3200 x 10^{-2}	2.3316 x 10^{-2}

In order to be coherent with the evaluation of the coefficients reported in Table 6.1, the same values of voltage step Δv=50 mV and standard deviation σ=0.029 are used in the evaluation of (6.14).

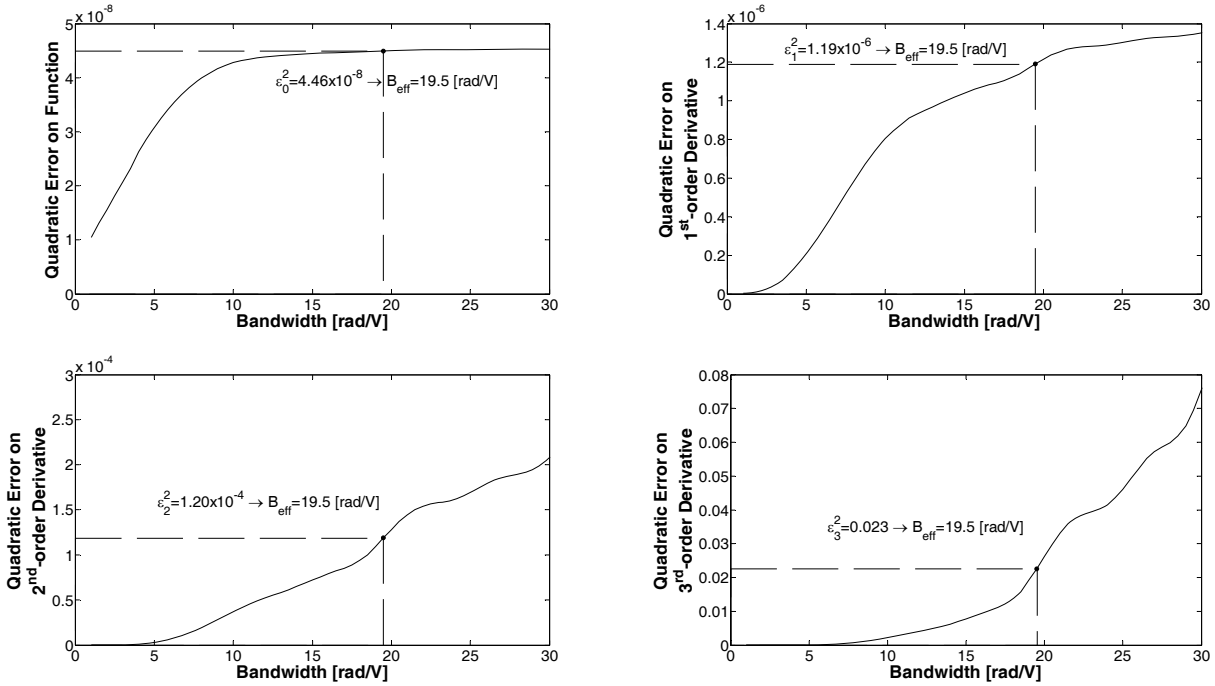

Fig. 6.5. Deviation errors evaluated through (6.19)-(6.20) for different guess values of the equivalent bandwidth. The effective bandwidth B_{eff} is calculated in correspondence with the error values listed in Tab. 6.1.

As already pointed out, in the hypothesis that $f(v)$ is a nearly band-limited function, an effective bandwidth B can be defined so that (6.17) can be substituted by (6.19)-(6.20). Deviation error evaluations (n=0,1,2,3) through (6.19)-(6.20) are shown in Fig. 6.5 for different guess values of the B parameter. After comparison with the values reported in Tab. 6.1, the effective bandwidth (B_{eff} in Fig. 6.5) is evaluated as about 19.5 rad/V, corresponding to the theoretical Nyquist sampling voltage step:

$$\Delta v_N = \frac{\pi}{B_{eff}}. \tag{6.23}$$

A Δv_N value of about 161 mV is calculated in our example and the initially adopted measurement step $\Delta v \equiv \Delta v_{GS}$ =50 mV is found out as corresponding to about three times the Nyquist rate.

The proposed approximating method is then compared with standard PWL and piece-wise cubic Splines, which are readily available in most of the commercial CAD tools. Reconstruction of the measured function and its n^{th}-order derivatives up to the 5^{th} order are shown in Fig. 6.6 for two different sampling rates (only odd n^{th} order derivatives are reported here).

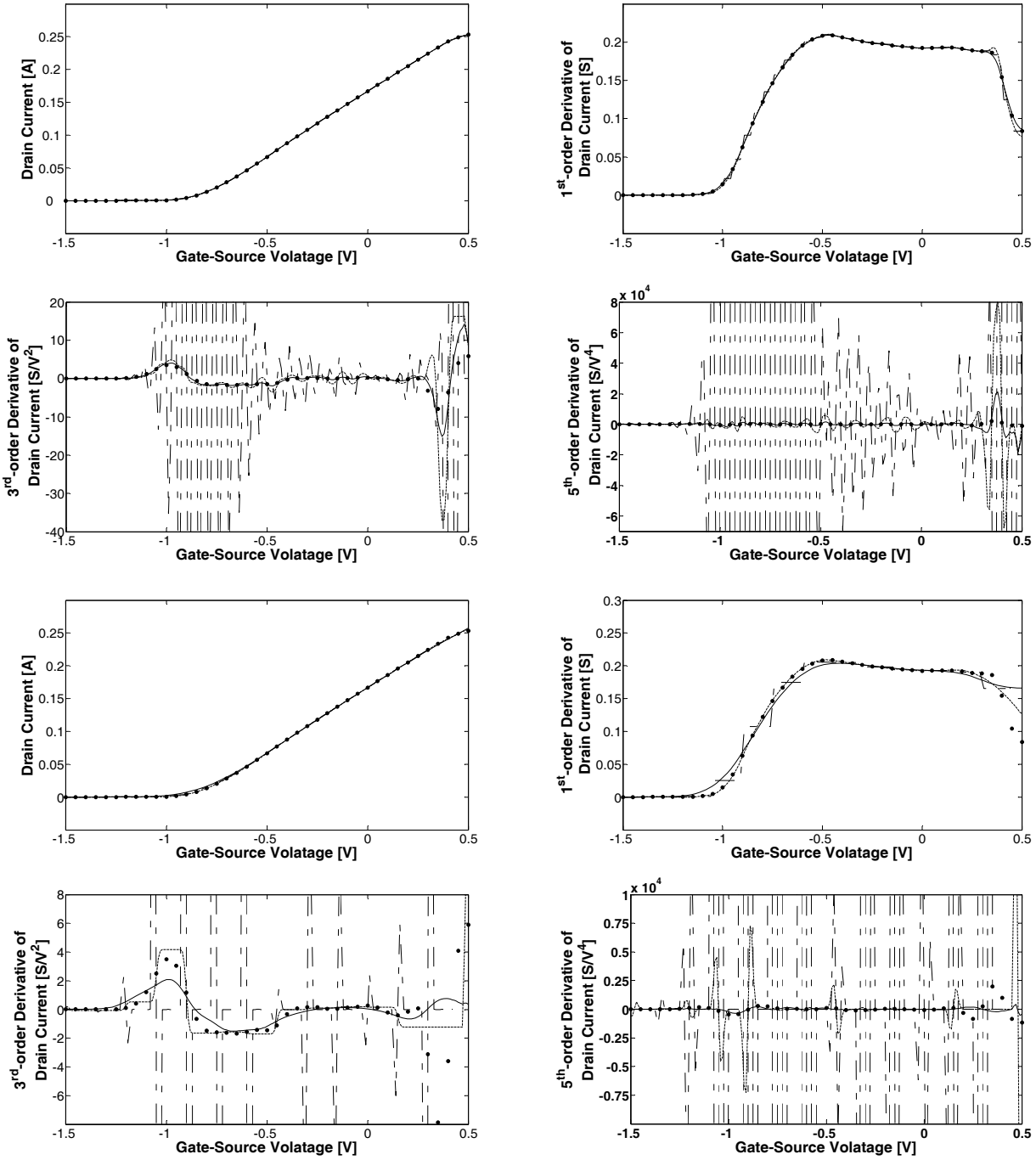

Fig. 6.6. I/V trans-characteristic of the 0.25 μm PHEMT at V_{DS} = 5 V and its derivatives with respect to V_{GS}. Comparison between the measured functions (dots) and the reconstructed functions using PWL interpolator (dashed-dot lines), cubic-splines (dashed lines) and the proposed approximation formula (solid lines). Two different voltage sampling rates are adopted for the reconstruction: 1) almost three-times the Nyquist sampling rate: $\Delta v = 50mV$ (upper four plots) and 2) the almost Nyquist sampling rate: $\Delta v = 150mV$ (lower four plots).

Finally, the proposed approach is used for the data approximation in the EV model [4] of the same 0.25 μm GaAs PHEMT. In this framework, not only static and low-frequency I/V current functions are reconstructed, but also typical C/V characteristics. Intermodulation distortion results at 37 GHz are shown in Fig. 6.7 for a power amplifier operating in AB-Class. Extremely accurate

predictions are obtained even at very low power levels, where the representation of the local nonlinearities through data interpolation plays a primary role.

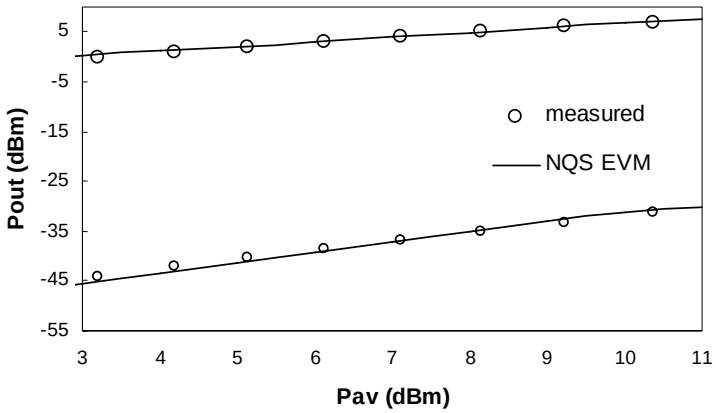

Fig. 6.7 IMD the 0.25 μm PHEMT at 37 GHz (Class-AB bias). Meas. (circles) vs. LUT-based Equivalent Voltage Model [4] (solid line). Z_S=49.547Ω-j*9.65Ω, Z_L=30.7Ω-j0.88Ω.

6.2 Conclusion

A function reconstruction technique has been presented in this chapter, by outlining the analogy existing between function sampling in the voltage domain and signal sampling in time. The proposed procedure, which also defines a smooth data extrapolation method, is shown to provide extremely accurate descriptions of the function and its derivatives not only over the initial grid of voltages but in any evaluating condition. Practical calculation of the effective bandwidth and criteria for the design of a nearly ideal FIR-LPF are provided. Experimental validation is carried out by means of measured I/V characteristics of a GaAs microwave PHEMT.

In the next chapter, a slightly different topic is dealt with: the electron device degradation. In fact, great interest could have a model capable of predicting the long-term device performances, accounting for the eventual degradation suffered during the operating conditions. To this aim, the first step is to characterize the device degradation: a suitable measurement setup will be described in Chapter 7 and preliminary experimental results will be shown.

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Chapter 7

Electron Device Degradation

Microwave circuit design requires an accurate and complete experimental characterization of electron devices, in order to extract empirical device models providing accurate predictions at different bias and loading impedance conditions. However, electron devices may "change" their characteristics when observed at different time instants under identical forcing excitations. Two repetitions of the same measurement procedure (e.g., a DC I/V characteristic investigation over a given bias grid) can give significantly different results. Analogously, an electrical parameter under test (e.g., the device transconductance g_m) can show a considerable time dispersion even under steady-state operation (e.g., periodic or quasi-periodic regime forced by sinusoidal excitations).

Since the whole device is subjected to time dispersion, theoretically, each characteristic or parameter (defined under DC or AC operation) could be a good indicator of device dispersion; nevertheless some parameters have been considered more interesting than others due to their intuitive impact on device performance. A significant example, well-reported in the literature, is the breakdown walkout, that is the increasing values obtained at each measurement trials for the drain-gate and drain-source breakdown voltages (BV_{DG} and BV_{DS}, respectively), experimentally observed in field-effect microwave transistors (MESFETs, HEMTs, PHEMTs) when the device is biased under high electric field [1]-[4]. It is worth noting that the breakdown voltage (and consequently its walkout) is extremely important in amplifier design, since it limits de facto the power achievable by a given technology: for this reason, new microwave device technologies (e.g., GaN) are oriented to maximize this parameter. The breakdown walkout is a permanent effect; it could appear as a beneficial effect, but it is often accompanied by the degradation of other key electrical parameters of the device such as, for instance, I_{DSS}, g_m or the threshold voltage, even though to a minor extent. Moreover, important drops in RF output power have been observed after long lasting strong gain compression operation, provided that the combination of bias, matching networks and signal drive causes the dynamic load line to reach the reverse pre-breakdown region [5]. This degradation of the device characteristics, in fact, can be related to the stress that the device physical structure suffers under specific operating conditions involving high electric fields and/or high current densities.

Progressive modification (i.e., degradation) of the device electrical response is induced with respect to the one originally offered at its very first connection to the measurement system. This is clearly evident in the presence of critical operation, such as the reverse hot-electron discharge from gate in FETs, but can be also observed in correspondence with more “conventional” and nominally safe operating conditions, as when the device is employed in a class-A power amplifier and operates well inside the compliances on maximum power dissipation.

The empirical investigation on the degradation of electron device characteristics is usually carried out by forcing the transistor samples in DC stressing operation for a relatively long time (from minutes up to several hours): electrical modifications are, then, observed either at the end of the stress procedure or during the execution of the test (e. g. [1]-[7]). Exploitation of DC measurement set-ups gives great advantages in terms of hardware simplicity and accuracy-control capabilities. However, in such a case the device is excited according to very different regimes with respect to operation in actual microwave nonlinear circuits. Instead, degradation mechanisms inducing the walkout of the device characteristics may be stimulated also under dynamic operation, in a way much more similar to realistic conditions encountered in actual circuit applications. Nevertheless, a very few contributions can be found in the literature which deal with stress procedures carried out under nonlinear dynamic operating conditions (e.g., see [8]-[13]).

We have assembled a fully automated laboratory set-up, which is capable of inducing stress mechanisms in a given electron device not only under quiescent, bias-dependent operation, but also in a non-linear dynamic regime [13]-[14]. The AC forcing signal can be injected indifferently either at the input or the output port of the microwave electron device. In addition, the device characteristic walkout can be observed both at the end of a given stress procedure and during its execution, by monitoring the time-varying DC components and acquiring the waveforms of the parameter of interest.

In the following the hardware implementation of the laboratory set-up and its functional aspects are described, together with the control software which fully automates the measurement procedure. Several experimental examples of time dispersion observed under both DC and RF stress conditions are also provided.

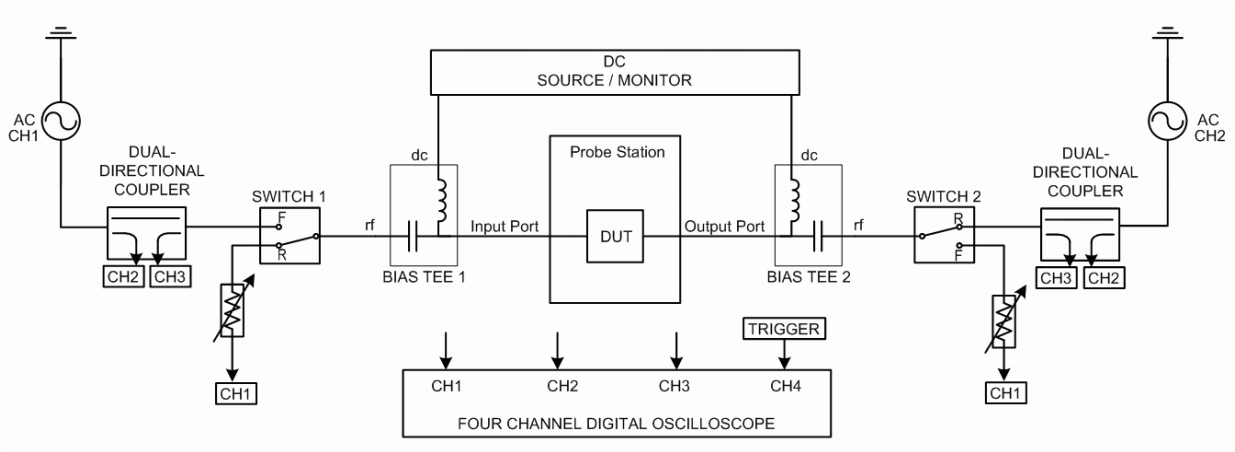


Fig. 7.1. Architecture of the proposed nonlinear RF measurement system.

7.1 A New Measurement Setup

7.1.1 Hardware Description

The functional representation of the system architecture is shown in Fig. 7.1. The measurement set-up allows for the characterization of the walkout of the DUT response by driving it under either *forward* or *reverse* dynamic excitation conditions. More precisely, we will refer to *forward operation* when the AC signal is applied at the device input port (gate/base for FETs/bipolars in a common-source/-emitter configuration), and to *reverse operation* when the AC signal is injected at the output port (drain/collector).

In order to avoid sources of uncertainty related to the system mounting, two switches have been adopted to easily swap between the two basic configurations: when the switches are settled in position **F** the forward operation is selected, whereas when they are in position **R** the DUT works under reverse excitation.

The two independent output channels of an arbitrary function generator (in our case a Tektronix AFG320 having a 50-Ω output impedance) are adopted to feed the DUT with voltage sinusoidal waveforms, in the frequency range of several MHz, under forward or reverse operation. The system exploits a high resolution (4 μV; 20 fA) adequately accurate (V: 0.05%, I: 0.2%) bias system that, besides providing the voltage/current bias levels, monitors the average values of the electrical quantities at the two device ports (a HP4155B semiconductor analyzer). Two bias tees with bandwidth [100 kHz – 6 GHz] and low insertion loss (0.15 dB) are used for a suitable DC and RF path separation, and also for ensuring the stability of the operation. In fact, the presence of the bias tees allows to properly terminate the device avoiding oscillation problems.

The system switches in Fig. 7.1 are set for driving the DUT under reverse excitation. In this case, switch 2 connects the ac generator channel 2 to the device output port; both the incident and reflected waves are monitored by means of a broadband [10 kHz – 1 GHz] dual-directional coupler. Switch 1, instead, connects the DUT input port to an oscilloscope through a variable resistor, which allows to obtain different, purely resistive terminations in series with the 50-Ω/1-MΩ oscilloscope channel input impedance.

Three different waveforms are sampled on the system RF paths: the incident and reflected voltage waveforms at the output port of the selected AC generator channel, and the voltage waveform at the device input port. To this end, a digital oscilloscope (Agilent 54845A) with four input channels (each one operating independently up to 4 GSa/s) is adopted and triggered by means of the function generator.

The operation under forward mode is straightforward: it is forced by simply connecting the device input port to the AC generator channel 1 and the output port to the oscilloscope through the appropriate switch configuration. Thus, the system offers two different operation modes for stressing the device under non-linear dynamic conditions.

The great advantage of adopting the forward mode is essentially that the DUT is stressed under operating conditions similar to those involved in a microwave circuit. It is worth mentioning that under static conditions it is not possible to obtain similar information: for instance, when the device is biased for class-A operation without application of an RF signal, no stress is observed at all. Nevertheless, most of the works in the literature concerning the characterization of stress phenomena have been carried out under high voltage and\or high current quiescent operation; this is largely due to the fact that under these conditions an accelerated degradation of the device can be observed. By means of the proposed set-up, similar device stresses (but under dynamic condition) can be obtained by exploiting the reverse operating mode: for example, a FET device can be biased well under its pinch-off voltage and a sufficiently low drain bias voltage can be applied, in such a way to avoid static device stress: successively, the AC signal can be applied moving *dynamically* the device into the stress zone by increasing the AC amplitude.

As mentioned above, the system works at a moderately high frequency range, but well below the typical microwave frequencies. In fact, once large signal dynamic operation is forced, the device stress phenomena are practically not influenced by the actual operating frequency (e.g., see [15]): neither the linear parasitic access network or the high-frequency charge storage variation gives rise to stress phenomena. However, the operation frequencies adopted for the set-up must be well above the cut-off (some hundreds of kHz) of the LF *dispersive phenomena* (traps, self-heating) [16]. Otherwise, the choice of an excitation frequency in the dispersive region could determine a strong,

undesired dependence of the device response on the particular frequency adopted. Thus, the device walkout is investigated in an appropriate bandwidth, by forcing the degradation under dynamic conditions without involving the microwave reactive effects, with great advantages in terms of set-up architecture simplicity and reliability of the calibration procedures.

The measurement set-up can be obviously exploited to stress the device also under conventional static conditions by simply switching off the DC generator.

7.1.2 Control Software Description

When dealing with time dispersion characterization a large amounts of experimental data have to be collected, since very long-lasting measurements are typically required. For such a reason, measurement feasibility is strictly related to the automation software, which has to be considered an invaluable part of the measurement system. Moreover, the hardware flexibility (i.e., the capability of performing measurements under very different operations, switching between different configurations) has to be appropriately managed. For the proposed setup, the measurement procedure has been fully automated by means of a control software developed in the LabVIEW environment.

The software front panel is shown in Fig. 7.2. Depending on the DUT technology (FET or bipolar) or on desired measurements, the user chooses either a voltage or current bias by means of suitable source selectors and also sets up the voltage/current bias levels. Proper compliances on max current/voltage must also be set to protect the device: the measurement is, in fact, stopped if one of the two channels reaches its compliance value. In addition, the user can choose the hold time of the DC source/monitor unit before starting the first measurement (T_{hold}^{dc}), the sampling interval (T_{step}^{dc}) and the total number of samples of DC quantities to be acquired (N_s). Analogously, the number of oscilloscope successive acquisitions (N_a) and the waiting time before the first one (T_{hold}^{osc}) must also be set up, as well as the amplitude of the trigger and of the voltage sinusoidal waveform feeding the DUT in dynamic stress conditions. A DC stress can be simply obtained by switching off the function generator.

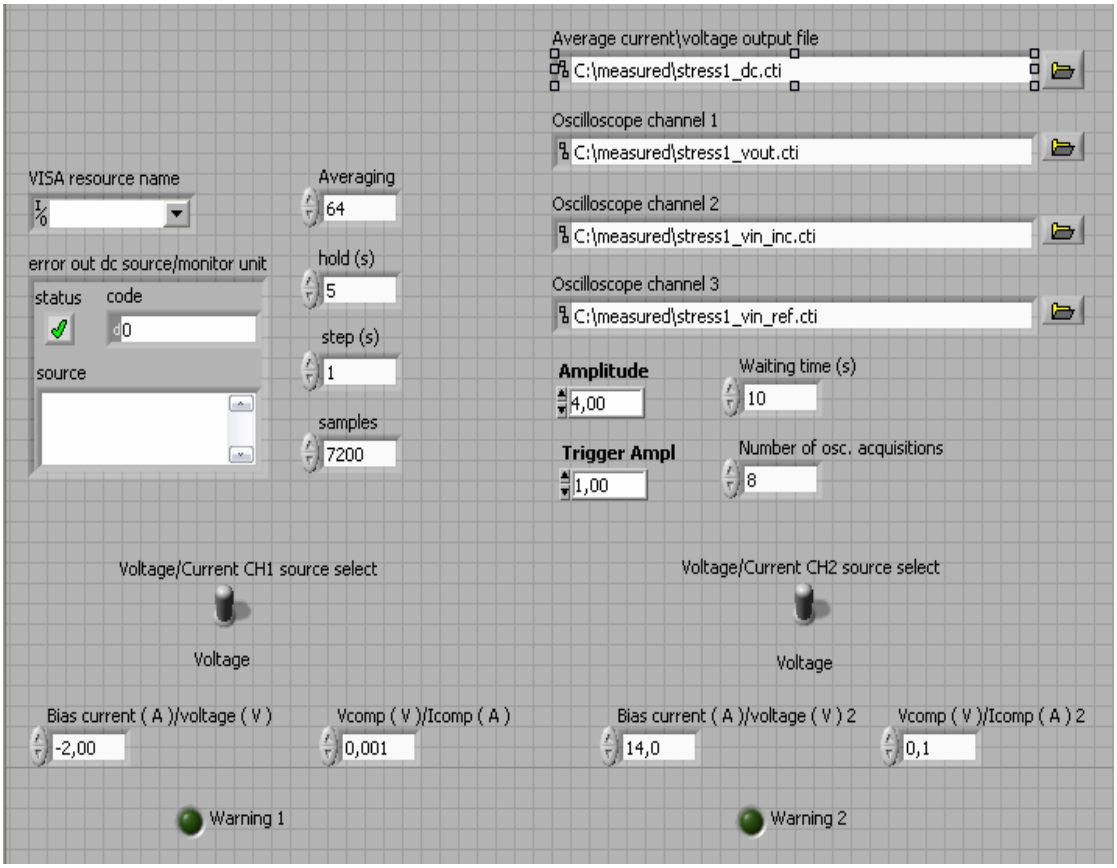


Fig. 7.2. Control panel of the automated measurement set-up.

The control algorithm is composed of three sequential stages:

1. instrument initialization;
2. DUT excitation and data acquisition;
3. data storage.

In the first phase, the bias system, the function generator and the oscilloscope are initialized according to the parameters specified by the user. In particular, the software computes the time step between the waveform acquisitions as $T_{step}^{osc} = (T_{Tot} - T_{hold}^{osc} - T_{meas}^{osc} \cdot N_a)/N_a$, where $T_{Tot} = T_{hold}^{dc} + T_{step}^{dc} \cdot N_s$ is the total measurement duration and T_{meas}^{osc} is the time required by the oscilloscope to sample a given period number of the waveforms.

The number N_a of waveform acquisitions must be consistent with the total measurement time T_{Tot}, so the software also controls that the calculated T_{step}^{osc} is positive, otherwise the routine execution is stopped and a warning message is sent to the user. The oscilloscope timing for the waveform acquisitions is plotted in Fig. 7.3.

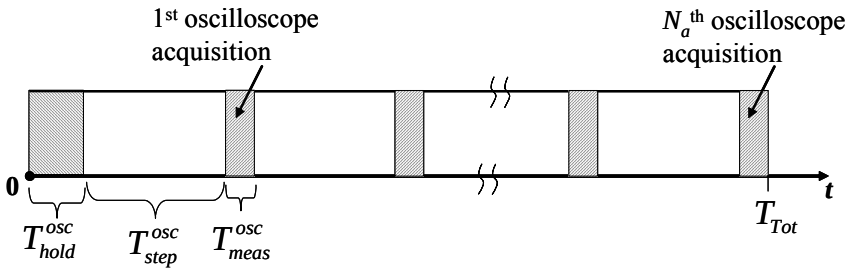


Fig. 7.3. Timing of the waveforms acquired by the oscilloscope.

The second stage of the control algorithm undertakes for the DC and ac DUT excitation, to be maintained during the whole time T_{Tot}, and for the acquisition of the measured data. Any event requiring the routine termination, such as any compliance reached or any unit oscillating, is also monitored.

Finally, the software writes all the gathered data into several files, in the 'citifile' format which is largely used by microwave CAD tools, so that they are immediately available to the user.

7.1.3 Experimental Examples: Forward Operation Mode

In this Section, some examples of device time dispersion forced in nonlinear dynamic operation through the proposed set-up will be provided. In particular, commercial on-wafer GaAs PHEMTs having 0.25-μm gate length and different gate widths are considered.

The proposed measurement set-up can be used to study the device walkout directly under dynamic operating conditions, which are similar to those associated with the actual circuit application.

As a preliminary experimental example, a 900-μm device is biased in the on-state region (V_{GS} = -0.9 V, V_{DS}=10V) and a 0.9-V amplitude AC signal applied to the gate port, according to the 'forward' set-up configuration. The load impedance in this test is 150 Ω (being the sum of the 100-Ω variable resistor and 50-Ω oscilloscope channel input impedance): this value is chosen so that the dynamic load line at the drain port reaches the pre-breakdown region. The duration of the stress is 500 seconds.

The DC characteristics $I_G(V_{DS})$ (for V_{GS} = -2 V), measured before and after the stress, are compared in Fig. 7.4, showing a significant device walkout, induced through nonlinear dynamic operation.

As clearly shown in Fig. 7.4, the dynamic stress modifies the device DC characteristics. Nevertheless, the most important issue is to quantify how much the device dynamic performances are degraded. To this aim, an 800-μm GaAs PHEMT device is biased according to class-A power

amplifier operation (V_{GS} = -0.6 V, V_{DS}= 8 V) and a 0.6-V amplitude AC signal is applied to the gate port. The load impedance in this test is 150 Ω. In Fig. 7.5, the corresponding dynamic load-line ($I_D(t)$ vs. $V_{DS}(t)$) is plotted, superimposed to the measured DC $I_D(V_{GS}, V_{DS})$ characteristics.

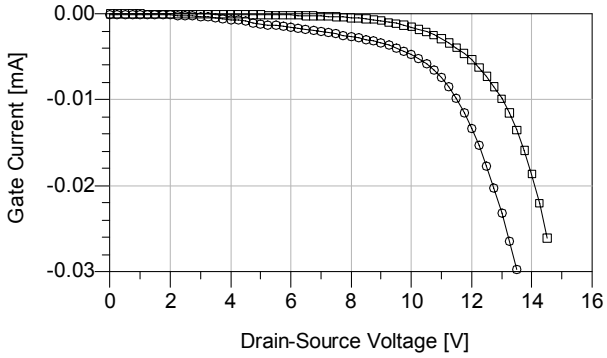


Fig. 7.4. Walkout observed in the DC gate current versus drain-source voltage after the stress of a GaAs PHEMT under 'forward' dynamic operating conditions: before (circles) and after stress (squares).

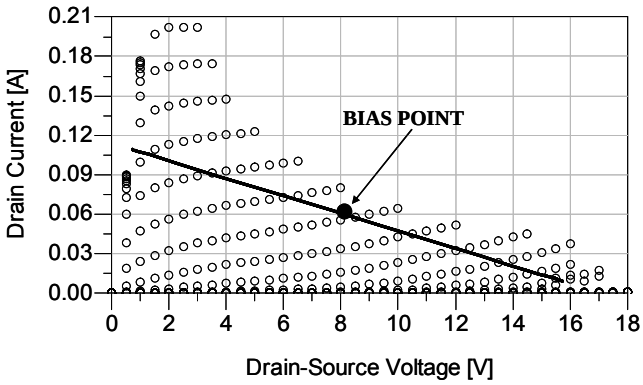
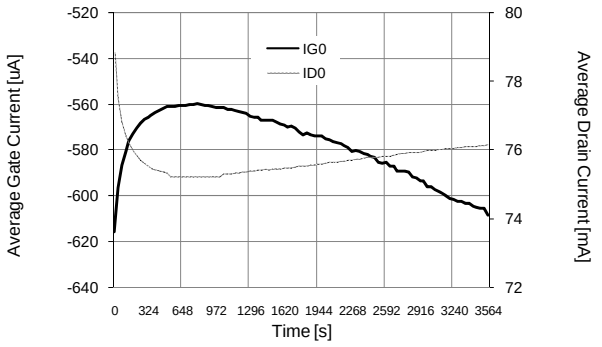
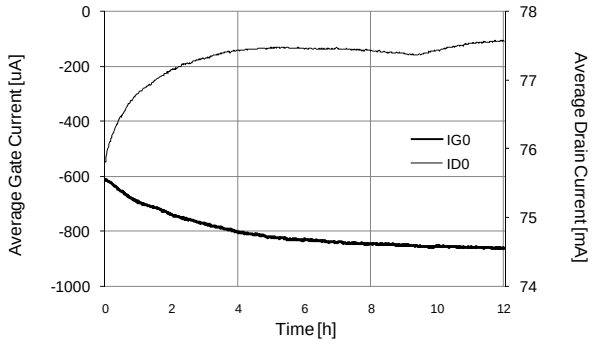


Fig. 7.5. Dynamic load-line (continuous trace) superimposed to the measured DC drain current characteristics obtained for V_{GS} ranging between -1.8 V and 0 V.

Two sequential tests are carried out, 1 hour and 12 hours long, respectively; the corresponding average values of the gate and drain currents as a function of time are shown in Fig. 7.6, while drain voltage waveforms acquired during the 12 hour stressing time are shown in Fig. 7.7. As it can be seen, waveforms look very similar one to each other. Nevertheless, an enlarged view of the peak drain voltage region clearly highlights the progressive device degradation (see Fig. 7.8).



(a)



(b)

Fig. 7.6. Gate and drain current walkout during the two sequential dynamic stress steps, carried out through forward operating mode. In particular a) refers to the 1-hour long stress and b) to the 12-hours long stress.

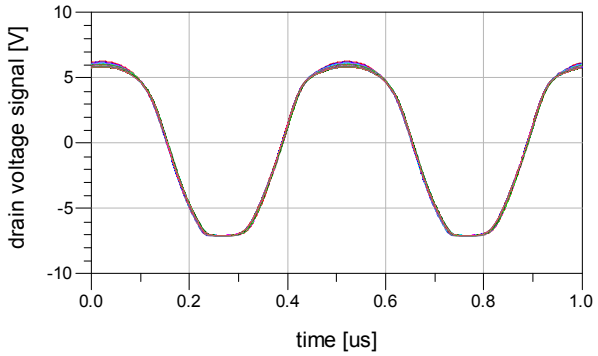


Fig. 7.7. Dynamic drain voltage waveforms acquired during the 12-hour stress.

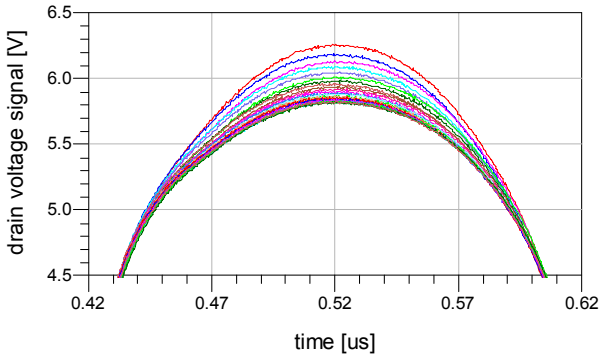


Fig. 7.8. Zoom on the peak of the drain voltage waveforms acquired during the 12-hour long stress.

The measurement system capability of acquiring the dynamic electrical quantities at the device ports, makes it naturally predisposed for the evaluation of the time dispersion of figures of merit which are of fundamental interest for microwave circuit design. As an example, a meaningful parameter to assess device degradation can be identified in the output power which is shown in Fig. 7.9 and 7.10 as a function of time for the two different tests: a 10% decrease in the device output power was found after the 12-hour long stress. The consistency between the electrical parameters investigated is well evident by comparing Fig 7.6.a and Fig. 7.9. The latter, in fact, shows an initial improvement of the device performance in correspondence with the decreasing trend that the average drain and gate currents present in Fig. 7.6.a up to 800 s: at successive time instants both the AC output power and the average currents present, instead, an opposite time-derivative.

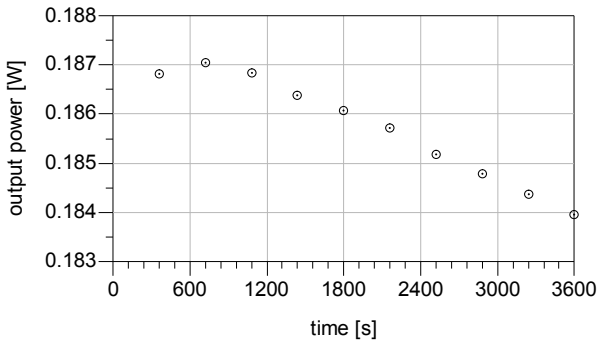


Fig. 7.9. Time dependence of the device output power during the 1-hour long stress.

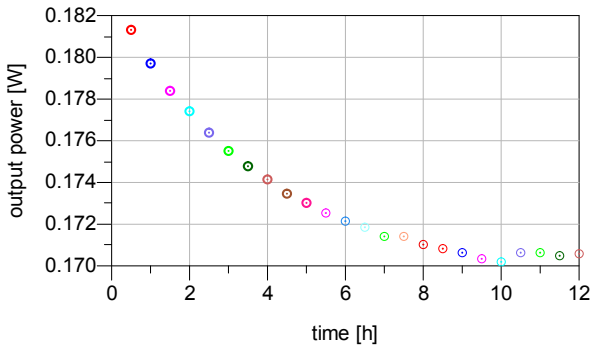


Fig. 7.10. Time dependence of the device output power during the 12-hour long stress.

7.1.4 Experimental Examples: Reverse Operation Mode

Accelerated device degradation can be obtained by exploiting the reverse operating mode of the proposed set-up: in such a case the device is *dynamically* forced into high-field electrical conditions by means of an AC signal applied at the drain port.

A first significant example of dynamic stress in reverse mode is shown in Fig. 7.15. It was carried out by means of the above described measurement setup, in reverse mode configuration: the device was biased at V_{GS0} = -2.2 V and V_{DS0} = 12 V (a non-stressing condition) and a 2-MHz signal, with a 5.5-V amplitude, was applied to the drain, moving dynamically the device into a high voltage drain region. The monitored average gate current, plotted in Fig. 7.11, shows an appreciable time dispersion. In addition, during the stress procedure, the ac component of the excitation has been switched off, leading the device in the quiescent, non-stressing condition (the gate reverse current instantaneously drop to a negligible level). However, when the signal is applied again, the average component of the current I_G reassumes the value corresponding to the last stressing instant, confirming the irreversibility of the device walkout also under dynamic operations, in agreement with what has been largely observed on the basis of DC investigations [1].

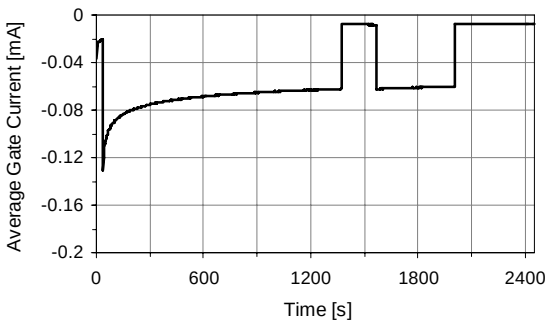


Fig. 7.11 Evolution of the average component of the PHEMT gate drain dynamic current during an off-state ac reverse stress

Three different and sequential stress procedures have been performed on a 900-μm GaAs PHEMT device under off-state conditions (i.e., with a completely depleted channel status).

The first stress is carried out by simply applying a DC bias (V_{GS} = -2.2 V and V_{DS} = 16.2 V, corresponding to an initial gate reverse current of about 0.3 mA/mm) to the device for one hour: the observed time dispersions of the gate and drain currents are plotted in Fig. 7.12-a.

In the second stressing phase, the full features of the measurement set-up in the 'reverse' configuration are exploited in order to force the device in a similar but *dynamic-type* stress. The device is biased at V_{GS} = -2.2 V and V_{DS} = 12 V, a 2-MHz signal with 5.5 V amplitude being applied to the drain port, and the gate port being closed on the 1 MΩ impedance provided by the oscilloscope channel. The duration of this stress is still one hour: the time-drifting of the *average* components of the gate and drain currents is reported in Fig. 7.12-b. These two first stressing tests show that both the DC currents under static excitation, and the average components of the currents under dynamic operation, decrease during the corresponding stress: they initially modify quite rapidly, and later more slowly, eventually presenting an asymptotic trend.

The third stress step has been carried out by applying constant DC currents to the device (I_G = -164 μA and I_D = 200 μA), for 30 minutes. In this case, it is the drain-source voltage V_{DS} to drift, increasing throughout the stress procedure, as shown in Fig. 7.12-c: this is due to the need for increasing electric field in order to guarantee the same (stressing) value of the gate reverse current.

After each of the three stress steps described above, the DC characteristic $I_G(V_{DS})$ has been measured (for V_{GS} = -2.2 V) as a figure of the device degradation, and the three curves are compared in Fig. 7.12-d with the unstressed device behavior, showing a shift towards an asymptotically stable condition, in agreement with the trend shown by the currents.

This experimental example put in evidence the usefulness of the proposed measurement set-up as an adequate tool for the investigation of electron device degradation under dynamic conditions. The off-state dynamic stress performed by means of our set-up causes a shift in the DC characteristics in qualitative agreement with the walkout resulting by a conventional, static off-state stress. This is reasonable since the physical phenomena involved in the degradation process do not change, provided that the device is kept during the tests within the pinched-off channel region. The fundamental difference between static and dynamic stress conditions mostly lies in the different nonlinear degradation laws induced.

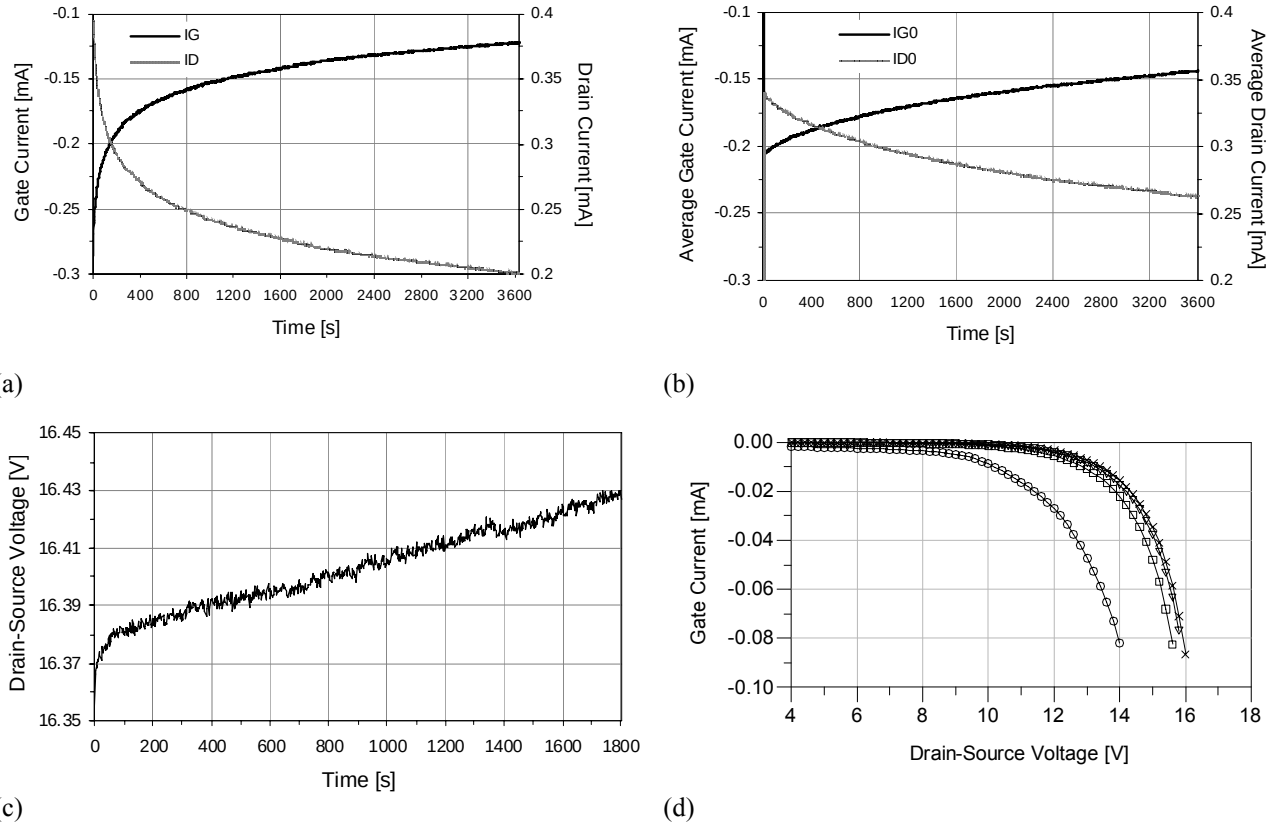


Fig. 7.12. Sequential stress tests on a GaAs PHEMT under off-state conditions. (a) Gate and drain current walkout during the first stress step with constant DC voltages. (b) Average gate and drain current walkout during the second stressing procedure performed under dynamic conditions in 'reverse' configuration. (c) Time dispersion of the drain-source voltage during the third stress step (constant DC currents). (d) DC gate current versus drain-source voltage for VGS =-2.2 V : unstressed device (circles), after the first DC stress (squares), after the ac stress (triangles) and after the last current-controlled DC stress (crosses), respectively.

By adopting the reverse set-up operation mode the device dynamic performances degradation may be also quantified. An 800-μm device is biased at V_{GS} = -2.2 V and V_{DS} = 12 V, and a 2-MHz, 6-V amplitude ac signal (larger than in the previous experiment) has been applied to the drain port, the gate port being closed on the 1 MΩ impedance provided by the oscilloscope channel. In Fig. 7.13, the trend of the time-dependent gate and drain current average values are shown. This operation mode is very different with respect to the previous experiment (Fig. 7.12-b); indeed, the average currents are very high (taking into account the off-state bias condition) and the drain current is definitely higher than the gate one.

During this stress experiment, the device is temporary forced under class-A operating conditions (forward operation of the set-up) in order to observe the output power degradation. As it can be seen in Fig. 7.14, a 20% decrease in the device output power is rapidly obtained (after just three hours), confirming that the operation mode involved in this test is very stressful for the device performances. It is well evident from Fig. 7.14 that after the first-hour stress the device has

apparently reached an almost asymptotic condition; this is perceivable in Fig. 7.15 also, where the progressive device degradation is more explicit.

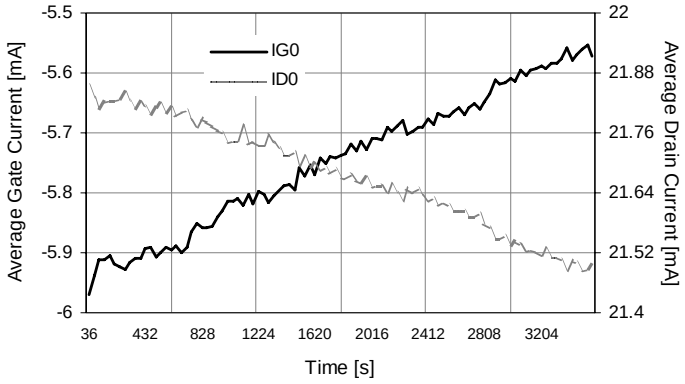


Fig. 7.13. Gate and drain current walkout during the stress step with 6-V ac amplitude.

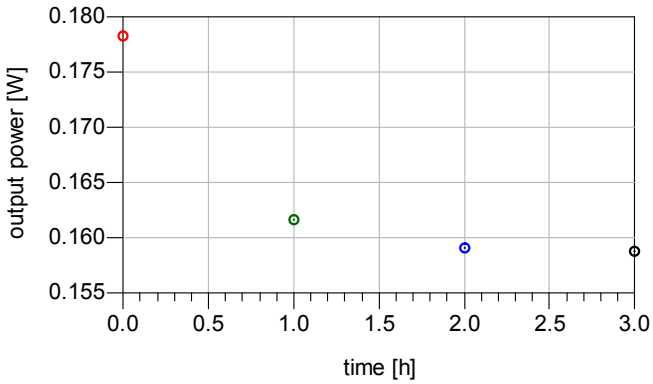
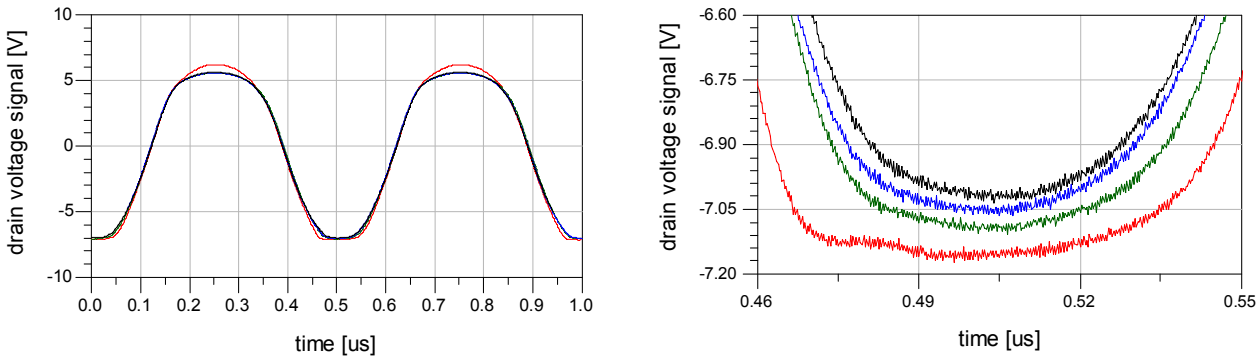


Fig. 7.14. Device output power under class-A operation: unstressed device (red, at time = 0), and during the reverse stress.



(a) (b)

Fig. 7.15. Drain voltage waveforms acquired before (red line) and during the reverse stress. (a) Entire waveforms and (b) enlarged view of the lowest voltage region.

7.1.5 Considerations on the Device Degradation Velocity

Since the breakdown walkout is recognized as a good indicator for the device degradation, some interesting observations can be drawn by relating the degradation velocity to the gate current [14]. To this aim, a DC accelerated stress was carried out on a new, unstressed, 0.25-µm PHEMT with 800-µm width, at V_{GS} = -2 V and V_{DS} = 11.2 V (corresponding to a gate current of 0.2 mA/mm: we chose, in fact, to define the breakdown walkout at a more conservative value than the usual 1 mA/mm). The stress lasted about 12 hours and a half and the gate current was continuously monitored (Fig. 7.16-a). The correspondent breakdown walkout $W(t)$ is plotted versus time in Fig. 7.16-b. We define here the walkout $W(t)$ as the voltage variation $\Delta V_{DS}^{BD}(t)$ needed to observe, at any time instant t, the same I_G value of the unstressed device (i.e., I_G = 0.2 mA/mm at t=0).

In order to reduce the spurious oscillations due to the measurement uncertainty, the two sets of data, $I_G(t)$ and $W(t)$, were fitted through polynomial functions: a 10th order was empirically chosen for polynomials, as the best trade-off between the fitting accuracy and the elimination of spurious oscillations. The obtained analytical curves are compared with data in the figures 7.16-a and 7.16-b. The numerical derivation versus time of the breakdown walkout W leads to the device degradation velocity, plotted in Fig. 7.16-c. Finally, this degradation velocity was related to the gate current in Fig. 7.16-d. An almost linear relationship was found, i.e. $v_W(t) \doteq dW(t)/dt \simeq \alpha + \beta \cdot I_G(t)$. This seems to confirm that the gate current value can be considered as a good indicator for the degradation velocity in electron devices.

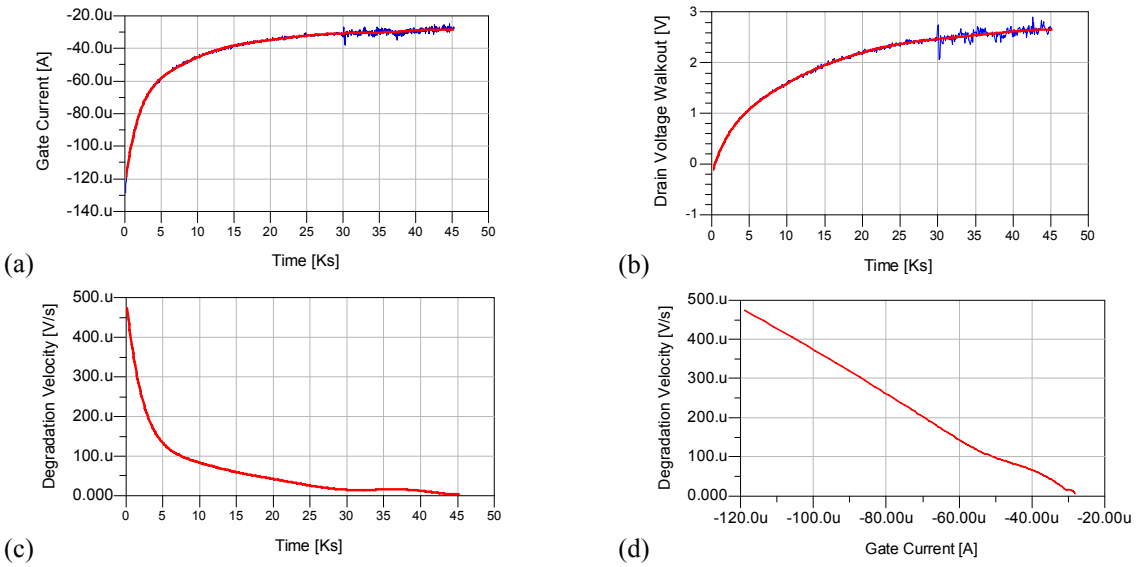


Fig. 7.16 DC accelerated stress (V_{GS} = -2 V, V_{DS} = 11.2 V) and post-processing. Measured gate current and breakdown walkout (blue, noisy trace) fitted by 10th order polynomial functions (red, continuous line) in (a) and (b), respectively. Device degradation velocity versus time and versus gate current in (c) and (d), respectively.

7.2 Conclusion

A fully-automated, technology-independent measurement system has been proposed aimed at the empirical characterization of microwave electron device degradation.

The hardware set-up has been widely discussed, highlighting how it can be implemented by means of completely conventional measurement instrumentation, commonly available in any microwave laboratory. The control software and measurement procedure have been also detailed. It is worth mentioning that the control software represents a key feature in order to obtain highly accurate measurements during long lasting stress procedures.

A large set of experimental results have been provided, under both static and nonlinear dynamic RF operating conditions, in order to definitely show the set-up potentiality in investigating device degradation phenomena. In particular, measurements carried out under the different system operation modes, clearly prove the set-up original ability of quantifying the time-dependent degradation of device dynamic performances. Moreover, collected data also confirm that the time evolution of some important well-known walkout effects, when observed through the proposed set-up under dynamic stressing conditions, is qualitatively (but clearly not quantitatively) consistent with the results obtained through DC measurements, which are widely described in the literature.

Finally, the presented measurement system definitely owns all the required capabilities to be a valuable aid in identifying and\or validating nonlinear models capable of predicting the device degradation phenomena, under static and dynamic operation.

Thanks to this measurement setup, we found that an almost linear relationship can be found between the device degradation velocity and the gate current value, once the breakdown walkout is assumed as indicator for the degradation.

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Conclusion

In the previous chapters I summarized the research activity of my PhD course. The most important result obtained has been the development of the Equivalent Voltage model. This is a simple empirical model, mainly based on the separation, in the device behaviour, of nonlinearity and memory effects: the dynamic phenomena are modelled by means of linear equivalent voltages, which control the associated, nonlinear and virtually memory-less, intrinsic device.

The EV approach has shown to be greatly versatile: it has been successfully applied to model the nonquasi-static effects arising at high frequencies in GaAs PHEMTs (Chapter 3), as well as to model the nonquasi-static and the low-frequency dispersive phenomena in GaN-based devices (Chapter 4). Good results have been also achieved in the application of the EV concept for the modelling of a Cold-FET for the design of wideband resistive mixers based on GaN technology (Chapter 5).

However, other types of models have been also extracted. In particular, an empirical, LUT-based model for dispersive effects in AlGaN/GaN HEMT has provided good results, shown in Chapter 4, while a previously published nonquasi-static model has been validated for a GaAs PHEMT in cold-FET configuration in Chapter 5.

Most of the developed models are based on look-up-tables, thus great importance is covered by the data interpolation algorithm: the good level of accuracy reached with our models is partly due to the original data approximation/interpolation algorithm described in Chapter 6.

Finally, an important role has been covered in my research activity by the device characterization: it is, in fact, the basis of empirical modelling. During this activity, a measurement setup has been assembled, aimed to characterize the device degradation in actual operative conditions for power amplifiers. The results obtained on the study of the breakdown walkout in GaAs devices have been shown in Chapter 7: they are a good starting point towards the modelling of the device degradation law, in order to be able to predict the device performance at the end of its life.

List of Publications

International Journals

- D. Resca, V. Di Giacomo, A. Raffo, R. Cignani, A. Santarelli, G. Vannini, F. Filicori, D. Schreurs, F. Medjoub, N. Thouvenin, C. Gaquière, "Nonlinear Modelling of InP Devices for W-band Applications", accepted for publication in *Cambridge University Press – EuMA International Journal of Microwave and Wireless Technologies*, 2009.
- I. Melczarsky, P.L. Gilabert, V. Di Giacomo, E. Bertran, F. Filicori, "Behavioral Modeling and linearization of a mm-wave Power Amplifier", accepted for publication in *Cambridge University Press – EuMA International Journal of Microwave and Wireless Technologies*, 2009.
- A. Raffo, V. Di Giacomo, P. A. Traverso, A. Santarelli, G. Vannini, "An Automated Measurement System for the Characterization of Electron Device Degradation under Nonlinear Dynamic Regime", accepted at *IEEE Transaction on Instrumentation and Measurements*
- A. Santarelli, D. Resca, A. Raffo, V. Di Giacomo, P. A. Traverso, G. Vannini, F. Filicori, "Optimal function approximation for empirical look-up-table device models", *International Journal on Microwave and Optical Technology*, Vol. 3, N. 3, pp. 165-174, July 2008.
- A. Santarelli, V. Di Giacomo, A. Raffo, F. Filicori, G. Vannini, R. Aubry, C. Gaquière, "Nonquasi-Static Large-Signal Model of GaN FETs through an Equivalent Voltage Approach", *Wiley Int. J. of RF and Microwave Computer-Aided Engineering*, vol. 18 N. 6, pp. 507-516, Nov. 2008.
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Proceedings of International Conferences

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- V. Di Giacomo, A. Santarelli, A. Raffo, P. A. Traverso, D. Schreurs, J. Lonac, D. Resca, G. Vannini, F. Filicori, M. Pagani, "Accurate Nonlinear Electron Device Modelling for Cold FET Mixer Design", in *Proc. EuMIC 2008 Conf.*, Amsterdam, 27 – 28 Ottobre 2008.
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