Electrical Characterization and Modeling of Pulse-based Forming Techniques in RRAM Arrays

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Abstract

The forming process, which corresponds to the activation of the switching filament in Resistive Random Access Memory (RRAM) arrays, has a strong impact on the cells' performances. In this paper we characterize and compare different pulse forming techniques in terms of forming time, yield and cell-to-cell variability on 4 kbits RRAM arrays. Moreover, post-forming modeling during Reset operation of correctly working and over formed cells has been performed. An incremental form and verify technique, based on a sequence of trapezoidal waveforms with increasing voltages followed by a verify operation that terminates when the expected switching behavior has been achieved, showed the best results. This procedure narrows the post-forming current distribution whereas reducing the reset switching voltage and the operative current. These advantages materialize in a better control of the cell-to-cell variability and in an overall time and energy saving at the system level.

Keywords: RRAM array, forming, read window, energy saving

1. Introduction

Resistive Random Access Memories (RRAM) gathered increasing interest in the last few years [1]. However, an intensive research activity is still to be performed on this innovative technology in order to increase RRAM reliability and performance. After the concept validation on single cells [2, 3, 4], the characterization of array structures is mandatory to bring such technology to a maturity level [5]. RRAM behavior is based on the possibility of electrically modifying the conductance of a Metal-Insulator-Metal (MIM) stack: the Set operation moves the cell in a low resistive state (LRS), whereas Reset brings the cell back to a high resistive state (HRS). To activate such a switching behavior, some technologies require a preliminary forming operation [6, 7, 8, 9]. Even if forming process is performed just once, this initial state plays a fundamental role in determining the subsequent array and system performance [10]. The effectiveness of the forming process depends on its ability in creating homogeneous conductive conditions among the cells thus easing successive Set/Reset operations. Standard forming is performed by applying either a voltage ramp or a voltage/current pulse to each cell individually [7]. The former method has a major drawback due to the filament conductance control being not tight enough. This results in larger cell-to-cell variability and larger disturb sensitivity [7, 11].

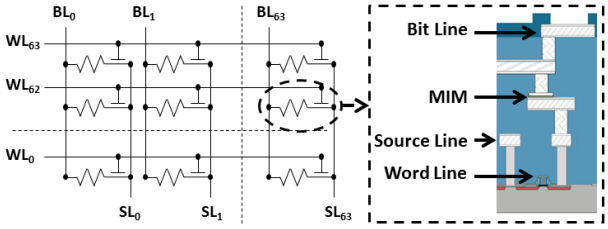

Figure 1: Schematic of the 4 kbits arrays characterized in this work and structure of a RRAM cell.

As an alternative, forming process can be performed through a sequence of pulses featuring the same voltage. While the forming time can be minimized using a single pulse with high compliance and voltage parameters, the forming yield is limited since the applied energy is not sufficient to complete the forming process in all cells [5]. Several pulse-based forming alternatives have been proposed to increase the applied energy and therefore the yield by using long pulses or sequences of short pulses at constant voltage [7].

In this paper different pulse-based forming techniques are compared in terms of forming time, yield and cell-to-cell variability on 4 kbits RRAM arrays. Considering the peculiarity of each cell in terms of the switching behavior activation, it is shown that a tight control of the forming process allows taking profit on a long term basis during the successive Set/Reset operations [12, 13]. Among all the investigated techniques, the best results have been obtained through a form and verify procedure, already proposed for Set/Reset operation [12], although form-

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ing performance of such technique have not been evaluated yet. Such method, hereafter referred to as Incremental Form and Verify (*IFV*) leverages on the application, to any single cell, of a sequence of trapezoidal waveforms with increasing maximum voltages, each step being followed by a current read operation that monitor the cell resistance. When a cell reaches a predefined read current value after the pulse application the procedure is interrupted, so that all cells are brought into a comparable electrical condition. In fact, even if the cell requires longer forming time, *IFV* offers a superior advantage by significantly reducing the cumulative number of Set/Reset pulses during cycling and, consequently, the overall power consumption of the memory peripheral circuitry. After-forming modeling of Reset I-V operations has been performed through Quantum-Point Contact (QPC) model [14], showing that if a too high conductance is reached during forming the filament became hard to disrupt in the successive Reset operation, resulting in faulty behavior [11, 15]. Moreover, it is shown that thanks to the verify procedure implemented during forming such faulty behavior can be avoided.

2. Memory architecture

The architecture of the 4 kbits arrays and the structure of RRAM cell characterized in this work are depicted in Fig.1. The memory cells consist in a select NMOS transistor manufactured in 0.25 μm BiCMOS technology, which also sets the current compliance, whose drain is in series to a variable resistor (i.e., the resistive switching element) connected to the bitlines. The variable resistor is a MIM stack constituted by: 150 nm TiN top and bottom electrode layers deposited by magnetron sputtering, a 10 nm metallic Ti layer acting as oxygen exchange layer, and a 9 nm HfO_2 AVD-deposited layer [5]. The resistor area is equal to 1 μm^2.

3. Experimental setup

Tab. 1 summarizes the Forming, Set, Reset and Read parameters used in this work. Three different forming schemes have been characterized:
a) Single pulse, denoted as *Pulse* in Fig. 2(a): V_{BL} = 3.5 V, V_{WL} = 1.4 V, with pulse duration T_{pulse} = 10 μs and a finite $t_{rise} = t_{fall}$ = 1μs to avoid overshoot effects [16].
b) Incremental Form, denoted as *IF* in Fig. 2(b): the bitline voltage V_{BL} was increased with a sequence of increasing voltage pulses from 2 to 3.5 V with ΔV_{BL} equal to 0.1 V, a wordline voltage V_{WL} of 1.4 V and T_{pulse} = 10 μs, $t_{rise} = t_{fall}$ = 1μs.
c) Incremental Form and Verify (*IFV*), Fig. 2(c): pulses were applied with increasing V_{BL} from 2 V up to 3.5 V with two different ΔV_{BL} equal to 0.1 V and 0.01 V, respectively, V_{WL} = 1.4 V and T_{pulse} = 10 μs, $t_{rise} = t_{fall}$ = 1μs. After each forming pulse the cell read current I_{read} was measured: if I_{read} > 19 μA the forming process was interrupted and the cell marked as formed. Fig. 3 shows the distributions of the IFV forming voltages, confirming that the specific voltage conditions triggering the forming behavior are quite different for each cell within the array.

Table 1: Summary of Forming, Set, Reset and Read parameters.

Operation	V_{BL} [V]	V_{SL} [V]	V_{WL} [V]	T_{pulse} [μs]
Pulse Form	3.5	0	1.4	10
IF Form (ΔV_{BL} = 0.1 V)	2-3.5	0	1.4	10
IFV Form (ΔV_{BL} = 0.1 V)	2-3.5	0	1.4	10
IFV Form (ΔV_{BL} = 0.01 V)	2-3.5	0	1.4	10
Set (ΔV_{BL} = 0.1 V)	1.5-3.5	0	1.4	10
Reset (ΔV_{SL} = 0.1 V)	0	1.5-3.5	2.8	10
Read	0.2	0	1.4	10

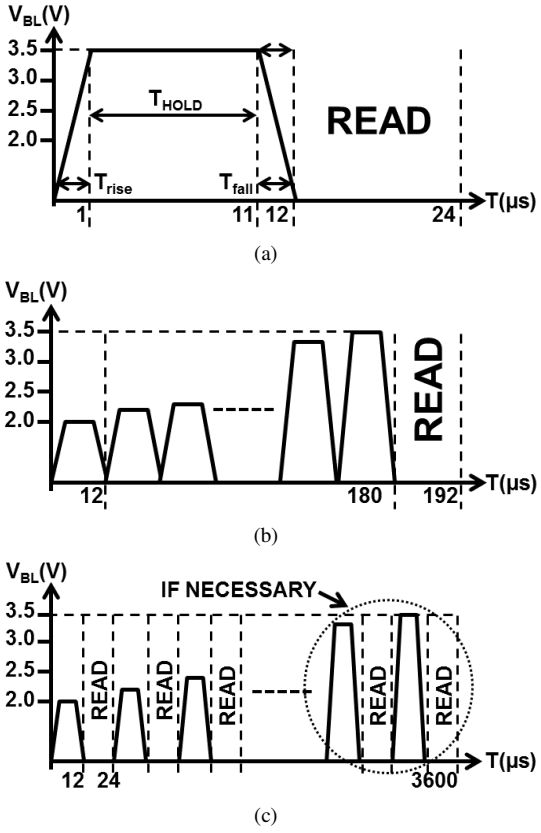
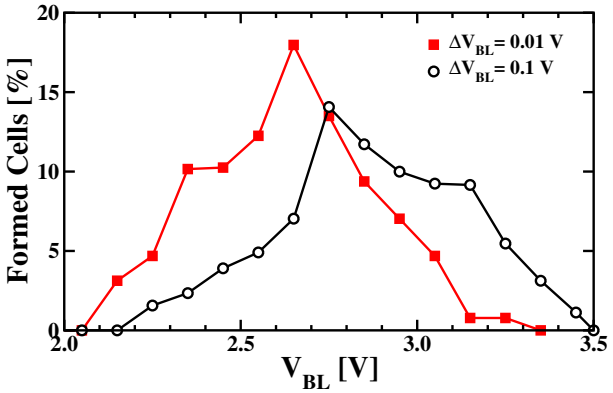


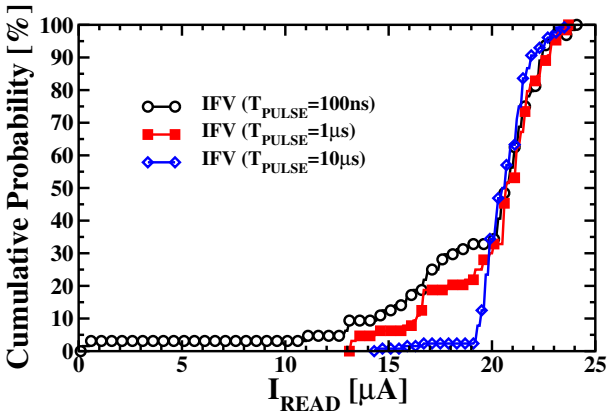
Figure 2: Pulse (a), *IF* (b) and *IFV* (c) schemes.

All the forming schemes considered in this paper base on pulse widths of 10 μs. This is mainly due by two factors: performance/variability concerns, and technological limitations of the integrated array. Concerning the former factor, the authors have tried different pulse widths for IFV forming scheme using ΔV_{BL} = 0.01V: 100 ns, 1 μs, and 10 μs. As shown in Fig. 4, the lower is the pulse width, the lower is the energy supplied to the cell for the forming operation, leading to poor forming yield and large inter-cell variability [17]. The trend of the results reported here applies also for IFV with larger ΔV_{BL} and for IF, and Pulse scheme. From the technology viewpoint, it must be reminded that the developed 4kbits arrays feature a peripheral circuitry that drives and routes all the signals on the memory cells through large multiplexers and selectors that, along with the process-induced variability, limits the duration of pulse



(a)

Figure 3: Distributions of the forming voltages during *IFV* for the ΔV_{BL} = 0.01 V and ΔV_{BL} = 0.1 V cases.



(a)

Figure 4: Cumulative I_{read} distributions after IFV with ΔV_{BL} = 0.01 V and different pulse widths.

width on a narrow range of values. However, the results shown in this paper and the experimental methodology, especially concerning the IFV scheme, apply without lack of generality to any optimized RRAM technologies, where shorter pulse widths can be adopted.

The cell current I_{read} was measured by applying V_{BL} = 0.2 V, V_{WL} = 1.4 V and a read time T_{read} = 10 μs, t_{rise} = t_{fall} = 1μs. The Set/Reset operations were performed by using an Incremental Step Pulse algorithm [18, 19], by increasing V_{BL} from 1.5 V up to 3.5 V with ΔV_{BL} = 0.1 V, V_{WL} = 1.4 V and T_{pulse} = 10 μs, t_{rise} = t_{fall} = 1μs during Set and by increasing the sourceline voltage V_{SL} from 1.5 V up to 3.5 V with ΔV_{SL} = 0.1 V, V_{WL} = 2.8 V and T_{pulse} = 10 μs, t_{rise} = t_{fall} = 1μs during Reset. Forming, Set, Reset and Read pulse operations are performed by applying the V_{SL}, V_{BL} and V_{WL} cell-by-cell, sequentially.

4. Forming Results

Cell forming time and yield obtained with each method are reported in Tab. 2. Forming yield is calculated as the cell percentage that shows a read verify current after forming I_{read} >19 μA, ensuring the creation of a conductive filament. The choice of 19 μA both as a read current threshold criterion to assess and claim the actual creation of a conductive filament during forming, and as a forming yield criterion is ascribed to stability and variability concerns that have been taken into account from previous results shown in literature [17, 20]. Concerning the stability, it is important to ensure that the creation process of the conductive filament in the HfO_2 will be utmost homogeneous, and that the so formed filament would be easily disrupted in consecutive RESET operations. As demonstrated in [20], if it is not adopted a sufficiently high read current threshold, large oscillations during forming and unstable SET/RESET behavior may appear during the memory cell lifetime. In order to account for the intrinsic variability of the RRAM technology exploited in this work, it must be ensured also that the average I_{read} calculated on the entire array is in the range between 18 μA and 24 μA. Forming with read current threshold lower than 18 μA generally produces unstable memory cells that will fail after few SET/RESET cycles [20], whereas forming with a threshold current higher than 20 μA usually display larger array inter-cell variability, as indicated in the values provided in Table 3. *IFV* average and worst case time (i.e. requiring the highest number of pulses) are reported since *IFV* forming time is different from cell to cell. Even if *Pulse* forming is shown to be the fastest, the very low yield result confirms that the energy provided by this forming technique is insufficient for most of the memory cells in the array. For this reason this forming scheme will be no further considered in this paper. The highest forming yield is obtained using ΔV_{BL} = 0.01 V (about 99%), therefore only this *IFV* variant will be considered further on.

Table 2: Forming Methods Timings and Yield.

	Time [μs] average	Time[μs] worst case	Yield [%]
Pulse	12	12	54
IF (ΔV_{BL} = 0.1 V)	180	180	77
IFV (ΔV_{BL} = 0.1 V)	216	360	87
IFV (ΔV_{BL} = 0.01 V)	1584	3600	99

Table 3: Array average read currents and Inter-cell variability [17] after forming with different thresholds.

Forming Threshold [μA]	Array average I_{read} [μA]	Array inter-cell variability [μA]
19	20.58	1.26
20	20.88	1.77

Fig. 5 shows I_{read} distributions of correctly formed cells (i.e. reaching the 19 μA target) for all the schemes considered in this work. As it can be observed, the distributions related to the *IFV* scheme exhibit a lower dispersion of the current values, thus resulting in a better control of the cell-to-cell variability.

5. After-forming Set/Reset

LRS and HRS read current cumulative distributions measured after the first Set and Reset operations are reported in

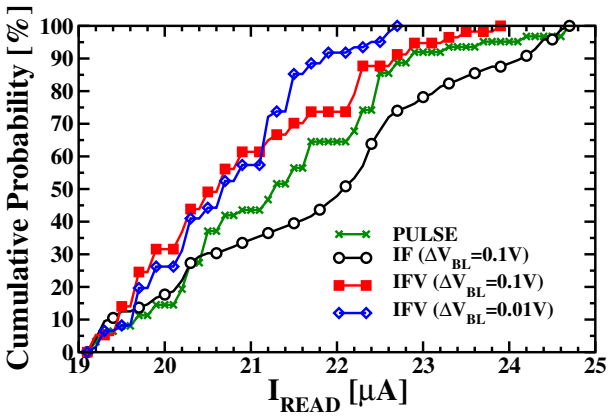


Figure 5: Cumulative I_{read} distributions of correctly formed cells after Pulse (54%), IF (77%), IFV with ΔV_{BL} = 0.1 V (87%) and IFV with ΔV_{BL} = 0.01 V (99%) forming operations.

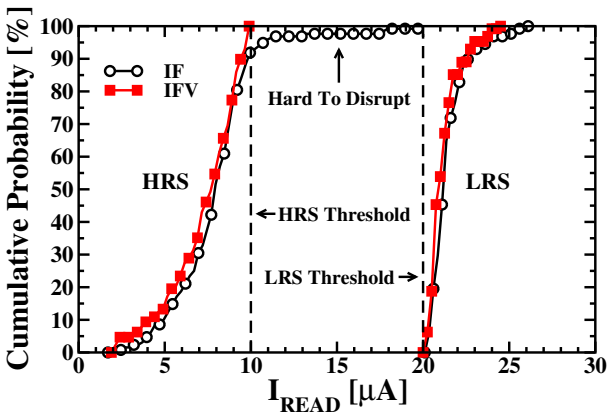


Figure 6: IF and IFV cumulative I_{HRS} and I_{LRS} distributions measured at endurance cycle 1.

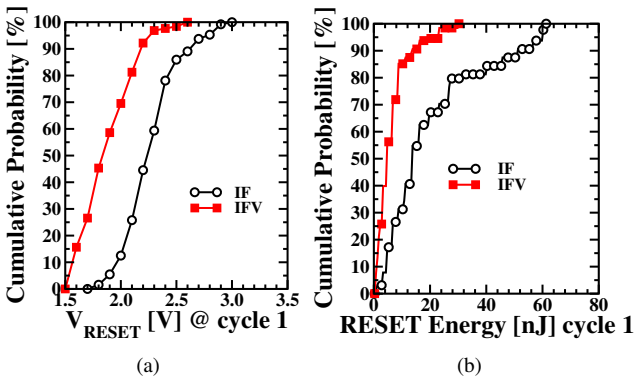


Figure 7: Cumulative distribution of the reset switching voltages (a) and overall Energy required to perform Reset operation (b) at Set/Reset cycle 1 for *IF* and *IFV* (ΔV_{BL} = 0.01 V) forming schemes.

Fig. 6. It can be observed that Reset failed on some *IF* formed cells (denoted as *Hard to disrupt*) showing read current values above the HRS threshold fixed to I_{read} =10 μA, whereas Reset operation has been correctly performed on all *IFV* formed cells.

Experimental results show that the *IFV* technique exhibits a lower Reset switching voltage and a reduced operation current: Fig. 7 (a) show the cumulative distribution of the reset switching voltages measured on fresh devices for *IF* and *IFV* (ΔV_{BL} = 0.01 V) forming schemes. The advantages are ascribed to a higher filament geometry control devised by the *IFV* scheme. Fig. 7 (b) shows the cumulative distribution of the energy required to perform Reset operations. The overall energy required to disrupt the conductive filament has been calculated as:

$$E = \sum_{i=1}^{n} V_{pulse,i} * I_{pulse,i} * T_{pulse} + V_{read} * I_{read,i} * T_{read} \quad (1)$$

Where n is the number of reset pulses applied during incremental pulse operation, $V_{pulse,i}$ is the pulse voltage applied at step i, $I_{pulse,i}$ is the current flowing through RRAM cell during pulse i application, T_{pulse} = 10μs is the pulse length, V_{read} =0.2 V is the read voltage applied during verify operation, $I_{read,i}$ is the current read during read verify step i, and T_{read} = 10μs is the verify pulse length.

According to these results, the *IFV* advantages after forming are clear. As a matter of fact, as demonstrated in Fig. 3, each cell is formed with its proper filament geometry in order to achieve the 19 μA current, thus allowing to counteract the intrinsic technological variability that would be impossible without a verify procedure.

6. Post-Forming modeling

Reset I-V characteristics have been measured after-forming to analyze the conductive filament properties through QPC model [3, 14, 21]. Two different behaviors can be observed for correctly working cells (a) and hard to disrupt cells (b), reported in Fig. 8. The differences in the HRS current values can be ascribed to the differences in the filament size [4]. The black dashed line shows the limit $I = G_0 V$ with $G_0 = 2e^2/h$ the quantum conductance unit corresponding to the creation of a single mode nanowire, where e is the electron charge and h the Planck's constant. Within this framework, $I = G_0 V$ sets a limit: in case of $I > G_0 V$ more than a single conductive filament or a single filament with more than one mode must be taken into account: this means that on hard to disrupt cell a residual part of the conductive filament is still present after Reset operation since High Resistive State (HRS) curve measured is over the limit. HRS I-V curves fitting has been performed through QPC (lines). HRS current is calculated according to the expression:

$$I = \frac{2e}{h} G/G_0 \left(eV + \frac{1}{\alpha} Ln\left[\frac{1 + e^{\alpha(\Phi - \beta eV)}}{1 + e^{\alpha[\Phi + (1-\beta)eV]}} \right] \right) \quad (2)$$

where Φ is the barrier height (bottom of the first quantized level), $\alpha = t_B \pi^2 h^{-1} \sqrt{2m^*/\Phi}$ is a parameter related to the inverse of the potential barrier curvature (assuming a parabolic longitudinal potential), $m^* = 0.44 m_0$ is the effective electron mass and t_B is the barrier thickness at the equilibrium Fermi energy. β takes into account how the potential drops at the two ends of the filament: since the constriction is highly asymmetric β=1 has been used (almost all the applied voltage drops close to the Ti layer). G/G_0 is a conductance parameter equivalent to

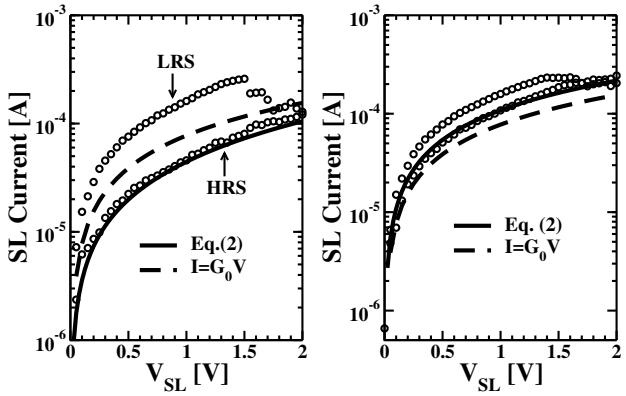


Figure 8: Reset I-V characteristics measured after forming and HRS fitting through eq.(2) on correctly working cells (a) and hard to disrupt cells (b).

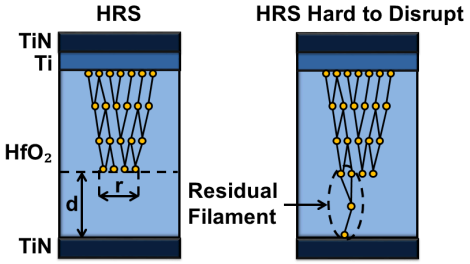


Figure 9: Schematic showing the conductive filament shape after reset (HRS) for correctly working and hard to disrupt cells.

the number of filaments at very low voltages: in a very approximate way, a single highly conductive filament can be viewed as a parallel combination of elementary nanowires [22].

The conductive filament obtained after Reset on correctly working cells and hard to disrupt cells is depicted in Fig. 9: in case of good reset the presence of a potential barrier is assumed on HRS state, hence the average barrier length d and the radius of the constriction r have been calculated according to [14]. On the contrary, assuming the absence of a potential barrier on hard to disrupt cells, the normalized conductance of the filament G/G_0 has been calculated using large negative values for Φ in the above expression, since in such condition the barrier plays no role (neither β nor α affect the results) and a large negative barrier is a trick to eliminate the barrier effect.

Fig. 10 shows the HRS curves obtained after Reset I-V operation on *IF* (a) and *IFV* (b) formed cells. It can be observed that *IF* show higher conductance values than *IFV*: only 39% of *IF* formed cells showed HRS curves below $I = G_0V$ whereas 65% of *IFV* formed cells showed HRS curves below the limit. Even if such hard to disrupt cells percentages are very high, incremental step Reset algorithm allowed obtaining a strong reduction on both *IF* (around 9%) and *IFV* cells (0%), as shown in Fig. 6. $I = 2 * G_0V$ and $I = 0.8 * G_0V$ are reported as upper and lower limit, respectively.

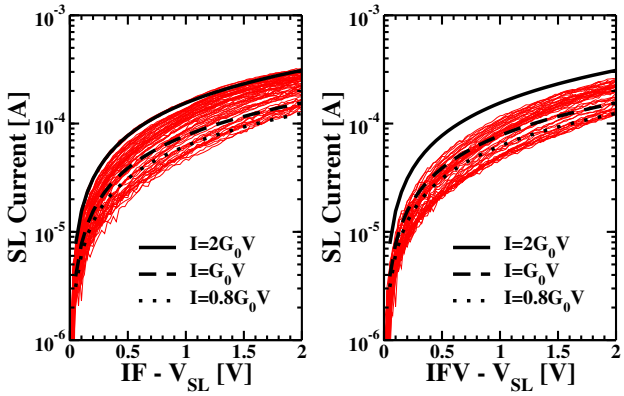


Figure 10: HRS curves obtained after Reset I-V operation on *IF* (a) and *IFV* with ΔV_{BL} = 0.01 V (b) formed cells.

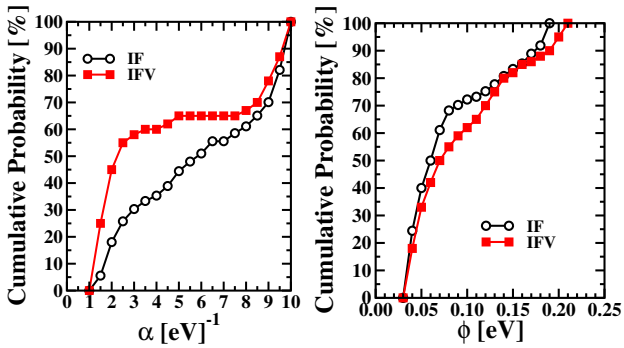


Figure 11: Cumulative distribution of α and Φ fitting parameters used on correctly working cells.

6.1. *Good Reset fitting*

In case of correct Reset operation (i.e. HRS curve below $I = G_0V$) fitting has been performed assuming $G/G_0 = 1$ and the presence of a potential barrier. The cumulative distributions of α and Φ fitting parameters used on correctly working cells are reported in Fig. 11. The cumulative distributions of calculated barrier length d and radius r of the constriction for correctly working cells are reported in Fig. 12: *IFV* cells show smaller r. These values are sensitive to the effective mass, which is unknown with certainty, so that they should be considered for comparative purposes only. The barrier in HRS is very low for both forming methods so it only affects the low voltage part of the I-V curve, after that a linear behavior can be observed.

6.2. *Hard to disrupt fitting*

In case of hard to disrupt cells fitting has been performed assuming large negative Φ values, α fixed to 1 (even if α and Φ play no role in such condition) and $G/G_0 \geq 1$ due to the presence of the residual filament. Fig. 13 shows the cumulative distribution of G/G_0 conductance values fitting parameters used on hard to disrupt cells: it can be observed that *IF* hard to disrupt cells resulted in higher conductance values.

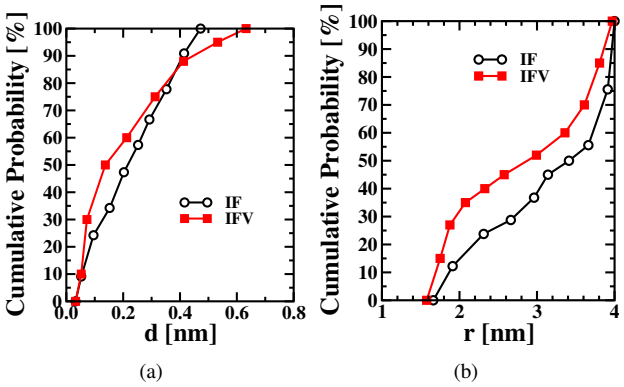


Figure 12: Cumulative distribution of calculated barrier length d (a) and radius of the filament constriction r (b) on correctly working cells.

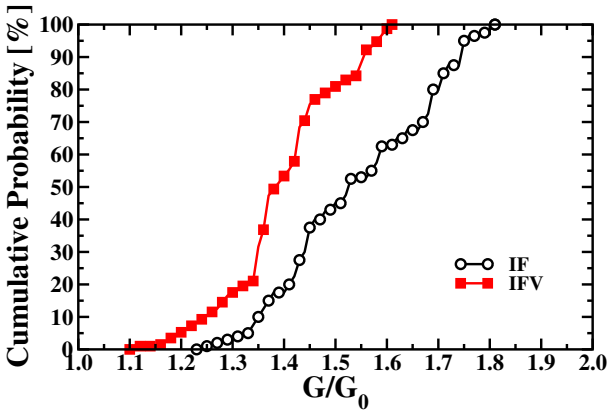


Figure 13: Cumulative distribution of G/G_0 fitting parameters used on hard to disrupt cells.

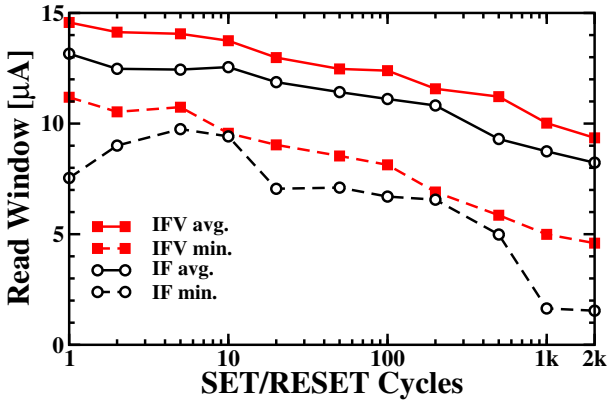


Figure 14: Average and minimum read windows as a function of the Set/Reset cycle number for *IF* and *IFV* (ΔV_{BL} = 0.01 V) forming schemes.

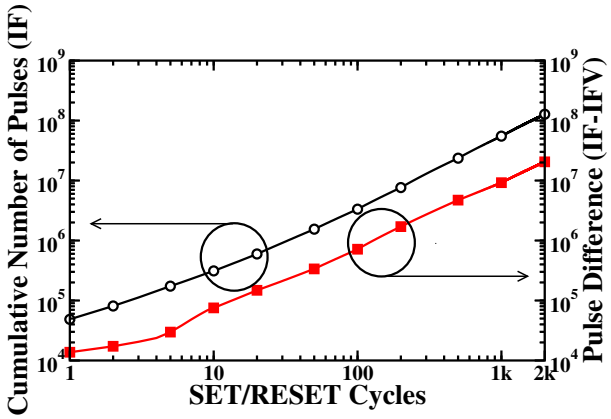


Figure 15: Cumulative number of Set/Reset pulses applied to the entire memory as a function of the cycle number for the *IF* forming scheme (left axis) and cumulative pulse number saving for the *IFV* (ΔV_{BL} = 0.01 V) forming scheme with respect to *IF* (right axis).

7. Endurance analysis

To quantify the advantages obtained through *IFV* forming during lifetime, 2k endurance cycles have been executed. Fig. 14 plots the *IF* and *IFV* average and minimum read windows, calculated as in [23], as a function of the Set/Reset cycles. The advantages of the *IFV* scheme are even appreciable during cycling: as far as the average criterion is considered, the average read window gain during cycling of the *IFV* scheme on the *IF* method sets around 7%, representing a marginal yet non negligible advantage. When the minimum criterion is considered, the average read window gain during cycling increases up to 37%. This represents once again a plus for the *IFV* scheme since it demonstrates its enhanced ability in Set/Reset tail bits (i.e., cells harder to be switched) reduction [24]. The read window closure due to endurance degradation [25] could be attributed to the impact of impurities in the metal-organic AVD precursor, in particular to carbon [26].

The ultimate advantage of the *IFV* is shown in Fig. 15, which exhibits the cumulative number of Set/Reset pulses applied to the entire memory array during the 2k cycles experiment as a function of the cycle number for the *IF* technique and the relative saving that can be obtained with *IFV*. The saving in terms of the total number of Set/Reset pulses during cycling is mainly due to a lower Reset switching voltage required by cells formed with *IFV*.

All the described advantages translate, both during the design stage of larger arrays such as [27, 28] and at a system level, in shorter switching/operating times, less operative energy for the Reset operation, and in lower power consumption for the circuitry driving either the bitlines or the sourcelines.

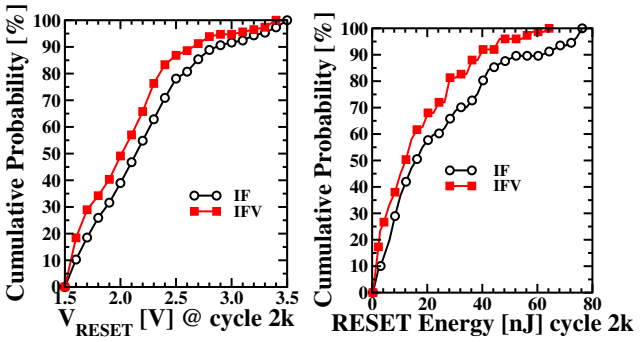
Experimental results show that even after 2k cycles *IFV* technique exhibits a lower Reset switching voltage and a reduced operation current: Fig. 16 (a) show the cumulative distribution of the reset switching voltages for *IF* and *IFV* (ΔV_{BL} = 0.01 V) forming schemes.

Fig. 16 (b) shows the cumulative density function of the energy required to perform Reset operations: while the advantages after forming are clear, the energy gap is reduced during cycling because of device degradation.

Fig. 17 shows the difference between *IF* and *IFV* average energy (a) and time (b) required to perform Set and Reset operations during cycling, calculated as

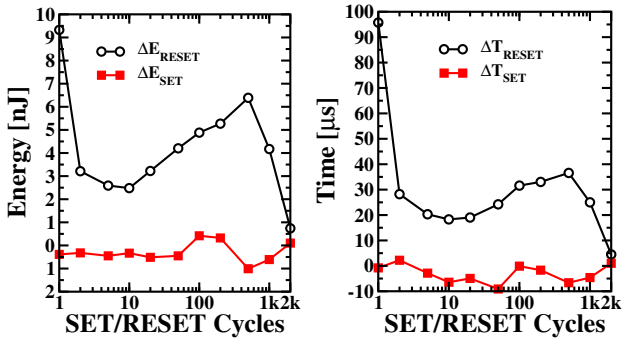
$$\Delta E_{Reset/Set} = E_{IF,Reset/Set} - E_{IFV,Reset/Set} \quad (3)$$

$$\Delta T_{Reset/Set} = T_{IF,Reset/Set} - T_{IFV,Reset/Set} \quad (4)$$



(a) (b)

Figure 16: Cumulative distribution of the reset switching voltages (a) and overall Energy required to perform Reset operation (b) at Set/Reset cycle 2k for *IF* and *IFV* (ΔV_{BL} = 0.01 V) forming schemes.



(a) (b)

Figure 17: Average difference between *IF* and *IFV* (ΔV_{BL} = 0.01 V) Energy (a) and Time (b) required to perform Set and Reset operations as a function of the Set/Reset cycle number.

Set energy has been calculated as previously reported in (1) for Reset operation. Reset operation requires a higher number of pulses compared to Set, resulting in higher energy and time constraints. Even if *IFV* Set energy and time requirements are shown to be slightly higher, the advantages in terms of Reset energy and timing are clear until 2k cycles. After that, the device degradation reduces *IFV* advantages.

It is worth mentioning that the main drawback of the *IFV* forming technique could lie on the longer forming times for cells requiring high forming voltages compared to the *IF* scheme, mainly because of the verify operation between the forming steps. However, it must be pointed out that this operation is performed just once, therefore its latency increase is favourably traded with the time saved during the subsequent Set/Reset operations.

8. Conclusions

Different pulse forming techniques have been applied to form RRAM arrays and compared in terms of forming time, yield and cell-to-cell variability. After-forming modeling of correctly working and hard to disrupt cells has been performed through QPC, showing that thanks to a tight control during forming the creation of hard to disrupt filaments is avoided. A form and verify technique, consisting in a sequence of trapezoidal waveforms with increasing voltages terminated when the expected switching behavior is achieved, showed the best results thanks to a tight control of the conductive filament creation. Its advantages in terms of the post-forming switching conditions homogenization, read window gain, operative current, cumulative number of pulses, energy and time required for switching during cycling have been demonstrated.

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