This article may be downloaded for personal use only. Any other use requires prior permission of the author and AIP Publishing.
The following article appeared in E. Peréz et al., JVST B 35, 01A103 (2017), and may be found at https://avs.scitation.org/doi/10.1116/1.4967308.
The DOI of the published version is: https://doi.org/10.1116/1.4967308

Impact of Temperature on Conduction Mechanisms and Switching Parameters in HfO_2-based 1T-1R RRAM Devices

Eduardo Pérez[a)] and Christian Wenger

IHP GmbH/Leibniz-Institut für Innovative Mikroelektronik, Im Technologiepark 25, 15236 Frankfurt (Oder), Germany

Alessandro Grossi, Cristian Zambelli and Piero Olivo

Dip. di Ingegneria, Universitá degli Studi di Ferrara, Via G. Saragat 1, 44122 Ferrara, Italy

Robin Roelofs

ASM, Kapeldreef 75, 3001 Leuven, Belgium

[a)] Electronic mail: perez@ihp-microelectronics.com

In this work, the impact of temperature in the range from -40 ºC to +150 ºC on the leakage mechanism and resistive switching voltages of 1T-1R HfO_2-based devices is investigated. By using incremental step pulses with an additional read and verify algorithm, the devices are switched from the high resistive state (HRS) to the low resistive state (LRS) and vice versa. In the HRS, the leakage current values are not affected by the temperature, suggesting a tunnel-like conduction mechanism through the filament constriction. By applying the Quantum-Point Contact (QPC) model this temperature independence is attributed to compensation between the width and the height variations of the tunnel barrier. In contrast to the HRS, the leakage currents values of the LRS are decreasing linearly with raising temperature, suggesting a metal-like conduction mechanism. Therefore, the On/Off ratio is slightly decreasing with increasing temperature. Regarding the switching voltages, no impact of temperature was found,

ensuring stable switching cycles of the devices in the relevant temperature range for applications.

I. INTRODUCTION

Resistive Random Access Memories (RRAM) based on HfO_2 is one of the most promising technology candidates for replacing Flash memories[1-4]. RRAM behavior is based on the possibility of electrically modifying the conductance of a Metal-Insulator-Metal (MIM) stack: the Set operation moves the cell into a Low Resistive State (LRS), whereas Reset operation brings the cell back to a High Resistive State (HRS)[5, 6]. This technology has shown fast low-power switching operations, high-integration density[7, 8], and compatibility with CMOS processes[9]. However, a complete understanding of RRAM conduction mechanisms is still lacking.

For this purpose, a complete characterization in the relevant temperature regime was performed in AC mode through the Incremental Step Pulse with Verify Algorithm (ISPVA)[10-12]. In addition, DC mode characterization was performed in the same temperature range, in order to extract the most relevant Quantum-Point Contact (QPC) model parameters such as tunnel barrier height and width from the Current-Voltage curves[13, 14].

II. EXPERIMENTAL

The 1T-1R memory devices are constituted by a select nMOS transistor manufactured in CMOS technology (width of 1.14 µm and length of 0.24 µm), which

also sets the current compliance, whose Drain is in series to a resistive Metal-Insulator-Metal (MIM) stack as illustrated in Fig. 1.

The resistive MIM cell is integrated above the metal line 2 of the CMOS process. The MIM cell consists of a $TiN/HfO_2/Ti/TiN$ stack. The 150 nm TiN layers and the 7 nm Ti layer are deposited by magnetron sputtering; the 8 nm HfO_2 layer is grown by Atomic Layer Deposition (ALD) using an halide based precursor, resulting in an amorphous HfO_2 film. The MIM cells area is 600 x 600 nm^2.

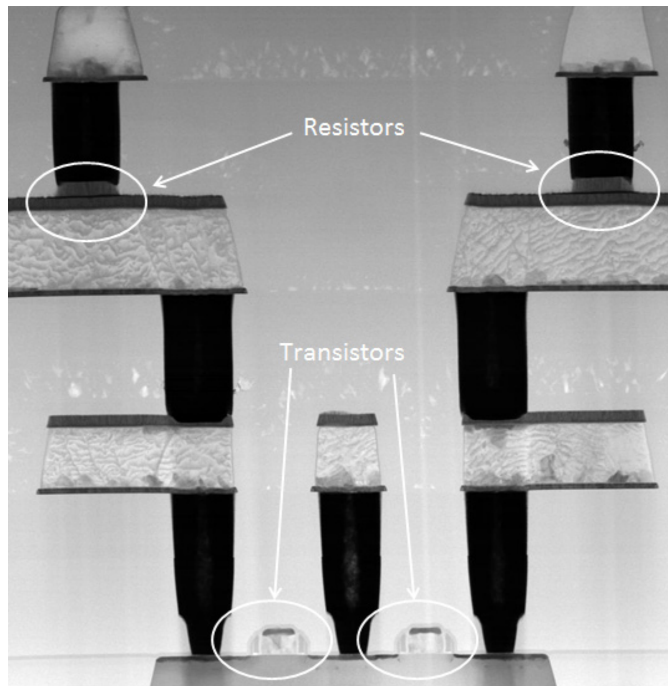


FIG. 1. TEM cross-sectional image of two neighbored 1T-1R devices with NMOS access transistors and $0.6\times0.6\ \mu m^2$ resistive MIM cells.

III. EXPERIMENTAL RESULTS AND MODELING

The electrical characteristics were obtained by means of a set-up based on the Keithley 4200-SCS semiconductor characterization system working together with the

Cascade PA200 semi-automatic probe system. In order to ensure a reliable accuracy for statistical calculations 60 1T-1R devices were characterized.

In order to perform the AC mode characterization in the temperature range from -40 to + 150 ºC, the Incremental Step Pulse with Verify Algorithm (ISPVA) was applied. This technique consists of a sequence of increasing voltage pulses (V_{pulse} = 0.2 - 5 V, V_{step} = 0.1 V, T_{pulse} = 10 µs, $t_{fall/rise}$ = 1 µs) to the Drain terminal during Set operation, whereas this sequence of pulses is applied to the Source terminal during Reset operation, as illustrated in Fig. 2. The applied transistor Gate voltage values were V_G = 2.8 V and V_G = 1.5 V, respectively. After every pulse a Read-verify operation is performed with V_G = 1.5 V, V_{Read} = 0.2 V (applied at the Drain) for 10 µs. When the Read current reaches the target value of 10 µA the Set operation is stopped, whereas the Reset operation is stopped when the target value of 2 µA is achieved. Both Programming and Reading operations in ISPVA are performed at the same temperature.

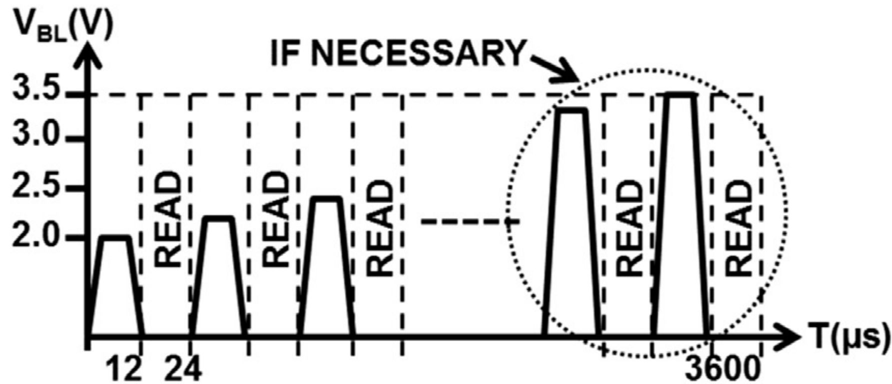


FIG. 2: Incremental Step Pulse with Verify Algorithm (ISPVA): Pulses were applied with increasing V_{BL} from 2 V up to 3.5 V with ΔV_{BL} equal to 0.1V and T_{pulse} = 10 µs until the threshold values for HRS and LRS are achieved.

In order to illustrate the impact of the temperature onto the inter-cell variability[15], the cumulative probability of the LRS and HRS currents after applying the read and verify operation is evaluated. As shown in Fig. 3, the HRS currents are not impacted by temperature. In contrast to the HRS state, there is a clear increase of the dispersion and the mean value of the LRS current state with decreasing temperature.

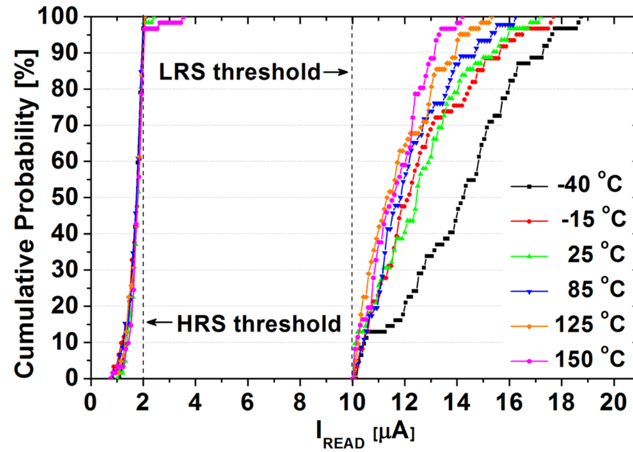


FIG. 3. (Color online) HRS and LRS current cumulative probabilities in AC mode at the selected temperature values. The target current values for the set and reset operations are also marked.

Fig. 4 illustrates the variability of the LRS currents at the selected temperatures of -40, + 25 and + 150 ºC. The LRS threshold value of 10 µA is used at all measurements; therefore a kind of accumulation occurs next to the threshold value of 10 µA at temperatures higher than 25 ºC. With increasing temperature, the variability of the read-out distribution is strongly reduced.

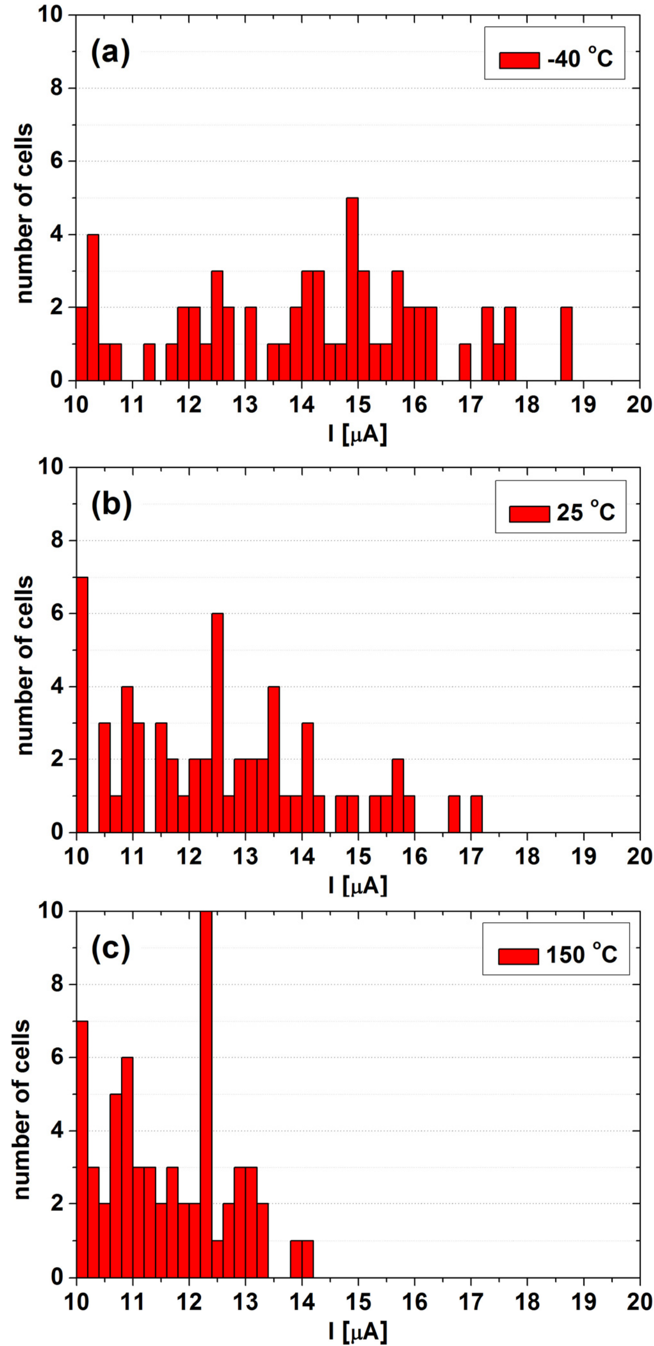


FIG. 4. (Color online) Distribution of LRS current values in AC mode at (a) -40, (b) 25 and (c) 150 ºC.

The average current values of the HRS and LRS as function of temperature are illustrated in Fig. 5. Concerning the LRS, a slope of about -10^{-2} μA/ºC was obtained, which means that the conduction mechanism of the LRS is metallic-like[16]. This linear

temperature dependence was already reported by Walczyk et al.[17] (HfO_2 deposited by Atomic Vapour Deposition) and evaluated based on[13]:

$$I_{LRS} \approx \frac{1}{1 + R_{LRS}^0[1 + \rho(\mathrm{T} - \mathrm{T}_0)]} \quad (1)$$

where R_{LRS}^0 is the LRS resistance at T_0 = 293 K and ρ is a temperature coefficient. In contrast, Puglisi et al.[19] did not find that reduction of the LRS leakage. This disagreement in temperature behavior could be caused by the differences in the used measurement techniques. The slope of the HRS is, with 10^{-4} μA/ºC, 100 times lower than the LRS one, suggesting a tunnel-like conduction mechanism[20]. Caused by the impact of temperature on the LRS, the On/Off ratio slightly decreases from 8 at -40 ºC to 7 at +150 ºC. Walczyk et al.[17] reported an even higher reduction (from 20 to 5).

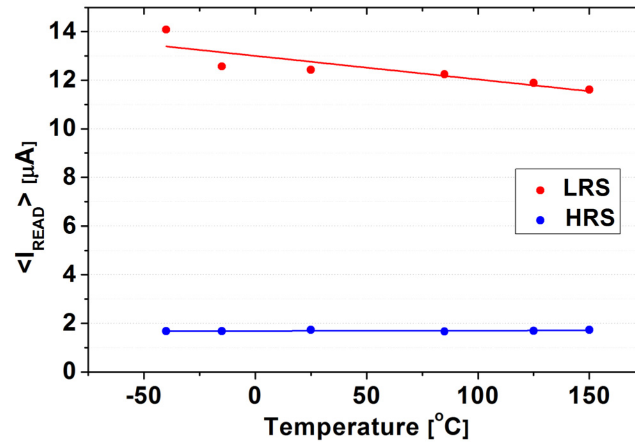


FIG. 5. (Color online) Average values of the HRS and LRS currents as function of temperature.

In order to ensure that the temperature impact on the LRS of the 1T-1R device is solely caused by the MIM resistor, the nMOS transistor is investigated separately. The gate voltage of 1.0 V was chosen, which is different to the voltage values used for

Set/Read (1.5 V) and Reset operations (2.8 V). But, the different MIM resistance values in LRS and HRS, connected in series with the select transistor, cause a similar voltage drop in V_{DS} of the transistor. The drain current of the nMOS device in the temperature range of interest is shown in Fig. 6. The Drain current of about 22 μA is not affected by the change of temperature. Therefore the linear increase of the LRS current in Fig. 5 is caused by the metallic behavior of filamentary based leakage mechanism and not by the transistor itself.

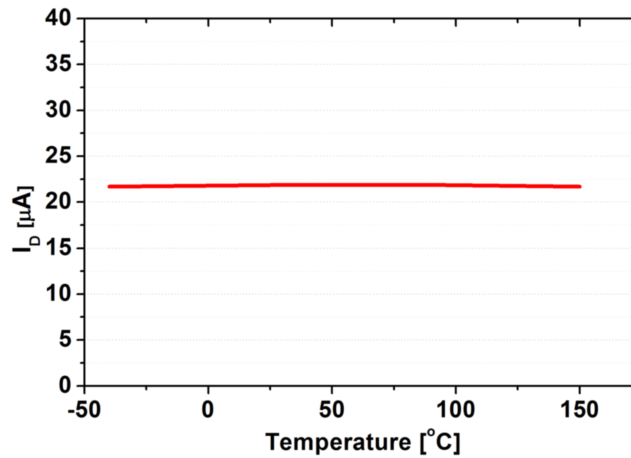


FIG. 6. (Color online) Drain current of the nMOS select transistor as function of temperature.

As illustrated in Fig. 7, the switching voltages V_{Res} and V_{Set} are not affected by the increase of temperature. This temperature independent behavior of both operations provides very good devices stability in the relevant temperature range, which is desirable for applications of the RRAM technology.

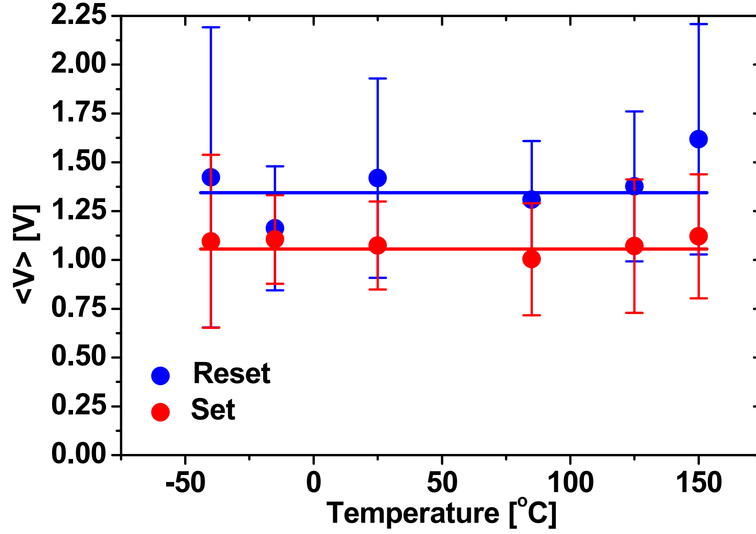


FIG. 7. (Color online) Average values of the Set and Reset switching voltages and their variation with temperature.

The measurement mode only impacts the filament conduction (based on oxygen vacancies[18]) in a quantitative way but not in the conduction mechanism itself. Therefore Current-Voltage HRS characteristics measured in DC mode were used to analyze the conductive filament properties by applying the QPC model at the considered temperature range[13]. In this measurement mode double voltage-sweeps were applied on the Source/Drain terminals (Reset/Set operation, respectively), while recording the Current-Voltage curves. The first sweep (programming step) starts at 0 V and stops at 5 V with a step of 0.05 V, whereas the second one (read out step) follow the opposite voltage trail recording the current in the new state (HRS/LRS, respectively). The applied voltage values V_G were the same as in DC mode, respectively.

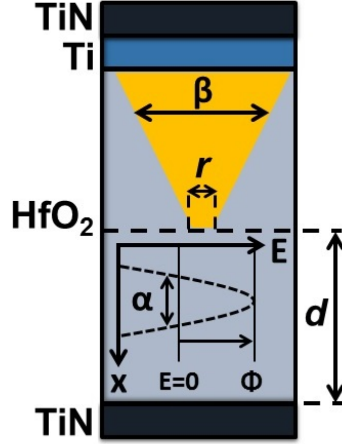


FIG. 8. (Color online) Schematic illustration of the conductive filament shape after the Reset process.

QPC model is based on the idea that there is a constriction point in the filament in HRS. This point is defined as an energy barrier. Both the filament and the energy barrier are characterized by three main parameters: ϕ is the barrier height at the constriction, α is related to the barrier curvature (assuming a parabolic longitudinal potential) thus with the barrier width, and β takes into account how the potential drops at the two ends of the filament. Fig. 8 illustrates the conductive filament shape after the reset process. The relationship between them can be seen in the model HRS current equation[14]:

$$I_{HRS} = \frac{2e}{h}\left\{ eV + \frac{1}{\alpha}\ln\left[\frac{1+\exp\{\alpha[\phi-\beta eV]\}}{1+\exp\{\alpha[\phi+(1-\beta)eV]\}}\right]\right\} \quad (2)$$

The fitting parameters were extracted from 60 devices. By means of Eq. (2) a fitting process was performed with a Least Mean Square algorithm over each HRS Current-Voltage curve. The baseline values were taken from A. Grossi et al.[12]. Then the fitting process was performed applying successive refinements. The average and dispersion values of ϕ and α are shown in Fig. 9.

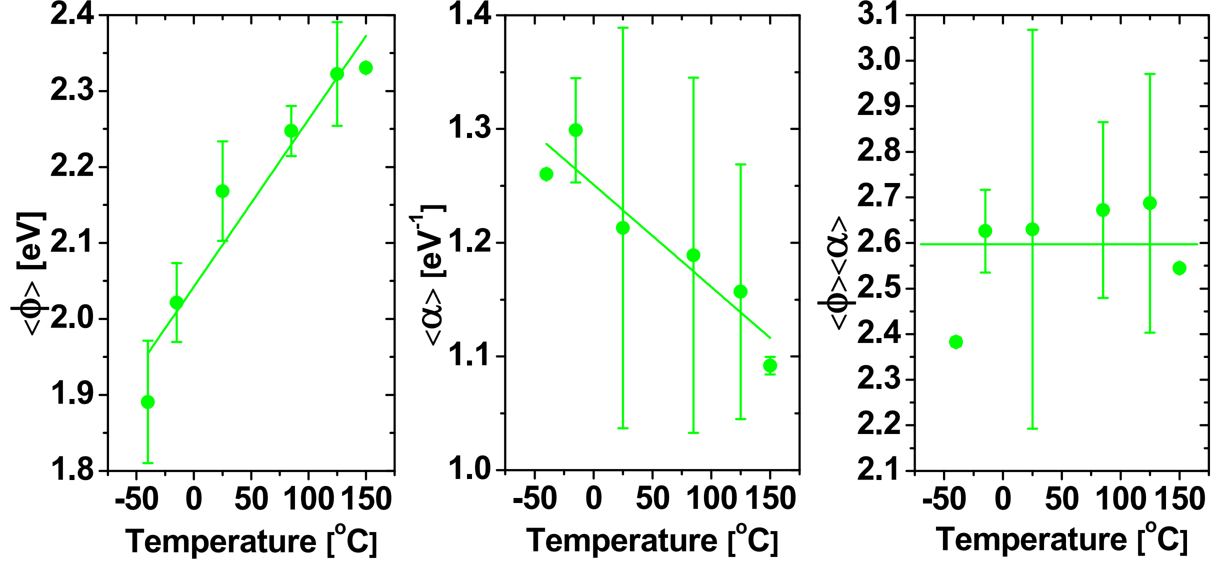


FIG. 9. (Color online) Average and dispersion values of the (a) ϕ and (b) α parameters and (c) their product ϕ· A as function of temperature.

QPC parameters variation shows two opposite temperature effects that change the barrier shape in the constriction point of the filament in HRS[14]. The extracted parameter α is proportional to the width of the barrier [13]. At higher temperatures, the barrier height is increased, whereas the width of the barrier is decreased, as schematically illustrated in Fig. 10. In LRS, the top of the barrier is supposed to be under the energy reference level (E = 0 eV), being the conduction in the constriction point ballistic-like. This theoretical explanation would be consistent with the fact that the conduction through the oxide in LRS state is dominated by the metallic-like conduction attributed to the filament.

Although the parameters α and ϕ were extracted independently from the IV-characteristics, there is a clear correlation between these two parameters [21], which could be captured by assuming that the product of α and ϕ is constant, as illustrated in Fig. 9c. The strong temperature independent correlation indicates that there is a real correlation between width and thickness of the conduction filament's constriction.

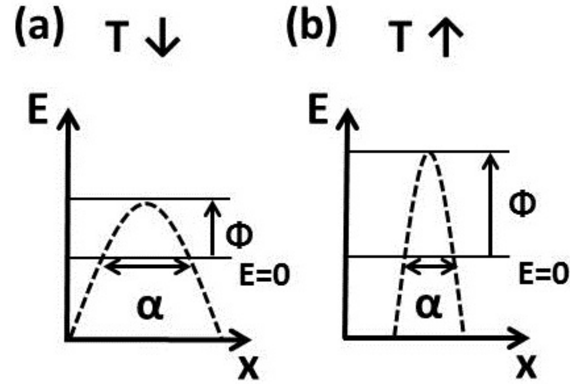


FIG. 10. (Color online) Schematic view of the barrier shape at the filament constriction point, considering (a) low and (b) high temperatures.

Finally the dimension of the constriction point is evaluated by using the barrier parameters: the length (d) and the radius (r) (see Fig. 8). The length is comprised between 0.51-0.46 nm and the radius between 0.35-0.31 nm.

IV. CONCLUSIONS

The temperature dependence of the conduction mechanism and the switching parameters of 1T-1R HfO_2-based devices have been investigated. The corresponding measurements were done in AC mode to figure out the temperature characteristics in application-like conditions and as well as in DC mode for applying the Quantum Point Contact model.

Concerning the leakage current characteristics, the impact of temperature on LRS and HRS is different. In the case of HRS, a tunnel-like conduction mechanism in the filament constriction is supported by a compensation effect between two QPC parameters. In the case of LRS, a metallic-like conduction mechanism is observed,

supported by the linear temperature dependence of the current. Moreover, this phenomenon causes a slight reduction of the On/Off ratio with increasing temperature.

Regarding the behavior of the switching voltages, the temperature variations did not impact the Set and Reset voltage values, which is of high importance for stable RRAM operation.

ACKNOWLEDGMENTS

This work was supported by the European Union's H2020 research and innovation programme under grant agreement Nº 640073 and also supported by ENIAC Joint Undertaking 2013-2, PANACHE Nº 621217.

[1]Q. Lv, S. Wu, J. Lu, M. Yang, P. Hu, and S. Li, J. Appl. Phys. **110,** 104511 (2011).

[2]A. Gyanathan, and Y. Yeo, J. Appl. Phys. **110,** 124517 (2011).

[3]V. Kannan, and J. Rhee, J. Appl. Phys. **110,** 074505 (2011).

[4]S. Nigo, M. Kubota, Y. Harada, T. Hirayama, and S. Kato, J. Appl. Phys. **112,** 033711 (2012).

[5]C. Zambelli, A. Grossi, P. Olivo, D. Walczyk, T. Bertaud, B. Tillack, T. Schroeder, V. Stikanov, and C. Walczyk, IEEE Int. Conf. on Microelectronics Test Structures (ICMTS), 2731 (2014).

[6]A. Grossi, C. Zambelli, P. Olivo, E. Miranda, V. Stikanov, T. Schroeder, C. Walczyk, and Ch. Wenger, IEEE Int. Memory Workshop (IMW), 1–4 (2015).

[7]H.-Y. Lee, P.-S. Chen, C.-C. Wang, S. Maikap, P.-J. Tzeng, C.-H. Lin, L.-S. Lee, and M.-J. Tsai, Jpn. J. Appl. Phys. **46,** 2175–2179 (2007).

[8]Y.S. Chen, H.Y. Lee, P.S. Chen, P.Y. Gu, C.W. Chen, W.P. Lin, W.H. Liu, Y.Y. Hsu, S.S. Sheu, P.C. Chiang, W.S. Chen, F.T. Chen, C.H. Lien, and M.-J. Tsai, IEEE Int. Electron Devices Meeting (IEDM), 1–4 (2009).

[9]B. Govoreanu, G.S. Kar, Y.-Y. Chen, V. Paraschiv, S. Kubicek, A. Fantini, I.P. Radu, L. Goux, S. Clima, R. Degraeve, N. Jossart, O. Richard, T. Vandeweyer, K. Seo, P. Hendrickx, G. Pourtois, H. Bender, L. Altimime, D.J. Wouters, J.A. Kittl, and M. Jurczak, IEEE Int. Electron Devices Meeting (IEDM), 31.6.1-31.6.4 (2011).

[10] F.T. Chen, H.Y. Lee, Y.S. Chen, Y.Y. Hsu, L.J. Zhang, P.S. Chen, W.S. Chen, P.Y. Gu, W.H. Liu, S.M. Wang, C.H. Tsai, S.S. Sheu, M.J. Tsai, R. Huang, Sci. China Inf. Sci. **54,** 1073–1086 (2011).

[11]K. Higuchi, T. Iwasaki, and K. Takeuchi, IEEE Int. Memory Workshop (IMW), 1–4 (2012).

[12]A. Grossi, C. Zambelli, P. Olivo, E. Miranda, V. Stikanov, C. Walczyk, and Ch. Wenger, Solid State Electron. **115,** 17–25 (2016).

[13]E. Miranda, C. Walczyk, C. Wenger, and T. Schroeder, IEEE Electron Dev. Lett. **31,** 609 (2010).

[14]E. Miranda, D. Jimenez, and J. Suñé, IEEE Electron Dev. Lett. **33,** 1474 (2012).

[15]A. Grossi, D. Walczyk, C. Zambelli, E. Miranda, P. Olivo, V. Stikanov, A. Feriani, J. Suñé, G. Schoof, R. Kraemer, B. Tillack, A. Fox, T. Schroeder, Ch. Wenger, and C. Walczyk, IEEE Trans. Electron Dev. **62,** 2502 (2015).

[16]J. Bardeen, J. Appl. Phys. **11,** 88-111 (1940).

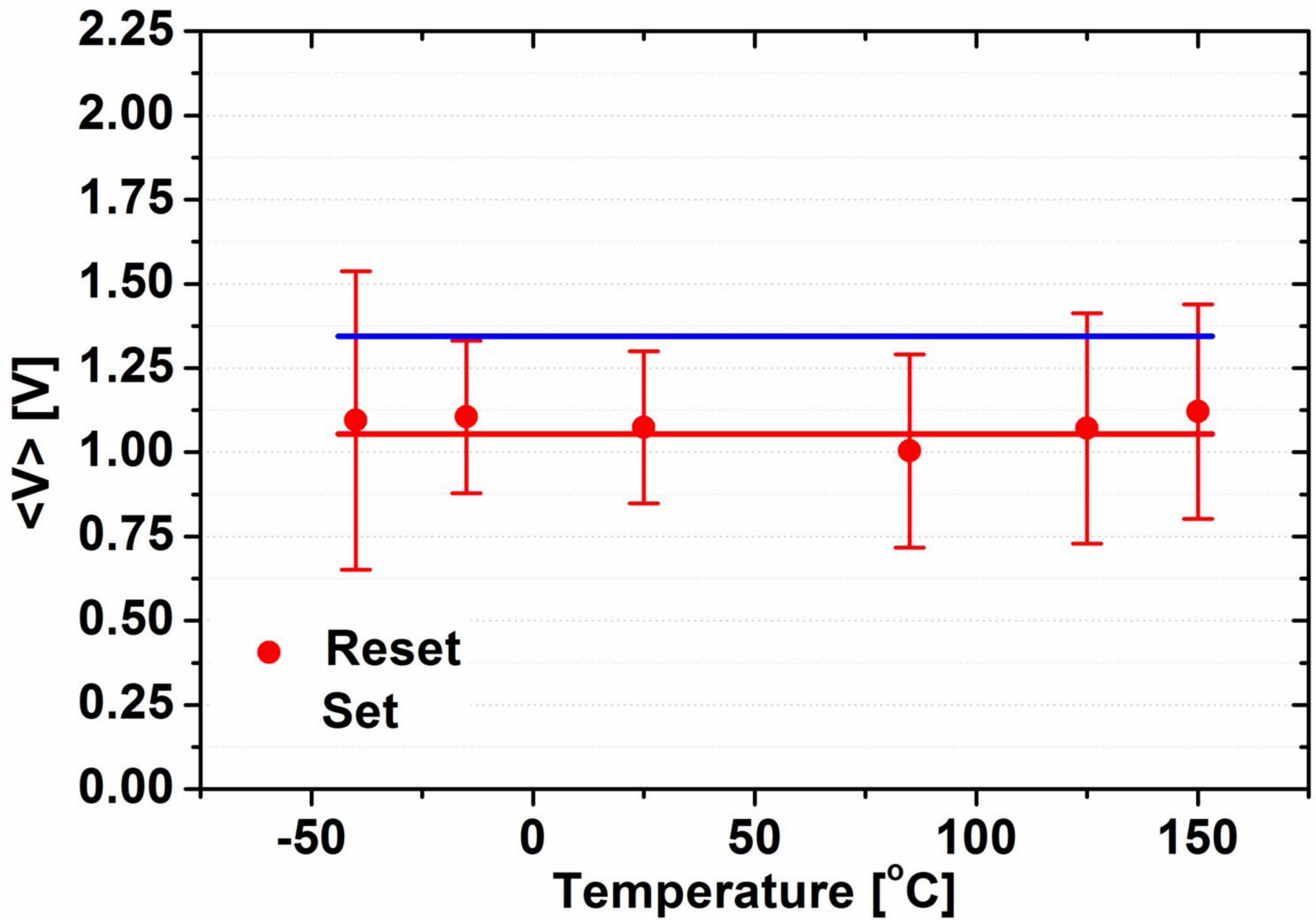
[17]C. Walczyk, D. Walczyk, T. Schroeder, T. Bertaud, M. Sowinska, M. Lukosius, M. Fraschke, D. Wolansky, B. Tillack, E. Miranda, and Ch. Wenger, IEEE Trans. Electron Dev. **58,** 3124 (2011).

[18]Y.S. Lin, F. Zeng, S.G. Tang, H.Y. Liu, C. Chen, S. Gao, Y.G. Wang, and F. Pan, J. Appl. Phys. **113,** 064510 (2013).

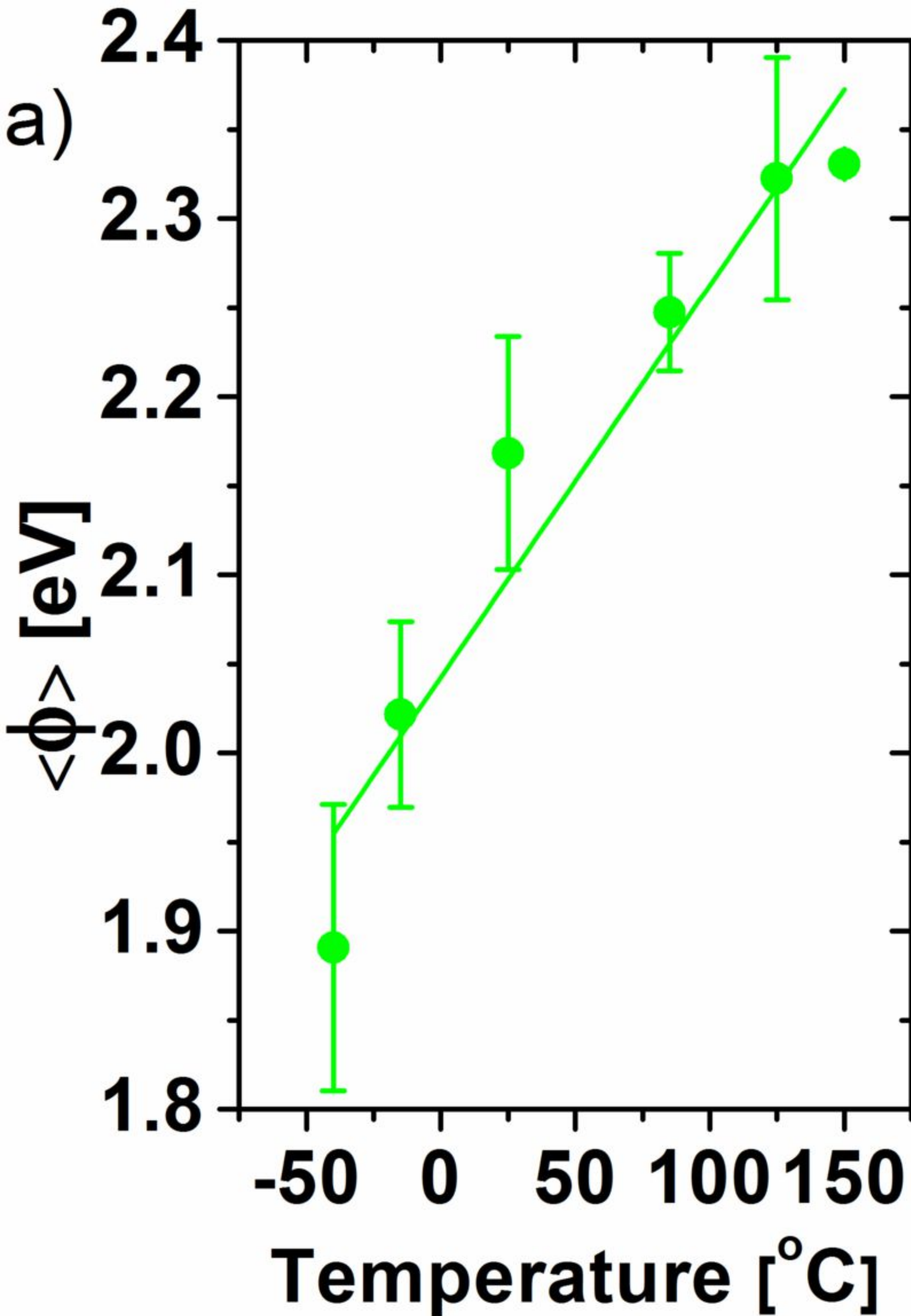
[19]M. Puglisi, A. Qafa, and P. Pavan, IEEE Electron Dev. Lett. **36,** 244 (2015).

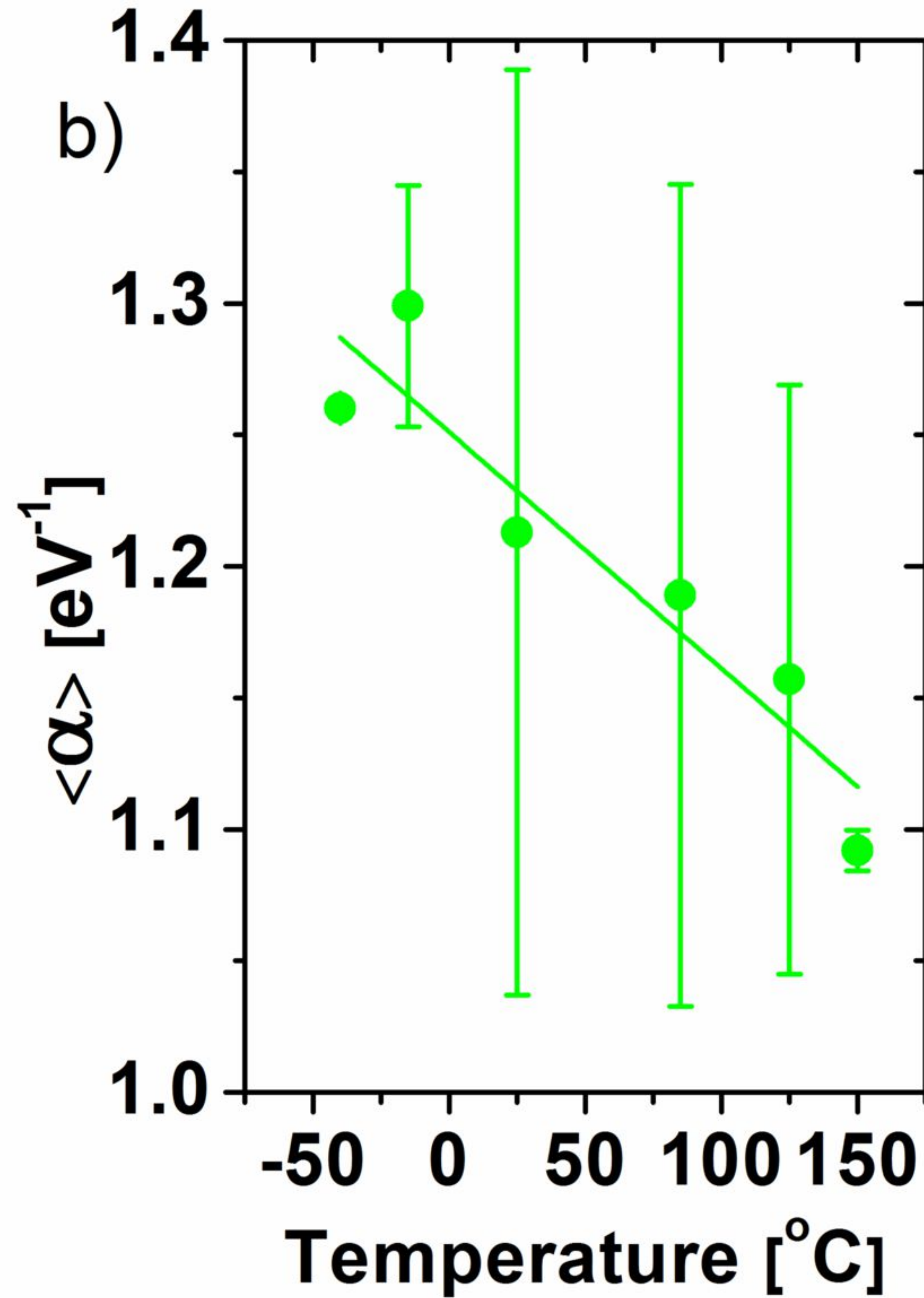
[20]F.-C. Chiu, Advances Mater. Sci. Eng. **2014,** 578168 (2014).

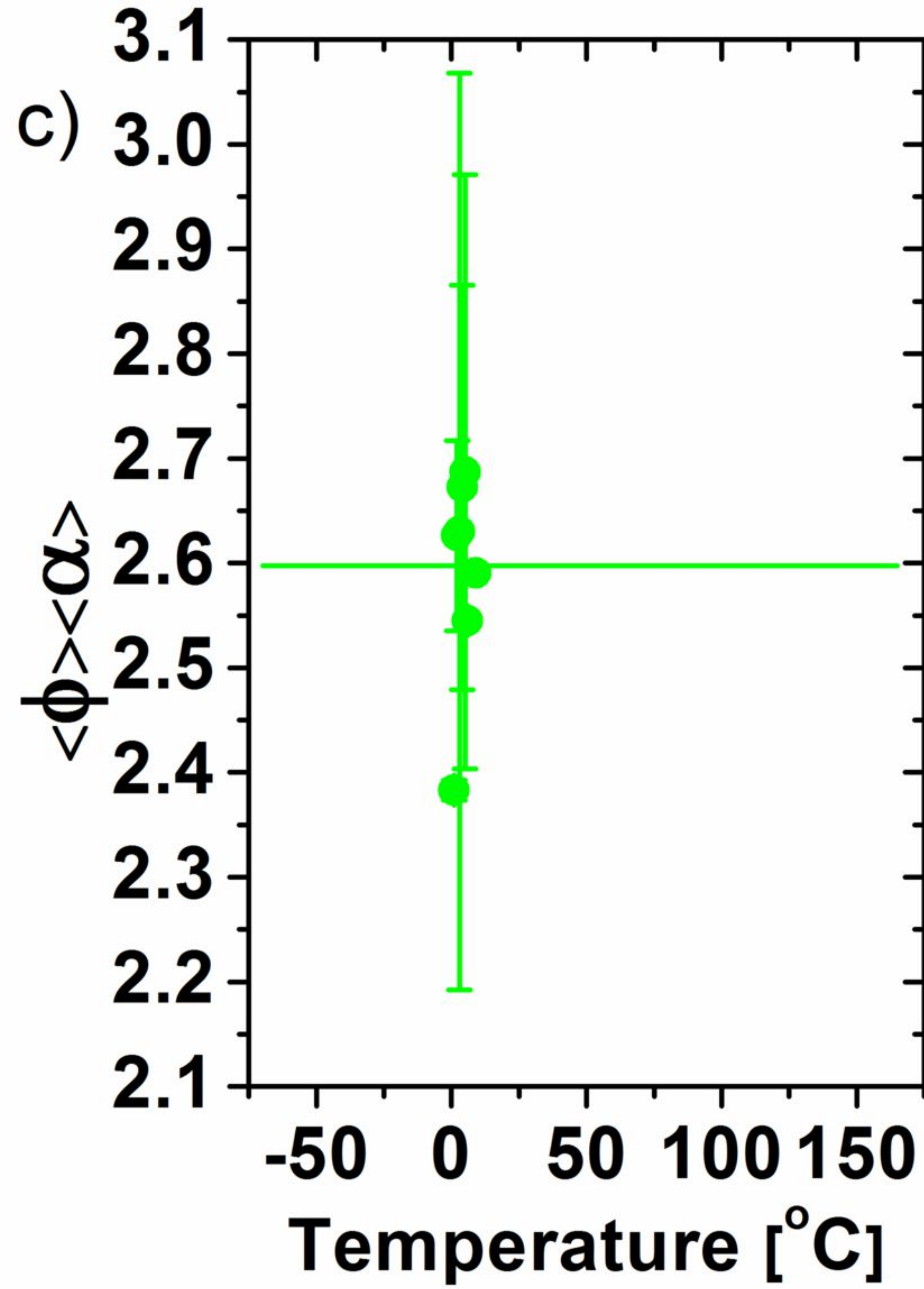
[21]X. Lian, S. Long, C. Cagli, J. Buckley, E. Miranda, M. Liu, J. Sune, 2012 13th International Conference on Ultimate Integration on Silicon (ULIS) (pp. 101-104).

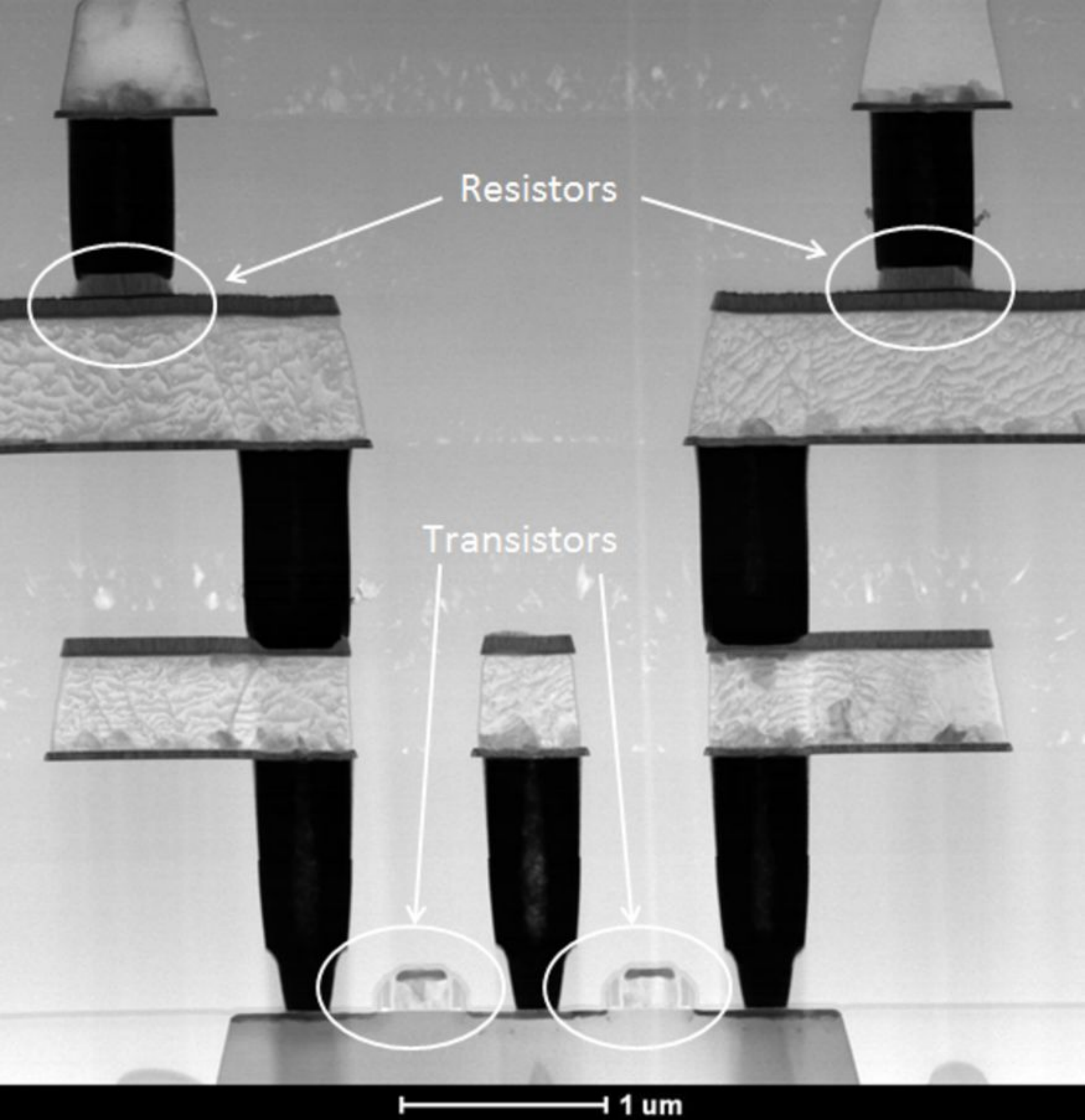


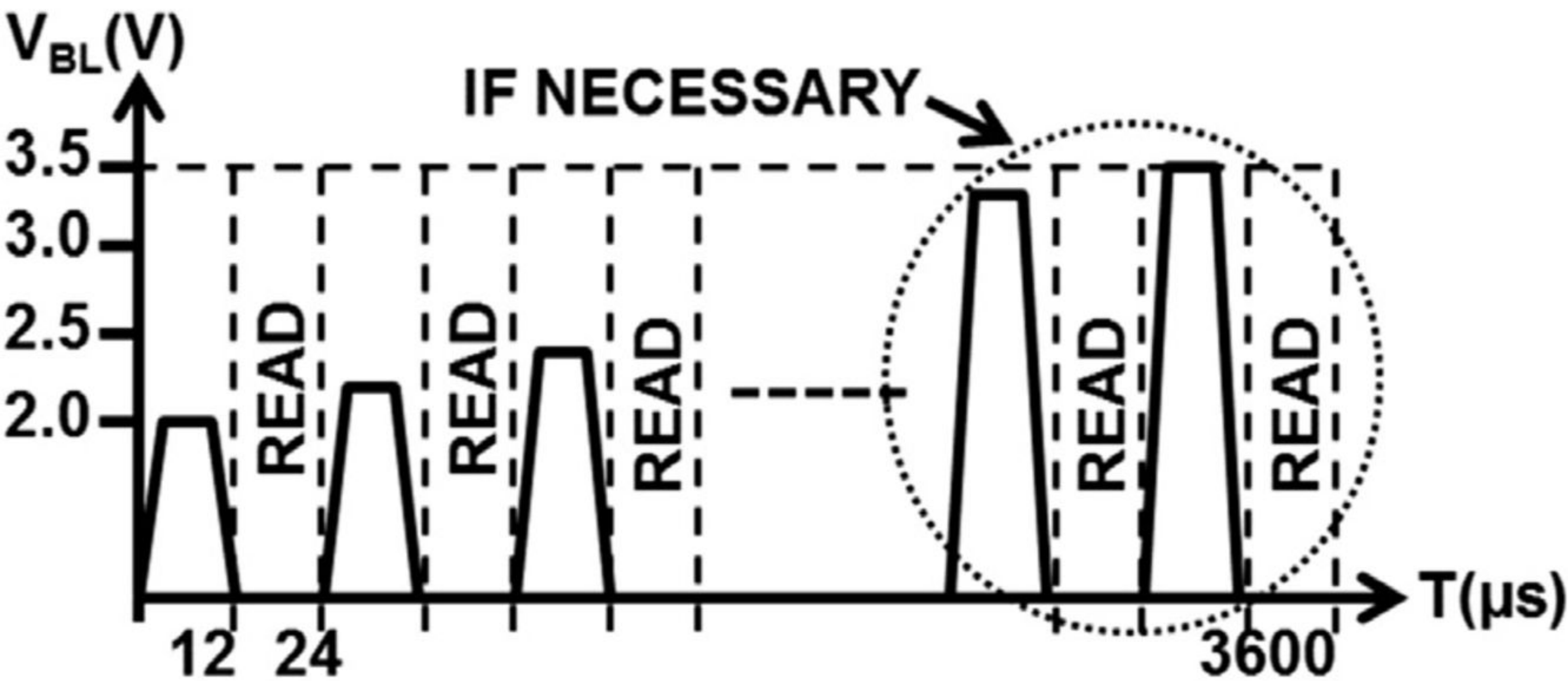
2.25
2.00
1.75
1.50
1.25
1.00
0.75
0.50
0.25
0.00
<V> [V]
-50
0
50
100
150
Temperature [°C]
Reset
Set


a)
2.4
2.3
2.2
2.1
2.0
1.9
1.8
<ϕ> [eV]
-50
0
50
100
150
Temperature [°C]

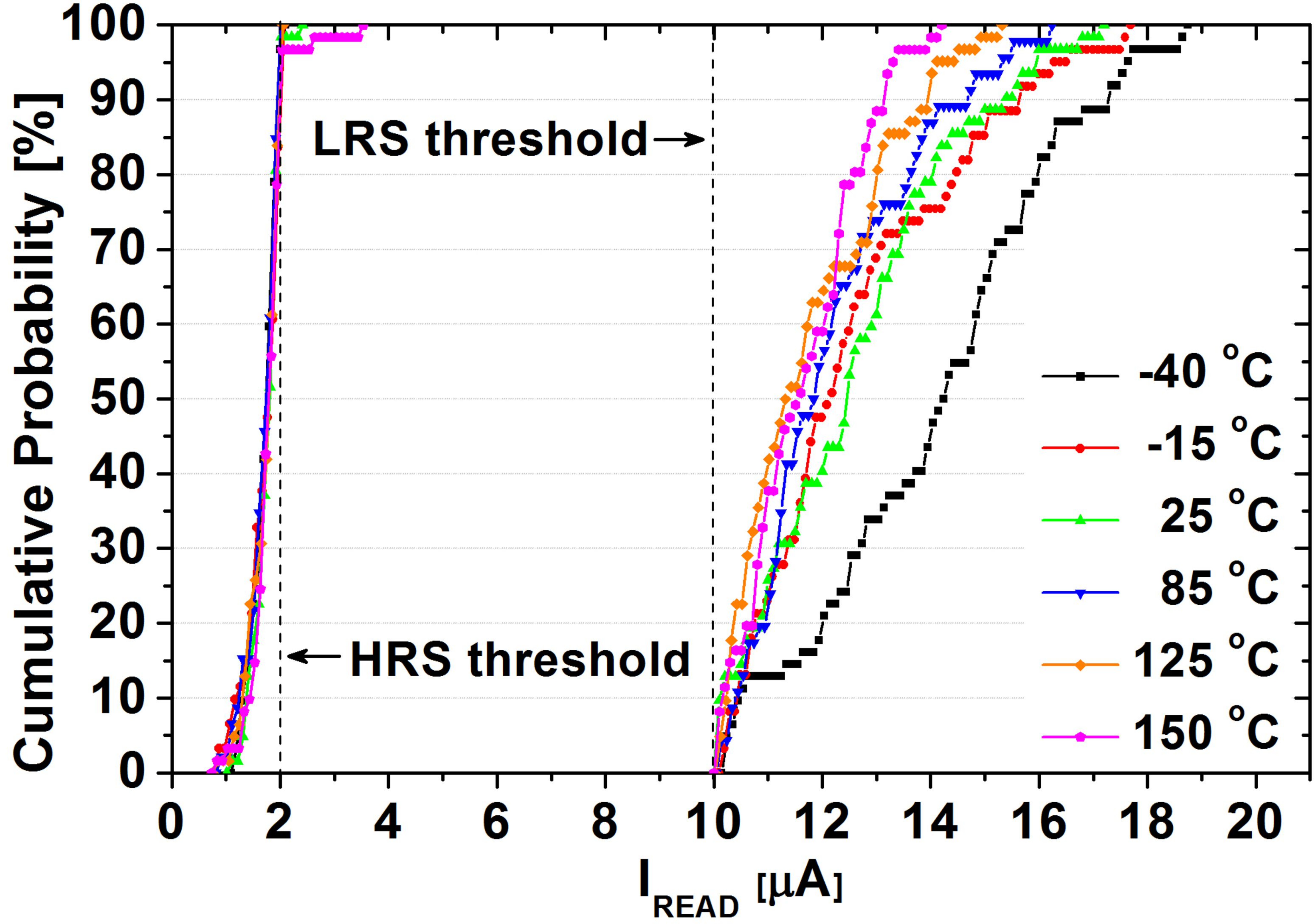

b)
1.4
1.3
1.2
1.1
1.0
<α> [eV-1]
-50
0
50
100
150
Temperature [°C]

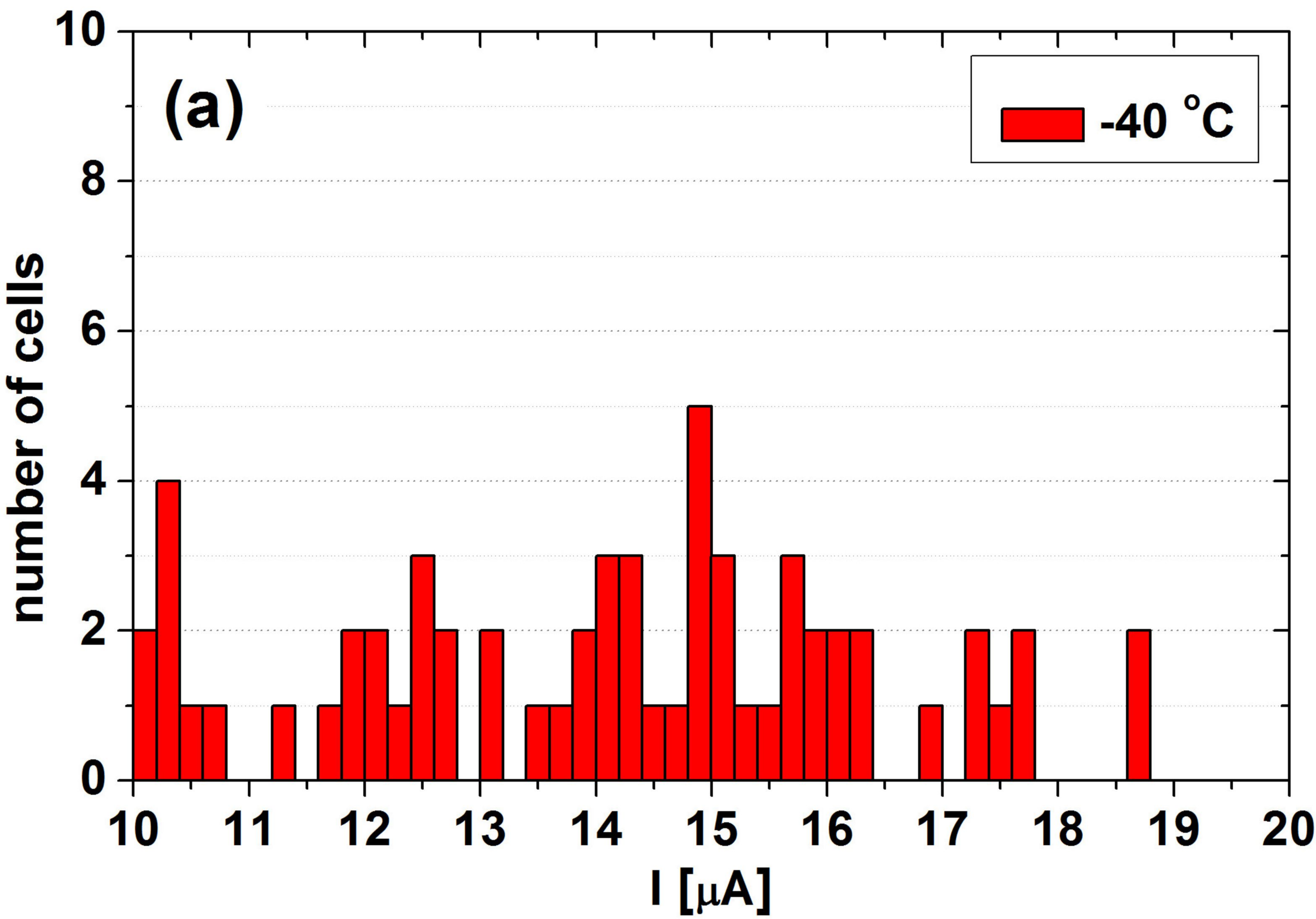

c)
3.1
3.0
2.9
2.8
2.7
2.6
2.5
2.4
2.3
2.2
2.1
<ϕ><α>
-50
0
50
100
150
Temperature [°C]

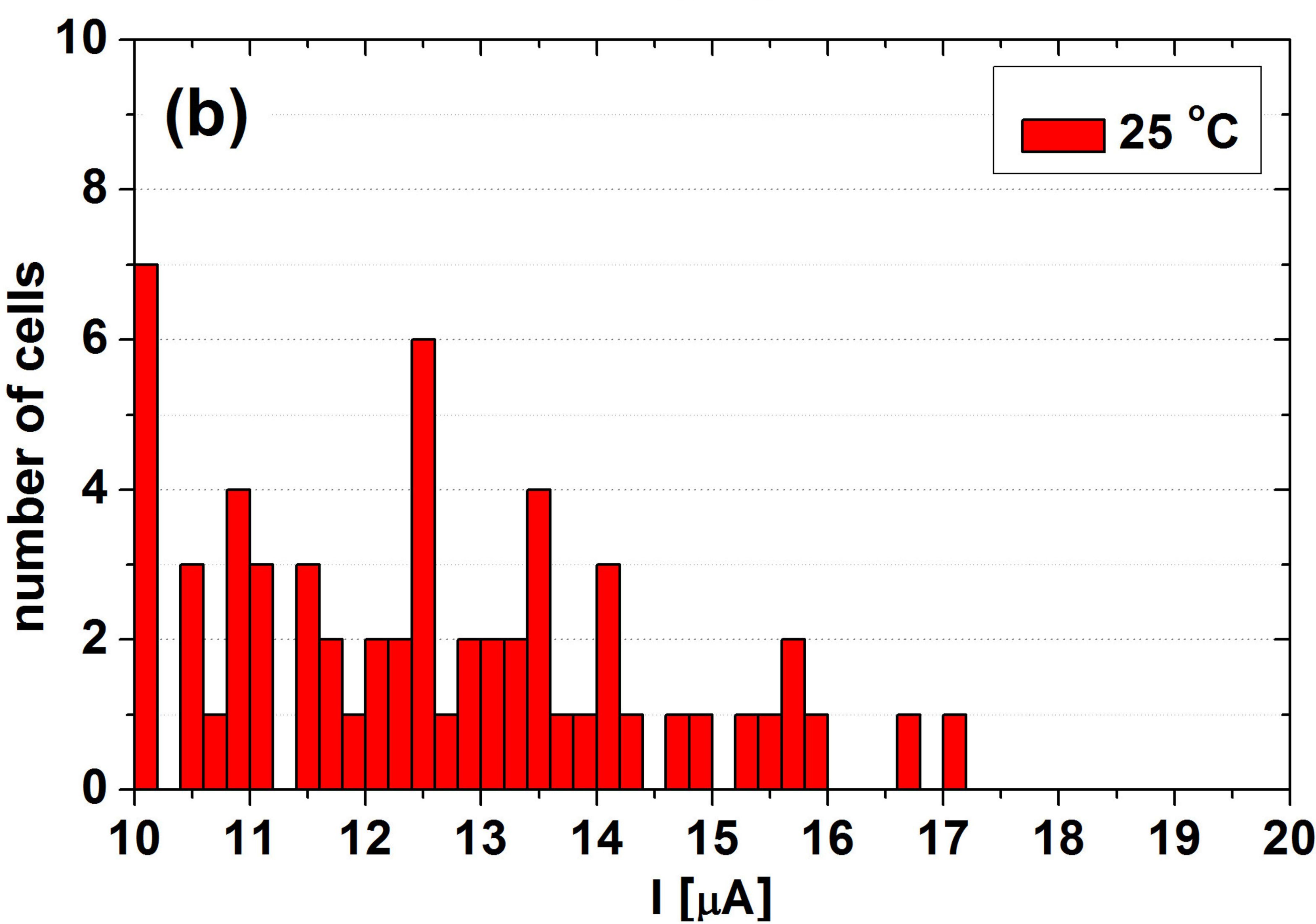

Resistors
Transistors
1 um

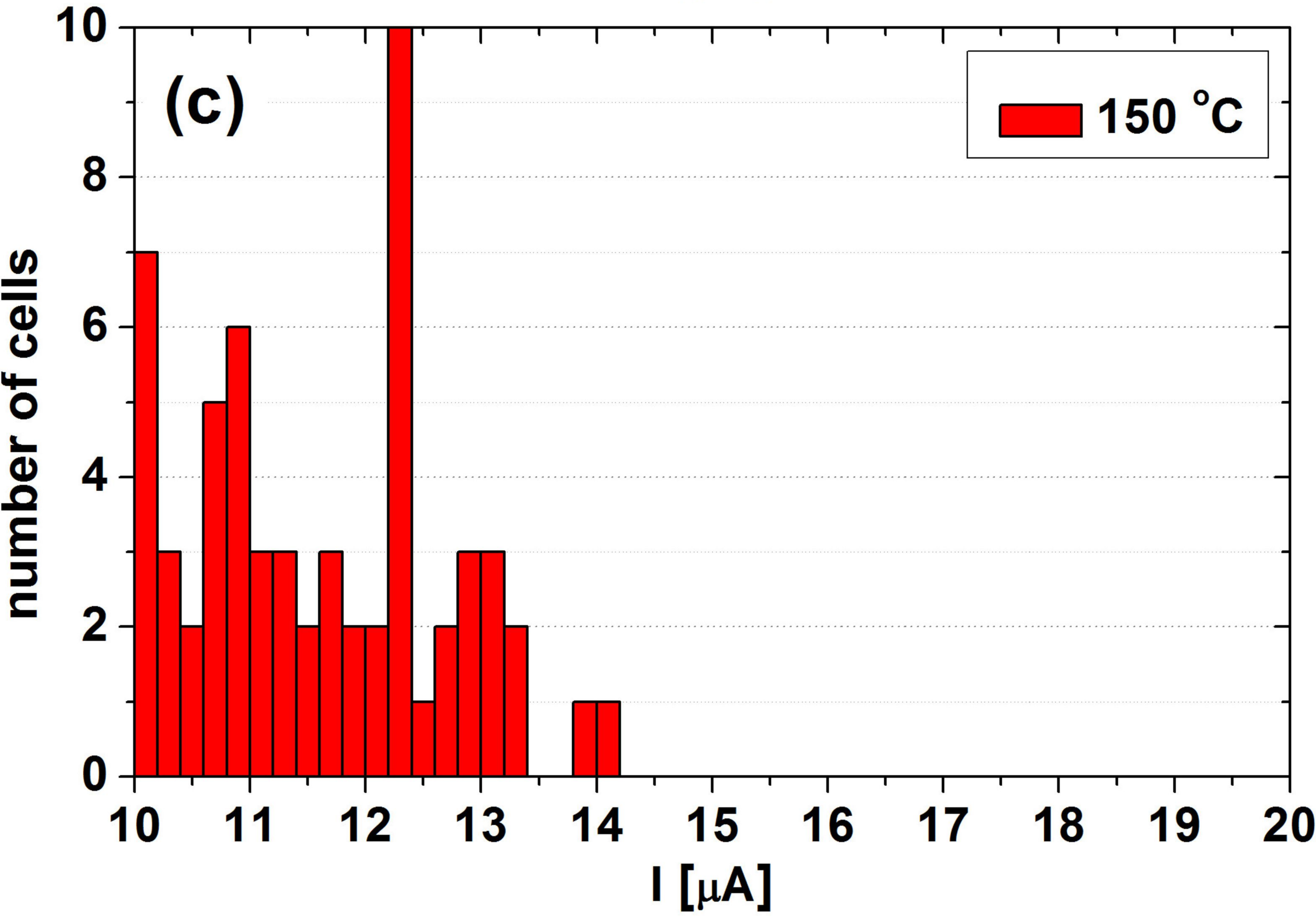


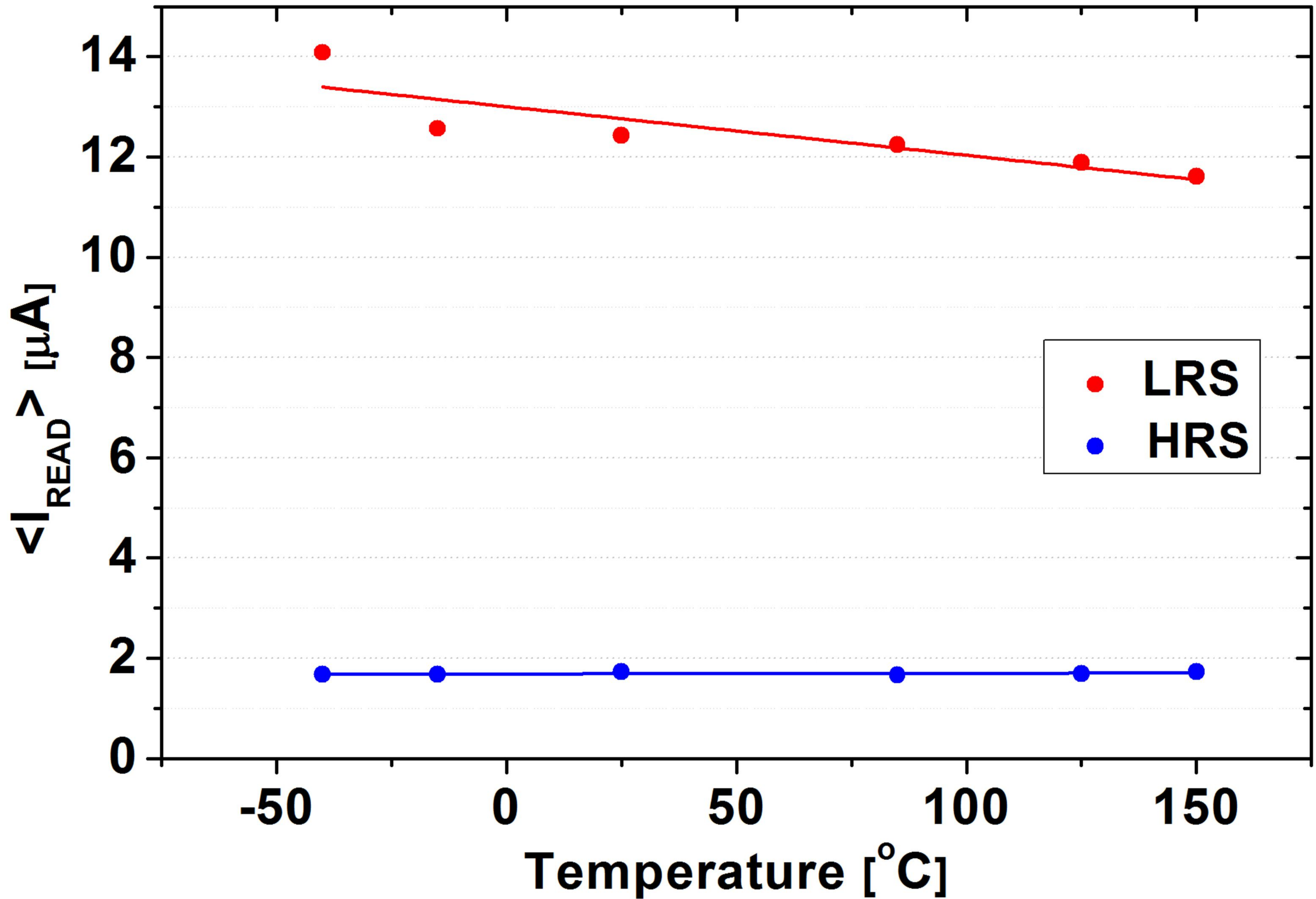
V_{BL}(V)
IF NECESSARY
3.5
3.0
2.5
2.0
READ
READ
READ
READ
READ
T(μs)
12
24
3600

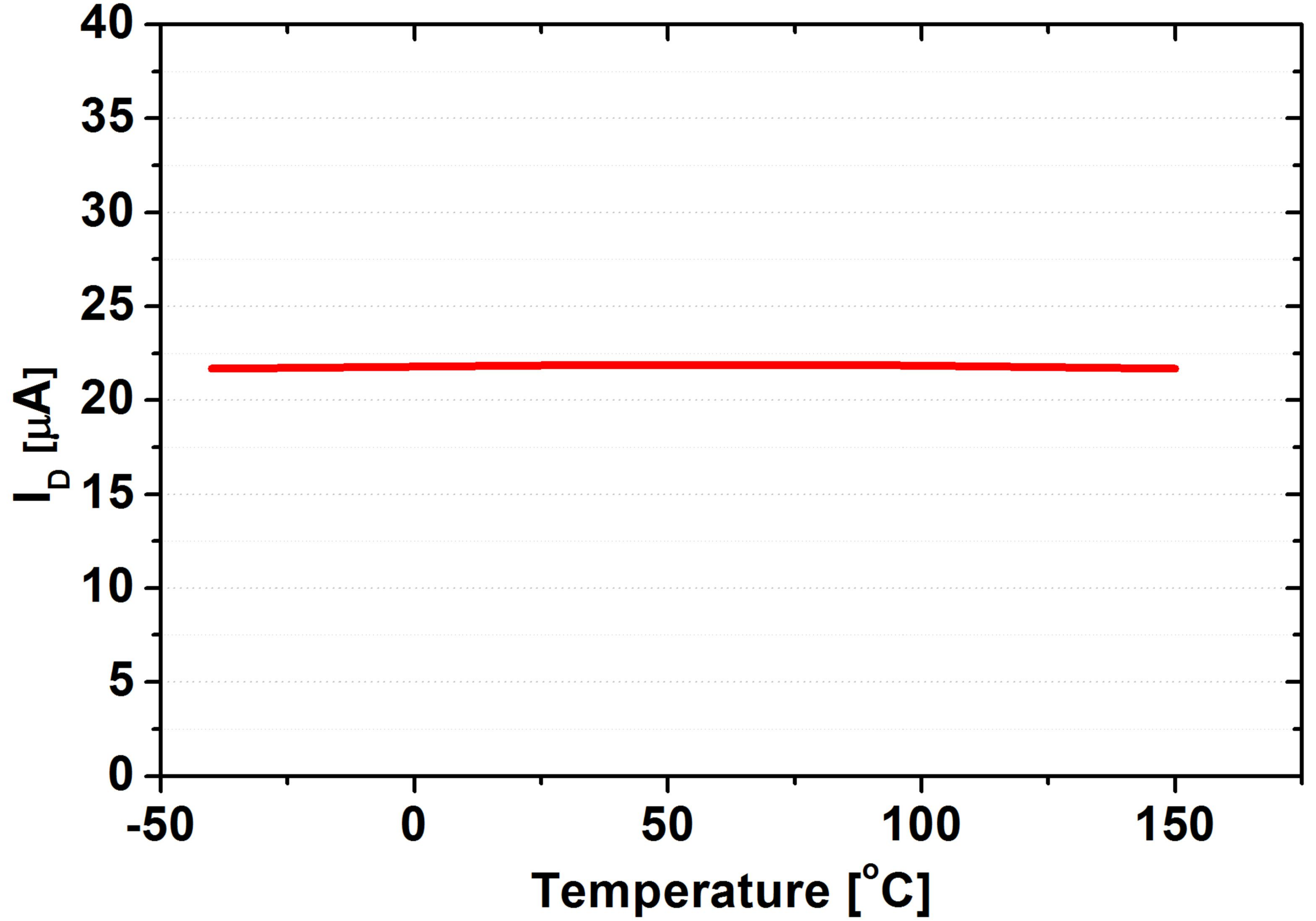

Cumulative Probability [%]
100
90
80
70
60
50
40
30
20
10
0
LRS threshold
HRS threshold
-40 °C
-15 °C
25 °C
85 °C
125 °C
150 °C
0
2
4
6
8
10
12
14
16
18
20
I_READ [μA]


(a)
-40 °C
number of cells
I [μA]
0
2
4
6
8
10
10
11
12
13
14
15
16
17
18
19
20

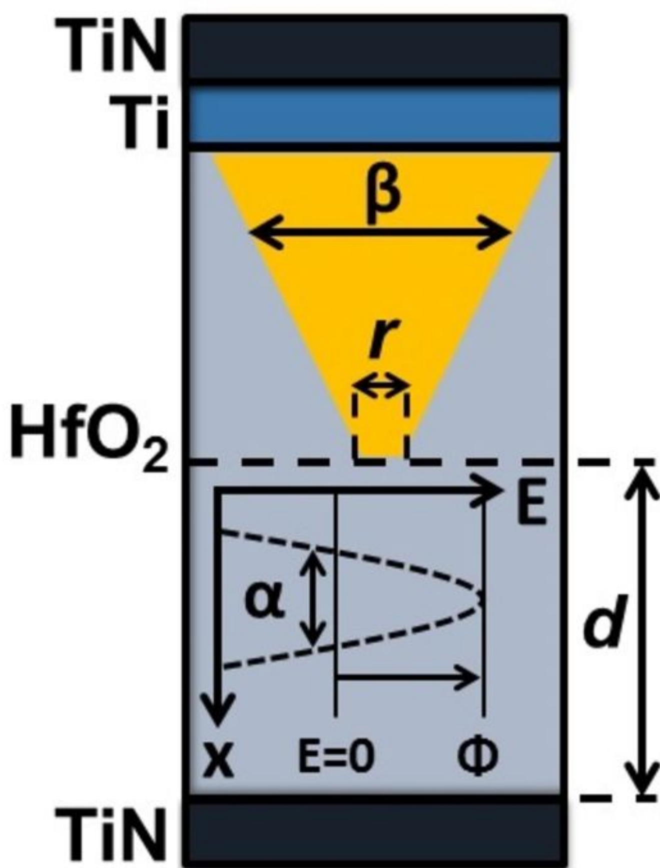

(b)
25 °C
number of cells
I [μA]
0
2
4
6
8
10
10
11
12
13
14
15
16
17
18
19
20

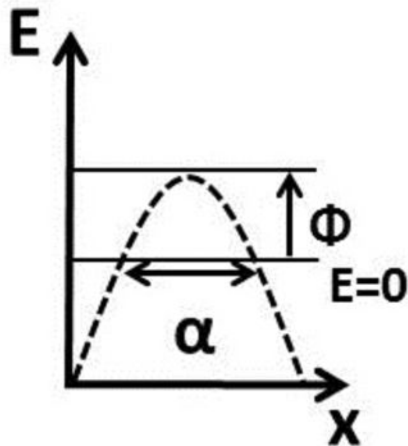

(c)
150 °C
number of cells
I [μA]
0
2
4
6
8
10
10
11
12
13
14
15
16
17
18
19
20

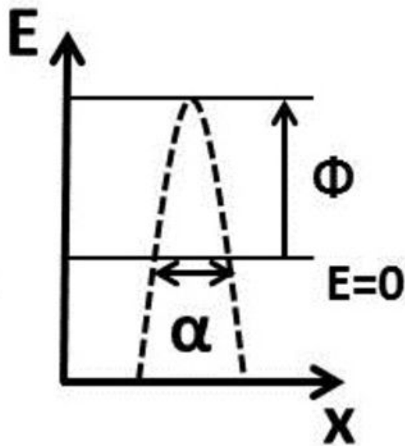

14
12
10
8
6
4
2
0
-50
0
50
100
150
Temperature [°C]
<I_READ> [μA]
LRS
HRS



40
35
30
25
20
15
10
5
0
I_D [μA]
-50
0
50
100
150
Temperature [°C]


TiN
Ti
β
r
HfO2
E
α
d
x
E=0
Φ
TiN


(a)
T ↓
E
Φ
E=0
α
X


(b)
T ↑
E
Φ
E=0
α
X