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Radiation hard design of HfO_2 based 1T1R cells and memory arrays

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***Abstract*—In this work the electrical performance of a Rad-Hard designed 1T1R device based on the combination of an Enclosed Layout Transistor (ELT) and an TiN/HfO_2/Ti/TiN based resistor are presented for the first time. Moreover, an architectural solution for 1Mbit radiation hard RRAM array implementation is proposed.**

I. Introduction

Semiconductor memories, among rad-hard integrated circuit scenario, are one of the most critical topics for space applications. Actually both volatile and non-volatile memories, excluding few exceptions, are integrated using standard processes and standard architectures. This means that the final device is typically at least Rad-tolerant and not Rad-Hard and failure during mission is avoided using Error Correcting Code techniques including redundancy at the board level. Since standard silicon memories, such as flash memories tend to fail under irradiation, a new approach is envisaged: the development of a specific memory technology, so called resistive random-access memory (RRAM). The switching effect of the RRAM devices is determined by the formation and modification of conductive filaments composed of oxygen vacancies, which are controlled through the motion of oxygen anions by an applied electric field [1]–[4]. The intrinsic radiation tolerance of RRAM significantly reduces sensitivity to radiation-induced bit upsets [5]. Nevertheless, the 1T1R structure of the memory array consists of NMOS access transistors, which are sensitive to radiation [6]. In standard NMOS devices, ionizing radiation may generate holes trapped in the gate oxide, and the trapped holes could induce leakage paths from the drain to the source region. A suitable approach to eliminate the leakage path in NMOS transistors is to adopt a gate-enclosed layout [7]. For the first time, we will present the electrical performance of a Rad-Hard designed 1T1R device based on the combination of an Enclosed Layout Transistor (ELT) and an TiN/HfO_2/Ti/TiN based resistor, as shown in Fig. 1.

II. Memory architecture

From the architectural point of view a 1Mbit test vehicle implementing RRAM array will be presented. In order to achieve an increased resistance against radiation the single bit is the result of the contribution of two RRAM cell located in different array locations; this guarantees an internal redundancy (no reference cells are required for read mode operations) and a wider margin window in a sensing module very similar to SRAMs. In Fig. 2 is shown the architectural approach where two arrays (left and right) contain left cells and rights cells: a 1 is the result of a low resistance in the left cell (red circle) and a high resistance in the right cell (green circle), vice-versa for a 0. The differential cell approach, thanks also to the independence of row decoding final stages and column decoding switches, guarantees resistance against Single Event Effects (SEEs) disturbs in all conditions (Read, Set and Reset modes).

The 1Mbit device will be the result of the ensemble of eight 128kbit modules (see Fig. 2) each having its own decoding scheme, ATD (Address Transition Detection) and sense amplifier. This architectural approach protect the test vehicle against Multiple Bit Upset (MBU) reducing every contribute from charged particle to at least only one Single Event Upset (SEU) as already demonstrated in previous SRAM devices [8], [9]. Even if complete of all decoding schemes the 1Mbit (2Mcells) device also contains Direct Memory Access (DMA) in order to provide the possibility to characterize the behavior of RRAM cells independently from the sensing scheme and setting/resetting circuitry. This freedom degree enable the access via ATE equipment for all analysis related to set and reset state distributions and a better approach to the real characterization of the resistive state of the cell in very different conditions (voltage gate, drain and source).

III. Conclusions

The analysis performed demonstrated the validity of the developed ELT at different temperatures, allowing to investigate and understand the properties of the technology. The proposed memory architecture allows to achieve an increased resistance against radiation thanks to internal redundancy and to access RRAM cells through ATE equipment for characterization.

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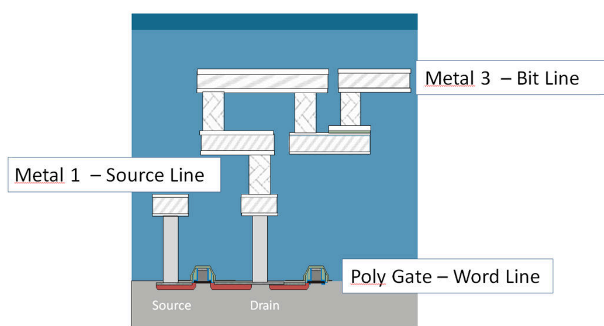
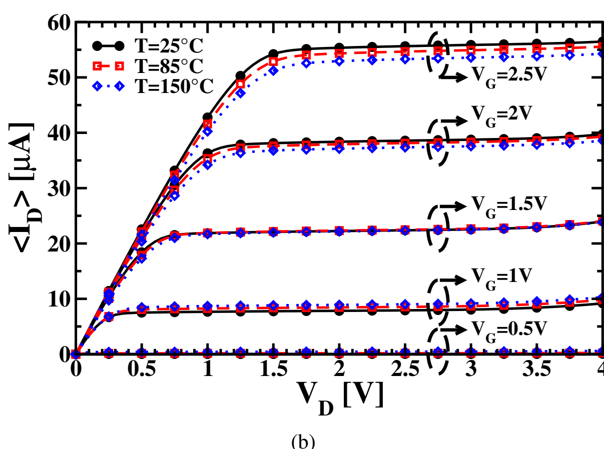


(a)



(b)

Fig. 1. Schematic cross view of the Rad Hard designed 1T1R cell (a). Current Voltage characteristics of the access ELT (b).

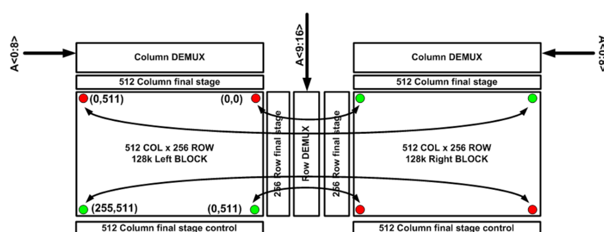


Fig. 2. Single Bit Architecture of the 1Mbit (2Mcell) test vehicle implementing RRAM array.

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