RRAM Reliability/Performance Characterization Through Array Architectures Investigations

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***Abstract*—The reliability and performance characterization of each non-volatile memory technology requires the thorough investigation of dedicated array test structures that mimic the real operations of a fully functional integrated product. This makes no exception also for emerging non-volatile memories like the Resistive Random Access Memory (RRAM) concept. An extensive electrical characterization activity performed on test vehicles manufactured in a CMOS backend-of-line process allowed the first glance estimation of operation modes and reliability threats typical of this technology. In this paper, it is provided a review of the most important issues like forming instabilities, optimal set/reset operation finding, and read disturb to provide a guideline either for a further technology optimization or an efficient algorithms co-design to handle these reliability/performance threats.**

***Index Terms*—RRAM; test-structures; array; reliability; performance**

I. Introduction

The Resistive Random Access Memories (RRAM) are a promising candidate to become a key memory technology in several applications. From a technological standpoint, embedded HfO_2-based RRAM devices are interesting because they offer compatibility with the standard CMOS backend-of-line (BEOL) process scheme and very fast operation times, mostly below the 100 ns limit. Extensive characterizations have been performed in the framework of a concept-validation for possible replacement of existing non-volatile memory technologies, trying to ease the evolution from single cell test structures to fully functional integrated array products [1]–[4].

In the last decade, most of the analysis, especially those devoted to provide a solid understanding of the physical mechanisms ruling the RRAM operations, have been performed on simple 1T-1R architectures where a select transistor or a diode is connected in series to the resistive element [3]. However, although this demonstrated competitive features with respect to the traditional floating gate-based Flash technology, single devices are not ideal to study the statistical distribution of the inter-cell variability of memory elements. Moreover, that solution does not allow a thorough characterization of the typical issues evidenced in a memory product such as disturbs, cells interaction, sub-optimal writing algorithms or cell faults due to process induced variability.

In this work we will present a review of the most important issues retrieved during the electrical characterization of 4kbits RRAM memory array test structures with the associated control circuitry designed in a 0.25 μm BiCMOS technology node [5]. The results will show that some important reliability threats that could severely limit the ramp-up of the RRAM arrays toward a technology mature level, can be addressed by simply acting on the operative conditions of the cells within the array and on the algorithms that handle the read/write operations. The common analysis performed in these test arrays are mainly related to the evaluation of the performance and of the reliability features of the technology, through the application of voltage/current waveforms at dedicated test pads for the following operations: forming, set, reset, and read. The applied waveforms shape, duration, and amplitude determine the behavior of the array either on a short time-scale (e.g., characterization of the read window, determination of the variability, etc.) or on a longer time-scale (e.g., endurance and retention evaluations).

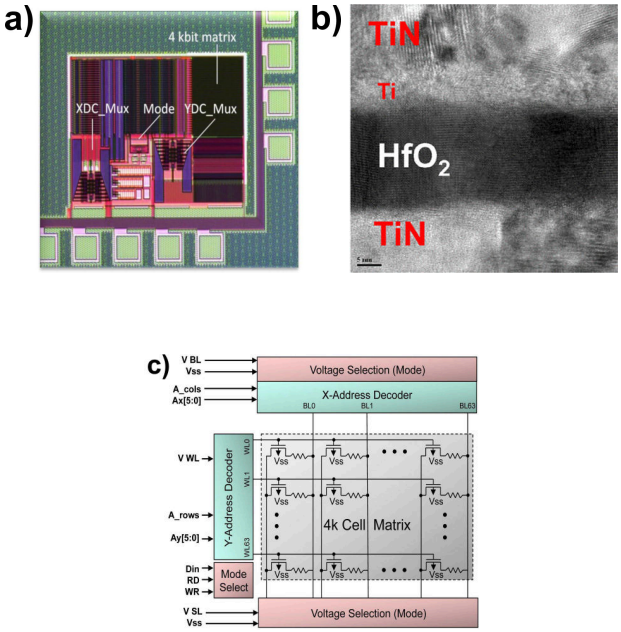

Fig. 1. Microphotograph of the 4kbits memory array with control circuits (a). Cross-Sectional STEM Image of the integrated MIM stack in the ReRAM Cell (b). Simplified block diagram of the memory array (c).

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II. Test vehicle manufacturing

The structure of the 4kbits memory array (see Fig. 1) is described by four architectural blocks: the array of 4096 1T-1R RRAM cells; a wordline (WL) address decoder (XDC MUX); a bitline (BL) address decoder (YDC MUX); and an operation control circuitry (Mode) to handle read and write operation commands. The memory cells are constituted by a select NMOS transistor featuring W=1.14 μm and L=0.24 μm in series to a variable resistor connected to the bitlines.

The variable resistor is a Metal-Insulator-Metal (MIM) stack fabricated on 150 nm TiN bottom electrodes deposited by magnetron sputtering with sheet resistances in the order of 10-50 Ωsq^{-1} directly on the last metallization of the BiCMOS process. Next, HfO_2 films of 9nm thickness were grown in an AVD chamber at 320 °C using $Hf[N(MeEt)]_4$ precursor and O_2 as reactive gas. Finally, 10 nm Ti and 150 nm TiN were sputtered onto the HfO_2 layer [6], [7]. To investigate the impact of the MIM area on the memory performances and variability two different arrays have been integrated using 0.6 μm^2 and 1 μm^2 resistor area, respectively.

III. Forming operation variability and instabilities

RRAM behavior is based on the possibility of electrically modifying the conductance of a Metal-Insulator-Metal (MIM) stack: the Set operation switches the cell into a high conductive state, whereas Reset brings the cell back to a low conductive state. Some technologies like HfO_2-based RRAM require a preliminary forming operation to activate such a switching behavior by creating a conductive filament (CF) in the dielectric material [5], [8]–[10]. Even if such forming process is performed just once, it plays a fundamental role in determining the system performance [10]. A deep understanding of the forming process allows recognising faulty cells in the array from scratch and to get a first glance insight on the cells reliability and performances during lifetime. Forming usually consists in the application of a quasi-DC sweep on the BL up to V_{BL} = 3.5 V with step voltage equal to 0.025 V. To prevent hard breakdown, the saturation current of the select transistor is controlled by the WL voltage fixed at V_{WL} = 1.4 V, which translates into a compliance current almost equal to 300 μA. The forming process in the array could be accelerated by selecting multiple rows and/or columns simultaneously using the Mode circuitry. After the operation it is possible to read the array content by applying V_{WL} = 1.4 V and a read voltage V_{BL} considerably lower than the switching voltages requested for the set and reset operations.

Fig. 2 depicts the variability of the forming voltage distribution and the cumulative probability data of the read currents measured on the entire array before and after the forming operation. The large variability in forming voltages indicates the peculiar behavior for each of the cells in the array. Before forming the read currents are distributed around a mean value μ = 4.03 μA with a standard deviation σ = 0.48 μA, whereas after forming the average current were distributed around μ = 30.31 μA with a standard deviation σ = 0.23 μA. These

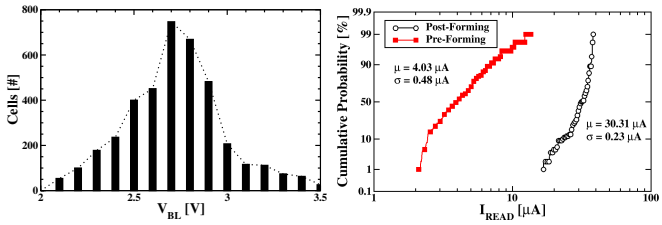

Fig. 2. Forming voltage distribution (left) and distributions of the read current in a ReRAM array with 1μm^2 MIM area before and after forming (right) [7].

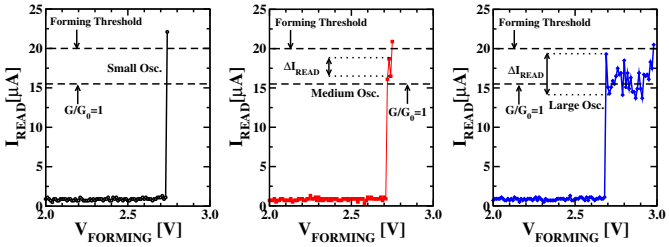

Fig. 3. Three different behaviors observed during forming process: small (left), medium (centre) and large (right) read-verify current oscillations [11].

results are obtained on arrays based on 1 μm^2 MIM area, however similar results are found in 0.6 μm^2 MIM area arrays. The analysis of the pre-forming distribution allows an indirect insight on the process induced variability in the MIM stack. In this technology, pre-forming currents larger than 10 μA usually indicate leaky cells due to fabrication issues such as the intrinsic variability of the HfO_2 deposition process [5]. This source of variability is also responsible for forming failures (i.e., cells that are unable to be formed), which is considered as a major contribution for the array yield loss (i.e., 40% of the cells in the array). A possible solution for this reliability threat has been proposed in [7] by using a forming-retry operation on the cells that are not able to create a CF, increasing the yield up to 99%.

Another issue retrieved during forming operation is the intrinsic instability of the created CF that could impact on the successive set/reset switching operations [11]. Indeed, by monitoring the cells forming behavior through an incremental pulse forming technique it is observed that the read current during forming could exhibit, in some cells, an oscillatory behavior (see Fig. 3). These oscillations interpreted either as the charging of a trap close to the surface of the conductive filament (CF) or the movement of an atom/defect in the filament [12], has been investigated in terms of reliability and cell-to-cell variability during 1k endurance cycles and 100k stress pulses in different cycling conditions.

Fig. 4 shows the cumulative distributions of the resistance ratio, set and reset switching voltages calculated after cycling. Resistance ratio is calculated as the ratio of the set state read current and reset state read current I_{LRS}/I_{HRS} at $V_{read} = 0.2V$. The cells formed with smaller oscillations are shown to require higher V_{SET} and V_{RES} after 1k cycles: that means small oscillations correspond to wider filaments. The Resistance Ratio, V_{SET}, V_{RES} average values and dispersion

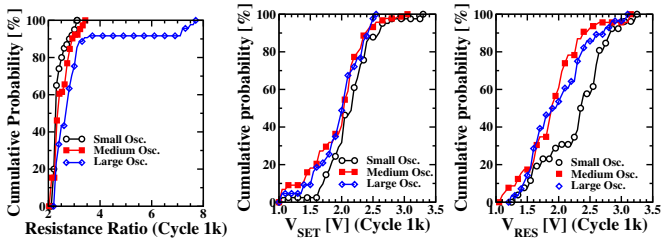

Fig. 4. Resistance ratio, V_{SET}, V_{RES} cumulative distributions for the different forming oscillations groups calculated on cycled devices [11].

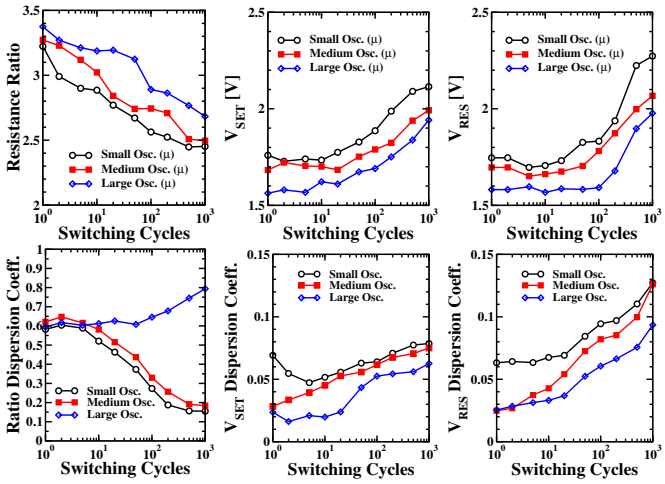

Fig. 5. Resistance Ratio, V_{SET} and V_{RES} average values and dispersion coefficients calculated during cycling [11].

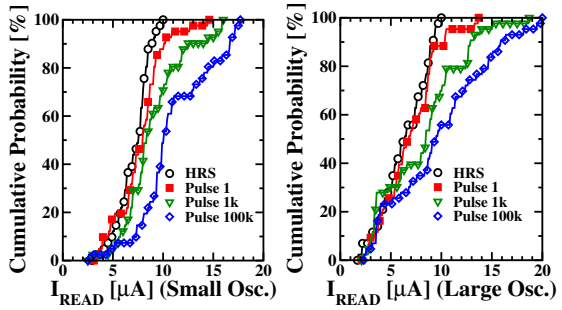

Fig. 6. Cumulative distributions of the read currents (with $V_{read} = 0.2V$) measured during set stress on HRS after different number of disturb pulses, at endurance cycle 1 [11].

coefficients calculated during cycling are reported in Fig. 5. To evaluate the cell-to-cell variability the dispersion coefficient of I_{LRS} and I_{HRS} distributions, defined as (σ^2/μ), has been used. Resistance ratio of cells with large forming oscillations show both higher average value and dispersion coefficient in all cycling conditions: that means large fluctuations correspond to narrower filaments. V_{SET}, V_{RES} average values and dispersion coefficients are shown to increase during cycling: switching voltages on cells formed with large oscillations show lower average values and dispersion in all cycling conditions. This indicates cells with lower V_{SET}, V_{RES} have a not fully developed filament: this explains the large fluctuations. One

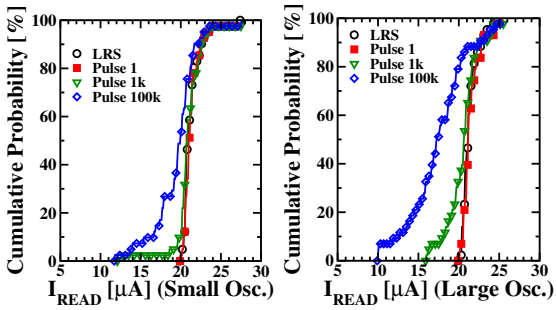

Fig. 7. Cumulative distributions of the read currents (with $V_{read} = 0.2V$) measured during reset stress on LRS after different number of disturb pulses, at endurance cycle 1 [11].

reason of the parameters dispersion could be the root mean square surface roughness of HfO_2 films due to the columnar structure of the TiN bottom metal electrode [13].

To evaluate the disturbs immunity of each cells group, 100k reset stress pulses have been applied after set with $V_{stress,res} = 0.8V$, $T_{stress,res} = 10\mu s$ and 100k set stress pulses after reset with $V_{stress,set} = 0.8V$,$T_{stress,set} = 10\mu s$ at different cycles. Set/reset stress voltage pulses with 0.8V have been used since it's almost half of the average set/reset switching voltage measured on fresh devices. Cumulative distributions of the read currents measured after reset (HRS), set (LRS) and during set and reset stress on fresh devices are reported in Fig. 6 and Fig. 7, respectively: in both cases cells formed with larger current oscillations show a lower disturb immunity. That reveals larger fluctuations indicate a not so well formed filament thus more prone to exhibit lower immunity.

All these findings summarize the importance of the forming operation in the lifetime of a RRAM array.

IV. Optimal SET/RESET Operation

The average set and reset characteristics in a RRAM array feature the same variability observed in forming [6], [14]. Moreover, as usually evidenced in RRAM technology [1], the read current I_{HRS} shows a larger range of variability compared to I_{LRS}, as evidenced in Fig. 8 showing the cumulative distributions of the set/reset switching voltages calculated on the entire array. These results indicate that an optimization of the set/reset operations is mandatory to reduce the impact of the device variability, whereas minimizing the array yield loss due to non-switching cells. To this purpose, the analysis in [15] compared DC and pulsed set/reset operations featuring different durations and voltages. A set of 10000 set/reset cycles has been considered for the analysis.

SET operation in DC mode has been performed increasing the bitline voltage V_{BL} from 0 to 3.5V with V_{step} = 0.1V ($T_{step,DC}$ = 50μs) and the wordline voltage fixed to V_{WL} = 1.4V. RESET operation in DC mode has been performed increasing the source line voltage V_{SL} from 0 to 3.5V, with V_{step} = 0.1V ($T_{step,DC}$ = 50μs) and V_{WL} = 2.5V. In pulsed mode operation the wordline voltage has been fixed to V_{WL}

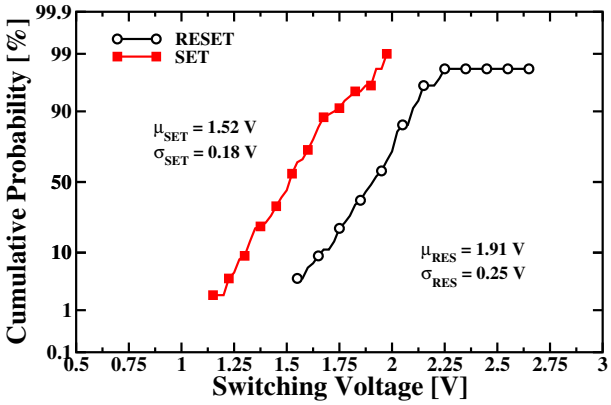

Fig. 8. Cumulative distribution of the set and reset switching voltages in the entire RRAM array [15].

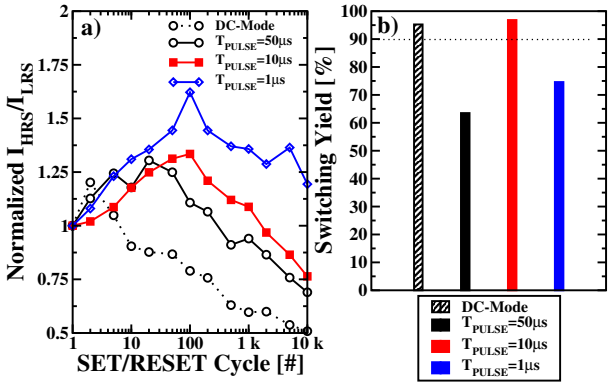

Fig. 9. Normalized read current Ratio (a) and Switching Yield (b) evaluation for different set/reset modes (DC and pulses with different durations) during cycling. V_{pulse} = 3V for pulsed modes [15].

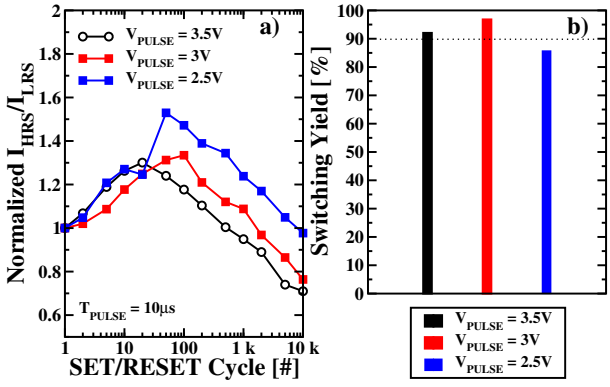

Fig. 10. Normalized read current Ratio (a) and Switching Yield (b) for different set/reset pulse amplitudes during cycling. T_{pulse} = 10μs [15].

= 1.4V during SET and V_{WL} = 2.8V during RESET, while different bitline/sourceline voltages and durations have been investigated.

In Fig. 9 a comparison between DC and pulsed mode with different durations at fixed V_{pulse} = 3V is depicted. Fig. 9a shows I_{HRS}/I_{LRS}, normalized with respect to that calculated at cycle 1, as a function of the set/reset cycle

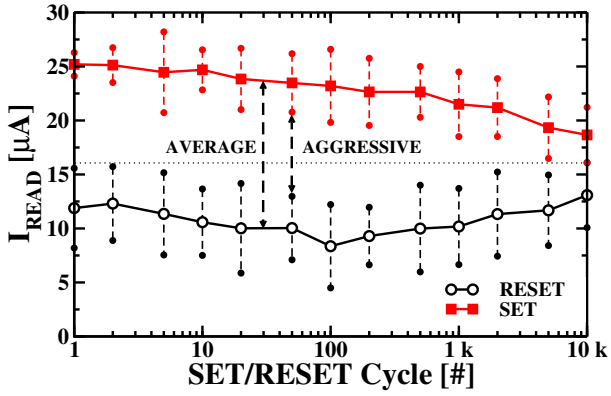

Fig. 11. Set and reset read current behavior during cycling with V_{pulse} = 3V, T_{pulse} = 10μs. Average and aggressive read window calculation points are indicated [15].

number for different pulse durations. In all cases a non-monotonic behavior is observed, eventually ending up with a significant I_{HRS}/I_{LRS} reduction with the exception of the shortest pulse duration (T_{pulse} = 1μs). Fig. 9b shows the switching yield (i.e., the percentage of cells in the array that actually toggles between set/reset states) of each set/reset mode providing an interesting trade-off: pulses with a too short or too long duration result in a lower yield compared to an average timing condition. Similar considerations can be derived by the analysis of Fig. 10, where the dependencies of the normalized I_{HRS}/I_{LRS} and that of the switching yield are evaluated in cycling for different pulse voltages considering the optimal pulse duration (T_{pulse} = 10μs).

From a physical point of view, this phenomenon can be explained as follows: while pulses with too low voltages or durations create too small filaments showing low current in set condition, too high voltages or durations create too big filaments hard to disrupt in the following reset operation. Both cases result in a lower yield compared to an average condition.

Starting from the best pulse conditions (T_{pulse} = 10μs, V_{pulse} = 3V) the read window closure has been analyzed as a function of set/reset cycling (see Fig. 11). Current reading has been performed at V_{WL} = 1.4V, $V_{BL,read}$ = 0.2V, T_{read} = 10μs. The average read current trend and the standard deviations are plotted for set and reset. It can be observed that the device variability of the cells in the array remains almost constant during cycling. Fig. 12 shows the read window ($I_{LRS} - I_{HRS}$) closure calculated using both the array average and aggressive (i.e., considering the worst-case condition) conditions. In this study, the endurance failure criterion is defined as the point where the aggressive read window case falls below 3μA [3], that is the limit for the sense amplifiers to discriminate between states. The read window show the same behavior for each pulse condition: an increase can be observed during the first cycles due to a variability reduction, followed by a closure after the degradation of the HfO_2 material stack. Short pulse durations and voltages result in a smaller read window due to a higher device variability caused

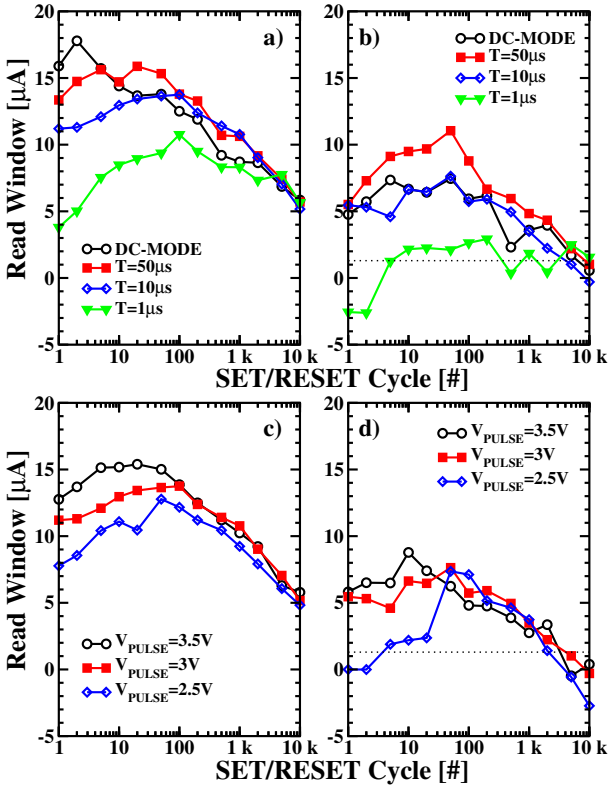

Fig. 12. Read Window trends in cycling. Average (left column) and aggressive (right column) measurements: a) and b) same conditions as Fig. 9 c) and d) same conditions as in Fig. 10. The limit for the set/reset discrimination is depicted at read window = $3\mu A$ [15].

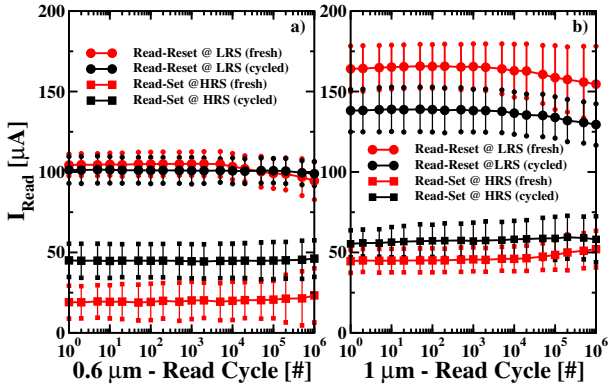

Fig. 13. $V_{dd}/2$ pulse stress effect measured on 0.6 μm^2 (a) and 1 μm^2 4kbit RRAM devices (b), in both set (LRS) and reset (HRS) condition.

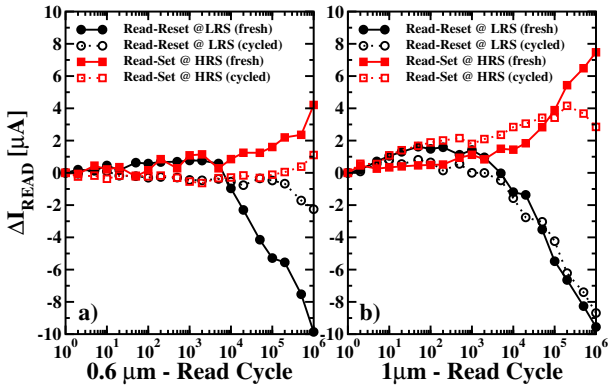

Fig. 14. Average read current variation measured during $V_{dd}/2$ pulse stress measured on 0.6 μm^2 (a) and 1 μm^2 4kbit RRAM devices (b).

by incomplete set/reset switching.

V. Read disturbs and instabilities

One major issue in RRAM technology is read instability [16]: consecutive reads on the same memory cell can yield widely fluctuating results, and/or cause permanent changes to the resistance itself. This behavior has been attributed to numerous physical mechanisms such as, random telegraph noise (RTN) due to capture and emission of trapped electrons [17], disturb due to the read electric field [18], diffusion of traps/vacancies [19], and retention/relaxation effects [20]. Conventionally, read instability has been measured on single-cell structures, with focus on specific physical mechanisms. An investigation of the disturb has been performed also using Costant Voltage Stress (CVS) on a large amount of samples, although the conditions used were not representative of a real array utilization [21].

On crossbar-based arrays, which is one of the potential array integration topologies offered by RRAM technology [3], [4], unselected WLs and BLs can be grounded or biased with a $V_{dd}/3$ or $V_{dd}/2$ scheme. In order to evaluate the impact on unselected WLs and BLs during set/reset opearation in the worst-case condition, the $V_{dd}/2$ biasing effect on reset and set wordlines has been evaluated on 0.6 μm^2 and 1 μm^2 RRAM arrays. 10^6 $V_{RESET}/2$ pulse have been applied on set wordlines, while 10^6 $V_{SET}/2$ pulse have been applied on reset wordlines where V_{RESET} and V_{SET} are the average reset and set switching voltages, respectively. The disturb effect has been evaluated on both fresh and cycled devices, after 10k set/reset pulse operations with V_{pulse} = 3 V, T_{pulse} = 10 μs. Fig. 13 shows the average set/reset read currents and their standard deviation measured during 10^6 stress pulse on 0.6 μm^2 (Fig. 13a) and 1 μm^2 (Fig. 13b) devices, for both fresh and cycled test chips. The dielectric material degradation in the MIM stack makes reset and set switching less effective, reducing the stress sensibility as well. The average current variation observed during stress is depicted in Fig. 14. The $V_{dd}/2$ stress caused a higher read current shift on fresh devices, for both 0.6 μm^2 and 1 μm^2 4kbits RRAM devices.

Ideally, considering device and circuit design margins, read resistance variation should be less than 10%. Error Correction Codes can also assist in recovery from less frequent, larger resistance fluctuations, but the occurrence of the resistance variation should be less than 1% for effective data integrity. The Read Error Rate, calculated as the fraction of cells showing a resistance variation higher than 10% during $V_{dd}/2$ stress is depicted in Fig. 15. Fresh devices show a higher error rate than cycled devices (after 10k set/reset cycles) for both 0.6 μm^2 and 1 μm^2 arrays. Although the average read current variation is higher in 1 μm^2 array, the error rate is lower with

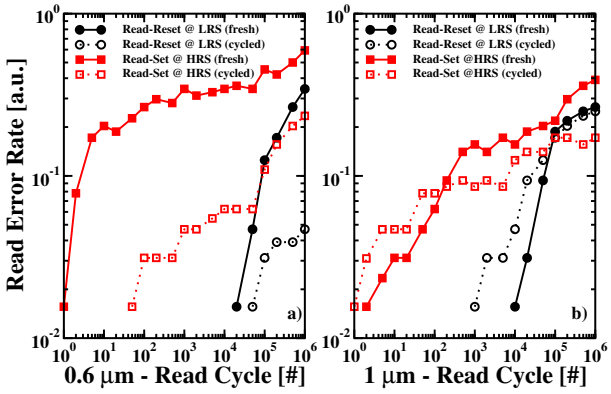

Fig. 15. Read Error Rate calculated on on 0.6 μm^2 (a) and 1 μm^2 4kbit RRAM devices (b). Full and dotted lines refers to fresh and cycled devices, respectively.

respect to that of 0.6 μm^2 devices because of a higher average set and reset currents that render the fluctuations less effective. Read disturb with set polarity stress on fresh devices in reset state is the operation that shows the highest read error rate for both 0.6 μm^2 (a) and 1 μm^2 (b) technologies, due to the conformation of the CF.

VI. Conclusions

In this review paper it was presented a detailed electrical characterization of different RRAM arrays manufactured in a compatible BiCMOS process. The analysis was entirely focused on the reliability and performance assessment of the integrated RRAM technology, through the depiction of the major issues retrieved during the characterization. Concerning the forming operation it was presented the relationship between this preliminary operation and the lifetime behavior of the array, by tackling also the typical cell-to-cell variability features. This activity lead to the search of the optimal set/reset parameters to improve the read window budget and the cycling features. Finally, the analysis of the read disturbs with their implications in advanced cross-bar architectures was evaluated showing that the integration of Error Correction Codes along with the RRAM memory is mandatory to guarantee the full data integrity.

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