Compact Modeling of Negative V_t Shift Disturb in NAND Flash memories

Cristian Zambelli, *Member, IEEE,* Fabio Andrian, Seiichi Aritome, *Fellow, IEEE,* and Piero Olivo

***Abstract*—The negative V_t shift disturb is one of the new scaling limiters for the NAND Flash technology, since it severely affects the reliability of ultra-scaled products, lowering the read margin between the distributions in multi-level cell architectures. However, even if the phenomenon was thoroughly investigated, it lacks a proper model to be exploited for the development of tailored management solutions. In this paper we have developed a compact model for the negative V_t shift disturb simulation in NAND Flash arrays. The model accurately reproduces experimental data retrieved on a 26 nm technology. The application of the model for fast and accurate statistical assessments of the reliability-loss induced by the disturb is shown through the execution of Monte Carlo simulations.**

***Index Terms*—NAND Flash memory, Reliability, Negative Vt shift, Anode Hole Injection, Simulation, Compact Models**

I. INTRODUCTION

The NAND Flash memories scaling down to the mid-1X-nm generation [1] massively relied on the Self-Aligned Shallow Trench Isolator (SA-STI) cell structure [2].

Although this is the state-of-the-art architectural solution to reduce the Floating Gate-Floating Gate (FG-FG) interference along the WordLine (WL) in NAND Flash arrays [3], the high electric field applied to the cells during both the program and the erase operation, may introduce some reliability and performance constraints on the NAND Flash system.

In fact, when a cell is inhibited from programming it can suffer a disturb attack from adjacent aggressor cells (i.e, cells to be programmed) either sharing the same BitLine (BL) or sharing the same WL. When the disturb is in the BL direction, the victim cell suffers only from the FG-FG interference, whereas when the disturb is on the WL direction the negative V_t disturb comes into play overlapped with the FG-FG interference. In fact, for technology nodes in the 2X-3X-nm range, it was observed a disturb phenomenon that produces a negative shift of the threshold voltage in the cells that share the same WL and that are inhibited during program (see Fig. 1) [4], [5]. The term ”negative” is used by [4], [5] to emphasize that those cells feature a threshold voltage shift that goes in the opposite direction compared to the shift produced by the mere FG-FG interference. This disturb significantly broadens the threshold voltage V_t distributions obtained after the application of the Incremental Step Pulse Programming (ISPP) algorithm [6], therefore limiting the read window margin of multi-level cell (MLC) and triple-level cell (TLC) architectures. Such a threat may add serious obstacles in the future development of the V_t placement algorithms for further scaled technology nodes [7], leading to severe optimizations required at system level to guarantee an acceptable inherent reliability [8], [9].

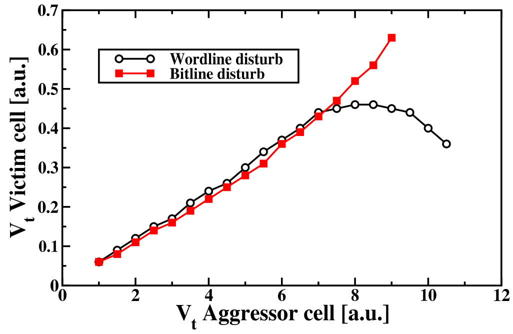

Fig. 1. Evidence of the negative V_t shift disturb in the WL direction retrieved on a 26 nm NAND Flash technology [5].

In [5] it was presented a detailed experimental characterization of the phenomenon and a first glance explanation of its occurrence in NAND Flash. However, an accurate model suitable for technology predictions, design optimizations of memory arrays, and reliability evaluations is still missing. Within this scenario, the compact modeling approach [10]–[13] should be favored with respect to the *Technology Computer Aided Design* approach, especially if statistical considerations need to be drawn in a time-efficient way from large Monte Carlo simulations.

In this paper we present a compact model of the negative V_t shift disturb that accurately takes into account the physical mechanisms involved in its insurgence on scaled NAND Flash architectures. Its implementation was embedded into the PSP model [14] using Verilog-A to be exploited in conjunction with a SPICE simulation program. Its validation was provided by reproducing a large set of experiments performed on a 26 nm MLC NAND Flash technology [15] that considers different structures of the SA-STI cell and different bias sequence configurations applied to the cells during the program and inhibit operations. The simulation results show a good agreement with the experimental data by capturing also the cell-to-cell variability effects in the disturb through Monte Carlo simulations.

II. NAND FLASH CELL COMPACT MODEL

In the SA-STI cell, as shown in Fig. 2a, the cells' floating gate (FG) is patterned with the STI to avoid the overlap with the insulator edge corners. Then the sidewall of the FG is used to increase the cells' coupling ratio, with respect to planar structures, thanks to the larger capacitance between the FG

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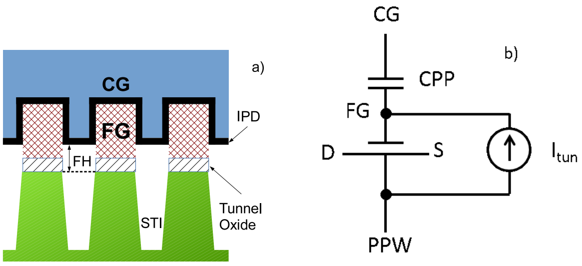

Fig. 2. Cross-section along WL direction of a NAND Flash where three SA-STI cells are depicted (a) and the correspondent SA-STI cell compact model (b).

and the control gate (CG). Moreover, the field height (FH), that is calculated as the distance between the cells' active area (AA) where tunneling takes place and the interpoly dielectric (IPD) (i.e., the top of the STI in this case), is reduced to additionally increase the coupling ratio.

Its compact model description (Fig. 2b) consists in a metal-oxide-semiconductor (MOS) transistor whose gate terminal, representing the cell's FG, is connected in series with the IPD capacitor C_{PP} [16]. The physical parameters of the cell such as the channel length (L), width (W), and tunnel oxide (t_{tun}) are those retrived from a 26 nm SA-STI cell technology [15] and are fed into the PSP model. The IPD ($SiO_2/Si_3N_4/SiO_2$) thickness is around 12 nm and the considered FH ranges from 10 nm (i.e., small FH) to 20 nm (i.e., large FH). The C_{PP} is calculated in the cell compact model as:

$$C_{PP} = \frac{\epsilon_{ox} \cdot A}{EOT_{IPD}} \tag{1}$$

where $EOT_{IPD} = t_{ox1}+(t_n*\epsilon_{ox}/\epsilon_n)+t_{ox2}$ is the equivalent oxide thickness of the IPD, being ϵ_n the Si_3N_4 dielectric constant, ϵ_{ox} the SiO_2 dielectric constant, and t_{ox1}, t_n, t_{ox2} the first SiO_2, the Si_3N_4, and the second SiO_2 layer thicknesses in the IPD, respectively. The term A is the effective C_{PP} area calculated with the trapezoidal shape approximation of the FG [10] as:

$$\begin{aligned} A = \Bigg[& W - 2t_{FG}\cot\theta \\ & +2\left(\frac{t_{FG}-FH}{\sin\theta}\right) + 2\left(t_{ox1}+t_n+t_{ox2}\right)\Bigg]L \end{aligned} \tag{2}$$

where t_{FG} is the FG thickness and θ is the oblique angle of the FG.

The programming of a memory cell through the Fowler-Nordheim (FN) tunneling mechanism is simulated by the current source I_{tun} connected between the FG and the pocket p-bias well (PPW) terminal shared by all the array elements. The equation governing I_{tun} in the PSP model is:

$$I_{tun} = AA \cdot \alpha_1 \cdot F_{tun}^2 \cdot exp\left(-\frac{4}{3\hbar} \cdot \sqrt{2qm_{ox}} \cdot \frac{\phi_b^{3/2}}{F_{tun}}\right) \tag{3}$$

where α_1 is a fitting constant to calibrate the tunneling efficiency from the experimental data, m_{ox} is the electron effective mass in the tunnel oxide assumed equal to 0.4, and ϕ_b is the Si/SiO_2 interface potential barrier at the electrons injection point assumed equal to 3.1 eV. The electric field across the oxide (F_{tun}) has been calculated as $F_{tun} = (V_{FG} - V_{FB} - V_t - V_{boosting})/t_{tun}$, where V_{FG} is the cell's FG bias during programming operation, V_{FB} is the flat band voltage, V_t is the cell's threshold voltage and $V_{boosting}$ is the voltage generated in the self-boosting program/inhibit scheme to selectively isolate a memory cell from programming [6]. For simplicity $V_{boosting}$ has been included as an input node in the PSP model to enable/disable the tunneling by applying a fixed voltage.

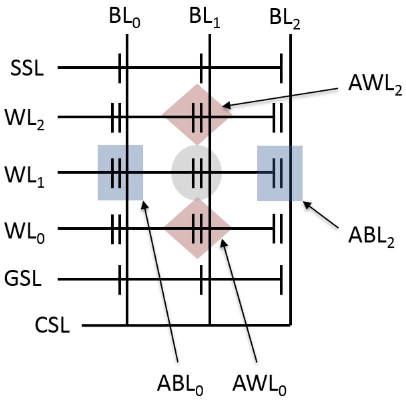

Fig. 3. NAND Flash array model considered for negative V_t shift disturb simulations. The victim cell is highlighted in the circle whereas aggressor cells on the WL and BL directions are in the rectangles (ABL0 and ABL2) and diamonds (AWL0 and AWL2), respectively.

The following equations model the cell's V_t variation as a function of the charge injected in the FG by I_{tun} as well as the saturation of the programming characteristics due to the CG current [17]:

$$\begin{aligned} Q_{FG} &= C_{PP} * (V_{FG} - V_{CG} - V_{FB,CG-FG}) \\ &= Q_{FG0} + \int I_{tun} - \int I_{CG} \end{aligned} \tag{4}$$

$$V_t = V_{t0} - \frac{Q_{FG}}{C_{PP}} \tag{5}$$

where eq. (4) is the charge neutrality equation that takes into account the initial charge set into FG as $Q_{FG,0}$, as well as the flat-band voltage between CG and FG indicated as $V_{FB,CG-FG}$ and eq. (5) calculates the cell's V_t starting from the initial voltage V_{t0} and the FG's charge content. The Q_{FG0} and V_{t0} terms have been introduced to put a cell into a defined starting voltage state.

III. NAND FLASH ARRAY COMPACT MODEL

The state-of-the-art compact models for NAND Flash array simulations successfully deal either with physical phenomena affecting the cell-to-cell variability [10] or with string-based analysis of the electrostatic conditions leading to the cell-to-cell interference [11], [12]. However, the development of a

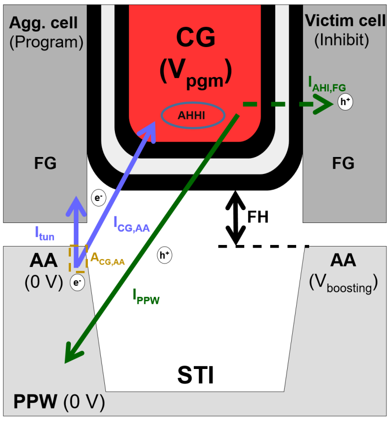

Fig. 4. Current sources and electron/hole flows during a program operation considering an aggressor and a victim cell along WL_1.

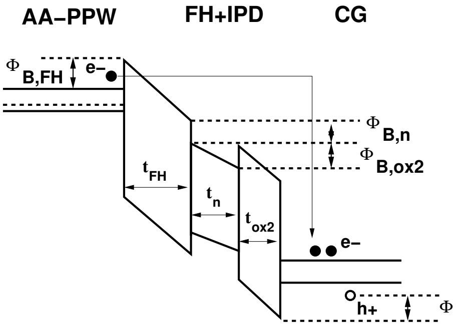

Fig. 5. Band diagram of the AA-PPW/FH+IPD/CG cross-section in the cells structure depicted in Fig.4.

model of negative V_t shift disturb requires both a wordline-based simulation and a precise physical model of the electron flows in bitline-adjacent memory cells that is currently missing in other models.

Fig. 3 shows the array considered in this work. To improve the computation speed it is exploited a 3×3 matrix of Flash cells connected to the bitlines and to the common source line (CSL) through the string select line (SSL) and the ground select line transistors (GSL), according to the interconnections indicated in the figure. The wordline to be analyzed in the simulations is WL_1, whereas the other wordlines are identical to the considered one and only set the boundary conditions for the cell-to-cell interference. The FG-FG interferences along the WL and the BL directions have been modeled in the array SPICE model including parasitic capacitors connected between the FG of a cell and its neighbour FGs. The capacitance values have been extracted from 3D TCAD simulations following the guidelines provided in [18].

IV. CURRENT SOURCES INVOLVED DURING WL PROGRAMMING

To clarify the sources of the negative V_t shift disturb it is mandatory to understand the currents involved during the program operation performed along a WL.

By considering the aggressor/victim configuration represented in Fig. 4, where either ABL0 or ABL2 is the aggressor on the inhibited BL1-WL1 cell, there is a common V_{pgm} bias applied on both cells' CG. Since the aggressor is not inhibited its AA potential is equal to 0 V and therefore the effective F_{tun} across the tunnel oxide allows the electron tunneling to the FG with a current I_{tun} calculated as in eq. (3). At the same time, due to the SA-STI cell geometry, the CG voltage generates a significant electric field crowding on the STI corner of the aggressor cell by exerting a direct control of its AA current distribution [19]. This translates into a current, indicated as $I_{CG,AA}$, that can be calculated with the analytical formula in eq.(15) derived for IPD multi-layer barriers (see Fig. 5) [20]. In such equation α_2 is a fitting constant, m_n is the electron's effective mass in Si_3N_4 assumed equal to 0.3, $\phi_{B,FH}$ and $\phi_{B,ox2}$ are the potential barriers of the first and the last IPD layers assumed equal to 3.1 eV and 2.9 eV, $\phi_{B,n}$ is the potential barrier of the middle IPD layer assumed equal to 2.2 eV, t_{FH} is sum of the FH and the thickness of the first IPD layer, respectively. The term $A_{CG,AA}$ in eq.(15) is the fraction of the active area in a SA-STI NAND cell that is sensible to the CG direct electrostatic control and is calculated as $A_{CG,AA} = k \cdot W \cdot L$, where k is a percentage value between 20% and 25% when a 26nm NAND Flash technology is considered [10]. The relationship of the electric fields in the IPD layers is derived from Gauss's law as:

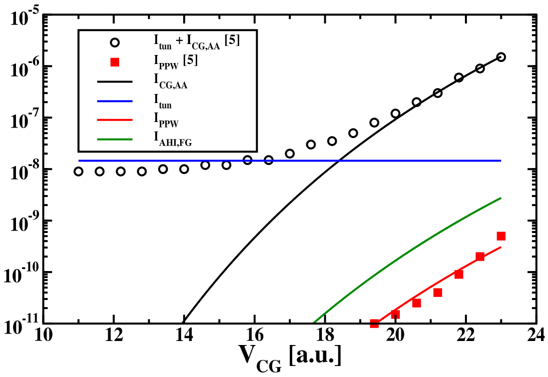

Fig. 6. Experimental (symbols) and simulated (lines) currents as a function of the CG voltage applied to the cells structure depicted in Fig.4.

$$
\begin{aligned}
F_{FH} &= \frac{V_{CG} - (\phi_{CG} - \phi_{PPW})}{(EOT_{IPD} + FH)} \\
&\approx \frac{V_{CG}}{(EOT_{IPD} + FH)} = \frac{\epsilon_n}{\epsilon_{ox}} \cdot F_n \qquad (6)
\end{aligned}
$$

where $(\phi_{CG} - \phi_{PPW})$ is the difference in the CG and PPW work functions.

The inhibition of the victim cell by the self-boosting scheme (i.e., AA potential equal to $V_{boosting}$) blocks that current flow. Charge trapping into IPD and Trap-Assisted-Tunneling currents are not considered for sake of simplicity [21]. The $I_{CG,AA}$ generates an additional current in the aggressor cell region due to the Anode Hole Injection (AHI) phenomenon [22], [23] that can flows either through the STI back to the PPW or through the IPD in the victim cell region directly toward its FG [5]. This is a hole current that can be expressed as:

$$I_{AHI} = I_{PPW} + I_{AHI,FG} \tag{7}$$

where I_{PPW} is the portion of the AHI current flowing back to the PPW and $I_{AHI,FG}$ is the portion of the AHI current flowing to the victim cell FG. These currents can be calculated as:

$$I_{PPW} = I_{CG,AA} \cdot \gamma \cdot \theta_{PPW} \tag{8}$$

$$I_{AHI,FG} = I_{CG,AA} \cdot \gamma \cdot \theta_{AHI,FG} \tag{9}$$

where γ is the quantum yield for the AHI process [24], θ_{PPW} is the holes' transmission probability through the CG-IPD-FH-PPW region, and $\theta_{AHI,FG}$ is the holes' transmission probability through the CG-IPD-victim cell FG region. The transmission probabilities have been calculated according to these equations:

$$\begin{aligned}\theta_{PPW} = {} & exp^{-\frac{4}{3}\sqrt{\frac{2m_{p,ox}}{\hbar}}\frac{\phi_{Bh,FH}^{3/2}-\left(\phi_{Bh,FH}-qF_{FH}t_{ox1}\right)^{3/2}}{qF_{FH}}} \\ & \times exp^{-\frac{4}{3}\sqrt{\frac{2m_{p,n}}{\hbar}}\frac{\left(\phi_{Bh,n}-qF_{FH}t_{ox1}\right)^{3/2}}{qF_{n}}} \\ & \times exp^{-\frac{4}{3}\sqrt{\frac{2m_{p,ox}}{\hbar}}\frac{\left(\phi_{Bh,ox2+FH}-qF_{FH}t_{ox,1}-qF_{n}t_{n}\right)^{3/2}}{qF_{FH}}}\end{aligned} \tag{10}$$

$$\begin{aligned}\theta_{AHI,FG} = {} & exp^{-\frac{4}{3}\sqrt{\frac{2m_{p,ox}}{\hbar}}\frac{\phi_{Bh,FH}^{3/2}-\left(\phi_{Bh,FH}-qF_{IPD}t_{ox1}\right)^{3/2}}{qF_{IPD}}} \\ & \times exp^{-\frac{4}{3}\sqrt{\frac{2m_{p,n}}{\hbar}}\frac{\left(\phi_{Bh,n}-qF_{IPD}t_{ox1}\right)^{3/2}}{qF_{n}}} \\ & \times exp^{-\frac{4}{3}\sqrt{\frac{2m_{p,ox}}{\hbar}}\frac{\left(\phi_{Bh,ox2}-qF_{IPD}t_{ox,1}-qF_{n}t_{n}\right)^{3/2}}{qF_{IPD}}}\end{aligned} \tag{11}$$

where $m_{p,ox}$ is the hole effective mass in the SiO_2 assumed equal to 0.75 for the first IPD layer and 0.2 for the last IPD layer, $m_{p,n}$ is the hole effective mass in the Si_3N_4 assumed equal to 0.2 and $\phi_{Bh,FH}$ is the potential barrier of holes calculated as in [23]. The electric field F_{IPD} is considered approximately equal to $F_{IPD} = V_{CG} - V_{FG,victim}/EOT_{IPD}$, whereas F_{FH} can be calculated as in eq.(6). Once again, the relationship of the electric fields in the IPD layers is derived from Gauss's law. For the range of V_{CG} applied in this work it is found that $\theta_{PPW} < \theta_{AHI,FG}$. In this case eq.(7) can be approximated as:

$$\begin{aligned}I_{AHI} & = I_{PPW} + I_{AHI,FG} \approx I_{AHI,FG} \\ & = I_{CG,AA} \cdot \gamma \cdot exp\left(-\frac{8\pi\sqrt{2m_{p,ox}}/3hq}{F_{IPD}}\phi_p^{3/2}\right)\end{aligned} \tag{12}$$

Eq. (12) is generally valid for IPDs until the electric field applied across the materials stack guarantees the generation of hot holes (i.e., hole energies in the 5-6 eV range) [25].

Fig. 6 shows the simulation of the different current contributors compared with the experimental results obtained through charge carrier separation experiments performed on large cell-structured capacitors [4]. In those experiments the V_{FG} was kept constant to allow the calibration of the model behavior when the V_{CG} is varied, therefore the I_{tun} contribution was constant.

The $I_{AHI,FG}$ is the only contribution to lower the victim cell's V_t, that is calculated in the model as:

$$Q_{victim} = \int I_{AHI,FG} \tag{13}$$

$$V_{t,victim} = V_{t0,victim} + \Delta V_{t,FG} + \frac{Q_{FG0,victim} - Q_{victim}}{C_{PP}} \tag{14}$$

where $V_{t0,victim}$ and $Q_{FG0,victim}$ are the terms introduced to put the victim cell into a defined starting voltage state, and $\Delta V_{t,FG}$ is the victim cell threshold voltage variation due to the FG-FG interference.

V. NEGATIVE V_t SHIFT DISTURB SIMULATION RESULTS

The first concern to address in the simulation of the negative V_t shift disturb is its dependency on FH. Fig. 7 shows the simulation of two aggressor cells (i.e., ABL0 and ABL2) and of a victim cell (i.e., ABL1) during the application of the ISPP algorithm on WL1 using a programming voltage V_{pgm} from 10.5 to 17 in 0.5 steps. The aggressors were assumed to be in the erased state (although experimental measurements are shown from $V_t > 0$), whereas the victim is assumed to be at a $V_{t,victim} = 1$. The aggressor cells V_t ISPP transient is captured by the model, indicating the ability to describe the behavior of an average cell by only applying Eqs. (1)-(5). Two different behaviors of the victim cell $\Delta V_{t,victim}$ are evidenced and accurately simulated by the model, in relationship with the considered FH for a 26 nm NAND Flash technology. In the experiments performed on the 26nm NAND Flash array test vehicle the ISPP operation on the aggressor cells started from an erased state (i.e., $V_t < 0$). Since it was not possible to measure the V_t of NAND Flash cells in the erased state, the aggressor cells programming characteristics are shown only when $V_t > 0$. However, the FG-FG interference with the victim cell is present already in the first steps of the ISPP algorithm (i.e., $V_{pgm} < 10.5$). This translates into a residual interference measured in both small and large FH cells equal to 0.2. In small FH SA-STI cell structures the FG-FG interference is lower with respect to the large FH case due to the increased shielding effect of the CG between ABL0/ABL2 and ABL1 FGs. However, the generation of the $I_{CG,AA}$ current is favored in the former case due to a reduced IPD/FH tunneling barrier and therefore I_{AHI} and, consequently, $I_{AHI,FG}$ increase.

An additional consideration can be derived in terms of the negative V_t shift disturb dependency on the programming voltage applied to the aggressors. In the actual page program sequence of a MLC NAND system with ISPP and bit-by-bit verify operation [6], the aggressor cell V_t can be placed in three different states. Dependently on the chosen target V_t, a different number of V_{pgm} pulses are applied to the aggressors before the self-boosting inhibit operation takes place [2]. If the aggressors require low V_{pgm} values to reach the target the victim cell $V_{t,victim}$ shifts only because of the FG-FG interference, since during the inhibit operation there is no

$$
\begin{aligned}
I_{CG,AA} &= A_{CG,AA} \cdot \alpha_2 \cdot F_{FH}^2 \\
&\times \left(\phi_{B,FH}^{1/2} - \left(\phi_{B,FH} - qF_{FH}t_{FH}\right)^{1/2} + \frac{\epsilon_n}{\epsilon_{ox}}\sqrt{\frac{m_n}{m_{ox}}}\left(\phi_{B,n} - qF_{FH}t_{FH}\right)^{1/2} + \left(\phi_{B,ox2} - qF_{FH}t_{FH} - qF_n t_n\right)^{1/2} \right)^{-2} \\
&\times exp\left[- \frac{8\pi\sqrt{2m_{ox}}}{3hqF_{FH}} \left(\phi_{B,FH}^{3/2} - \left(\phi_{B,FH} - qF_{FH}t_{FH}\right)^{3/2} + \frac{\epsilon_n}{\epsilon_{ox}}\sqrt{\frac{m_n}{m_{ox}}}\left(\phi_{B,n} - qF_{FH}t_{FH}\right)^{3/2} \right.\right. \\
&\qquad \left.\left. + \left(\phi_{B,ox2} - qF_{FH}t_{FH} - qF_n t_n\right)^{3/2} \right) \right] \qquad (15)
\end{aligned}
$$

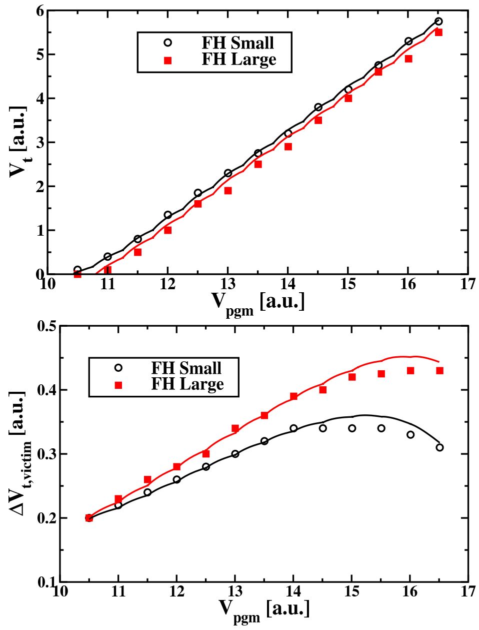

Fig. 7. FH dependency of the V_t in the aggressor cells during programming transient (top) and of the $\Delta V_{t,victim}$ (bottom). Model results (lines) are shown along with experimental data [4] (symbols).

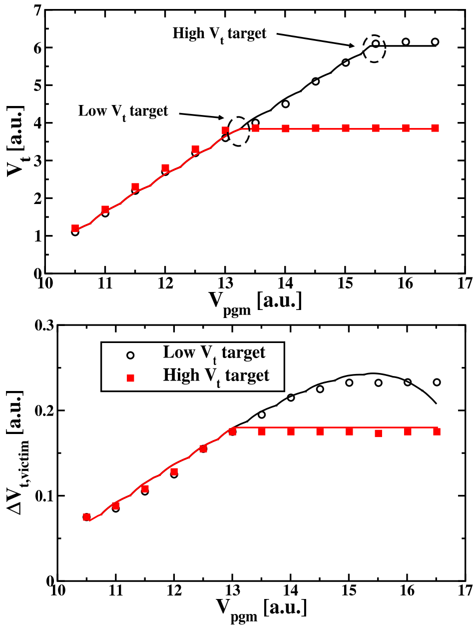

Fig. 8. Aggressor cells V_t transient during ISPP when inhibit is either at low V_t or high V_t target (top) and resulting $\Delta V_{t,victim}$ shift (bottom). Small FH cell structure is considered. Model results (lines) are shown along with experimental data retrieved from large cell-structured capacitors [4] (symbols).

generation of the I_{AHI} current being the AA potential in the aggressors equal to $V_{boosting}$. On the contrary, if high V_{pgm} values are required by the aggressors, the negative V_t shift becomes visible, and the victim cell V_t starts to decrease. Fig. 8 shows the simulation of two different programming targets for the aggressors and their effect on the victim cell.

The negative V_t shift disturb depends also on the programming speed of the aggressors. Given that, it is important to quantify this factor to be exploitable in Monte Carlo simulations that deal with the variability effects in NAND Flash arrays [10]. The largest disturb is appreciable when the aggressor cells are slow to program, as shown in Fig. 9. The reason is due to the larger number of program pulses applied on WL1 during the ISPP, that will subject the aggressors under the non-inhibited condition for longer, thus enhancing the generation of hot holes potentially flowing toward the victim cell's FG. The developed compact model allows reproducing the different programming speed features of the aggressor cells by fitting the experimental data using the geometrical parameters (e.g., t_{tun}, W, L, etc.) of the aggressors and the fitting constant α_1 in the Eq. (3). Once the right parameters are found the geometrical characteristics of the victim cell are kept constant to show the sole impact of the aggressors. The simulation were performed using HSPICE with a CPU time required for the simulations of about three seconds per 3 × 3 NAND Flash array configuration.

VI. RELIABILITY-LOSS ASSESSMENT OF THE DISTURB

A possible application of the proposed compact model is the evaluation of the disturb impact on the reliability of a NAND Flash memory. The case study concerns the estimation of the victim cell V_t distribution broadening due to the negative V_t shift disturb induced by different aggressor programming patterns. Such an activity is useful for system designers to evaluate either new V_t placement algorithms or customized error-correction codes strategies.

The experimental victim cell ΔV_t distributions, measured as the difference between the victim cell V_t before and after the disturb, are retrieved from a 16kbits cells page of a 26 nm MLC NAND Flash test chip programmed with the three following patterns: *i)* ABL0 and ABL2 programmed to a high V_t; *ii)* ABL0 programmed to a high V_t and ABL2 is erased (i.e., $V_t < 0$); *iii)* ABL0 and ABL2 programmed to low V_t. The

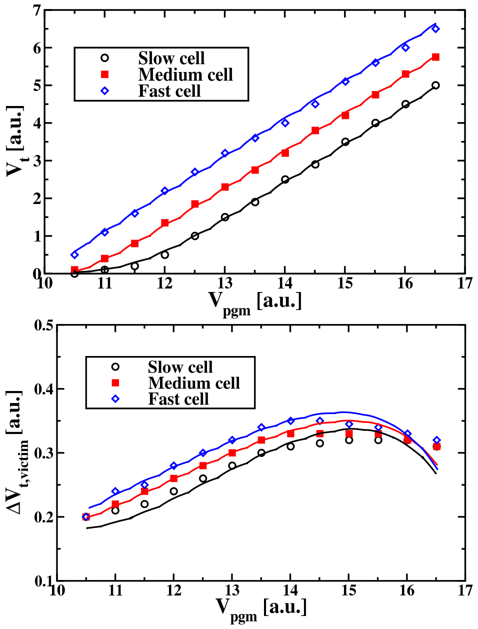

Fig. 9. Speed dependency of the V_t in the aggressor cells during programming transient (top) and of the $\Delta V_{t,victim}$ (bottom). Small FH cell structure and high V_t target for the aggressors are considered. Model results (lines) are shown along with experimental data [4] (symbols).

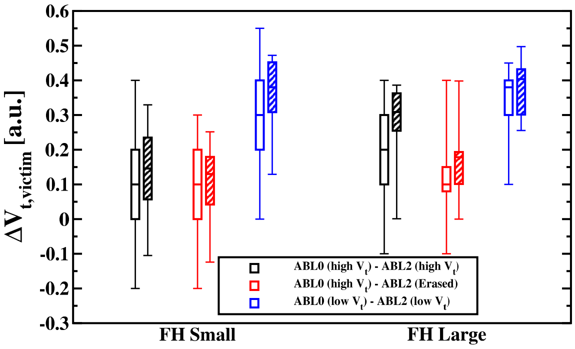

Fig. 10. Boxplot of the experimental [4] (empty pattern) and the simulated (diagonal pattern) $\Delta V_{t,victim}$ distributions representing the median, first and third quartiles, and outliers retrieved for 16 kbits cells.

TABLE I
VARIABILITY COEFFICIENTS USED IN ΔV_t SIMULATIONS

Parameter	σ
$W, L[nm]$	0.1
$t_{tun}[nm]$	0.1
$t_{IPD}[nm]$	0.1
$FH[nm]$	0.5
$Q_{FG0,victim}[aC]$	25
$Q_{FG0}[aC]$	15
$V_{t0}[V]$	0.1
$V_{t0,victim}[V]$	0.1

same programming patterns were simulated with the proposed compact model through a Monte Carlo approach, in which both the aggressor and the victim cells geometrical parameters were varied by following a Gaussian distribution. Table I resumes the parameters and their variability coefficients (i.e., distribution σ) used in the simulations.

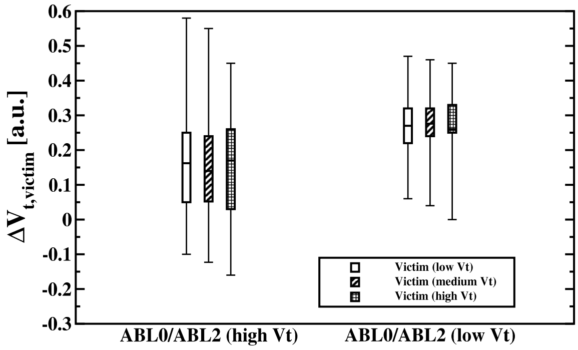

Fig. 11. Boxplot of the simulated $\Delta V_{t,victim}$ distributions considering different victim cell programming state. Simulations are performed on small FH cell structure and are retrieved for 16 kbits cells.

As shown in Fig. 10, when ABL0/ABL2 aggressors are programmed to low V_t the $\Delta V_{t,victim}$ is mainly impacted by the FG-FG interference. When ABL0/ABL2 are programmed to a high V_t the victim cell starts to suffer from the negative V_t shift disturb, that broadens the victim cell V_t distribution dependently on the number of aggressors (one or two). Different FH have been considered in the analysis to increase the consistency of the results. In the case of ABL0/ABL2 programming at lower V_t starting from the erased V_t distribution, the victim cells will suffer only from FG-FG interference. The slower aggressor cells cause the larger victim cell ΔV_t because they will receive a higher number of ISPP pulses in order to reach the target V_t, as shown by experimental data in Fig. 9. On the other hand, when ABL0/ABL2 are programmed to a high V_t, they start programming from a V_t level higher than the erased one as done in MLC NAND Flash programming algorithms [26]. In this case the victim cell ΔV_t becomes smaller for slow aggressor cells [4], [5]. This means that the negative V_t shift in victim cells is much larger in the case of slow aggressor cells. This is ascribed to the fact that the inhibit condition of the victim cells is maintained for longer time since a higher number of ISPP pulses needs to be supplied to the aggressor cells to reach the target V_t.

Simulation results considering different victim cell's V_t are provided in Fig. 11, reflecting the general experimental trends provided in [5]. As retrieved by experimental results in [5], it is evidenced that when the victim cell is programmed to a high V_t state the corresponding negative V_t shift is slightly higher than what retrieved when victim cell is programmed to a low V_t state. This is ascribed to the fact that when the victim cell is programmed to high V_t values, its FG is negatively charged, then it could gather more positive charge generated by AHI during the aggressor cells programming. This feature has been implemented in the model by changing the γ coefficient of eq.(12) in a range between 0.1 and 0.5. For high γ values (between 0.45 and 0.5) it is possible to model the victim cell V_t in a high V_t state, therefore with a FG strongly negative charged with greater capability to attract holes. On the contrary, for low γ values (between 0.1 and 0.2) it is possible to simulate the victim cell in a low V_t state and therefore with a FG exhibiting a lower capability to attract holes.

The Monte Carlo simulations generally confirm the trends expected by literature data like [5] and [4]. The discrepancies retrieved are mainly ascribed to the absence of two components in the NAND Flash array model: the cell-to-cell interference due to direct channel coupling that dominates in sub-30 nm NAND Flash technologies [11], and the back-tunneling current (i.e., current flows from aggressor cell FG to CG) during aggressor cells programming with consequent carrier trapping into IPD [5]. Both components can be added to the present model by simply including their equations. However, the computation speed will be largely affected especially by the inclusion of the latter contributor and most of the time it is required to extract many different geometrical parameters from the NAND Flash cells that are not directly available. Furthermore, the choice of excluding their contribution is related to the range of V_{pgm} used by the experimental data provided in [5], that most of the time are not sufficient to trigger both phenomena. By considering this model corner it is possible to still achieve a minimum accuracy up to 80%, which can be acceptable for a NAND Flash compact model compared to previous works [11], [12], [18].

VII. CONCLUSION

In this paper, a compact model for the simulation of the negative V_t shift disturb in NAND Flash memory arrays has been presented. The model accurately reproduces the disturb behavior under different experimental scenarios retrieved on a 26 nm MLC NAND Flash technology. The equations describing the physics underlying the disturb phenomenon have been included in the PSP model using Verilog-A, allowing a good degree of model parameterizations and flexibility for future applications like simulations and optimizations of large arrays. The model is able to assess, through Monte Carlo simulations performed using HSPICE, the impact of the disturb on the read window margin of a MLC technology.

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