Characterization of the Over-Erase Algorithm in FN/FN embedded NOR Flash arrays

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***Abstract*—The over-erase algorithm is the state of the art procedure exploited in NOR Flash architectures to increase the memory reliability against the over-erase phenomenon mainly caused by either fast or erratic bits. In FN/FN architectures, since the soft-programming operation involved in the algorithm uses the same physical mechanism of the erase operation, its execution potentially triggers additional failures. In this paper, a detailed characterization of the soft-programming failures is provided by categorizing their statistical occurrence in order to capture their relationship with the failures exposed after the execution of the algorithm. A model of the failure rate is then derived to provide a rough guideline for over-erase algorithm optimization in terms of performance and reliability.**

***Index Terms*—Over-erase algorithm, flash memories, fn/fn, soft-programming, reliability**

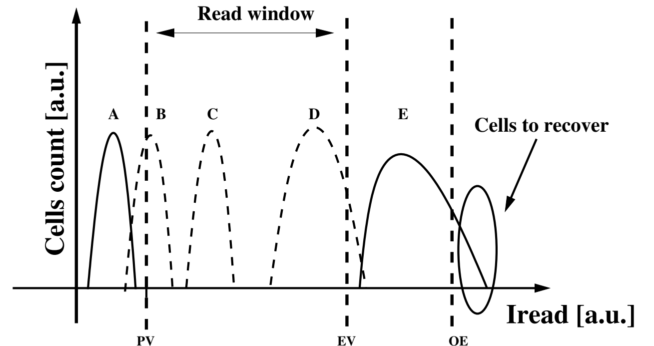

Fig. 1. Evolution of the I_{read} distributions during an erase operation from distribution A to distribution E. At the end of the operation, some cells display a current higher than the OE level.

I. Introduction

Embedded Flash memories integrated in microcontrollers for automotive applications belong to safety-critical environments where reliability represents a major concern. The most common array architecture exploited in those components is the NOR Flash, thanks to its low read access latency and a relatively long endurance of the storage medium [1]. Among the several technology variants that can be integrated [2], the Fully Fowler-Nordheim (FN/FN) concept stands out due to its lower energy consumption required in the programming operation and a relative ease of integration for large density products [3], [4].

From the reliability viewpoint, the erase operation has always been an issue for every NOR technology so far [5], and special emphasis has been put on the reduction of the standard erase failure mechanisms by implementing proper correction algorithms aiming at a memory fail rate reduction below 1 ppm [6], [7]. In the majority of the NOR Flash products an Over-Erase Algorithm (OEA) is exploited to recover fast erase bits or erratic bits [2], [8]. If during an erase operation relying on the Fowler-Nordheim (FN) tunneling mechanism a cell goes into a depletion state (i.e., assuming a negative threshold voltage) or below a threshold voltage reference level caused by an anomalous tunneling behavior [9], [10], a time consuming recovery procedure is applied by soft-programming the cell towards a specified verify level [2].

However, since the cell concept relies on the FN mechanism both for the program and the erase operation, all the reliability concerns regarding the latter applies as well as for the soft-programming operation involved in the OEA, which in turn could trigger a new failure rather than recovering a previous one. This consideration becomes important in the design stage of the optimal OEA scheme and consequently on the proper Error Correction Codes (ECC) and redundancy strategies to cope with this issue [11].

In this paper it will be shown, through a detailed experimental characterization of 1T-NOR FN/FN-based Flash cells, the physical classification of the potential soft-programming reliability threats and their impact on the inherent reliability offered by the OEA. It is also derived a failure rate model applied in an automotive scenario that shows the benefits of using OEA schemes that trade their reliability with performance yet guaranteeing the failure rate requests of such applications.

II. Erase and over-erase algorithms

The erase algorithm in NOR Flash usually performs as follows: starting from a program condition where all the cell currents of a sector are below a Program Verify (PV) level (distribution A in Fig. 1), a set of erase pulses is applied to all the cells until their currents are above an Erase Verify (EV) level (distribution E in Fig. 1).

However, some of the erased cells may reach the EV level faster than the other cells in the array sector (distribution D in Fig. 1). Therefore every further erase pulse applied to those cells drives their currents into an Over-Erased (OE) condition, which is considered critical for the reliability since a single cell on a bitline that is over-erased causes the complete bitline failure in 1T-NOR architectures [10] and unwanted current consumption in 2T-NOR architectures [12].

The goal of the recovery algorithm is to selectively soft-program the cells whose read current I_{read} is above the OE

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This work has been partially funded by the Bando Giovani Ricercatori from Universitá degli studi di Ferrara (Italy) 5xmille 2009 contribution.

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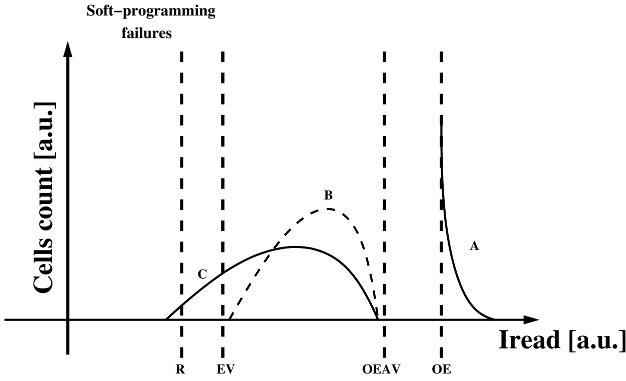

Fig. 2. Example of the evolution of the I_{read} distributions for the cells to be recovered (distribution A) with the OEA. The distribution B represents the target final distribution, whereas distribution C evidences the potential presence of cells that crosses the EV or even the R level.

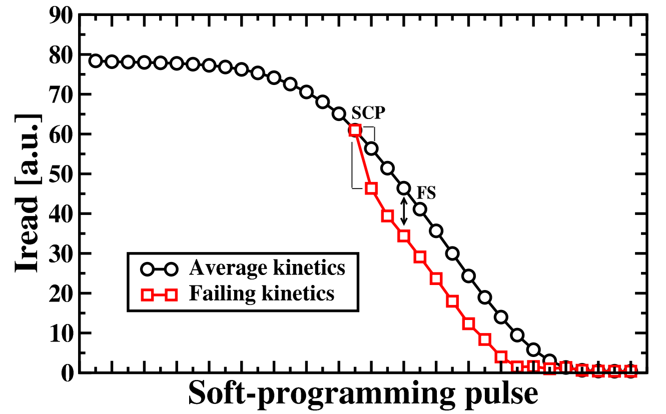

Fig. 3. Example of the average (circles) soft-programming kinetics retrieved during the characterization. An example of the deviation from the average kinetics (squares) is provided to indicate the classification parameters SCP and FS.

level (distribution A in Fig. 2) in order to drive their currents between a verify level denoted as $OEAV$ and the EV level (distribution B in Fig. 2). However, since in the FN/FN concept the soft-programming operation uses the same physical mechanism of the erase operation, it is possible to observe some cells whose read current suddenly crosses, during soft-programming, the EV level or even the discrimination level to distinguish between a programmed and an erased distribution indicated as R (distribution C in Fig. 2). Although the former effect seems to not directly produce a visible failure, it becomes not tolerable in Confidence Level Tests (CLT) [7] because it represents an unwanted read window budget reduction that limits the memory robustness against wear- and retention-induced failures. The latter case, on the contrary, produces an immediate failure evidence that is experienced during the successive memory read operations.

Although this threat would not cause a direct failure, it still represents a reliability concern since it requires an ECC engine to keep the overall memory failure rate below a target ppm value, thus degrading the memory read access time.

III. Experimental setup

The analysis of the OEA reliability has been performed on a cells population of 2 Mbits exploiting the FN tunneling for program, erase, and soft-programming operations. The architecture of the array is a 1T-NOR.

The analysis of the OEA failures that crosses the EV level or even the R level would require the analysis of the soft-programming kinetics for those cells up to EV and R by setting a proper $OEAV$ condition. However, since both levels can be changed either by the user or during memory tests to assess the read window margins, it is important to understand the failures behavior throughout the entire kinetics. Therefore, the procedure devised in this work for the failures characterization consisted in soft-programming the over-erased cells by using an incremental constant step voltage algorithm, without deliberately stopping the OEA at the $OEAV$ level. Using this approach, a defined number of soft-programming pulses has been applied to each cell. With this methodology the soft-programming kinetics of all the over-erased cells has been fully characterized regardless of the OEA verification level thus allowing the estimate of the relationship between soft-programming failures and OEA failures. The sequence of programming, erasing, and soft-programming an array sector (i.e, an erase cycle) has been repeated 200 times, allowing several evaluations of the in-cycling features typical of the OEA.

The read current I_{read} for each cell has been measured by using a fast Direct Memory Access (DMA) mode, after each soft-programming pulse, for the entire 200 erase cycles.

IV. Soft-programming failures classification

The soft-programming failures that are responsible for the OEA reliability reduction are associated to the presence of erratic-programming bits [13]. They are ascribed to the creation/annihilation dynamics of positive charge clusters in the cells' tunnel oxide [9], [14]. Such clusters are assumed to be created by the Anode Hot Hole Injection (AHHI) [15] occurring during FN operations, whereas their annihilation is ascribed to either recombination from thermally emitted electrons or by clusters' holes detrapping [16], [17]. The interplay of those phenomena affects the soft-programming kinetics of the cells, resulting in a deviation from an average behavior calculated for each of the cells on the erase cycles that does not exhibit anomalous behaviors (see Fig. 3). This effect can be represented by a sudden modification of the soft-programming kinetics slope, whose nominal value, in the central region of the kinetics, mainly depends on the OEA step voltage granularity [18]. Such a slope change depends on the positive charge cluster properties present in the tunnel oxide [14], [19], [20], resulting in a temporary increase of the equivalent OEA voltage stepping, thus lowering the algorithm control on the over-erase recovery kinetics.

Two parameters have been defined to describe the soft-programming failure occurrences for the over-erased memory cells in an erase cycle:

- Slope Change Point (SCP): the I_{read} value in the failing soft-programming kinetics corresponding to the modification of the expected slope with respect to the average

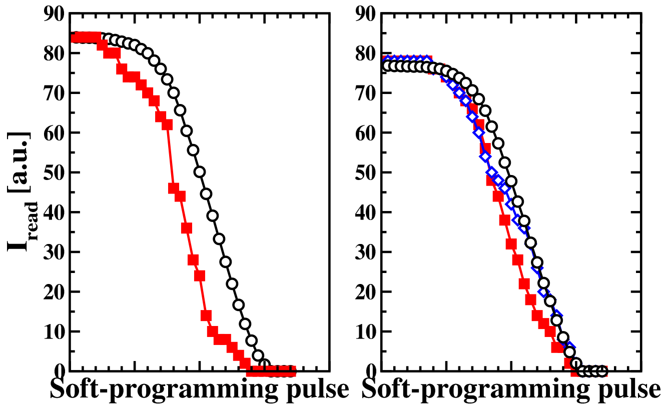

Fig. 4. Example of a Distributed event (a) and of a Mixed event (b) during soft-programming in cycling. The average soft-programming kinetics in cycling (circles) is plotted with the failing kinetics (squares and diamonds).

soft-programming kinetics. The slope must change by a factor two to be considered as a legit SCP since from characterization results of the Flash technology used in this paper it is evidenced that, when a cluster of positive charge is trapped in the cells tunnel oxide, it causes a tunneling current increase of about three orders of magnitude higher than the nominal values, leading to a modification of the soft-programming kinetics slope by a factor that depends on the position of the trapped charge [9], [14]. The minimum slope change factor retrieved when trapped charge is present is about two.

- Fail Shift (FS): the maximum I_{read} difference between the average and the failing soft-programming kinetics.

The extraction of these parameters for each failure event has been performed by specifying a 6σ discrimination limit on the FS, where σ is the resolution of the test equipment, in order to avoid the detection of *false positive* events [21].

The experimental characterization of the memory arrays evidenced two important features: the set of over-erased cells varies on a cycle basis, and each cell could exhibit multiple SCP occurrences retrieved in the soft-programming kinetics at a defined erase cycle. Based on this experimental evidence it is possible to provide a general classification of the soft-programming failures based on the typology of the events retrieved at a determined erase cycle:

- *Single event*: the soft-programming kinetics features only one SCP for all the cycles in which it deviates from the average
- *Distributed event*: the soft-programming kinetics always features more than one SCP for all the cycles in which it deviates from the average
- *Mixed event*: a mixture of the two previous classes during cycling

Fig. 4 shows two examples of soft-programming failures that have been categorized with the proposed classification system.

V. Experimental results

In this section the soft-programming failures statistical properties of the events will be evaluated to understand their link with the erratic bits physics.

A. The role of the soft-programming voltage step granularity

The soft-programming operation has been performed with two different voltage step granularity to understand the failure occurrences under different stress conditions (i.e, different electric field variations on the cell structure during the operation): large voltage steps, that results in roughly 10 - 15 soft-programming pulses applied to the cells to reach the $I_{read} < 10$ condition, and small voltage steps, that results in almost three times the number of applied soft-programming pulses. This schemes difference would turn into a fast yet coarse OEA for the former option, and into a slow but finely accurate OEA for the latter option. It must be pointed out that the $I_{read} < 10$ criterion to stop the algorithm has been chosen because the analysis of the soft-programming kinetics evidences that a characteristic kinetics saturation occurs below that current level. The potential events collected below that limit would therefore be affected by the physical phenomena occurring during the saturation (e.g., gate leakage currents) and not directly by the erratic phenomenology.

Fig. 5 shows the percentage of detected failure events in 200 erase cycles categorized using the aforementioned soft-programming failure classification system. The dominant failure mechanism is not the same for the two schemes. Indeed, the *Distributed event* failures dominate for large voltage steps with a percentage around 50%, whereas the *Single event* failures dominate for small voltage steps with a percentage around 80%. From a numerical point of view (i.e., absolute number of events) the ratio between the single events and the distributed ones is about three for the large voltage steps case and about two for the small voltage steps case. These results are in agreement with the physical background of the erratic bits phenomenon. Large voltage steps induce high electric field variations in the tunnel oxide during soft-programming and higher AHHI currents, therefore the insurgence of multiple SCP ascribed either to progressive positive charge build ups [17] or multiple charge clusters creation in the tunnel oxide [22] becomes more probable. On the contrary, small voltage steps during soft-programming are known to trigger less failures [23] thanks to the electric field variations reduction, and consequently the lowering of AHHI currents that lessens positive charge creation and reduces the slope change events. The effective reduction of these events consequently increases the probability of having only *Single event* failures.

B. SCP and FS parameters statistics

The statistical characterization of the soft-programming failures includes the analysis of the SCP and of the FS distributions for the two considered voltage steps granularity. The SCP parameter describes the memory cell susceptibility in relation to the AHHI, whereas the FS parameter is a marker of the strength of the positive charge cluster in the cells' tunnel oxide [10]. The *Mixed event* are not considered in the discussion since they represent a statistical mixing of the two previous failure classes.

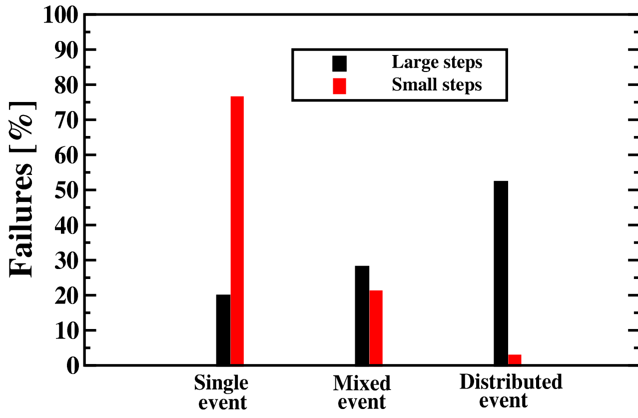

Fig. 5. Percentage of soft-programming failures categorized per event class using two different voltage schemes.

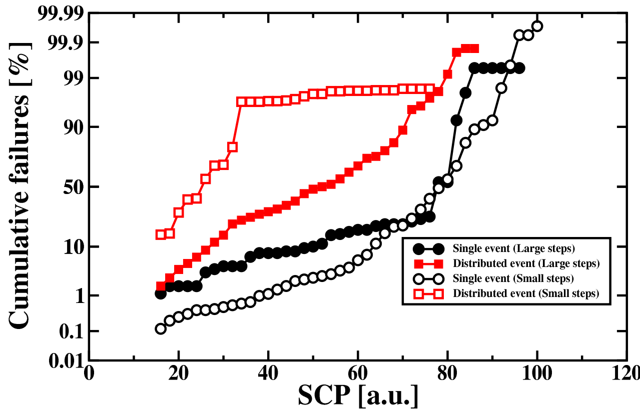

Fig. 6. Cumulative distribution of the SCP categorized per soft-programming failure event class for the two voltage schemes. Data are plotted on a normal probability plot.

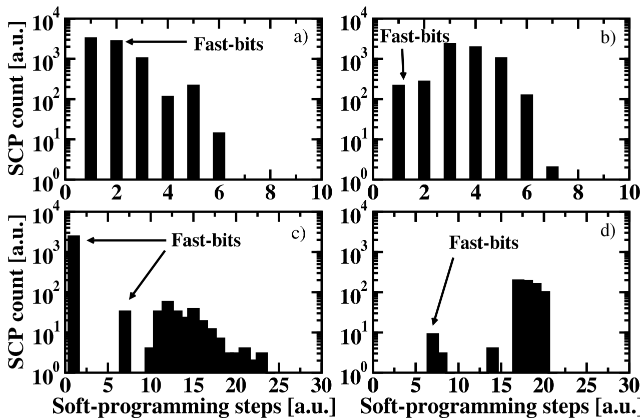

Fig. 7. $SCPs$ occurrences distributions as a function of soft-programming pulses for large voltage steps soft-programming scheme (top) and for small voltage steps soft-programming scheme (bottom). Plots a) and c) refers to *Single event* failures, whereas b) and d) refers to *Distributed event*.

As shown in Fig. 6, the SCP cumulative distribution for the *Single event* failure class shows that, for both voltage schemes, the events are distributed at higher I_{read} values (the distribution tails are at low probability values). This indicates that the majority of the soft-programming failures are in the first region of the soft-programming kinetics, and

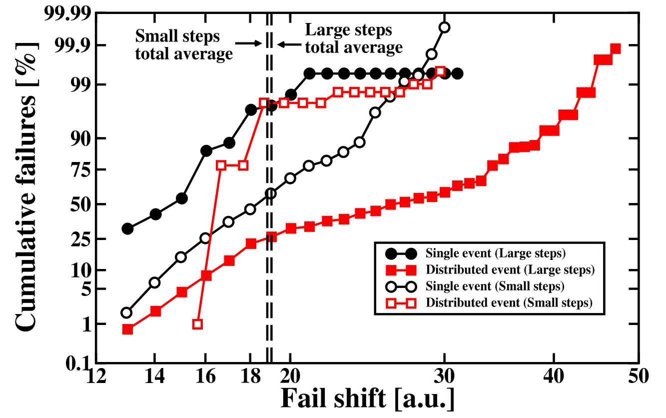

Fig. 8. Cumulative distribution of the FS categorized per soft-programming failure event class for the two voltage schemes. Data are plotted on a lognormal probability plot.

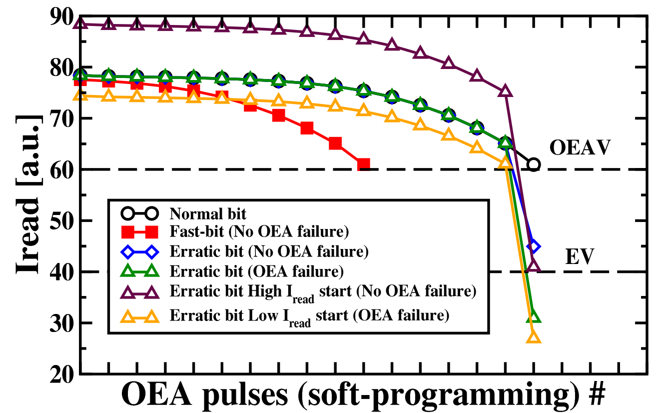

Fig. 9. Example of relationship between soft-programming failures and OEA failures. The dependency on the starting I_{read} level is also evidenced. The considerations drawn from this figure holds for different step voltage soft-programming schemes.

are typically ascribed to fast programming bits. Concerning the *Distributed event* failures it is possible to highlight that the events are distributed on a broader range compared to *Single event* failures as far as the large voltage steps scheme is considered and that this scheme presents a higher median value of the distribution compared to the small voltage steps scheme. It must be reminded that *Distributed event* failures feature multiple $SCPs$ that are the result of a progressive charge build-ups occurring during progressive soft-programming steps, thus explaining the SCP range broadening.

All these considerations are highlighted in Fig. 7, where the SCP distribution is shown as a function of the soft-programming step for both schemes. The main results of the figure are the evidence of the high number of fast bits retrieved for the single event failure type in both schemes (Slope Change Points are in the very first steps of the soft-programming kinetics), and the reduced range of steps in which the distributed events occurs compared to single events for the small steps voltage scheme.

An additional experimental result is shown in Fig. 8 by considering the FS cumulative distribution. It is observed that for large voltage steps scheme the contribution of the

Distributed event failures in the current shift is the highest, whereas for small voltage steps scheme the highest shift contribution comes from *Single event*. This result reflects the previous statistical evidences. However, it must be pointed out that if the average value of the FS statistics is calculated (i.e., not subdividing the failures per physical class) for the different voltage schemes, the values obtained are similar.

VI. Relationship between soft-programming failures and OEA failures

The soft-programming failures does not always represent a concern for the OEA. As a matter of fact, the OEA is robust against some classes of failure, that makes the algorithm reliable for its usage in memory products.

As shown in Fig. 9, the OEA failures depend on three factors: the starting I_{read} of the over-erased cells, the $OEAV$ level placement, and the memory read window margin that is represented by the placement of the EV level. All these factors, combined with the step voltage granularity exploited by the algorithm, determine the average number of soft-programming pulses applied to the cells. An OEA failure will occur if a soft-programming failure is experienced before the I_{read} crosses the $OEAV$ level at soft-programming pulse i, and the FS of that failure is high enough to drive the cells I_{read} below the EV or even the R level at the beginning of the soft-programming pulse *i+1*.

Let us indicate as OEA1 an algorithm that exploits large soft-programming voltage steps, and OEA2 an algorithm that exploits small soft-programming steps. Both algorithms assume a fictitious $OEAV$ level equal to $I_{read} = 60$. It is possible to retrieve a relationship between the soft-programming failures and the OEA failures dependently on the desired memory read window margin. In this work an EV level equal to $I_{read} = 40$ (i.e., standard margin) and an EV level equal to $I_{read} = 30$ (i.e., aggressive margin) are considered without lack of generality.

Both algorithms exhibit a significantly lower failure rate, compared to the soft-programming one, independently on the chosen margin (see Fig. 10), since most of the soft-programming failures occur in the very first region of the soft-programming kinetics (e.g., fast bits) with a FS that drives the I_{read} still above the EV level. In this way, the OEA stops correctly after crossing the $OEAV$ level.

What is interesting to point out is that both the OEA and the chosen margin affects the failure perception and therefore the failure classes distribution. By using the same classification system as for the soft-programming failures, most of the OEA failures, using a standard margin, are detected as *Single event*. Even if phenomenologically the soft-programming failures are produced over multiple $SCPs$, and therefore by a *Distributed event*, the first of those events, especially for the OEA1, is sufficient to trigger an OEA failure. If the aggressive margin is considered, the failure classes distribution tends to what previously retrieved for soft-programming failures. Straightforwardly, as the read window margin becomes aggressive a larger portion of the soft-programming kinetics is handled by the OEA, and therefore the failure classes relationship becomes stronger.

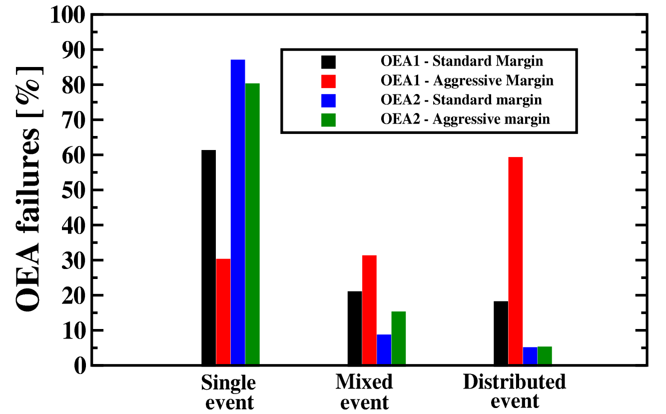

Fig. 10. Relationship between soft-programming failures and OEA failures categorized per failure class.

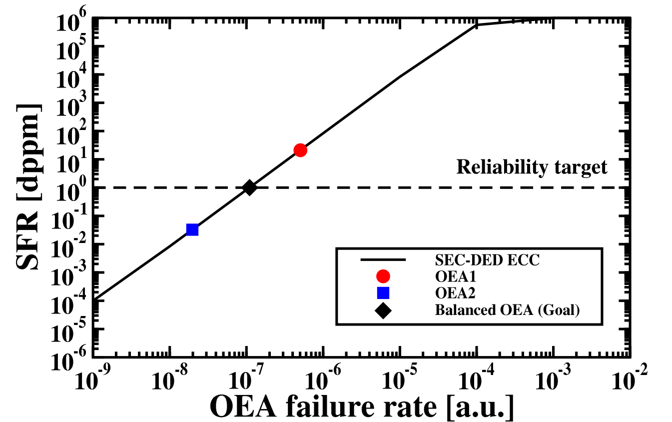

Fig. 11. SFR calculated for different OEA schemes assuming the usage of a SEC-DED ECC to correct failures.

VII. Balancing OEA performance and reliability

The reliability target for embedded automotive applications must guarantee an overall failure rate below 1 *dppm* to the memory user [24]. Concerning the OEA failures, this goal can be achieved, as shown by previous results, by tailoring the OEA algorithm with a repair strategy such as an ECC. The straightforward solution should be the usage of the finest OEA scheme to reduce the number of failures, while increasing the ECC correction strength to the maximum in order to be sure to correct all the residuals errors from the OEA. However, this approach would lead to an excessive performance reduction of the erase operation, and most of all, would seriously increase the read access time of the memory, that is calculated as the sum of the time to effectively access the data in memory and the time that ECC uses for potential data correction. The latter consideration is the reason underlying the massive integration of fast Single Error Correction-Double Error Detection (SEC-DED) codes in automotive products to reduce ECC overhead.

A model of the Sector Failure Rate (SFR) (i.e., the sector is the minimum erase unit where an OEA failure occurs) can be derived to better understand these thoughts. Let us consider a SEC-DED ECC schemes that supplements user data with parity bits which store enough extra information for the data to be reconstructed if one or more bits are corrupted by an OEA

TABLE I
RELIABILITY AND PERFORMANCE PROPERTIES OF THE DIFFERENT OEA CONSIDERED IN THIS WORK

	SFR	Average Access Time	Maximum Erase Time
OEA1	21 dppm	80 ns	4 s
OEA2	0.03 dppm	30 ns	11.5 s
Balanced OEA	1 dppm	40 ns	7 s

failure. The user and parity bits together are called *an ECC codeword (CW)* [25]. If the ECC can correct one failing bits per codeword, then the codeword will have an uncorrectable error if two or more bits fail. The probability that a codeword will fail is calculated as:

$$P_{CW} = \sum_{n=2}^{N} \binom{N}{n} \cdot \rho_{OEA}^{n} \cdot (1 - \rho_{OEA})^{N-n} \quad (1)$$

where N is the codeword size (assumed equal to 72 bits in this work), and ρ_{OEA} is the OEA failure rate. The SFR is then calculated as:

$$SFR = 1 - (1 - P_{CW})^{k} \quad (2)$$

where k is the memory sector size (i.e., 2 Mbits in this work) divided by the codeword length. Fig. 11 shows that OEA1 offers a higher SFR compared to OEA2, that is well below the reliability target limit. On the contrary OEA2 is slower than OEA1 almost by a factor three. By leveraging only on the OEA scheme structure (e.g., by changing the soft-programming pulse granularity or by using user adaptive $OEAV$ levels) it will be possible to achieve a sustainable erase and read performance, while providing at the same time a consistent reliability. In Table I it is provided a summary of the reliability and performance properties for the OEA1, OEA2, and the proposed balanced OEA algorithm. The average access time is calculated for each algorithm by assuming a 200 MHz memory clock frequency for a NOR Flash featuring a serial interface with 8 bits transfers and then summing the average time spent by the ECC for correction that is proportionally dependent on the SFR. Concerning the maximum erase time, it corresponds to the requested time to erase and execute the OEA with the maximum number of soft-programming steps on a sector.

VIII. CONCLUSION

In this paper it has been presented a detailed characterization of the OEA failures occurring in FN/FN NOR Flash technologies that exploit the FN mechanism for the soft-programming operation, that is generally valid both for 1T-NOR and 2T-NOR architectures. The experimental results evidenced that the analysis of the failure morphology, in terms of soft-programming kinetics variations and deviations from an average cycling behavior, allows understanding the role of the algorithm implementation basing on the chosen soft-programming step voltage. A detailed insight on the relationship between the soft-programming failures and the OEA failures proven that the definition of the read window margin impacts on the typology of detected failures after the algorithm execution. Finally, a solution to accurately trade the reliability and the performance of the OEA combined with the ECC use for failure correction has been shown.

ACKNOWLEDGEMENTS

The authors would like to thank A. Siviero for the invaluable help in the creation of the experimental setup and in the results evaluations.

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