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Coordinatrice: Prof.ssa Eleonora Luppi

Graphene Integration in Silicon Microelectronic Technology for Fabrication of Hybrid Devices

Settore scientifico disciplinare: FIS/03

Tutor:
Prof. Diego Bisero

Co-tutor:
Prof. Vittorio Morandi

Dottoranda:
Piera Maccagnani

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Contents

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A Giulia e Davide, infinito amore

"Non solo impariamo, ma impariamo anche a cambiare gradualmente la nostra struttura concettuale, e ad adattarla a ciò che impariamo. E quello che impariamo a conoscere, anche se lentamente e a tentoni, è il mondo reale di cui siamo parte. Le immagini che ci costruiamo dell'universo vivono dentro di noi, nello spazio dei nostri pensieri, ma descrivono più o meno bene il mondo reale di cui siamo parte. Seguiamo tracce per descrivere meglio questo mondo."

Sette brevi lezioni di fisica
Carlo Rovelli

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Abstract (Italian version)

Scopo di questo lavoro è lo sviluppo di un processo affidabile e riproducibile, dove i processi di crescita e trasferimento del grafene (Gr) sono integrati in modo efficace nella piattaforma tecnologica del silicio, per la fabbricazione di dispositivi innovativi in Gr. L'attualità di questa ricerca è confermata dall'iniziativa 2D Pilot Line, finanziata dalla CE e operativa dal 2021, che favorisce l'uso di materiali 2D promuovendo la fabbricazione di prototipi. Il lavoro di tesi è organizzato in 3 moduli: i) il **"modulo grafene"**, che consiste nella messa a punto dei singoli processi tecnologici (crescita, trasferimento del Gr sul substrato di Si, definizione e attacco delle strutture in Gr, ricoprimento del Gr). È il modulo base per l'integrazione del Gr nella piattaforma microelettronica. Grande attenzione è posta al mantenimento della qualità del Gr, controllata attraverso lo studio delle sue proprietà elettriche e strutturali. ii) Il **"modulo fabbricazione"**, in cui i processi messi a punto sono organizzati in un flusso tecnologico complesso, (compatibile con l'approccio back end of line). In questo modulo strutture di test e dispositivi di base in Gr sono fabbricati ed estesamente caratterizzati, con un duplice obiettivo: estrarre informazioni sulle principali proprietà del grafene, come drogaggio, mobilità, resistenza strato, resistenza di contatto, livello di Fermi, ecc., e studiare come esse si modificano per effetto dei processi eseguiti; e studiare l'interazione fisica tra Gr e Si. Particolare attenzione è posta alla resa e all'uniformità dei parametri nei dispositivi fabbricati, definendo opportune strutture di test e protocolli di misura, che attraverso l'analisi dei dati consentono la caratterizzazione dell'intero processo. iii) Il **"modulo applicativo"**. Sulla base delle informazioni ottenute nel modulo precedente, è definita la procedura (da intendersi come sequenza ottimizzata dei passi e dei controlli da eseguire) che consente la fabbricazione di dispositivi complessi. In questa tesi si è fabbricato un fotorivelatore in grafene che opera nel NIR. Un'estesa caratterizzazione elettrica e ottica ha consentito di studiare il ruolo del grafene sul suo funzionamento.

Tra le diverse strutture di test, ampio spazio è stato dedicato alla fabbricazione e caratterizzazione di diodi Schottky in grafene, e all'ottimizzazione della qualità dell'interfaccia Gr/Si, studiando diversi processi di trasferimento del Gr. I parametri tipici del diodo sono stati estratti utilizzando i metodi classici (sviluppati per i diodi metallo/Si), evidenziandone i limiti di validità dovuti alla dipendenza del livello di Fermi del Gr dalla tensione applicata. Nel tentativo di ottenere una migliore comprensione del meccanismo di conduzione nei diodi Gr/Si è stato sviluppato un modello, introducendo un'equazione che esprime la corrente in funzione del numero di cariche scambiate tra Gr e Si, e inserendo nelle equazioni del modello la dipendenza del livello di Fermi del Gr dalla tensione applicata. Il modello, utilizzato per il fitting delle misure sperimentali, ha evidenziato il ruolo giocato nella definizione della barriera Schottky del diodo dalla densità delle cariche di superficie in polarizzazione diretta e dallo strato invertito in inversa.

Come dispositivo finale è stato fabbricato un fotorivelatore in Gr, operante nel NIR,

dove il Gr è inserito all'interno di una cavità risonante, costituita da Si cristallino e Si amorfo, al fine di aumentarne la responsività. La caratterizzazione elettro-ottica nel NIR ha permesso di evidenziare un notevole aumento della corrente termo-ionica del dispositivo. Il fenomeno è stato studiato sviluppando un modello che riproduce gli andamenti sperimentali ottenuti e che lega l'aumento della corrente alla riduzione del livello di Fermi del grafene indotto dall'iniezione delle cariche rilasciate dalle trappole all'interfaccia Gr/Si amorfo per effetto della luce.

Abstract (English version)

The aim of this work is to develop a reliable and reproducible process to fabricate high quality graphene (Gr) devices, combining effective Gr growth/transfer and efficient fabrication technology. This is an emerging trend, further confirmed by the EC-financed 2D Pilot line, started in 2021 with the aim to make 2D materials integration accessible to EU companies, SMEs, and researchers, to promote prototyping of hybrid devices. The work of the thesis is organized in three modules: i) the **graphene module**, where all the technological processes required for the integration of Gr into the silicon (Si) microelectronic platform (Gr growth, transfer onto the Si substrate, photolithographic patterning and etching, and Gr encapsulation) are developed. Besides the process development, electrical and structural characterization are used to continuously check the Gr quality and study how Gr properties are affected by the technological processes. ii) The **fabrication module**, where the developed processes are organized in a process flow, compatible with the back end of line approach, and available for the fabrication of test structures and basic Gr devices. From these devices, information on the main Gr properties, (doping, mobility, sheet resistance, contact resistance, Fermi level, etc.) are extracted, and the physical interactions between Gr and Si are investigated. Yield and uniformity of device properties are key metrics for the fabrication technology, therefore test structures, measurement protocols and data analysis have been developed and exploited to characterize the full process. iii) The last module is the **application module**. The broad experience acquired through the fabrication of Gr test structures, has allowed a "best practice" procedure to be defined towards the fabrication of hybrid Gr devices. In this work, Gr photodetectors working in the NIR have been fabricated and fully characterized, studying the effect of the introduction of Gr on their performances.

The core of the work is represented by the Gr/Si Schottky junctions, fabricated using different Gr transfer procedures. Standard methods for the extraction of 3D diode parameters have been applied to 2D Gr diodes, identifying the region where each parameter should be extracted, and highlighting the voltage bias dependence of the Gr Fermi level and its effect on the diode's Schottky barrier height (SBH). Moreover, a model has been introduced, in order to account for the conduction mechanisms and shifts in Gr Fermi level that occurs by applying positive and negative bias to the Gr/Si junction.

In particular, a new equation, working in the region near the thermionic conduction and consistent with experimental measurements, was introduced. The model is used to fit experimental I-V, highlighting the important role played by charge surface density in forward bias, and by the inversion layer in reverse bias, in defining the value of the Gr/Si SBH that is established at the interface. Moreover, it has been demonstrated that different Gr transfer processes could affect the number of surface states, having an effect also on the final SBH of the Gr/Si junction.

The experience achieved on Gr/Si Schottky junctions was extended to the fabrication of Gr photodetectors (PD) working in the near-infrared (NIR). Here the graphene layer is physically embedded between a crystalline and a hydrogenated silicon layer realizing the resonant cavity, to enhance the detector responsivity. Under NIR illumination these PDs show an unforeseen increase in the thermionic current. This effect has been ascribed to the lowering of the Gr/c-Si Schottky barrier as a result of an upward shift of the graphene Fermi level induced by charge carriers released from traps localized at the Gr/amorphous Si interface under illumination. A complex model reproducing the experimental observations has been presented and discussed.

Summary of research activities

The work of this Ph.D. thesis was largely developed in the clean room of the Institute for Microelectronics and Microsystems (IMM) of CNR in Bologna, working on different technological processes (photolithography, oxide deposition, metal deposition, graphene growth, graphene transfer process), and taking advantage of the different characterization techniques available in the lab (Raman spectroscopy, SEM analysis, optical inspection, spectrophotometer analysis). For the technological fabrication of hybrid graphene devices, a complete process flow, compatible with a back end of line approach, was planned and the photolithographic masks were designed and fabricated. To electrically characterize the graphene layer, and some other processes required in the technological processes flow, different measurements have been set up: van der Pauw and in-line four probe method for the measurement of Gr sheet resistance, Hall measure to extract Gr carrier density and mobility, and circular TLM measurement to obtain information on the contact resistance. The classic methods used for diode's parameter extraction in metal/Si junction have been studied, highlighting their limits of application and defining a procedure for their application to Gr/Si junctions. To account for the conduction mechanisms and variation in the graphene Fermi level that occurs applying positive and negative biasing to the Gr/Si device, some work was dedicated to develop a model able to describe the transport mechanism in a Gr/Si junction. The model is based on a semi-phenomenological approach and includes a new equation, consistent with experimental measures, that adds to the classic diode equation, which works well in the thermionic regime. The experience gained on Gr/Si Schottky junction, was extended to the fabrication of Gr photodetectors (PD) working in the near-infrared. This activity was developed in the framework of the REVEAL project (NeaR-infrarEd resonant caVity enhancEd grAphene/siLicon photodetectors), funded by EC (Attract Project, Grant agreement n. 777222, in the Horizon 2020 Framework Programme for Research and Innovation). A model reproducing the experimental observations has been developed and discussed, highlighting the important role of traps on the current of the photodetector. Moreover, NEXAFS spectroscopy measurements were performed on the line BEAR, at the ELETTRA lab (proposal 20205096). The main purpose was to analyze the strain of graphene on copper and after transfer on silicon substrates, evaluating the effect of different transfer methodologies, using NEXAFS spectroscopy combined with RSXRR. The final aim was to perform measurements on hybrid graphene diodes, trying to correlate the strain in graphene film to diode's electrical performances. Unfortunately, no clear results have been obtained, mainly due to the difficulties in aligning the beam on the diode active area and to perform the measurements on devices under biasing.

The overall activities developed in the three years of the Ph.D. led to following publications and presentations in workshops or international conferences:

1. M. Casalino, P. Maccagnani, et al., Poster: "Near-Infrared Resonant Cavity En-

hanced Graphene-Silicon photodetectors", Conference Graphene 2019, 25-28 June Roma

2. P. Maccagnani, M. Casalino et al., Poster "Graphene-Silicon photodetectors", Workshop on "Wafer scale integration of 2D materials", 2019, November 12-13, Aachen, AMO GmbH,

3. M.Casalino, P. Maccagnani, et al., Oral presentation: Silicon meet Graphene for a new family of near-infrared resonant cavity enhanced photodetectors, 22nd International Conference on Transparent Optical Networks ICTON, 2020, July 19-23, Bari;

4. C. Barone; M- Bertoldo, R. Capelli, F. Dinelli, P. Maccagnani, N. Martucciello, C. Mauro, S. Pagano, Electric Transport in Gold- Covered Sodium–Alginate Free-Standing Foils. Nanomaterials 2021, 11, 565;

5. M. Cocchi, M. Bertoldo, M. Seri, P. Maccagnani, C. Summonte, S. Buoso, G. Belletti, F. Dinelli, and R. Capelli; Fully Recyclable OLEDs Built on a Flexible Biopolymer Substrate, ACS Sustainable Chemistry & Engineering 2021 9 (38), 12733-12737;

6. C. Summonte, P. Maccagnani, A. Maurizi, G. Pizzochero and G. Bolognini, Simulation of the optical properties of gold nanoparticles on sodium alginate (Poster); Conference EOSAM 2021, 13-17 Sept.2021, Roma

7. C. Barone, M. Bertoldo, R. Capelli, F. Dinelli, P. Maccagnani, N. Martucciello, C. Mauro and S. Pagano,Electric Transport in Gold-Covered Sodium–Alginate Free-Standing Foils, Nanomaterials, 2021, 11, 565

8. C. Barone, P. Maccagnani, F. Dinelli, M. Bertoldo, R. capelli, M. Cocchi, M. Seri and S. Pagano, Electrical conduction and noise spectroscopy of sodium-alginate gold-cobered ultrathinfilms for flexible green electronics, Scientific Reports, 2022, 12, 9861

9. L. Marchi, F. Dinelli, P. Maccagnani, V. Costa, T. Chenet, G. Belletti, M. Natali, M. Cocchi, M. Bertoldo, M. Seri, Sodium alginate as a natural substrate for efficient and sustainable organic solar cells, 2022, ACS Sustainable Chemistry & Engineering, ;

10. C. Summonte, A. Maurizi, R. Rizzoli, F. Tamarri, M. Bertoldo, G. Bolognini, and P. Maccagnani (corr. author), Experimental analysis and simulation of the optical properties of gold nano-particles on sodium alginate, Optical Materials Express, Vol. 12, No. 11, 1 Nov 2022;

11. T. Crisci, P. Maccagnani (corr. author), L. Moretti, C. Summonte, M. Gioffrè, R. Rizzoli, and M. Casalino, The Physics behind the Modulation of Thermionic Current in Photodetectors Based on Graphene Embedded between Amorphous and Crystalline Silicon, Nanomaterials 2023, 13, Issue 5, 872.

Introduction

Introducing Graphene into the Si planar technology

Silicon has been the principal material in microelectronics for more than five decades, thanks to its low cost, simple production and well defined processing routes. In the last fifteen years, a great deal of efforts and resources has been devoted to the study of two dimensional materials (2DM), especially graphene, an allotrope of carbon with impressive properties, as possible candidates for next generation electronics. Thanks to its excellent electronic properties (low electrical resistivity, high thermal conductivity, high current carrying capabilities), graphene is a promising material, potentially able to introduce important advancements in the field of micro- and nano-electronics, promising faster, more sensitive and even completely novel devices. The main route is the integration of graphene into conventional silicon-based fabrication lines, which has two main advantages: i) the use of well-established processing steps, with a relatively low engineering effort; ii) the three-dimensional (3D) integration of graphene into the silicon complementary metal–oxide– semiconductor (CMOS) platform, which may enable the combination of high-performance graphene devices with established CMOS readout circuitry, with production costs as low as conventional silicon technology. A recent study published in 2019 [1], showed the potential applications of 2DM-Si technology mapped as a function of time and integration complexity. The main feature of that study (Figure 1) is that the time has come for the introduction of 2DMs into many different systems, such as sensors, (gas, chemical and biological, Hall sensors, nano-electro mechanical systems, etc.), photodetectors and modulators for image sensors, light detection and ranging (LIDAR). All these devices can be fabricated using a back end of line (BEOL) approach[1], i.e. they can be realized on an integrated CMOS chip, that provides the driver, read-out and peripheral circuitry, while only the active sensor is fabricated using the 2DMs.

The huge potential impact of the integration of graphene and of GRMs in the semiconductor platform pushed the European commission to launch the €20 million project

[1]Semiconductor manufacturing is typically separated into Front End of Line (FEOL) and back end of line (BEOL) processing. FEOL includes all the processes mainly related to the device fabrication, and are generally the first steps in the silicon circuit fabrication process. While BEOL processes typically involves metal and diffusion barriers, and the temperatures reached are relatively modest ($\leq 450\,^{\circ}\mathrm{C}$.

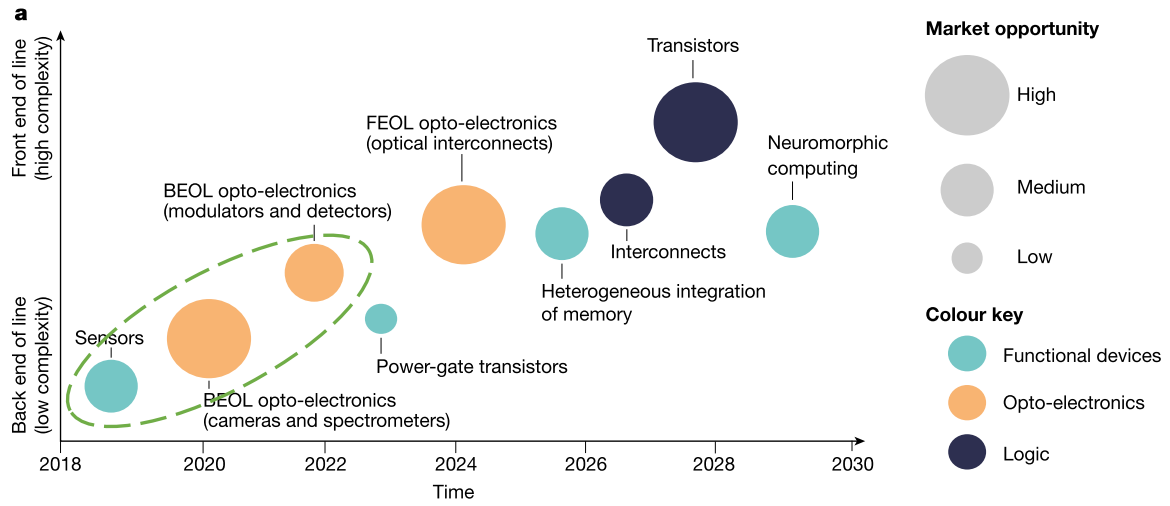

Figure 1: Forecast of applications of 2DM–Si technology mapped by time and integration complexity. The position of the circle indicates the time for a possible production of the different products with the 2DM-based technology. The area of the circles gives a qualitative estimation of the impact on the market. Complexity increases when moving from back end of line (BEOL) to front end of line (FEOL) integration (from [1]).

2D Experimental Pilot Line [2], in October 2020. This project will develop the modules for manufacturing the basic building blocks for GRM-based technologies, and will provide prototype services to companies, research centers and spin-offs, with the aim of pioneering the manufacturing of new prototype electronics, sensors and photonics using 2D materials.

This is the framework within which the work of this Ph.D. was carried out. The research activity has been developed at the CNR Institute for Microelectronics and Microsystems, Section of Bologna, where I work and where a technological Si platform for the fabrication of Si-based sensors and MEMS devices operates on a daily basis. The main aim that guided this work was to introduce 2DMs to our platform of classical working 3D materials for Si technology, starting with graphene, whose properties have been studied broadly in the last few years. The introduction of graphene (and more generally of a new material) into a standard platform faces several challenges and requires the development and implementation of new reliable and reproducible processes to maintain and use the physical properties of the new material in an efficient way. Moreover, working with a 2D material results in an additional challenge, because the 2D material is all surface, where also the conduction mechanisms take place.

Structure of the thesis

This Ph.D. thesis is organized in three main modules: i) the development of the technological processes to grow and process graphene; ii) the definition of an optimized process flow for the integration of Gr into planar Si technology and the fabrication of test structures to check the Gr quality and properties throughout the process; iii) the fabrication of a complete device to study how the introduction of Gr influences the device performances. With this structure in mind, the first part of the work (Chapter 1) is devoted to obtaining Gr films with good control over the number of layers, domain size and doping level, with proper monitoring of the related resistivity and conductivity. Then, it focuses on the development of the basic building-blocks (growth – transfer – quality control) for the integration of graphene with existing technology platforms, (CMOS platform), for the fabrication of compatible hybrid electronic devices in the fields of optoelectronics, photonics and electronics. Finally, it contains a careful investigation of how the graphene properties change due to the integration process and in relation to the adjacent layers that support or cover the graphene structures. As pointed out previously, this is of paramount importance, because the extraordinary properties of graphene are associated to its 2D surface, and every process capable of inducing surface modification could change properties of the material. Yield and uniformity of the device properties are key metrics for the fabrication technology, therefore test structures, measurement protocols and data analysis have been developed and extensively studied to characterize the overall process as well as each individual step. The second part of the work (Chapter 2) is devoted to the fabrication and characterization of test structures used to extract the main electrical and structural characteristics of the Gr. Significant effort was dedicated to Gr/Si junctions (GSJ). These structures require a simple fabrication process, and are a suitable platform to investigate the electronic properties and device transport mechanisms, and to study the physics occurring at the interface between a 2D and a 3D material. The challenge in GSJ fabrication is the ability to establish an intimate contact between graphene and silicon, avoiding chemical-structural modifications to the semiconductor and simultaneously preserving the unique properties of graphene. Two different transfer methods for graphene have been developed and used for the fabrication of Gr/Si junctions, paying attention to impurities and defects at the interface that may significantly alter the I-V curve, as occurs for conventional metal/ semiconductor diodes. Additionally, the low density of states close to the Dirac point makes the graphene Fermi level extremely sensitive to the amount of carriers injected into or from the semiconductor, determining a tunable Schottky barrier height (SBH), which in turn controls the current-voltage relationship of the GSJ. These features make the Gr/Si junction an excellent platform for the study of interface transport mechanisms. For this reason, a model was proposed, in order to account for the conduction mechanisms and shifts in Gr Fermi level that occur applying positive and negative bias to the GSJ. In particular, a new equation, working in the region near that of thermionic conduction and consistent with experimental mea-

surements was introduced. The model is used to fit the experimental measurements, and highlights the fundamental role played by charge surface density in forward bias, and by the inversion layer in reverse bias, in defining the value of the Gr/Si SBH that is established at the interface. The model has also shown that different Gr transfer processes could affect the number of surface states, having an effect also on the final SBH of the GR/Si junction. The last part of the work (Chapter 3) is related to the fabrication of Gr photodetectors (PD), working in the near-infrared (NIR), where Si has poor absorption. In these devices the Gr layer is embedded between a crystalline and a hydrogenated silicon layer, forming a resonant cavity to enhance the detector responsivity. Under NIR illumination, these PDs show an unforeseen increase in the thermionic current. This effect has been ascribed to the lowering of the Gr/crystalline Si Schottky barrier as a result of an upward shift in the graphene Fermi level induced by charge carriers released from traps localized at the Gr/amorphous silicon interface under illumination. A complex model reproducing the experimental observations has been presented and discussed. Responsivity of these PDs exhibits a maximum value of 27mA W^{-1} at 1543nm under an optical power of 8.7µW, which could be further improved at lower optical power.

Chapter 1

Graphene: growth, characterization and integration

Introduction

The introduction of a new material like graphene in a standard platform has to face several challenges and requires the development and implementation of new reliable and reproducible processes to keep and use the physical properties of the new material in an efficient way. The final aim of fabricating new hybrid graphene-devices with precise and reproducible performances, requires the science and technology of graphene to face major challenges:

- to obtain Gr film with good control of number of layers, domain size and doping level, with proper monitoring of the related resistivity and conductivity;
- to develop the basic building-blocks (growth – transfer – quality control) for the integration of graphene with existing technology platforms, like CMOS platform, for the fabrication of hybrid compatible electronic devices in the fields of optoelectronics, photonics and electronics;
- a better understanding of how the graphene properties change due to the integration process and in relation to the adjacent layers that support or cover the graphene structures. This because the excellent properties of graphene are related to its 2D nature, that is to its surface, so that every surface modification could change the material properties.

Chapter 1 deals with the most crucial technological aspects for the integration of graphene into complementary metal-oxide semiconductor (CMOS) platform and illustrates the work carried out during the thesis in terms of analysis of the state of the art,

choice of the more suitable processes and methodologies, and their development and application to graphene. In particular, the present Chapter will deal with the properties and structure of graphene (Section 1.1), with the production of graphene films (Section 1.2), with definition of the technological platform (Section 1.3), in terms of the technological processes for graphene transfer on silicon substrates (Section 1.4), graphene patterning (Section 1.5) and metal contact to graphene (Section 1.6). The last part of the chapter is dedicated to the techniques used to evaluate structural and electronic properties of graphene (Section 1.7).

1.1 Graphene structure and properties

Graphene is a two-dimensional allotrope of carbon in which the carbon atoms are arranged in hexagonal structure, as shown in Figure 1.1a. The primitive cell is composed by two non-equivalent atoms, A and B. The two sublattices are translated from each other by the carbon-carbon distance $a_i \sim 1.42\,\text{Å}$. Each carbon atom in the lattice has 4 valence electrons, three are used for the covalent bonding and occupy the in-plane sp^2 hybrid orbitals, while the remaining electron occupy the p_z orbital, that extends out of the basal plane. The planar orbitals with the three nearest-neighbor C atoms in the honeycomb structure are responsible for the stable σ-bonds, and define the binding energy and elastic properties of the graphene sheet. The electronic properties of graphene are defined by the $2p_z$ orbitals, with the π symmetry orientation and their overlap with neighboring atoms. The electronic structure of graphene can be described through the tight binding model, where the lattice symmetry is included as a periodic perturbation of the electrons occupying the atomic orbitals. Figure 1.1c shows the band structure of a single layer graphene, obtained with tight-binding calculations, with the Dirac cones at the K and K' high-symmetry points, where the conduction and valence bands form cone shapes that intersect at a single point. In intrinsic graphene, the Fermi level coincides with the intersection of the two Dirac cones at the Dirac point. The terminology "Dirac cone" and "Dirac point" are commonly used because an electron near one of the K points obeys the 2D Dirac equation for a massless fermion, and the graphene's two lattice sites takes the role of the spin degree of freedom in the Dirac equation. The slope of the Dirac cones is given by $\hbar v_F$, where $\hbar$ is the reduced Plank constant and $v_F \sim 10^8\,\text{cm}\,\text{s}^{-1}$ is the Fermi velocity. The Fermi level of graphene, E_F with respect to the Dirac point, is related to the carrier concentration (n, hole or electrons) by the Pauli blocking law:

$$E_F = \pm\hbar v_F \sqrt{\pi n} \tag{1.1}$$

positive for electron-doping and negative for hole-doping [3]. For these crystals the in-plane carbon atoms are connected by strong s-bonds, while adjacent layers are connected with weak van der Waals forces.

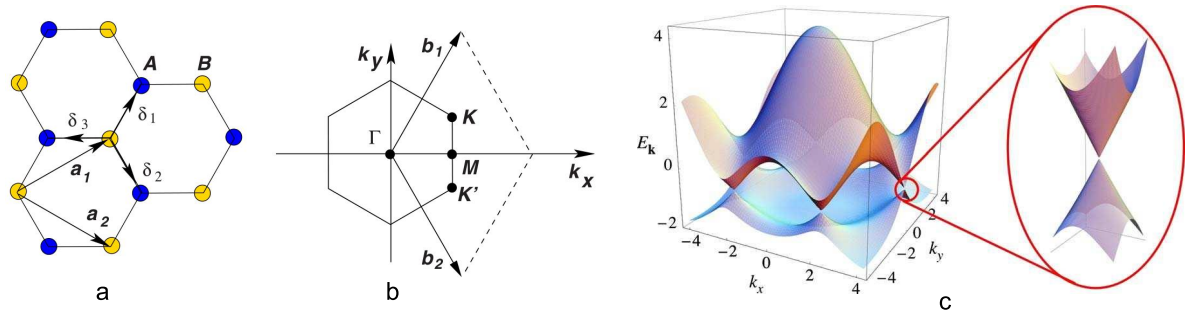

Figure 1.1: (a) The honeycomb lattice of graphene. The carbon atoms in blue and yellow occupy crystallographically non-equivalent lattice sites. a_i are the real lattice vectors, and δ_i are the nearest neighbor vectors. (b) The reciprocal lattice and first Brillouin zone, with the reciprocal lattice vectors b_i and high-symmetry points labeled; (c) Tight-binding band structure of graphene, with zoom in of the energy bands close to one of the two Dirac cones, on the right (from [3]).

The optical properties of graphene are tightly related to its conical and gapless electronic band structure. In fact, graphene is characterized by a universal value for the inter-band-transition-induced high frequency conductance of $q^2/(4\hbar)$ over a wide spectral range from visible to infrared. As a consequence, the transmittance of pristine graphene is frequency independent and only determined by the fine-structure constant $\alpha = q^2/(\hbar c)$, where q is the electronic charge, and c is the speed of light. For this reason, a monolayer graphene absorbs $\pi\alpha \sim 2.293\%$ of the incident light, a quite high value considering it's one atom thick, from visible to infrared, covering the optical fiber communication bandwidth, (typically from 1300 to 1600 nm). For multilayers graphene the light absorption of N-layer graphene is $N\pi\alpha$ (Figure 1.2).

The Fermi level of graphene is directly related to the optical absorption. In fact, Graphene has a very low density of states near the Dirac point as a result of its 2D nature, as well as its small Fermi surface. As a result, its Fermi level can be tuned electrostatically, that is applying a voltage to a capacitor consisting of a sheet of graphene separated from another conductor by some dielectric, the graphene's Fermi level can be shifted substantially. This process is often referred to as electrostatic doping or just doping, and is completely different from impurity doping used in silicon. Graphene has a high carrier mobility of $200000\,\mathrm{cm^2\,V^{-1}\,s^{-1}}$ at room temperature, therefore there is a great interest to use it for fabrication of ultrafast electronics/photonics devices. Photocarrier generation and relaxation processes in graphene are in the range of picoseconds, and graphene could operate at over hundreds of GHz.

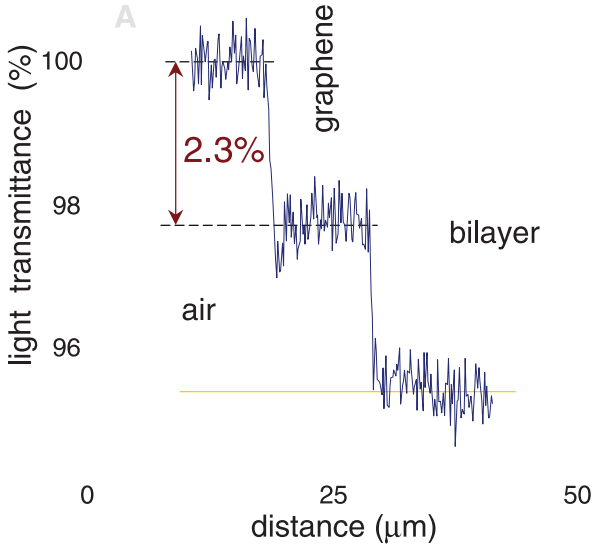

Figure 1.2: Optical absorption in graphene is approximately 2.3% for vertical incident light on pristine monolayer graphene, and doubles for the bilayer graphene (from [4]).

1.2 Synthesis of graphene films

The use of graphene in practical applications requires the preparation of large area and continuous graphene films with excellent properties. Based on its morphology, it's possible to classify graphene in 2 groups: graphene powders and graphene films. The first one is produced in large quantities and used dispersed in solvents for solution based and film-based applications. But for electronic applications, based on planar technology, graphene films are the preferred choice (Figure 1.3).

The most used techniques for obtaining graphene films are the mechanical exfoliation, epitaxy on silicon carbide or chemical vapor deposition (CVD) on catalytic metals [6].

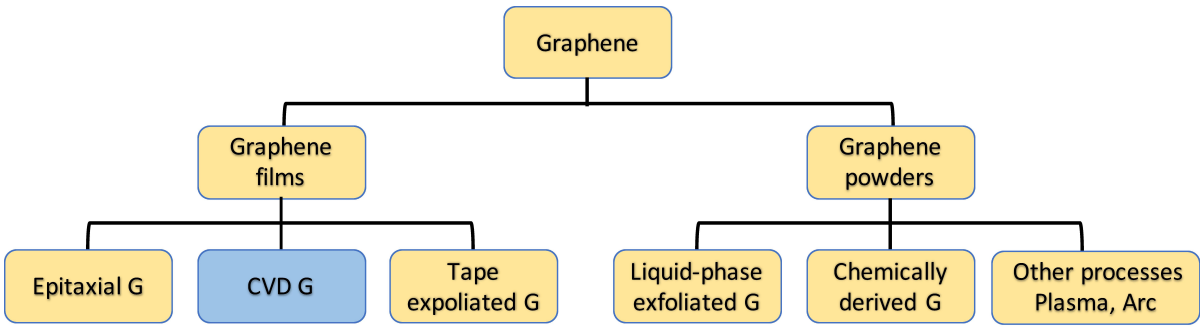

Figure 1.3: Different forms of graphene production [5].

Among these synthetic methods, CVD has been considered in the last years, one of the most promising, as it guarantees high-quality graphene films, relatively low cost production, and scalability to 200 mm or 300 mm wafer sizes. Several kinds of CVD processes can be used, including thermal CVD, plasma enhanced CVD, hot wall (the walls of the reactor chamber are kept at high temperature), cold wall (the wall of the reactor are not heated), etc. The most commonly used are thermal CVD and PECVD. Recently, a lot of efforts have been devoted to PECVD growth of graphene. In the PECVD system, electrons generated by the plasma are highly energetic and boost ionization, excitation and dissociation of hydrocarbons precursor at relatively low temperatures, enabling Gr growth on the desired substrates (such as SiO_2/Si wafer), in absence of metal catalysts and at temperatures compatible with the BEOL processes. Unfortunately, the resulting layers are quite defective and some work has still to be done to improve the quality of the Gr film. Anyway, PECVD Gr growth has great potential for electronics applications thanks to the low growth temperature and free post-transfer process. [7].
Deposition of high-quality graphene using thermal CVD process is based on transition metal catalytic substrates, like Cu, Ni or Cu alloys, and requires high temperature process (800–1000 °C). Exposing the transition metal to hydrocarbons gas (such as methane, benzene, acetylene or ethylene) at high temperature, there is a carbon saturation on the substrate and a thin film of carbon forms on cooling. The CVD process is more efficient and controllable, because the parameter window for controlling the Gr nucleation density and domain orientation is large, and enables large (> cm) single-crystal Gr growth. The main drawback of CVD growth is that for the integration of Gr into the Si platform, the catalytic metallic substrate must be removed and the thin and fragile one or few layer thick graphene film must be transferred to the silicon substrate.

A comparison between the different Gr film synthesis methods is reported in Table 1.1, along with their main advantages and disadvantages. In summary, exfoliated graphene has a high quality but poor industrial relevance, due to its reduced area. Epitaxial graphene is scalable and high quality, but also costly and limited to the type of processes it can be introduced into. CVD graphene offers a scalable, industrially relevant process which can produce high quality graphene, with CMOS and BEOL compatibility. The CVD Gr has also uniform thickness (mono- or few-layer) over the entire wafer. The uniformity arises due to the CVD growth mechanism which is a self-limiting process.

1.2.1 CVD growth of graphene

Among the transition metals, copper (Cu) is the most used for the synthesis of graphene, for two reasons: i) copper promotes the dissociation of methane at its surface at 1000 °C; ii) the solubility of carbon in copper is very low, even at high temperatures, self-limiting the growth of graphene to few layers. The most commonly used substrate for the Gr growth is a copper foil, which allows the production of very large graphene films, even in a roll-to-roll system [8]. But a thin Cu film deposited by physical vapor deposition (PVD)

Table 1.1: Comparison between graphene synthesis methods for integration in CMOS platform.

	Synthesis method		
	Mechanical exfoliation	Epitaxial growth	Chemical vapor dep.
High quality graphene	Yes	Yes	Yes
Large area production	No	Yes	Yes
Cost production	Low	High	Medium
Process scalability	No	Yes	Yes
CMOS compatibility	No	Partially	Yes
BEOL compatibility	Yes	No	Yes
Substrate independent	Yes	No	Yes

!

on a silicon wafer substrate can be also used as metal catalyst for the Gr growth, providing the use of a diffusion barrier between the silicon substrate and the Cu film, in order to prevent the diffusion of Cu into the silicon substrate. This approach is more wafer level compatible, but because of the Cu solubility in Si at the high deposition temperature used (1000 °C), it suffers from the diffusion of Si towards the Cu surface generating holes in the Gr film. Therefore, to suppress heavy sublimation and phase segregation, the graphene growth temperature should be kept lower than that usually used for metal foils, obtaining a Gr film with lower quality [9]. For this reason, the thin-metal Cu films are typically used for laboratory studies or experimental device fabrication, rather than large-scale and high- throughput production of highly crystalline graphene. Another important aspect of central importance for applications in electronics and optoelectronics is the growth of high-quality graphene on a large scale. To minimize the adverse impacts of grain boundaries in large area polycrystalline graphene, the synthesis of large single crystals of monolayer graphene is one of the key challenges for graphene production. Recently the direct CVD growth of monolayer Gr on an oxidized Si wafer has been demonstrated employing a thin film of Pt as catalyst [10]. The technique is very promising, but high temperature processes (in the range of $900 - 1000\,^{\circ}\mathrm{C}$) are required both for Pt annealing and Gr growth, limiting the application of the method to the FEOL process, when all the materials on the wafer can sustain high temperatures processes. The growth of graphene during FEOL requires to put great attention to all the subsequent processes to preserve the high quality of the graphene layer.

1.2.2 The graphene CVD deposition process at IMM

Thermal CVD growth of graphene on a copper foil is the process used in IMM. In this thesis, no special efforts have been dedicated to modify or improve the standard

Figure 1.4: Hot wall furnace used for graphene synthesis. (A) indicates the port where gases are introduced, (B) is the quartz tube where the copper foil is placed, (C) is the furnace connection to the vacuum pump and way-out connection for exhaust gases.

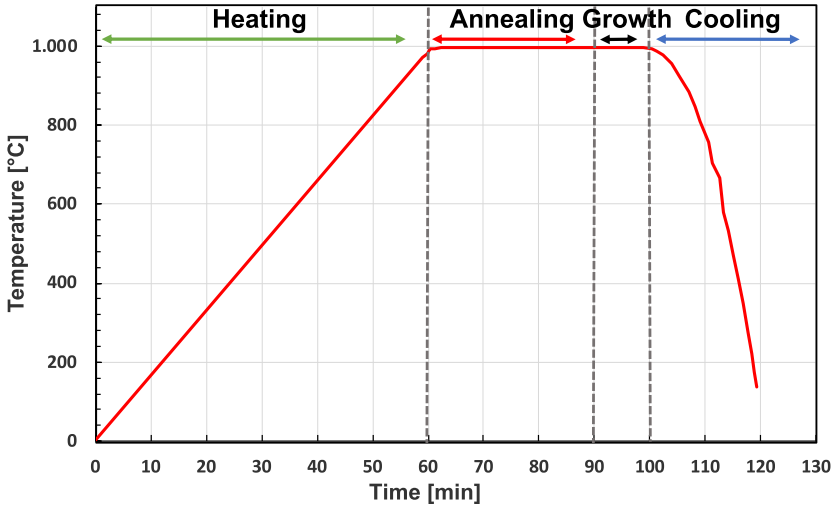

Figure 1.5: Schematics of the different steps used for the CVD synthesis of graphene film on a copper foil.

deposition process, because it's a well-established process, which produces reproducible large graphene films with good quality. The synthesis of CVD graphene is performed in the clean room of CNR-IMM, starting from a copper foil 25 µm thick, as catalyst. The copper foil is cut in pieces of $5 \times 3\,cm^2$, being careful not to create fold or ripples (which may determine overgrowths in the graphene film). Then the foil is inserted at room temperature in the quartz tube of the CVD furnace (Figure 1.4), covered with another piece of copper as a tent. After sealing the tube, the pressure is decreased to ~ 10 mbar and 1000 sccm (standard cube centimeter per minute) of argon are flown for 10 minutes saturating the tube, in order to reduce residues of other gases in the chamber. The growth of graphene is organized in three main steps (Figure 1.5):

1. Cu annealing in hydrogen, which eliminates all the impurities present on the surface and promotes the re-crystallization process. This step generates the enlargement of the copper crystals grain size, which are responsible for the dimension of grain size in the graphene film. Larger grain size guarantees a reduced number of grain boundaries in the Gr film, which are related to the degradation of Gr electrical and mechanical properties. [11]. In order to perform this step, the temperature is first ramped up at $16\,°C\,min^{-1}$, in a hydrogen flux. The annealing is performed for 30 minutes at 1000 °C, close to the melting point of pristine copper.

2. Graphene deposition is obtained adding in the tube a methane flux. Coming in contact with the heated copper, methane is subjected to a dehydrogenation reaction. The resulting extracted carbon rearranges in a solid phase, which is deposited on the Cu substrate, while the hydrogen exits from the tube with the gas flow. The methane flux has effect on the desired thickness for the graphene film. The process with H_2:CH_4 = 500:50 sccm (10 minutes) is used for monolayer graphene films, while with H_2:CH_4 = 10:144 sccm (30 minutes) a few-layer graphene film is obtained.

3. Cooling is the last step. Once completed the deposition step, the graphene-coated copper sample is extracted from the hot zone of the furnace and cooled in an argon flux (150 sccm) for few hours.

Under these operating conditions the size of the Cu grains and the Gr domains boundaries are in the range of hundreds microns.

1.3 BEOL integration of graphene

In the Semiconductor manufacturing, processes are organized in front end of line (FEOL) and back end of line (BEOL), depending on their positioning into the full production line. In general, FEOL includes the steps mainly related to transistor/device fabrication, while BEOL processing contains the fabrication of metal interconnects, with their dielectric

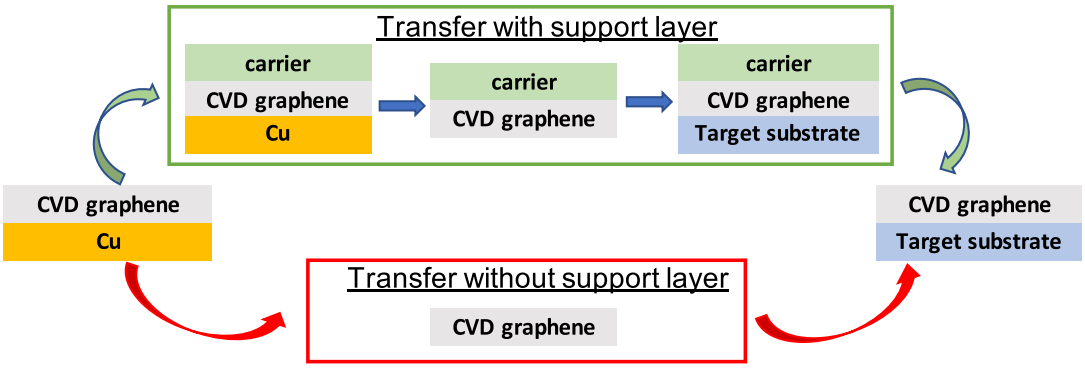

Figure 1.6: Schematic of various routes to CVD graphene on target substrates (from [5])

layers and diffusion barriers. Integration of a new material like Gr in the CMOS platform must take into account how its properties are affected by the entire process, but it's also important to evaluate the impact that this new material would have on the performances of standard devices. There is an important basic request that must be fulfilled for the integration in the silicon CMOS technology flow: the risk of cross contamination must be avoided. Therefore, if Gr is integrated during the FEOL steps, it will be placed far away from the active area of silicon devices, to avoid metal contaminations, because in FEOL high temperature processes ($\sim 1000\,^{\circ}\mathrm{C}$) are used, and the high temperature favours metal diffusion and creation of trap states in the Si bandgap, that affect device performances. Therefore, the BEOL integration approach seems to be the most safe technique. Moreover, the processing temperatures during the BEOL stages are lower ($< 450\,^{\circ}\mathrm{C}$ or $< 150\,^{\circ}\mathrm{C}$) because metals have already been deposited, therefore the thermal stress and degradation on Gr film is reduced [12].

1.4 Graphene transfer

Graphene transfer is an important step that bridges the high-quality graphene CVD grown on metal substrates to final applications. Transfer process (shown in Figure 1.6), consists in the separation (delaminating) of graphene layer from the metal, handling it and then lamination of graphene onto the silicon substrate, paying attention to its integrity. The graphene transfer should be accomplished with or without the use of a support layer. Each graphene transfer method has unique characteristics and the selection of a transfer technique largely depends on the final application.

Having in mind that the final application would be the integration of graphene in the CMOS platform, the main parameters guiding the choice of the transfer method will be low cost, scalability, reliability, high yield, and technological compatibility with the other steps of the process flow. Transfer with a support layer (typically a polymer),

permits to preserve the structural integrity of the thin graphene layer, but usually introduces surface contamination which degrades optical and electrical device performances. Unfortunately, conventional cleaning methods used in standard CMOS technology, such as oxygen plasma exposure, cannot be applied, as graphene would be etched. A certain surface cleaning of graphene should be obtained burning the residues, through a thermal annealing at 150–300 °C in reducing atmosphere [13], but it's hard to restore graphene performances to its intrinsic values.

Gr transfer without a support layer avoids the contamination from polymer and organic residues, permitting to obtain high quality for transferred graphene, but has great limitations. In fact, due to the lack of support, the very thin graphene membrane can be easily cracked after Cu removal by solution fluctuations, or by the surface tension of the etching solution. Thus, the reliability and yield for this graphene transfer method is low, and it's employed mainly for transfer of graphene membranes with reduced dimensions ($< 1\,\mathrm{cm}$) and for experimental studies.

Currently the polymer-based graphene transfer is the more reliable transfer technique for microelectronic applications, and the main limitations introduced handling graphene during transfer are kept under control.

1.4.1 Polymer based graphene transfer

Polymers are the most widely used support layer for large area graphene transfer, and are mainly responsible for the final quality of transferred graphene. Polymers are used to coat the graphene surface, with the double function of protecting and self-sustain the large graphene membrane during removal of the metal in the etching solution; and once transferred to the new substrate, the polymer is removed from graphene. In order to minimize the degradation of graphene's quality related to the transfer process, the polymer must have some important characteristics: i) flexibility, in order to assure conformal contact with graphene and the target substrate; ii) high mechanical stability, to provide sufficient mechanical support to the graphene films during and after the metal removal; and iii) must be easily removed from the graphene surface. An important parameter that regulates the final quality of graphene is the surface energy. A low surface energy is preferred for the polymer carrier, in order to have a weak adhesion force with the graphene surface and to easily remove the polymer, leaving few residues on the graphene film. On the other hand, the surface energy of the target surface should be high enough to guarantee a conformal contact between graphene and the substrate, which avoids the formation of cracks and wrinkles during the removal of the polymer. Several techniques are used to enhance the surface energy of the substrate, like treatments in oxygen plasma, or acid etching (piranha solution H_2O_2:H_2SO_4, 1:3) used to make the substrate hydrophilic; while in other cases the substrate is treated with functional groups able to render the surface more hydrophobic, inhibiting the formation at the interface between Gr and the substrate of a layer of water; or treatment are used to improve the interac-

tion with graphene, as APTES (3-aminopropyltriethoxysilane), that takes advantage of amine's affinity to carbon materials [14].

The typical steps used in polymer-based graphene transfer are:

1. spin coating of the polymer onto the graphene/Cu foil and curing at moderate temperature;
2. removal of the graphene layer from the backside of the Cu foil;
3. etching of the Cu substrate;
4. washing of polymer/Gr in deionized water for several times, followed by transfer of the polymer/Gr membrane onto the new substrate;
5. heating treatment to achieve the conformal contact between graphene and the new substrate;
6. removal of the polymer in a solvent.

For completeness, it's suitable to say that current industrial large-area transfer techniques usually rely on rolling processes, which ensure a higher production capacity, minimizing damages and structural contamination during transfer. The rolling process consists in laminate graphene and the transfer medium together, and then to laminate graphene onto the target substrates using a process based on the use of thermal release tape.

1.4.2 PMMA-assisted WET graphene transfer

PMMA (Poly-methyl methacrylate), is the most used support layer for graphene transfer and it's also the polymer mostly used in this thesis to protect graphene during the transfer process. In the following the main steps of the WET transfer process developed in this work are reported:

1. Spin-coating on one side of the as-grown CVD graphene on Cu foil with the PMMA solution in anisole. (PMMA 950 A7, MicroChem) [15].
2. Solvent evaporation from PMMA on hot-plate (200 °C, 2 minutes).
3. Cu etching in a solution of ammonium per-sulfate (PSA) in water (50g/L).
4. Rinse of the Gr membrane, replacing the etching solution with clean deionized water for multiple times, to accurately wash the Gr membrane.
5. Destination substrate is used to scoop the PMMA/graphene membrane from water, and then it's naturally dried in air overnight under fume hood at room temperature.

6. Heating treatment on hot-plate (200 °C, 2 minutes) to promote the conformal contact of Gr onto the substrate, removing trapped water residues, and reducing wrinkles and related strain in Gr film.

7. PMMA removal with solvent (vapors of boiling acetone).

Certainly, PMMA meets the first two requirements for a support layer (flexibility and mechanical support), but unfortunately the complete removal of PMMA in acetone is difficult, and some polymer's residues remain on the Gr surface, introducing a degradation in the electrical performances of transferred graphene (as higher sheet resistance and non-uniform doping). Post-transfer procedures have been developed to reduce the amount of polymer residues on the Gr surface, such as high vacuum high-temperature annealing in a mixture of H_2/Ar [13], laser treatment, [16] and plasma cleaning, but all these processes introduce defects in the graphene film. Both plasma treatment and high temperature annealing in hydrogen have been tested in this work, but they are not introduced in the flowchart for the hybrid Gr/Si devices fabrication, because they could introduce further defects in graphene, and we preferred to maintain the pristine graphene.

1.4.3 Poly(lactic acid), PLA-assisted WET graphene transfer

Aiming at reducing contamination on the transferred graphene film, the PMMA supporting layer has been substituted by a poly(lactic acid) (PLA). There are several different types of Polylactic Acid, with slightly different characteristics, but they are all produced from a renewable source, the lactic acid: $C_3H_6O_3$ (Figure 1.7), while traditional plastics are derived from nonrenewable petroleum. PLA has been selected among others polymers, because it's green and biodegradable, and at the mean time it's extremely robust, but also elastic [17], and its interaction with the graphene film is expected to be lower than PMMA, due to its lower surface energy [18]. Moreover, it can be easily removed by modest heating in ethilacetate (but also in chloroform or acetone). In particular, the amorph PDLA (poly D-lactic acid) produced by NautureWorks (product Ingeo 4060D) has been used in this work for transfer experiments. This PDLA has the component ratio L/D in the range 24:1 to 30:1, a glass transition temperature of 55–60 °C [19], and it's dissolved in ethylacetate.

PDLA films have been produced from a PDLA solution (2% and 4% wt in ethilacetate), by solvent casting (2 mL) and by spin coating (500 rpm, 60 sec), and dried up at room temperature. The PDLA thickness is extracted from optical spectroscopy measurements of transmittance and reflectance, performing simulation using the computer code *Optical* [20]. The same procedure reported in section 1.4.1 has been used, substituting PMMA with PDLA and properly optimizing the heating treatments to improve the adhesion to graphene. The samples obtained via drop casting of PDLA ($\sim 10\,\mu m$

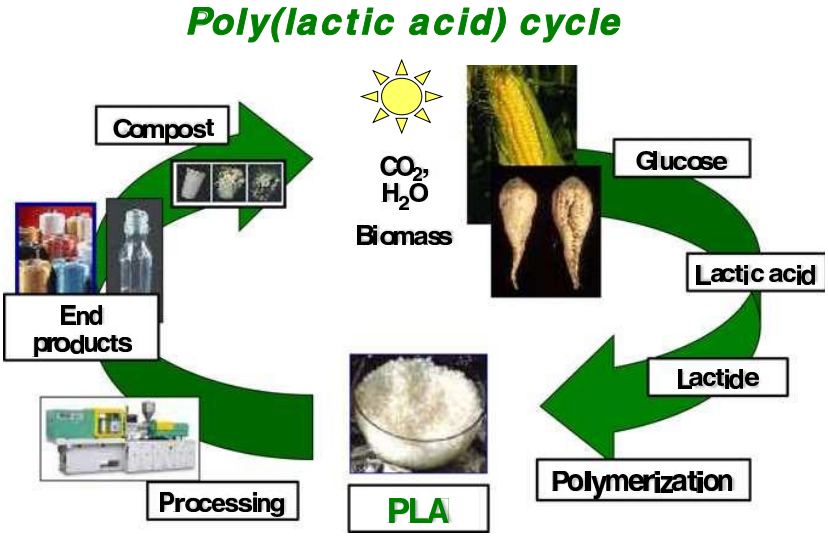

Figure 1.7: PLA life cycle with corn and sugar-beet; the biological systems use the solar energy by the process of photosynthesis (from [17])

thick), present a lot of air-bubbles after the graphene transfer. An annealing on hot-plate at 130 °C for 5 and 10 minutes is executed, in order to remove the bubbles and improve the conformal contact between graphene and the substrate. This annealing does not completely remove all the bubbles, and at the end of the process we obtain a low quality graphene film, with a lot of small holes (Figure 1.8b). The PDLA films (2% and 4%) spin-coated at 500 rpm are $\sim 1\,\mu$m thick, with high reproducibility. At the end of the transfer process, the graphene samples with spin-coated PDLA show a continuous graphene layer, with very low hole density and few polymer residues (Figure 1.8a).

1.4.4 Polymer assisted semi-Dry transfer techniques

During the WET transfer process, the graphene is extracted from an aqueous solution and put in contact with the substrate, so that some "water solution" is unavoidably trapped at the interface between the two layers. After drying and heating treatments, the most part of water is removed from the interface, but some water molecules are trapped and act as impurities, adding strain, or modifying the electronic structure of graphene and introducing doping. A semi-dry transfer method (called DRY for simplicity in this work), has been developed in this thesis, in order to minimize the introduced charge impurities during the transfer. The main steps used in the DRY transfer process are as follows:

1. Spin-coating on one side of the as-grown CVD graphene on Cu foil with the PMMA solution in anisole. (PMMA 950 A7, MicroChem) [15].

2. Solvent evaporation from PMMA on hot-plate (200 °C, 2 min).

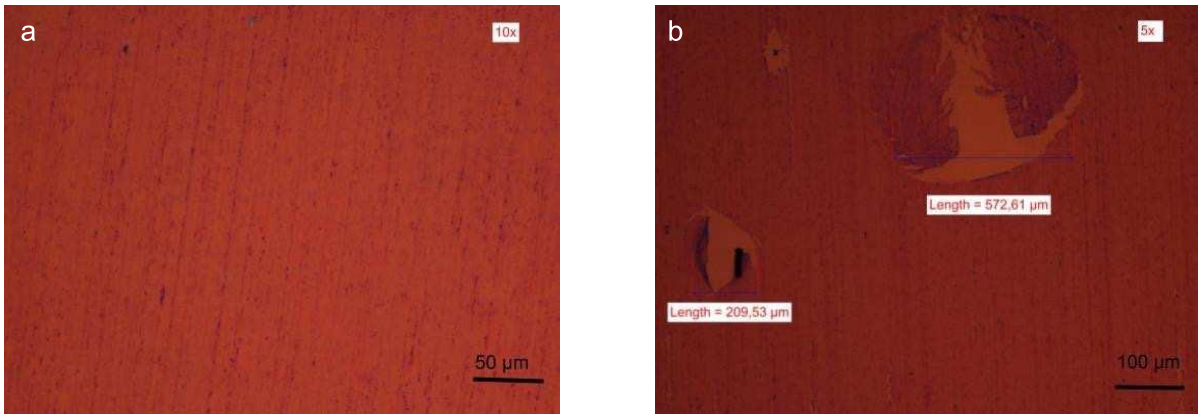

Figure 1.8: Microscope images of graphene at the end of the transfer process and after removal of PDLA, used as supporting layer. (a) Using spin coated PDLA polymer the graphene obtained is continuos, with no holes and few residues. (b) Using PDLA deposited per drop casting, the graphene film shows large areas where graphene has been removed. These holes correspond to the bubbles formed in the PDLA film. In these areas the graphene film was not in contact with the substrate, and removing PDLA the Gr film is also removed.

3. The PMMA/Gr/Cu sample is closed in a frame using a Kapton strip (75 µm thick), and leaving the back of the sample exposed to solution during etching.
4. Cu is etched in a solution of ammonium per-sulfate (PSA) in water ($50\,\mathrm{g\,L^{-1}}$).
5. Rinse of Gr membrane replacing the etching solution with clean deionized water for multiple times, to accurately wash the Gr membrane enclosed in the Kapton frame.
6. Drying overnight of the Gr membrane enclosed in the Kapton frame under fume hood at room temperature.
7. Adhesion of Gr to the Si substrate using a multiple step heating process (no use of water or solvents is required). This step promotes the conformal contact of Gr onto the substrate, reducing wrinkles and related strain in the Gr film. During heating the mechanical detachment of the Kapton frame from the Gr membrane takes place.
8. PMMA removal with solvent (vapors of boiling acetone).

The described transfer method is semi-dry, because Gr is exposed to water solution both during Cu etching and then is rinsed in water, but water or solvents are not used in the final transfer step. Anyway, some water or oxygen molecules could be adsorbed on the exposed Gr surface during the previous two steps in water, affecting its doping.

1.5 Graphene patterning

Aiming at the integration of hybrid devices based on 2D materials with large scale standard silicon technology, photolithography is the preferred patterning technique, because it's more efficient and has reduced costs than electron-beam lithography, widely used for fabrication of few nano-devices for research applications. The photolithography patterning allows the simultaneous fabrication of millions of devices, through the use of photo-sensitive resists that have to be dispensed onto graphene, and this photolithographic step must be repeated several times, at least to fabricate contacts, and for graphene patterning. Inevitably, the graphene surface is one more time contaminated by resist residues, not removable with standard cleaning procedures used for Si device (like oxygen plasma or etching in stripper solution, or harsh cleaning). Therefore, efforts for the development of reliable methods to obtain clean graphene surfaces are of great importance. Thermal annealing is widely used to remove resist residues. Heat treatments are usually performed in clean vacuum or in H_2 or Ar/H_2 atmosphere, at 200–300 °C, and are effective to reduce the contaminations [21]. As an alternative, it's possible to remove residual photoresist using a resist remover whose main compound is ethyl-2-pyrrolidone [14].

1.5.1 Photolithographic graphene patterning @ IMM

The main issue when fabricating graphene devices is to develop reliable methods in order to preserve the integrity of graphene surfaces, with low resist residues, because they can act as external scattering centers degrading the electrical transport properties of graphene. With this aim, different photoresists have been tested for the fabrication of graphene devices with optical lithography technique. Among them, best results have been obtained with PMMA (already used for graphene transfer), and with HPR-504. Both the photolithographic procedures described use low cost resists, standard mask aligner and standard exposure system for simultaneous fabrication of thousands of graphene devices.

Photolithography using PMMA polymer

PMMA is a transparent thermoplastic that can be used as positive resist for various radiation sources, such as deep U-V lithography, electron beam lithography, or x-ray lithography. Even if PMMA is usually patterned using wavelength shorter than 240 nm, patterning at 254 nm has also been demonstrated [22]. The interest in the 254 nm wavelength lies on the fact that it's particularly inexpensive to produce, being 254 nm the strongest peak in the spectrum of low-pressure mercury vapor lamp. Radiation sensitivity of PMMA is due to polymer chain scissions caused by the absorbed radiation. DUV exposure creates scissions in the polymer backbone, which decreases the average

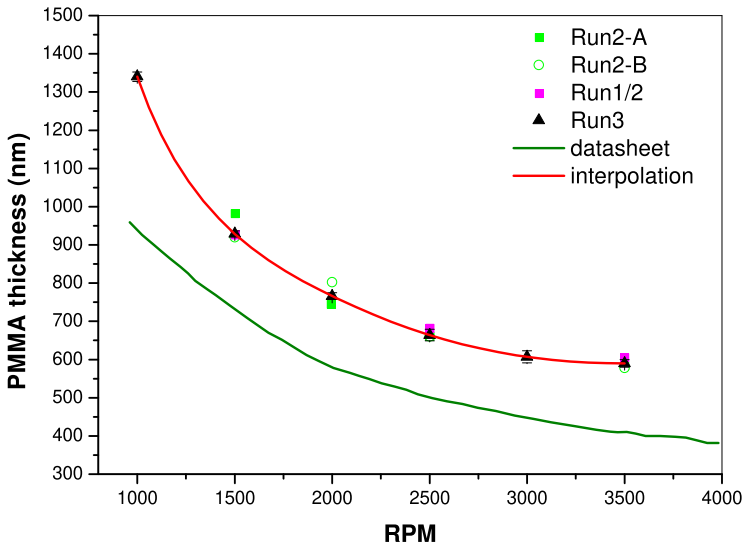

Figure 1.9: PMMA 950 A7 thickness versus spin speed. PMMA thickness is extracted from optical spectroscopy measurements of transmittance and reflectance. The reproducibility obtained on 4 runs is good, standard deviation is $< 5\%$.

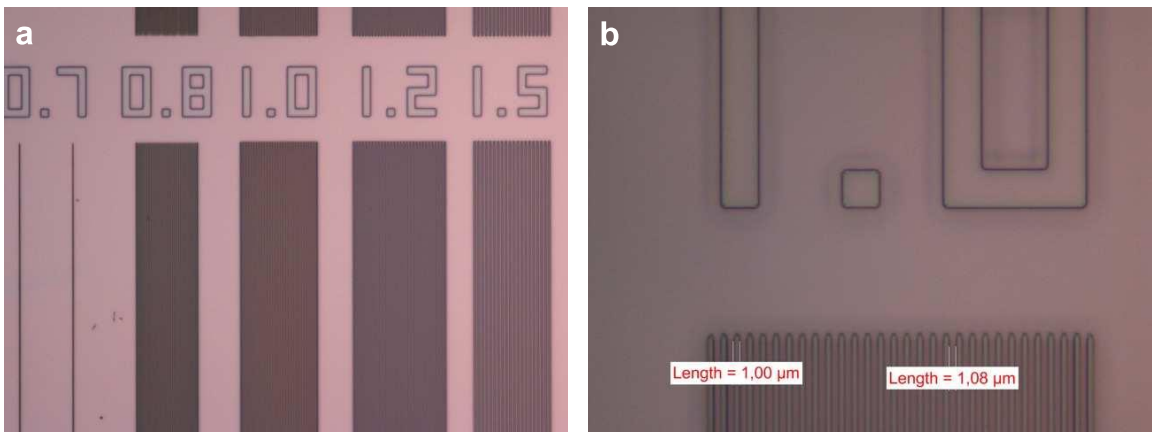

Figure 1.10: SEM images for PMMA lines lithographically defined with the total dose of 22500 mJ cm^{-2}, and developing in MIBK : IPA solution (1:3) at room temperature (22 °C) for 80 s. (a) PMMA lines down to 0.8 µm width can be obtained; (b) detail for well-defined 1 µm large lines, with 1 µm distance.

chain length and thus increases solubility. In this thesis PMMA 950 A7 in anisole (Microchem) has been used. PMMA is spun on the substrate; several samples have been prepared in order to verify the reproducibility of the deposition process and to define the relation between PMMA thickness and spinning velocity (Figure 1.9). PMMA thickness is extracted from optical spectroscopy measurements of transmittance and reflectance, performing simulation using the Optical software [20].

PMMA samples were exposed using low-pressure mercury vapor lamp (power of 1000 W), mounted on mask aligner Süss MA6, which provides non-collimated radiation with a nominal power of $4\,\mathrm{mW\,cm^{-2}}$ and a spectrum whose strongest peak is at 248 nm. Different PMMA samples have been prepared to explore different exposure doses (or times), finding that the total dose required for correct exposure of the PMMA resist is $22500\,\mathrm{mJ\,cm^{-2}}$. After exposure, samples were transferred to a developer bath with a solution of methyl isobutyl ketone (MIBK) and isopropanol (IPA) 1:3 at room temperature (22 °C). At the end, the development was quenched in an IPA bath at room temperature (22 °C) for 6 min, after which the samples were sprayed with IPA for another 10 s, and then blown dry with N_2. At the end of the photolithographic process, PMMA is removed in hot acetone. The full process developed for photolithographic patterning using PMMA as photoresist consists of the following steps:

- Dehidration in oven: 80 °C, 30 min.
- Spinning of PMMA 950k, molecular weight 7% in anisole (from Microchem): 2500 rpm for 45 sec.
- Prebake in hot-plate: 180 °C 70 s (PMMA thickness is ~ 750 nm)
- Exposure with Süss MicroTec mask aligner MA6 (mounting a low-pressure mercury vapor lamp) at wavelength of 248 nm, with a total dose of $22500\,\mathrm{mJ\,cm^{-2}}$.
- Developing in MIBK : IPA solution (1:3) at room temperature (22 °C) for 80 s.
- Rinse in IPA bath for 6 minute to quench the development.
- Wafers are blown dry with N_2 gun.
- Etching to remove the defined layer.
- PMMA removal in hot acetone and rinse in isopropyl alcohol (IPA).

Lithographic test strucures have been used to define the right exposure dose and developing conditions for PMMA, showing that the minimum feature size achievable with this process is 0.8 µm, and PMMA matrices with lines width of 1 µm , and separated by 1 µm, are well defined (Figure 1.10).

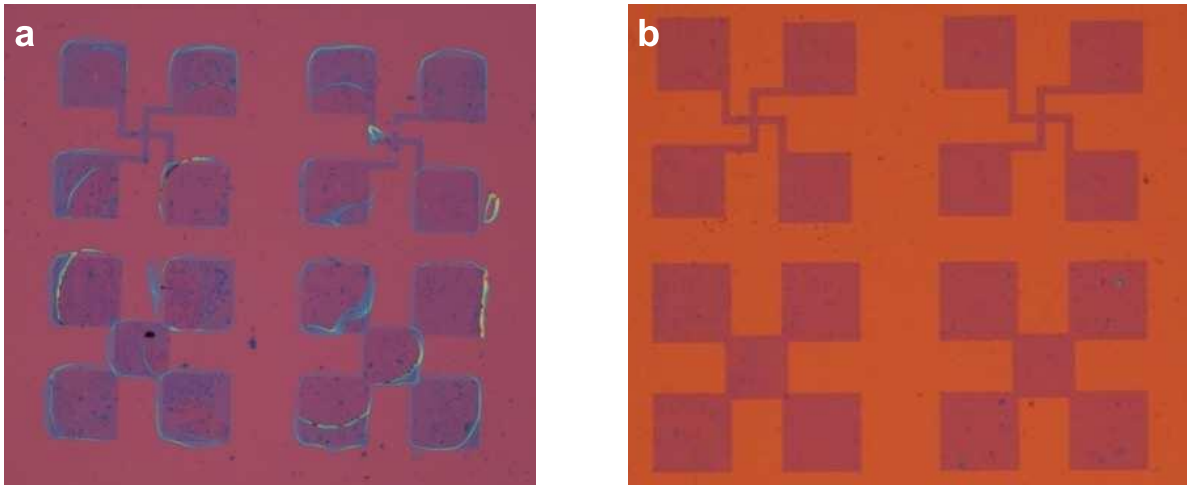

Figure 1.11: Graphene structures patterned using HPR–504 resist. Resist removal in hot acetone (a) is not effective and a lot of resist residues affects the graphene structures at the edges; (b) a modified exposure process permits the complete resist removal, obtaining clean graphene structures.

Photolithography using HPR–504 photoresist

HPR–504 (Fujifilm) is a well-known positive photoresist for g-line exposure, usually used in IMM for standard photolithographic processes in CMOS technology. The minimum achievable feature size is 2 µm, compatible with minimum dimension of the graphene structures. The photolithographic process with HPR–504 used on graphene is straightforward and identical as in conventional photolithography, and shorter compared to the process developed for PMMA. The HPR–504 resist (1.1 µm thick) demonstrates good adhesion properties on graphene samples, and good selectivity in the oxygen plasma process performed to etch graphene. The main issue to investigate is the effect of resist's residues on graphene electrical performances and how to remove these residues from the graphene surface after patterning. In standard Si technology the HPR series resists can be effectively stripped using Fujifilm Microstrip 2001, which is an alkaline photoresist stripper based on pyrrolidone. Unfortunately, Microstrip is aggressive, causing detachment of graphene from the substrate. As an alternative, resist can be removed using acetone, but this process is not clean and leaves a lot of resist residues on the edges of the graphene structures (Figure 1.11a). In order to apply the photolithographic process based on HPR–504 to graphene films, the standard procedure has been modified. In particular, the resist is exposed twice, the first time with the right dose of light to lithographically define the structures with proper geometrical dimensions; then, after the development step, the resist is exposed again using a high light dose (no mask is required). This second exposure is introduced to favors its removal after etching using

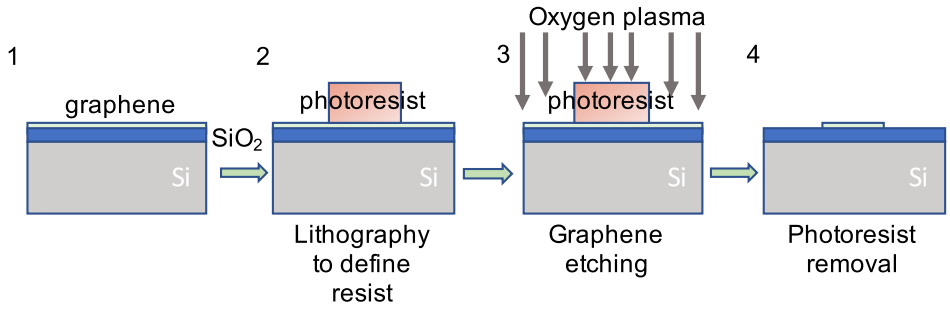

Figure 1.12: Schematic of the photolithographic fabrication of graphene structures: 1) graphene is transferred onto the oxidized Si wafer; 2) PR is deposited onto Gr and photolithographically exposed; 3) plasma etching of graphene in oxygen; 4) removal of the PR and cleaning of the graphene surface.

the developer solution Microposit 354 (Shipley), that completely dissolves the resist, minimizing the residues on graphene film (Figure 1.11b). The tests executed have shown that the double exposure does not modify HPR–504 resistance during the oxygen plasma process for graphene etching, and an etching rate in plasma of $\sim 60\,\mathrm{nm\,min^{-1}}$ has been found, fully compatible with the process used.

1.5.2 Graphene Patterning

The standard photolithographic process described in the previous paragraphs is used to pattern the graphene films, that is to fabricate graphene structures with defined geometries and dimensions. The process used is identical as in conventional photolithography:

- a photoresist is spin-coated onto the graphene surface, followed by a baking step;
- photoresist is exposed to UV light with a patterned mask and developed, so that the exposed photoresist is removed (PR used is positive);
- the graphene layer to be removed is etched using a dry etching process in oxygen plasma, while photoresist acts as mask, protecting the underlying graphene during etching;
- after etching, the photoresist is removed and patterned graphene structures are obtained on the substrate.

A schematic of the photolithographic process used to define graphene structures is shown in Figure 1.12. For graphene patterning both PMMA and HPR-504 resists have been used.

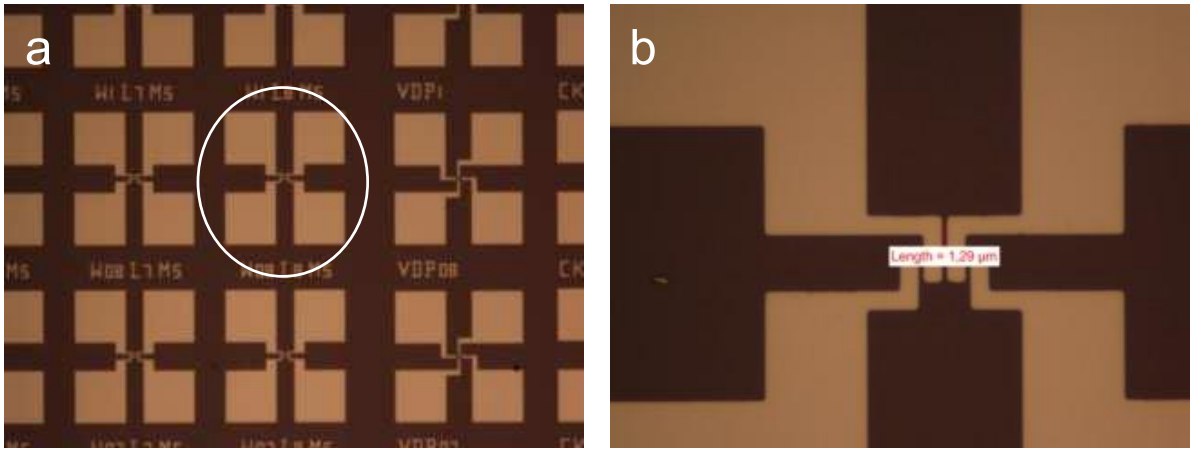

Figure 1.13: Metal pads and stripes defined via lift–off process using PMMA resist (a); magnified image of the structure in the white circle in (a), is shown in (b). Distance between the two metal lines is 1.29 µm (mask separation is 1 µm).

1.6 Contact to graphene

The small density of states in graphene near the Dirac point is responsible of the Fermi level shift in graphene for any charge transfer. Contacting Gr with a metal, the different work functions of the two materials causes a charge transfer through the interface, changing the electrical doping in graphene and shifting its Fermi level. The graphene Fermi level moves upward (towards the Dirac energy), when electrons move from metal to graphene, while when holes move from metal to graphene, its doping is increased and the Fermi level shifts downward.

The electrical contact to graphene is fundamental for fabrication of any device using graphene, and requires reproducible formation of low contact resistance and the use of CMOS compatible processes. As a general rule, the contact resistance must not introduce any significant contribution to the total device resistance.

Nowadays, is generally accepted that contact resistance to graphene is mainly influenced by the metal itself, because of the work function difference and of the bonding strength between metal and graphene (which is a weak connection, through van der Waals interaction, due to lack of dangling bonds in graphene), as well as by impurities and contaminations located at the interface, that for CVD graphene mainly consists of polymer residues coming from the transfer process. But also the geometries at the interface have an important role in charge transfer [23, 24]. As reported by Anzi [24], the contact resistance between metal and Gr can be reduced introducing holes in the contact area of graphene under the contact. Introducing holes, the edge contact between metal and graphene is grown, enhancing the carrier injection in graphene through the edges of the holes. Anzi tested several metals in his work, and the best results are obtained for

Au contacts: $R_c = 200\,\Omega\,\mu m$ for conventional top contacts, and $R_c = 23\,\Omega\,\mu m$ for holey contacts.

Taking advantage of the above studies, gold has been selected in this work as metal to contact graphene devices. Au film is deposited by RF sputtering at room temperature in a MRC 8622 RF system, working with a plasma power of 180 W. The technological process for fabrication of metal stripes and pads on graphene is based on the lift-off process, using PMMA as photoresist (the process is explained in section 1.5.1). PMMA has been used as resist for three main reasons: i) metal lines with dimensions and separations can be easily obtained using the photolithographic process based on PMMA resist; ii) the procedures to clean the graphene surface at the end of the photolithographic step are well known, because PMMA is also used for the graphene transfer to the silicon substrate; iii) negative photoresists usually used in our lab for the lift-off process request solutions (developer or remover) that are not compatible with graphene. Figure 1.13a shows the metal structures fabricated. A separation beween two metal stripes of 1.3 µm can be obtained using PMMA (Figure 1.13b).

Fabrication of transmission line (TLM) structures to measure the contact resistance arising at the metal/graphene interface are under development. Anyway, for large dimension devices, as those fabricated in this thesis, the contact resistance would not be an issue.

1.7 Graphene characterization

Considering the introduction of graphene in the Si platform for hybrid device fabrication, two are the main issues in defining the graphene quality:

1. to evaluate its electronic properties before fabrication of graphene devices, because transferred CVD graphene might show many defects and holes;

2. the investigation of how the graphene properties modify, as an effect of the technological steps executed along the device fabrication process.

A lot of attention must be put at every step, in order to define the starting quality of graphene, and to verify if these properties are preserved or how they have changed. In the following paragraphs the methods used to investigate conductivity, carrier density and mobility as key parameters for the graphene quality, will be presented. All these parameters can be derived by measurements of four-terminal electrical resistance, performed on planar samples, having 4 electrodes on the surface. The four-terminal method can be applied to CVD graphene transferred on an insulating or high resistivity substrate, and assumes a uniform and isotropic carrier mobility and carrier density of the sample. The electrical characterization of graphene has been performed following the guidelines produced in the framework of the European project GRACE [25]: Developing electrical characterization methods for future graphene electronics, [26].

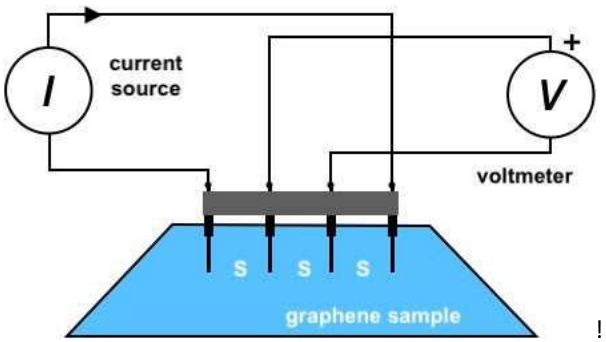

Figure 1.14: Schematic representation of the 4PP in line method.

1.7.1 Graphene sheet resistance

There are two main techniques for measuring the sheet resistance of thin films, both based on four-terminal electrical resistance.

In-line 4-point probe (4PP)

The 4PP method consists in four probes placed in a linear arrangement on the sample. To apply this method, three conditions must happen: i) the distance between probes (s) should be negligible compared to the sample dimensions; ii) the distance between the probes and the edge of the sample should be large compared to s (at least one order of magnitude larger), so that the edge effect on the electric field in the sample can be neglected; iii) the thickness of the measured layer must be small compared to its lateral dimensions (always true for graphene films). During the measurement, a current I is applied through the external probes, while the voltage drop V is measured between the internal probes. Sheet resistance is calculated using equation 1.2 for the ideal case, and introducing a correction factor to account for the real geometric conditions [27].

$$R_s = \frac{V}{I} 4.5324 \tag{1.2}$$

Van der Pauw method

The van der Pauw method is based on the measurement of two transresistances, performed on four contacts on the sample boundary. The transresistance of the sample, measured in two different configurations, is related to the sheet resistance by means of a mathematical theorem derived from conformal mapping theory [28].

From measurements performed in the configurations reported in Figure 1.15, the two

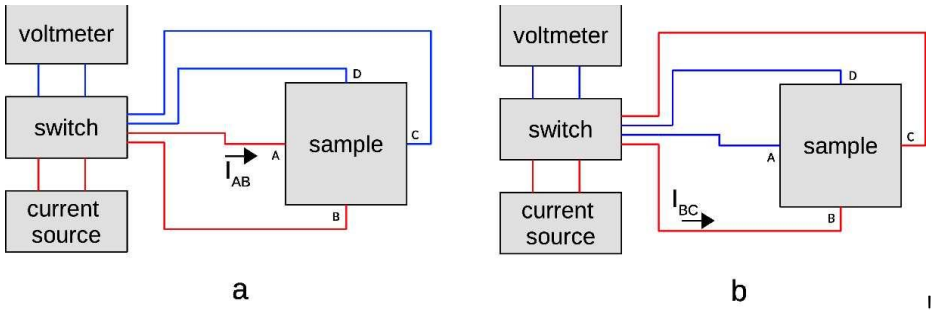

Figure 1.15: Schematic setup for the van der Pauw measurement, with the two configurations used for the measure of the transresistance $R_{AB,CD}$ (a) and $R_{BC,DA}$ (b). Red lines indicate the current flow, and blue lines the terminals used for voltage measure.

four-terminal transresistances are obtained:

$$R_{AB,CD} = \frac{V_{CD}}{I_{AB}} \tag{1.3}$$

and

$$R_{BC,DA} = \frac{V_{DA}}{I_{BC}} \,. \tag{1.4}$$

Considering the case of a symmetric sample geometry, the sheet resistance is expressed as:

$$R_s = \frac{\pi}{\ln 2} \frac{R_{AB,CD} + R_{BC,DA}}{2} \,. \tag{1.5}$$

A correction factor must be introduced in equation 1.5 to account for non-ideal configurations [29, 30, 31].

1.7.2 Graphene carrier density and mobility

The measure of carrier density and mobility in graphene is performed using the van der Pauw structure. This method has been selected because no fabrication steps are required, and samples must only have uniform material, with small ohmic contacts at the edges. Because no fabrication steps are required (graphene is directly transferred on the silicon substrate, where metal contacts have been already fabricated), this method permits to define the electrical properties of "pristine" graphene, immediately after its transfer on the desired substrate. Measurements of carrier density in graphene are based on the Hall effect. This method consists in the generation of a potential difference (Hall voltage, V_H), across a conductor with current I_B. Upon application of a perpendicular magnetic field, the charge carriers are deflected, due to the Lorentz force (see Figure 1.16). The Hall coefficient is expressed as [32]:

$$R_H = \frac{V_H t}{I_B B} = \frac{t}{q n_{3D}} = \frac{1}{q n} \,, \tag{1.6}$$

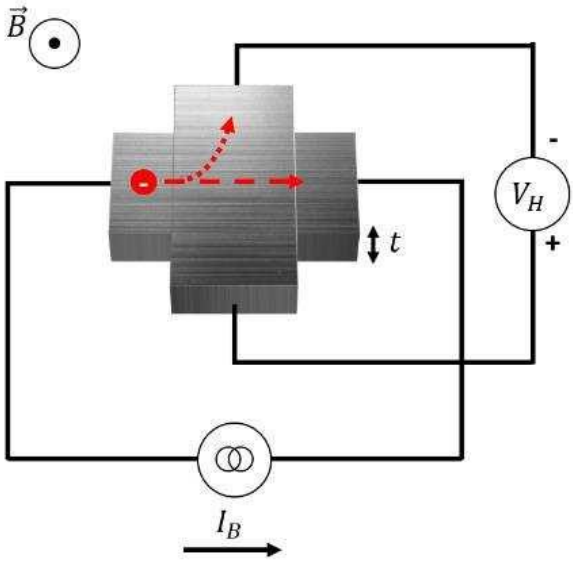

Figure 1.16: Setup for Hall effect measurement on n-type material. The charge carriers (electrons) are deflected (red curved arrow) due to the applied perpendicular magnetic field, and a negative voltage is generated.

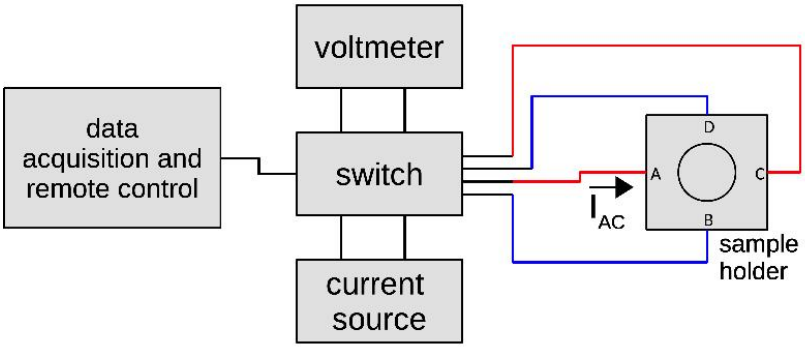

Figure 1.17: Scheme of the van der Pauw measurement setup. The sample holder (square) must be put in a permanent magnet for Hall measurements.

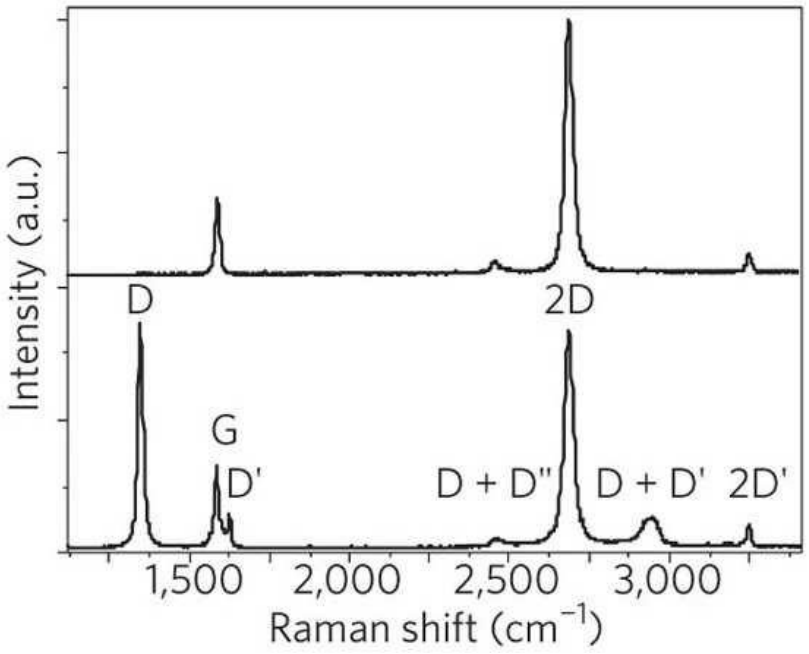

Figure 1.18: Raman spectra of graphene showing the main Raman features for pristine (top) and defected (bottom) graphene. The main peaks are labeled. [33].

where n_{3D} is the carrier concentration for the measured material with thickness t, and q is the elementary electronic charge. In this case, the measured material is graphene (a 2D material), therefore $t = 1$ and n is used. As a convention, the Hall voltage is negative for n-type materials, and positive for p-type ones. Because the values of I_B and V_H are known, the carrier concentration for the graphene layer is obtained from Equation 1.6.

The carrier mobility in graphene is obtained through the four-terminal resistance measure, with and without the magnetic field. The sample transresistance $R^0_{AB,CD}$ is measured applying a bias current I_{AC} and measuring the Voltage V_{BD}. Then the Hall effect is induced applying the magnetic field B, and the sample transresistance is measured again (Figure 1.17). The carrier mobility is given by:

$$\mu = \frac{\Delta R}{B R_s} \tag{1.7}$$

where ΔR is the transresistance difference due to the Hall effect, B is the intensity of the magnetic field and R_s is the sheet resistance.

1.7.3 Raman Spectroscopy

Raman spectroscopy is largely employed as characterization technique for graphene and carbon-based materials. This technique is used to determine the number and orientation

of layers, as well as the strain, doping, and the distance between defects, as a measure of the amount of disorder. Without entering in details in the principles behind Raman spectroscopy, and of how the different vibrational modes are originated, the main features of the raman spectrum for CVD graphene will be highlighted. The Raman spectrum of graphene has three distinct peaks [34]: the D peak at 1350 cm^{-1}, the G peak at 1580 cm^{-1} and the 2D peak at 2700 cm^{-1} (see Figure 1.18), which can be used to evaluate the quality of graphene samples. The G peak is due to an in-plane vibrational mode, not affected by defects; the D peak only appears in presence of defects, and it's strictly correlated to the amount of defects in the graphene film; the D' peak is located at slightly higher shift than the G peak and requires a defect to become activated; finally the 2D peak accounts for the amount of carbon in graphene with no defects in proximity. In the spectrum of high-quality and defect-free graphene, the 2D band is expected to have higher intensity compared to G band. Moreover, the I(D)/I(G) ratio can be used to calculate the mean distance between defects. This model has been proven valid for point defect evaluation in large ($\gg 30$ nm) graphene crystals, for excitation lines in the visible range [35].

$$\frac{I(D)}{I(G)} = (1.8 \pm 0.5) \times 10^{-9} \frac{\lambda^4}{L_D^2} \tag{1.8}$$

where L_D is the mean distance between defects in the graphene film and λ is the Raman wavelength (in nanometers). Equation 1.8 can be used to estimate the level of induced damage in the graphene film. Moreover, the intensity ratio $I(2D)/I(G)$ is used to identify the number of graphene layers. In particular, for high quality (defect free) single layer graphene, this ratio is 2, while it reduces for few layers graphene film. As a result, a Raman spectrum is a very useful technique for quality control, and for comparing different growth processes or samples used by different research groups.

1.7.4 Characteristic of the graphene films used in this work

The technological process flow that leads to graphene devices fabrication is complex, and consists of several steps which may modify the graphene properties. As already stated, any added step requires the control of graphene quality, in order to evaluate its effect. But it's also important to evaluate the properties of pristine graphene, in order to have a first insight of the quality of graphene, which guide the selection of graphene with the best quality for further fabrication processes. In this work, the following aspects have been investigated:

- Carrier concentration and mobility of transferred graphene. These parameters have important impact on the graphene Fermi level and on conduction in graphene lines, and will be used as benchmark to select the graphene deposition for Schottky diodes fabrication.

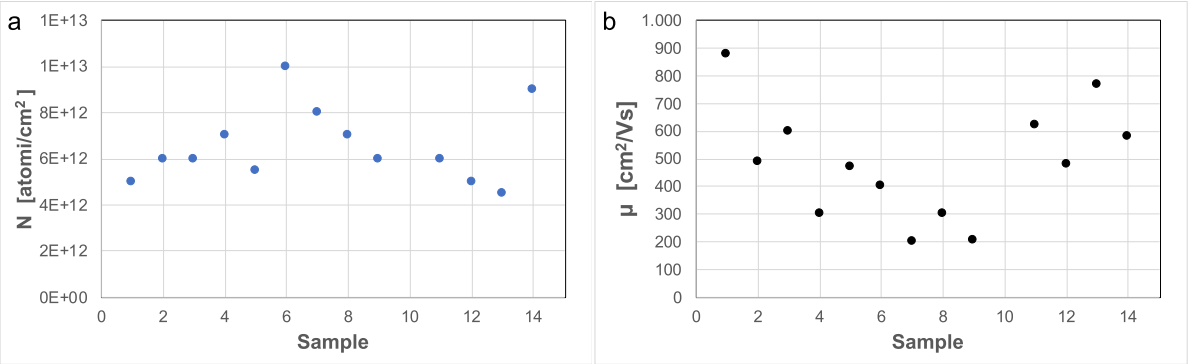

Figure 1.19: Magneto-transport measurements (Hall effect) of graphene samples in the van der Pauw geometry: a) hole carrier concentration, b) mobility. Measurements are performed in ambient and at room temperature.

- Conductivity properties of graphene. In fact, photolithographic steps could introduce contaminations, the etching steps could alter the graphene structure, and deposition of layers on top of graphene could introduce defects, altering graphene electrical properties, and severely affecting the performance of final devices.

Electrical characterization of graphene

For a rapid characterization of graphene on extensive area (typically at wafer level), standardized electrical measurements would be very useful, permitting the extraction of many important parameters, such as carrier concentration and mobility, sheet resistance, and Schottky barrier or Fermi level. The van der Pauw method is a very powerful technique, that permits to perform extensive and high throughput characterization of graphene, and has been used to extract information on the following aspects.

Carrier concentration and mobility of transferred graphene Carrier concentration and mobility have been measured for different graphene samples after transfer, and are reported in Figure 1.19 (numbers on the x-axis represent graphene samples obtained from different deposition processes). Each point in the graph is the average of 5 measurements executed in ambient conditions, at room temperature. Hall measurements can be executed also in vacuum and at higher temperature, to study the effect of the desorption of water and oxygen molecules from the graphene surface on the electrical parameters. We can notice that the carrier concentration for our CVD graphene samples ranges from 0.6 to $1 \times 10^{13}\,\mathrm{cm}^{-2}$, a quite common value; while the value obtained for mobility is low and has a large spread, varying from 200 to $1000\,\mathrm{cm}^2\,\mathrm{V}^{-1}\,\mathrm{s}^{-1}$. The mobility of graphene is defined as the ratio between the graphene conductivity (σ) and the carrier charge

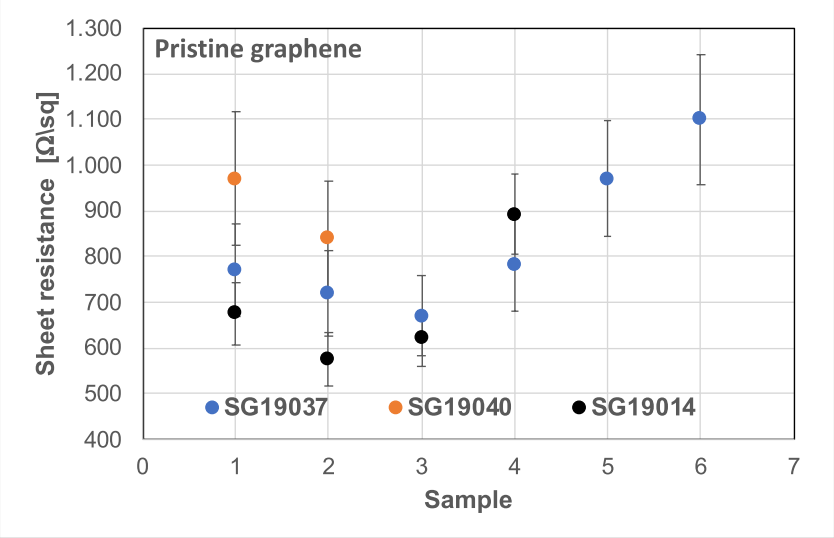

Figure 1.20: Comparison of the sheet resistance obtained for three different graphene deposition. For each sample is reported the average value of R_s obtained with 4PP measurements. Each sample consists of graphene transferred on oxide and not patterned.

density (N) [36]:

$$\mu = \frac{\sigma}{qN} = \frac{1}{R_s q n} \tag{1.9}$$

where q is the elementary electron charge, n is the carrier concentration in graphene and $1/R_s$ is the sheet conductance of graphene, because for a two-dimensional material the conductivity coincides with the sheet conductance. Therefore, $\mu \propto \frac{1}{R_s n}$, and mobility is high for reduced carrier density (= reduced graphene contamination) and low sheet resistance (high quality graphene with reduced defects and overgrown). It's important to notice that graphene carrier concentration plays an important role in determining the formation of the Schottky junction with low doped silicon, because the polarity of P-doped graphene would flip as a result of contact formation [37]. In particular, considering the Gr/Si junction fabricated in this work, the graphene carrier concentration must be $\sim 10^{13}\,\mathrm{cm}^{-2}$, and this is the parameter that guided the choice of graphene to be used for Gr/Si junction fabrication. Moreover, mobility in graphene plays an important role for carriers that move along the graphene foil, because is responsible of their velocity, but for vertical Gr/Si junctions carriers move perpendicularly to the graphene foil, and there is growing evidence that charge transport across the 2D-3D Schottky junction is mainly determined by the electronic properties of the 2D material [38]. In particular, current flow across the vertical Gr/Si Schottky junction can be expressed using a constant related to the electronic properties of graphene, where mobility is not present [39].

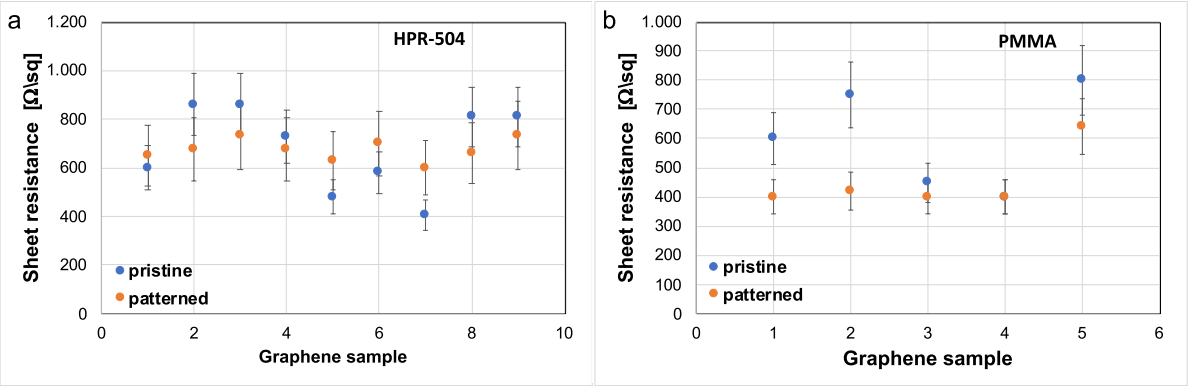

Figure 1.21: Sheet resistance for pristine and patterned graphene using (a) HPR-504 resist, and (b) PMMA.

Uniformity of graphene quality Measurements of sheet resistance are executed at room temperature and in ambient, with $RH \sim 45\% - 65\%$. Graphene foils from different CVD deposition, with dimensions of 2x3 cm^2, have been used. Figure 1.20 shows the sheet resistance obtained for pristine graphene (transferred and NOT patterned) with 4PP method. Measurements refer to three different CVD deposition (SG19014 – SG19037 and SG19040), and samples are obtained transferring different portions from the CVD grown graphene on Cu foil. Each point in Figure 1.20 is the average of 20 measurements; the obtained standard deviation on each sample is $\sim$ 13%. Therefore, each value in the graph returns a global mediate conductivity for each graphene sample. Within this framework, information of the inhomogeneity in R_s for a certain CVD deposition can be extracted from Figure 1.20. In particular, considering the deposition SG19037, six samples of transferred graphene have been fabricated and measured, obtaining a quite large distribution for the values, spanning from 660 Ω/sq to 1100 Ω/sq. And a similar situation is obtained also for the other depositions SG19040 and SG19014. Thus, based on these results, it's possible to say that the graphene films grown in our CVD system present quite high inhomogeneities, probably related to gas flow turbolence along the tube, confirming the relevance to characterize the graphene film prior to its use in device fabrication, in order to be aware of the electrical parameters of the graphene foil that will be used.

Comparison between PMMA and HPR-504 The sheet resistance measured on lithographically patterned structures is compared to values previously obtained for pristine transferred graphene. The comparison would give comprehension and awareness of each single process. In particular, the 4PP measurement permits to measure the graphene sheet resistance immediately after transfer, while patterned van der Pauw geometries give information on distribution and uniformity of sheet resistance after the

performed fabrication process (photolithography, layer deposition, etching, etc).

Changes in graphene sheet resistance R_s related to the photolithographic process, are reported in Figure 1.21. In this case, each graphene sample refers to a different CVD deposition (the numbers reported on x-axis). Each value of sheet resistance reported in the graphs is the average of ~ 20 measurements on each sample; the standard deviation is $\sim$ 15–20%.

Figure 1.21b shows that the graphene structures are characterized by a lower sheet resistance when PMMA is used for patterning. Using HPR-504 resist (Figure 1.21a), the sheet resistance values obtained on the different samples for pristine and patterned graphene, are inside the standard deviation, and half samples show reduced R_s, while the remaining half has increased R_s. Results obtained for PMMA could be explained considering the effectiveness of resist removal: additional deposition of PMMA for the photolithographic process, would probably improve the dissolution of residues from previous transfer step, both during removal of PMMA in the patterning step and in the following cleaning process. The results obtained for samples patterned with HPR-504 are not decisive, and we can only say that the use of HPR-504 should introduce limited changes in graphene sheet resistance.

Raman analysis of transferred graphene

The Raman spectra of graphene reported in the thesis were largely acquired using a Renishaw InVia microspectrometer, connected to the optical microscope Leica DMLM (objectives: 5x, 20x, 50x). Two excitation sources are available: laser Ar^+ (514.5 nm), laser diode (785.0 nm). The spectral resolution using the 50x objective is $2\,cm^{-1}$ for the laser diode, and $1.5\,cm^{-1}$ for the laser Ar^+. Spot dimensions are related to the applied power. For the 785 nm laser the spot is a rectangle, and working with 10% power the spot is $\sim 2\,\mu m$ width and $\sim 15\,\mu m$ length; while for the 514.5 nm laser the spot is circular, and working with 10% power the diameter is $\sim 2\,\mu m$. Concerning the method used for Raman peak fit, the D, G and 2D bands of Raman spectra were fitted by using a multi-peaks treatment based on the convolution of Lorentian single peaks. For the G band fitting a double peak (G and D') convolution was used. For the 2D band a multi-peaks convolution (D+D", 2D and D+D') was considered, but for our samples mainly the D+D" and 2D peaks were detected. The system used in this work for Raman analysis does not permit to perform maps on large areas, because no automated stage is integrated. In particular, the information obtained from a single Raman measurement refers to an area of few microns, and it's strictly related to the measured area. In this operating condition, Raman analysis should be used to extract a general information on the presence of defects in transferred graphene layer, but it's not possible to characterize the whole foil, evidencing if the graphene sample has areas with different number of layers, or the distribution of defects. Figure 1.22 shows the typical spectrum obtained for our graphene, sample SG19037, transferred onto an oxidized silicon substrate. The

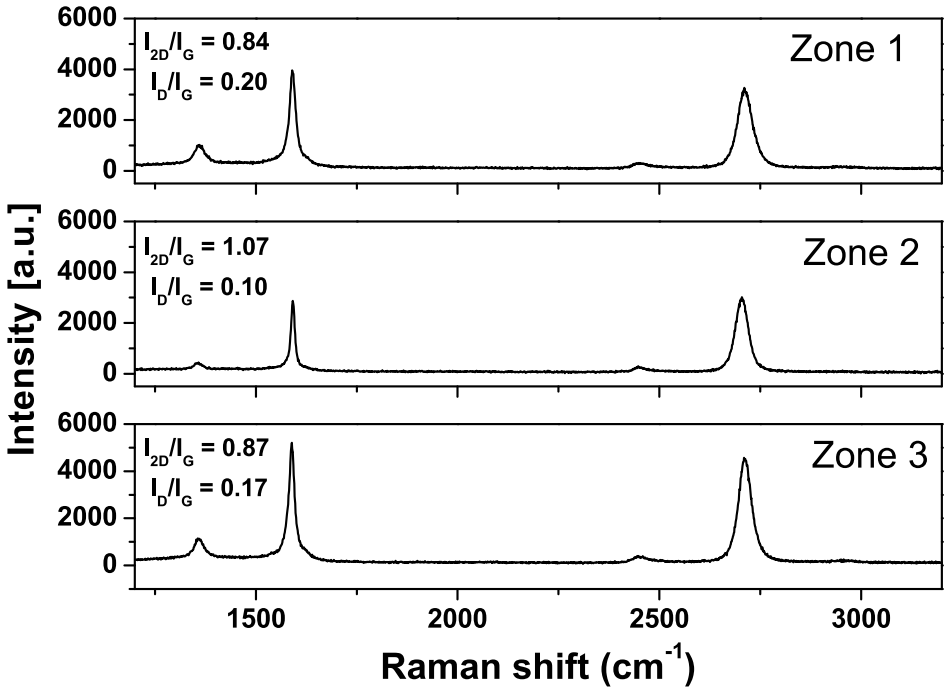

Figure 1.22: Raman spectra for SG19037 transferred graphene. The D, G and 2D bands are clearly evident. Spectra are taken with a laser working at 488 nm.

three measurements, performed in the center (zone 2), and near the edges (zone 1 and 3) of the graphene sample, show a peak D related to defects introduced by the transfer process. A small D' peak is also present at 1625 cm^{-1}, forming a unique peak with the G one. An estimation of the mean distance between defects is obtained from the ratio $I(D)/I(G)$ (Equation 1.8), obtaining 32 nm for the central region, which reduces to 23 nm near the edges (a quite low value, typical values obtained on other graphene samples are around 50 nm). The ratio $I(2D)/I(G)$ is ~ 1, indicating that the measured sample is a few layer graphene.

Chapter 2

Grafene-based device fabrication and characterization

Introduction

Introducing graphene into complementary metal oxide semiconductor (CMOS) technology, for the development of new and innovative graphene/semiconductor hybrid devices, requires a good understanding of the mechanisms which take place at the graphene and semiconductor interface. Graphene can form junctions with 3D or 2D semiconducting materials which have rectifying characteristics and behave as excellent Schottky diodes. Graphene-silicon junction (GSJ) requires a simple fabrication process, and it's a convenient platform to investigate the electronic properties and device transport mechanisms, and to study the physics occurring at the interface between a 2D and a 3D material, as well as between a zero and a definite bandgap system. The challenge in GSJ fabrication is the ability to establish an intimate contact between graphene and silicon, avoiding chemical-structural modifications to the semiconductor and simultaneously preserving the peculiar properties of graphene. As for conventional metal/semiconductor diodes, impurities and defects at the interface may significantly alter the I-V curve. Additionally, the low density of states close to the Dirac point, makes the graphene Fermi level extremely sensitive to the amount of carriers injected into or from the semiconductor, determining a tunable Schottky barrier height (SBH), which in turn controls the current-voltage relationship of the GSJ. These features make the GSJ a great platform for the study of interface transport mechanisms. Moreover, GSJ are key elements of many graphene-based devices like solar cells [40], photodetectors [41, 42], biological sensors [43], and also the semiconductor industry is largely interested in these heterostructures to replace ultra-shallow doped junctions in modern CMOS technologies and for high frequency applications.

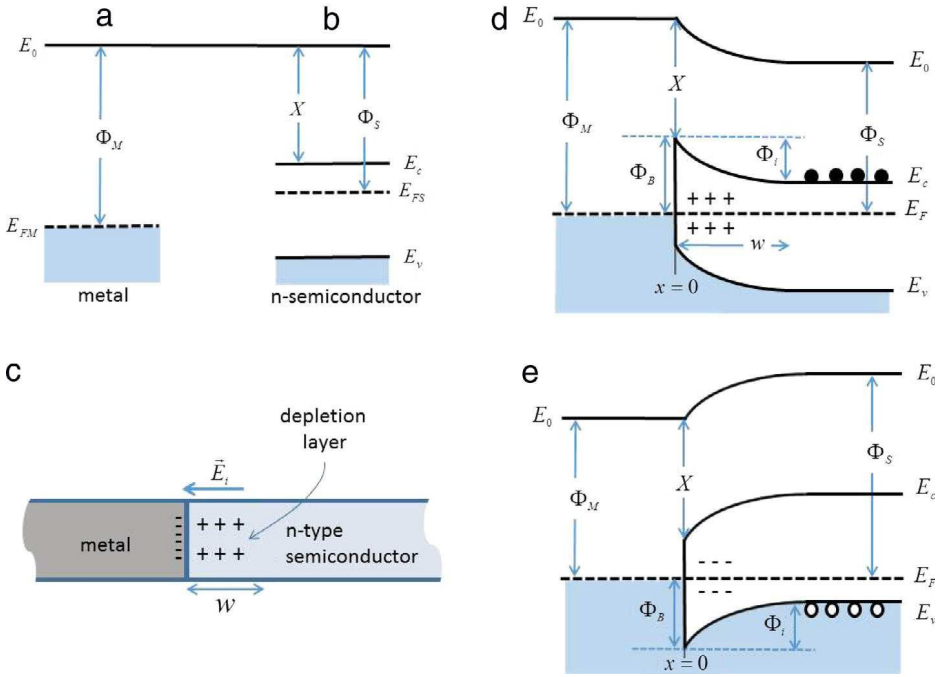

Figure 2.1: Schottky diode formed by a metal with high work-function, in contact with a lightly doped semiconductor (c); (a) metal with work function Φ_M and fermi energy E_{FM}; (b) semiconductor with work function Φ_S, electron affinity χ and silicon band structure with bandgap between E_C and E_V and Fermi energy E_{FS}; (d) band diagram at equilibrium for the ideal M/S junction for N-type semiconductor, w is the width of the depletion layer, Φ_i is the energy barrier to the flow of electrons (black dots) from semiconductor to the metal, and Φ_B is the Schottky barrier height (SBH) for the electron flow in the opposite direction; (e) ideal band diagram at equilibrium for P-type semiconductor (from [36])

2.1 The metal/silicon Schottky junction

The junction obtained putting a metal in intimate contact with lightly doped semiconductor, exhibits rectifying IV characteristics, similar to those of PN junctions, and is called Schottky diode. The energy diagram of this metal-semiconductor junction is shown in Figure 2.1, considering both N- and P-type semiconductor. When a contact between a metal with work-function Φ_M is established with a semiconductor having a different work-function Φ_S, charge transfer occurs until the respective Fermi levels align at equilibrium. For N-type semiconductor (Figure 2.1d), when $\Phi_M > \Phi_S$ the transfer of charge results in the formation of a depletion layer (or space charge region) at the semiconductor interface, rich of immobile positive ions. This layer has a width w from the

junction and corresponds in the band diagram of Figure 2.1d to the region with bands bent upwards. The formation of a depletion region in the semiconductor is a necessary condition for the achievement of a Schottky rectifying junction. When a depletion layer is formed in the semiconductor, the space charge is mirrored by a very thin layer of opposite-sign charge at the metal surface (Figure 2.1c). These two layers of opposite charge, which make the M/S junction, give rise to an electric field E_i and to a potential, named built-in potential at the junction (Φ_i, Figure 2.1d), which prevents further net charge diffusion between the semiconductor and the metal:

$$\Phi_i = \Phi_M - \Phi_S \,. \tag{2.1}$$

The corresponding energy, which prevents the diffusion of electrons from the semiconductor to the metal, is named Schottky barrier height (SBH) and can be expressed using the Schottky-Mott relation (valid in ideal conditions):

$$\Phi_B = |\Phi_M - \chi| \qquad \text{for N-type silicon} \tag{2.2}$$

$$\Phi_B = E_g - |\Phi_M - \chi| \qquad \text{for P-type silicon} \tag{2.3}$$

The SBH is a very important feature for the M/S rectifying junctions, in fact better rectifying characteristics are obtained for larger value of SBH. The barrier height is not related to the semiconductor doping level, but is determined by the choice of the materials used.

The forward current-voltage (I-V) characteristic of an ideal Schottky diode is usually described using the Cromwell-Sze model for thermionic emission and diffusion of carriers over the barrier [44], but the same equation can be derived also using the Landauer approach. Experimentally, Schottky diodes show deviations from ideal thermionic emission behavior, therefore a dimensionless parameter called the ideality factor, n, is usually included in the I-V relationship:

$$I = I_S \left[\exp\left(\frac{qV_D}{nk_BT} \right) - 1 \right] . \tag{2.4}$$

where I_S is the reverse saturation current, T the absolute temperature (in K), k_B the Boltzmann constant, q is the electronic charge and k_BT/q is the thermal voltage (25.6 mV at room temperature). The reverse current I_S can be expressed as:

$$I_S = A_{\text{eff}} A^* T^2 \exp\left(-\frac{q\phi_B}{k_BT} \right) \tag{2.5}$$

where A_{eff} is the effective area of the diode, A^* is the effective Richardson constant ($= 32\,\text{A}\,\text{cm}^{-2}\,\text{K}^{-2}$ for P-silicon), and ϕ_B is the diode SBH.

The ideality factor n has values between 1.0 and 1.2 for good quality real metal/Si junctions. Higher values measure the deviation from the ideal thermionic emission,

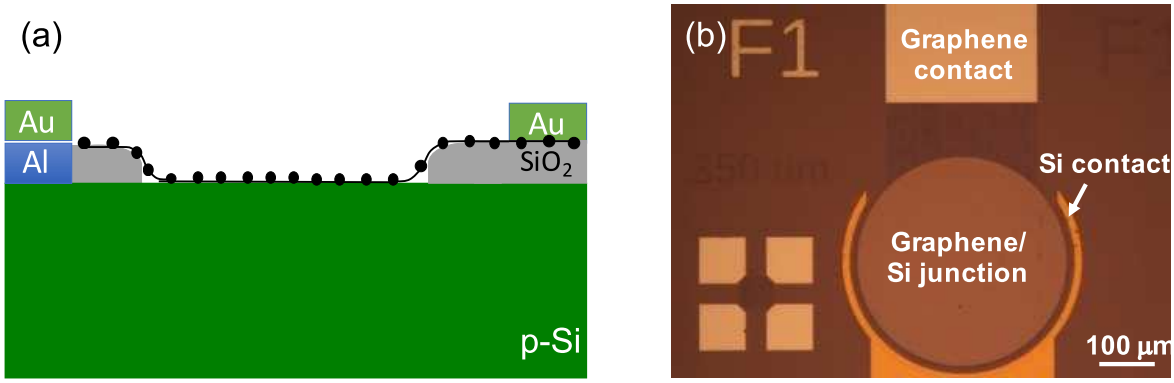

Figure 2.2: (a) Schematic diagram of a Gr/Si Scottky junction. The oxide layer on top of the silicon substrate is etched to form the active diode area, where graphene is in direct contact to the silicon substrate; (b) microscope image of a fabricated graphene/silicon diode, with metal contact to the Si substrate and to graphene layer.

taking into account how the presence of defects and other additional non-thermionic effects mediate the transport. Such effects include thermionic field emission and field emission, generation/recombination phenomena, unwanted insulating layer or defects inadvertently introduced at the interface during the fabrication process, which cause Schottky barrier inhomogeneity, bias- dependence of the SBH, edge leakage, etc. A more realistic model takes into account also the effect of the diode series resistance R_S, which is usually modeled with a series combination of a diode and a resistor through which flows the current I. The voltage V_D across the diode can then be expressed in terms of the total voltage drop V across the series combination of the diode and the resistor:

$$V_D = V - R_S I \,. \tag{2.6}$$

Hence, Equation (2.4) becomes:

$$I = I_S \left[\exp\left(\frac{q(V - R_S I)}{n k_B T} \right) - 1 \right] . \tag{2.7}$$

For $V_D > 3k_BT/q$ Equation (2.4) becomes:

$$I \simeq I_S \exp\left(\frac{qV_D}{nk_BT} \right) = I_S \exp\left(\frac{q(V - R_S I)}{nk_BT} \right) . \tag{2.8}$$

2.2 Fabrication of hybrid Graphene/Silicon diode

The first step in the fabrication of GSJ is the preparation of the silicon substrate. The technological process begins with the RCA cleaning of the Si substrate, followed by the

deposition of an insulating film, used as field oxide. A 120 nm SiO_2 film is deposited (via TEOS or LTO process) on low doped P-Si wafer ($\rho = 10$–$20\,\Omega\,\mathrm{cm}$). The silicon substrate is contacted on the front side, opening holes on the oxide and depositing the metals sandwich: 70 nm sputtered Aluminum, 10 nm Chromium and 70 nm of evaporated gold. The detailed process for fabrication of ohmic contact consists in an optical lithography process in which a negative photoresist (ma-N 1420, MicroResist Technology) is spincoated at 3000 rpm (obtaining 2 µm thickness), exposed to ultraviolet (UV) illumination through a Ni/Cr mask and developed. The bare silicon dioxide is then etched in a buffer oxide solution (BOE with NH_4F/HF (7:1) ratio) and, without removing the photoresist, a 50 nm thick Al-2% Si layer is sputtered on the sample. Then, a lift-off process, followed by annealing in forming-gas (mixture of N_2 + 10% H_2) at 400 °C for 20 min is used to obtain the ohmic contact. The complete fabrication of electrodes is obtained by thermal evaporation of Cr/Au (10 nm/70 nm) metals, lithographically defined via a second lift-off process. Au layer is introduced to protect Al (used for good ohmic contact to Si substrate), during the following processes in HF-based solutions. A matrix of 100 circular diodes with radius spanning from 200 µm to 500 µm is fabricated. The device active areas are lithographically defined using a positive resist (HPR-504, OCG Microelectronics Materials, spincoated at 4000 rpm, obtaining the thickness of 1.1 µm) and etching SiO_2 in standard BOE solution. Finally, the substrates are ready for graphene transfer. Graphene is deposited on a copper foil (25 µm thick) using the deposition process reported in Section 1.2.2, obtaining a few layers graphene film. Then, graphene is covered with 1 µm thick poly-methyl-methacrylate polymer (PMMA 950-A7, MicroChem). PMMA is used as graphene protection during etching of Cu in APS solution (ammonium persulfate, $50\,\mathrm{g\,L^{-1}}$ in water). Before graphene transfer, the silicon substrate is dipped in a solution of hydrofluoric acid (HF in water, 1:1000) for 30 seconds, to remove native oxide from diode's active areas. Two different procedures have been used for the transfer of graphene onto the patterned silicon substrates, with the aim of studying the effect of the transfer method on the interface between graphene and Si. The detailed technological steps used are reported in the following:

WET sample : the silicon substrate is immersed in HF:H_2O (1:1000) solution for 30 seconds, in order to remove the native oxide from the diode active area. Immediately after, we proceeded to the wet transfer of graphene in DI water. The procedure ended spraying isopropyl alcohol under the graphene film, in order to substitute or dilute the trapped water under graphene with alcohol.

DRY sample : we repeat the same procedure in hydrofluoric solution to remove native oxide from the silicon substrate. Then the substrate is rinsed in water for 30 seconds and finally immersed in isopropyl alcohol, to reduce the water content in the etched diode active areas. Immediately after, we executed the graphene transfer putting the Si substrate on the hotplate at 200°C, and laying down the

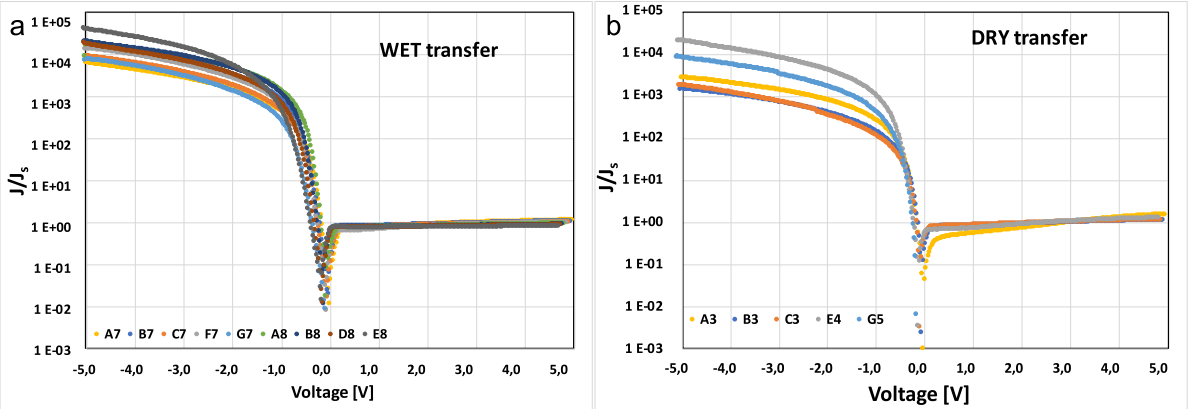

Figure 2.3: Semi-logarithmic plot of the normalized current-voltage characteristics of graphene/P-Si Schottky diodes measured at room temperature. Diodes are fabricated using different transfer process for the graphene film: WET transfer (a), and DRY transfer (b).

graphene foil (covered with PMMA) till the complete adhesion of the Gr foil to Si ($\sim$ 5 min), (see paragraph 1.4.4 for the detailed description of the process).

After drying, PMMA is removed from graphene in acetone vapors. Then, graphene is lithographically patterned using HPR-504 resist and dry etched in an oxygen plasma (25% O_2 + 75% N_2). Metal contact to graphene is fabricated evaporating Cr-Au (10 nm + 70 nm), defined via a lift-off process, using PMMA (exposed in DUV light, 248 nm) as photoresist. The device active area, A_{eff}, is defined by the graphene film in direct contact with silicon substrate. The schematic of a typical device structure is shown in Figure 2.2a, and the micrograph of a GSJ is reported in Figure 2.2b. The detailed technological process flow used for the fabrication of Gr/Si diodes is reported in Appendix A.1.

2.3 Graphene/Silicon junction (GSJ) electrical characterization

The current-voltage (I-V) measurements were performed at wafer level in a Karl-Süss probe station, in ambient atmosphere and in the dark, using four Keithley 238 connected to the prober through the switching matrix Keithley 707 (with 7072 and 7174 semiconductor cards). As convention, the bias voltage is applied to graphene, while the silicon substrate is grounded in all measurements. The sample consists of 100 circular graphene-Si diodes, with diameters of 500, 700, 800, 900 and 1000 µm.

The measured current-voltage (I-V) characteristics are reported in Figure 2.3 for

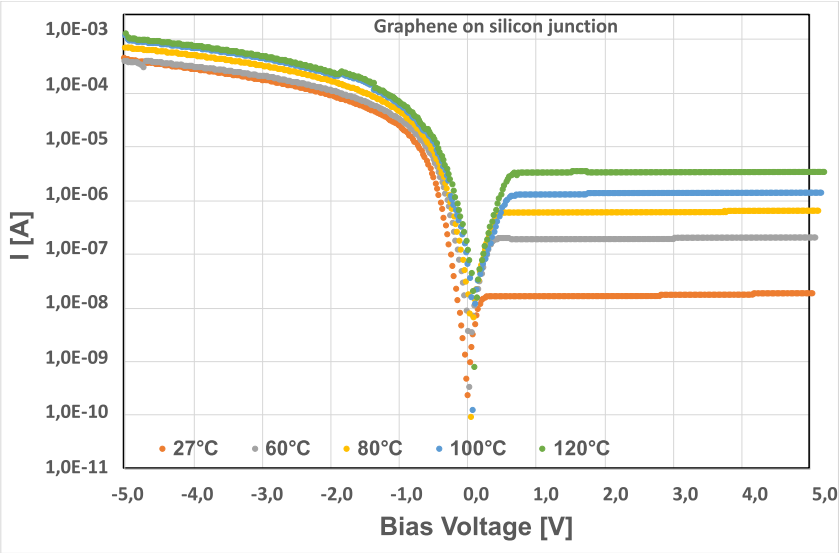

Figure 2.4: Semi-logarithmic plot of the current-voltage characteristic for a graphene/silicon diode measured at different temperatures.

wet (a) and dry (b) diodes with different active areas. The current density is normalized with respect to the saturation current (J_s). Both WET and DRY samples exhibit similar behavior for the diodes, with quite constant reverse current increasing the applied reverse voltage, and a rectification ratio around 3 orders of magnitude. When the forward bias is higher than $-0.6\,\mathrm{V}$, the $I-V$ characteristics are dominated by the series resistance R_S, which is the lump sum of graphene and substrate resistances. Figure 2.4 shows the $I-V$ for a Gr/Si diode for temperatures ranging from $300\,\mathrm{K}$ to $400\,\mathrm{K}$. We can observe an increase in the diode reverse current, because more electrons gain sufficient thermal energy to surmount the Schottky barrier, while the effect of temperature on forward current is less evident, because for forward voltages the current is dominated by the exponential dependence from the applied bias and by the effect of the series resistance.

2.3.1 Band diagram for GSJ

From a general perspective, the graphene/silicon junction may be handled using the standard model of metal- semiconductor Schottky junction. In particular, as reported in [45] for temperature higher than 260 K, the net current trough the Gr/Si junction can be described using equations 2.4 and 2.5. However, it's necessary to underline that there is a great difference between graphene and standard metals. In particular, graphene has a very small density of states in the vicinity of the Dirac point. For this reason, the charge exchange that takes place putting graphene in contact to a semiconductor, determines the shift of the graphene Fermi level with respect to that of isolated graphene. Likewise,

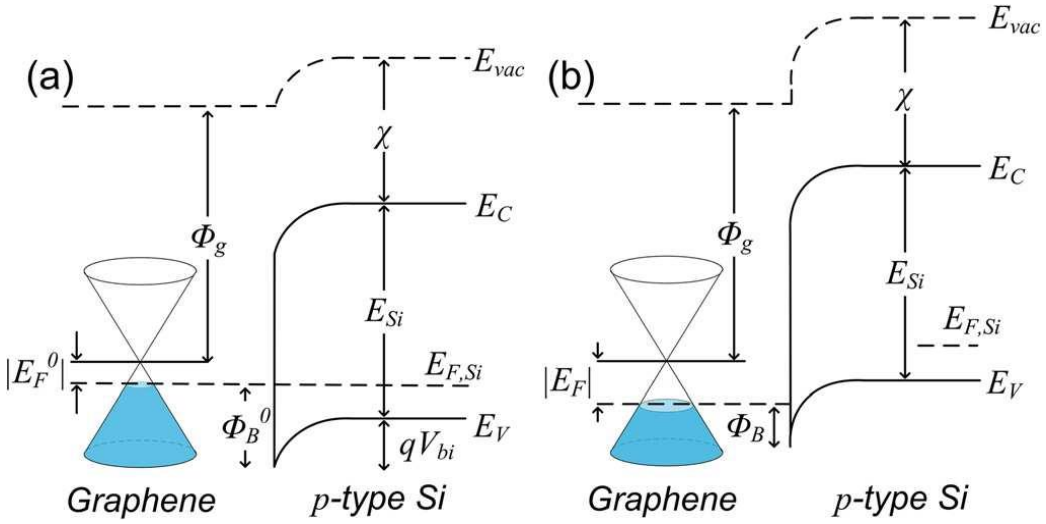

Figure 2.5: Energy band diagram for the graphene/P-Si Schottky junction (a) at thermal equilibrium and (b) under reverse bias V_R. E_{vac} is the vacuum level, χ,E_c, E_{Si}, $E_{F,Si}$, and E_V are the electron affinity, conduction band, bandgap, Fermi level, and valence band of Si, respectively. Furthermore, V_{bi} is the built-in voltage, Φ_g is the work-function of intrinsic graphene, E_F is the graphene Fermi-level shift, and Φ_B is the Schottky barrier height. The super- scripts "0" in part (a) refer to thermal equilibrium (i.e., zero-bias) values. Under reverse bias (b), the graphene Fermi level shifts further down relative to the Dirac point, decreasing Φ_B. (from [45])

when an external voltage is applied to the Gr/Si system, there is a shift of the graphene Fermi level, with respect to its equilibrium position, leading to a tunable Schottky barrier. This affects the Gr/Si built-in potential distribution, as well as the barrier height and the capacitance of the junction [37]. The change in graphene Fermi level, due to the charge transfer that occurs putting graphene in contact with P-silicon and due to applied bias is shown in Figure 2.5.

2.3.2 Methods for the extraction of GSJ parameters

Handling the GSJ using the standard model of metal-semiconductor contact, four main parameters are required for the complete description of the Schottky junction $I-V$ characteristics:

- the ideality factor n,
- the reverse saturation current I_S,
- the Schottky barrier height Φ_B, and
- the diode series resistance R_S.

The classic methods used for the extraction of these parameters for the metal/silicon Schottky junction can be applied also to GSJ, having in mind that graphene has a semimetal behavior, and a tunable Fermi level, which reflects on the diode Schottky barrier. The aim is to verify the applicability of standard methods to GSJ.

Method 1 : parameter extraction from I-V measurements for low forward bias [36]. Plotting the current I of the diode (Equation 2.7) in semi-logarithm scale (Equation 2.9), the diode $I-V$ characteristics in forward bias (considering fulfilled the conditions: $V > kT/q$ and $V \gg R_S I$) corresponds to a straight line.

$$\ln I = \ln I_S + \frac{qV}{nk_BT}. \tag{2.9}$$

when $V \to 0$ the semi-log plot loose its linear behaviour, for the "-1" presence in Equation (2.7). However, Equation (2.7) can easily be rewritten as follows [46]:

$$I = I_S \exp\left(\frac{q(V-R_SI)}{nk_BT}\right)\left(1-\exp\left(-\frac{q(V-R_SI)}{k_BT}\right)\right). \tag{2.10}$$

The semi-log plot of $I/\left(1-\exp\left(-\frac{q(V-R_SI)}{k_BT}\right)\right)$ vs. the applied voltage V, (in the condition of $V \gg R_S I$) is a straight line also for $V \to 0$:

$$\ln \frac{I}{1-\exp\left(-\frac{q(V-R_SI)}{k_BT}\right)} \simeq \ln I_S + \frac{qV}{nk_BT}. \tag{2.11}$$

Thus, the linear fitting of Equation (2.11) will be used to extract the value of the saturation current I_S at zero bias (the y-axis intercept) and the ideality coefficient n of the diode (the slope of the linear fitting), in the range of very low applied voltages.

Method 2 : parameter extraction from $I-V$ measurements for high bias voltage (Cheung method [47]). At higher forward bias ($|V| > 0.5\,\text{volt}$), the $I-V$ diode characteristics are dominated by the series resistance, which is the lump sum of contact, graphene and substrate resistances. In this region Equation (2.7) must be considered. For V high enough to neglect the term "-1" and taking the logarithm, Equation (2.7) can be written as:

$$V = \frac{nk_BT}{q} \ln \frac{I}{I_S} + R_S I \,. \tag{2.12}$$

Taking the derivative of Equation (2.12) with respect to I and using the equality $\mathrm{d}I/I = \mathrm{d}(\ln I)$, the Cheung's functions can be obtained from Equation (2.12):

$$\frac{\mathrm{d}V}{\mathrm{d}(\ln I)} = R_S I + \frac{nk_BT}{q} \tag{2.13}$$

and defining the function:

$$H(I) = V - \frac{nk_BT}{q} \ln \frac{I}{AA^*T^2} \tag{2.14}$$

Equation (2.12) can be rewritten using the function $H(I)$, as follows:

$$H(I) = R_S I + n\phi_B \tag{2.15}$$

Plotting $\mathrm{d}(V)/\mathrm{d}(\ln I)$ vs I, a line is obtained, whose slope is R_S and the y-axis intercept is nk_BT/q. Therefore, the ideality factor (n) of the diode can be extracted in the linear region of the $I-V$ curve, for forward bias in the range -0.5 to $-1\,\text{V}$. Using the n value so determined, the plot of $H(I)$ vs I will also give a straight line, whose y-axis intercept is equal to $n\phi_B$, while its slope provides a second determination of R_S, which can be used to check the consistency of the approach. It's important to underline, that the Cheung method is extremely sensitive to the bias voltage range applied, and this reflects on the determination of both the ideality factor n and the SBH.

Method 3 : parameter extraction from the temperature dependent $I-V$ characteristics in reverse bias (Richardson plot).
Equation (2.5) for the expression of the diode reverse saturation current, can be rearranged as follows:

$$\ln \frac{I_S}{T^2} = \ln(-AA^*) - \frac{q\Phi_B}{k_BT} \,. \tag{2.16}$$

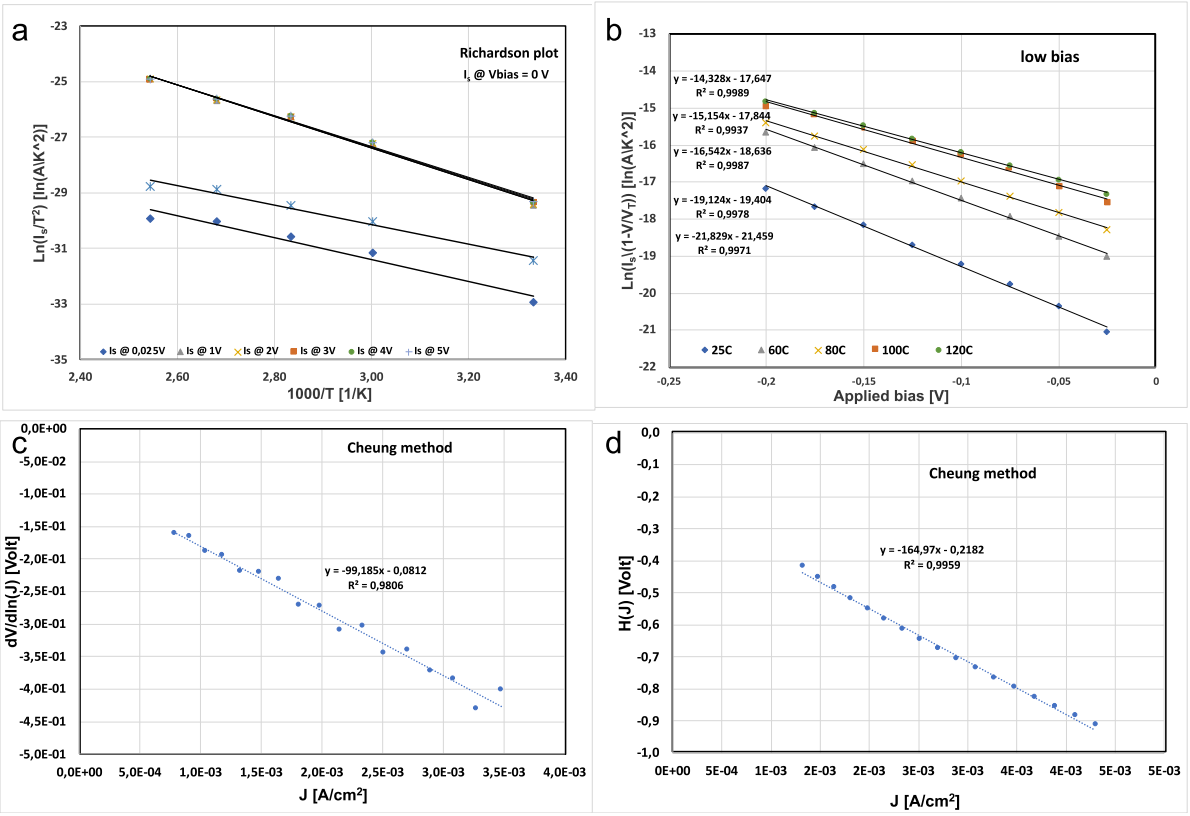

Figure 2.6: (a) Plot of $\ln(I_S/T^2)$ versus $1000/T$ (Richardson plot) with linear fit to extract the SBH, Φ_B, at different biases; (b) semi-logarithmic plot of Equation 2.11 versus the applied forward voltage (very low values) at different temperatures; Cheung's plot of (c) $\mathrm{d}V/\mathrm{d}\ln(J)$ versus J and (d) $H(J)$ versus J at 300 K.

In Equation (2.16) the series resistance term is ignored, since the analysis is based on reverse current only, where the contribution related to the series resistance is negligible. Therefore, the semi-logarithmic plot of I_S/T^2 vs $1/T$ (known as Richardson plot), is a straight line whose slope is $(q\Phi_B)/k_B$, and from the intercept we can extract the value of the Richardson constant A^* for the GSJ. The Richardson plot is obtained extracting the reverse saturation current measured for different temperatures at a defined reverse voltage. This procedure permits to investigate the variation of SBH with the reverse bias voltage. Applying this method to the system graphene/P-Si, we obtain the effective Richardson constant (A^*), that assumes values 5-7 orders of magnitude lower than the typical value of $32\,\mathrm{Acm^{-2}K^{-2}}$ of metal/P-silicon junction. These extremely low values for A^* could be explained considering the presence of an insulating layer at the diode interface [48], but it's also related to the linear momentum of electrons moving from Gr to Si in the perpendicular direction [38, 39]. Probably the formation of this native oxide is related to a small amount of water trapped between graphene and silicon during the transfer procedure. The presence of an insulating layer at the interface could introduce a tunneling attenuation factor for the reverse current, therefore Equation (2.5) can be rewritten taking into account also this attenuation (the following equation is valid for 3D/3D systems):

$$I_S = A_{\mathrm{eff}} A^* \exp\left(\chi^{\frac{1}{2}}\delta\right) T^2 \exp\left(-\frac{q\Phi_B}{k_B T}\right) \tag{2.17}$$

Where χ is the mean barrier height between graphene and silicon, expressed in eV, ($\sim 3\,\mathrm{eV}$), and δ is the thickness of the insulating layer, expressed in Å. Therefore, the tunneling attenuation can be included in the extracted value of the Richardson constant, which therefore is defined as:

$$A^{**} = A^* \exp\left(\chi^{\frac{1}{2}}\delta\right) \tag{2.18}$$

Using the expression above and the value extracted for the Richardson constant, it's possible to evaluate the thickness of the insulating layer at the diode interface, δ.

In order to obtain a reliable determination of the GSJ parameters, a method consisting in 4 steps has been defined, to simultaneously extract the full set of data using the methods described above:

STEP 1: At reverse voltages, extraction of the effective Richardson constant (A^{**}), of the Schottky barrier height at 0 bias (Φ_{B0}) and of the SBH for different values of the reverse bias ($\Phi_B(rev)$) from the linear fitting of semi-logarithmic plot of I_S/T^2 vs $1/T$ (Richardson plot, Figure 2.6a).

Table 2.1: Summary of the methodology defined for the reliable determination of the GSJ parameters. Classical methods used for Metal/Si Schottky diodes are applied.

Step / method	Bias	Condition	Equation	Extracted parameter
step 1 / **3**	Reverse bias *(Richardson plot)*	$V \to 0$	$ln(I_S/T^2) = \ln(-AA^{**}) - \frac{q\Phi_B}{k_B\mathrm{T}}$	Intercept = AA^{**} Slope = $\frac{q\phi_B}{k_B}$
step 2 / **2**	High forward *(Cheung)*	$V > 0{,}5\,V$	$\frac{dV}{d(lnJ)} = R_s A_{eff} J + \frac{nk_BT}{q}$	Intercept = n Slope = R_s
step 3 / **2**	High forward *(Cheung)*	$V - R_sI > 3nk_BT/q$	$H(J) = R_s A_{eff} J + n\phi_B$	Intercept = $n\phi_B$ Slope = R_s
step 4 / **1**	Low forward [0,02 – 0,2V]	$V > R_sI$	$\ln\frac{I}{1 - e^{-\frac{qV}{k_BT}}} = \ln I_s + \frac{qV}{nk_BT}$	Intercept = I_s ($V \to 0$) Slope = n from plot I_S vs T^{-1}: ϕ_B

STEP 2: At forward bias, from the linear fit of Equation (2.13) (Cheung's method), we can obtain the series resistance (R_S) and the diode ideality factor (n) (slope and intercept respectively, Figure 2.6c).

STEP 3: At forward bias, $H(I)$ (Equation 2.14) is calculated using the values of A^{**} (obtained in step 1) and n obtained in the previous step 2; then Equation (2.15) is plotted and fitted obtaining R_S and the value of Schottky barrier height for high forward bias ($\Phi_B(for)$) in the range -0.6 to $-1\,\mathrm{V}$, (Figure 2.6d).

STEP 4: At low forward bias, the linear fit of the semi-logarithmic plot of Equation (2.11) versus the applied voltage, permits to extract the diode ideality factor, n, and the zero bias reverse current for very low forward bias, in the range -0.03 to $-0.2\,\mathrm{V}$, (Figure 2.6b). This reverse current is then used to obtain the Schottky barrier height for very low forward bias (Φ_B(forw low bias)).

Table 2.1 summarizes the extraction of different parameters with the 3 methods as above described. The value for R_S reported in the table is the average of the two values obtained in steps 2 and 3.

2.3.3 Diode parameter extraction for GSJ

The GSJ fabricated and measured are characterized by a P-doped graphene layer, with carrier concentration $\sim 10^{13}\,\mathrm{cm}^{-2}$. As reported in [37] only in the limit of highly doped graphene, the GSJ approaches to a true Schottky junction.

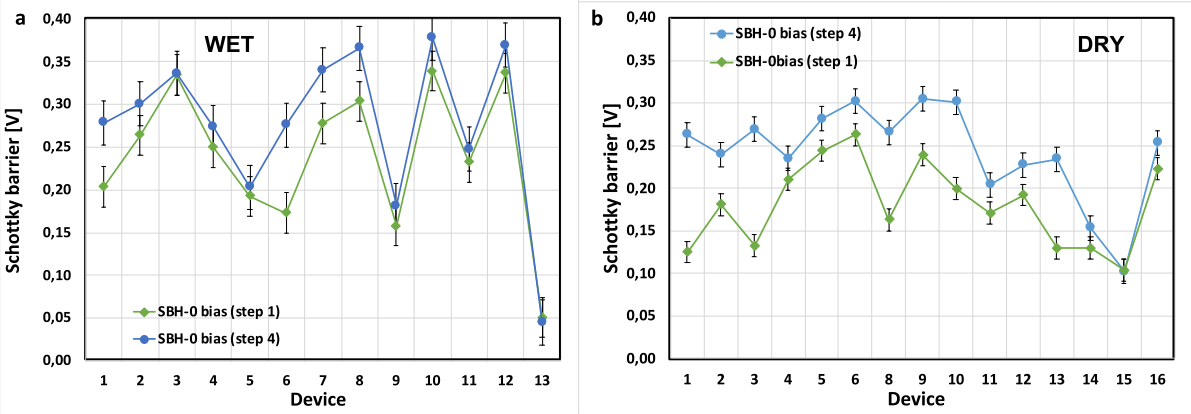

Figure 2.7: plot of Φ_{B0} values for (a) WET and (b) DRY Gr/Si diodes. The values are extracted as explained in step 1 (green lines) and in step 4 (blue lines).

Schottky barrier height The understanding of the formation of SBH in a graphene/silicon structure is very important for real applications of graphene in electronics and optoelectronics, because it could offer a precise control of $I-V$ device characteristics. A previous study [36] showed that for graphene/3D semiconductor, the SBH is faintly correlated to the semiconductor work function, thus the SBH is dependent on the atomic structure of graphene and 3D semiconductor interface. From a practical point of view, using the different methods, the Gr/Si junction SBH is extracted in 3 different conditions: i) near zero bias; ii) under forward bias; and iii) under reverse bias. Differently from Metal/Si junctions, where the same value is obtained in these conditions, for GSJ three different values for the Schottky barrier height are got, as shown in Table 2.2. This behavior can be explained having in mind what happens in graphene layer upon bias. The initial condition for the formation of a non ohmic contact between G and P-Si is that the work function of graphene is lower than that of P-Si:

$$q\Phi_g < q\Phi_S \tag{2.19}$$

Upon contact formation, at equilibrium (zero applied bias), there is a transfer of holes from Si to G to fulfill the Fermi level alignment of the two materials, which ends with the creation of the built-in potential. To mirror the charge in the depletion layer in Si, the graphene Fermi level moves away from Dirac point, and its work function is increased (relative to work function of isolated graphene, Figure 2.5a). Applying a forward bias to the G/P-Si diode (i.e. negative voltage applied to graphene), the depletion layer in silicon reduces and becomes very thin, therefore also the charge in graphene is reduced (graphene becomes less p-doped), and due to the low density of states of graphene, its Fermi level moves upward (towards the Dirac energy level), causing the barrier height for holes moving from P-Si to graphene to be reduced by the amount qV/n, (with V the applied voltage and n the diode ideality factor). Finally, in reverse bias (i.e. positive

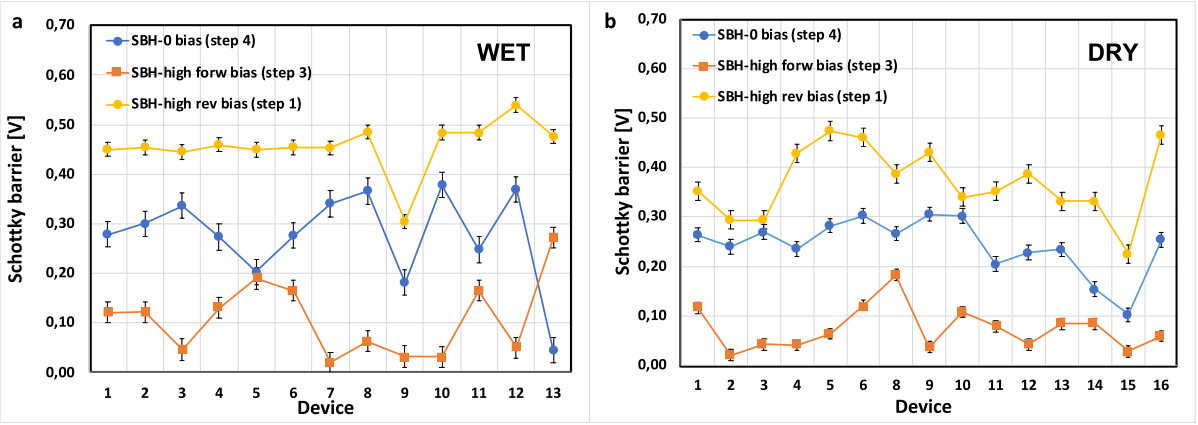

Figure 2.8: Plot of SBH values extracted for WET (a) and DRY (b) Gr/Si diodes for different bias conditions: zero bias (blue dots), high forward bias (orange dots) and high reverse bias (yellow dots).

	WET transfer	DRY transfer
SBH @ 0 bias [V]	0,277 ± 0,08	0,243 ± 0,05
SBH in forward bias [V]	0,108 ± 0,07	0,074 ± 0,04
SBH for reverse bias [V]	0,457 ± 0,05	0,370 ± 0,07

Table 2.2: Average values for SBH extracted from $I-V$ measurements for different applied bias. The values reported are the average of at least 13 measurements on different diodes.

voltage applied to graphene), the depletion layer in silicon is increased and the charge in graphene grows, so that the Fermi level of graphene moves away from the Dirac point (Figure 2.5b). The values for Φ_{B0} (that is near the zero bias condition), are obtained both in step 1 and step 4, and are shown in Figure 2.7a) for WET and in Figure 2.7b) for DRY diodes. The Φ_{B0} values obtained using the two methods are quite similar, and for most diodes differ for some tens on mV, a quite low difference considering that they work in reverse and forward bias, respectively. Therefore both methods can be used for the extraction of the Φ_{B0} parameter.

As previously stated, changing the biasing conditions (zero bias, reverse and forward bias) the Fermi level of graphene moves, and this reflects on the diode barrier height, as shown in Figure 2.8, where the value of SBH at high forward bias is obtained using the Cheung's method (step 3, orange dots), the value of SBH at high reverse bias is obtained using the Richardson plot (step 1, yellow dots), and the values of SBH at zero bias are the blue dots. The average values obtained for the SBH in the three different bias conditions are reported in Table 2.2. We can notice that WET diodes are characterized by higher

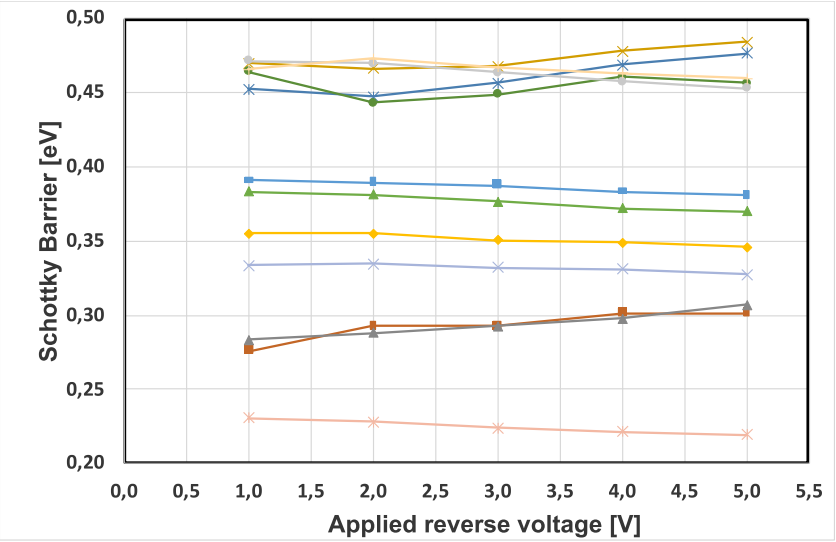

Figure 2.9: Dependence of SBH from the applied reverse bias, varying from 1 V to 5 V. The dependence is faint for a large number of diodes.

values of the SBH in the three regions with respect to the DRY diodes, even if this difference is within the standard deviation. Anyway, we can use this as a suggestion that the different surface preparation and transfer process used could have an effect on the final value of SBH, which is mainly influenced by the Gr Fermi level. But this occurence has to be further investigated. Moreover, from the Richardson plot (step 1), it's possible to evaluate the dependence of SBH from the applied reverse voltage. For all the diodes measured, the saturation reverse current is quite constant, thus the extracted SBH is only faintly affected by the applied reverse voltage (Figure 2.9), suggesting a pinned level for the graphene Fermi level for high reverse bias. This behavior will be explained in the next paragraph by the model developed.

Ideality factor As explained in section 2, the ideality factor n is introduced in the $I-V$ relationship to take into account the deviations from the theoretical thermionic emission of carriers (Equation 2.4). Its value is 1 for theoretical diodes, while is $2 > n > 1$ in real junctions [49]. For the GSJ, n value larger than 2 is commonly observed [36], and this high value is commonly related to the presence of an interfacial oxide layer and of surface roughness and defects, that can cause inhomogeneity in the SBH, introducing deviations from the thermionic emission transport. Two methods have been used in this work for the extraction of the ideality factor in GSJ. The Cheung method, where n is obtained from the linear fit of Equation (2.15), for forward voltages in the range -0.6 to -1 V. The second method extracts n (n-low bias) from the slope of the straight-line fitting Equation (2.11) versus V plot (method 1), for very low voltages, between

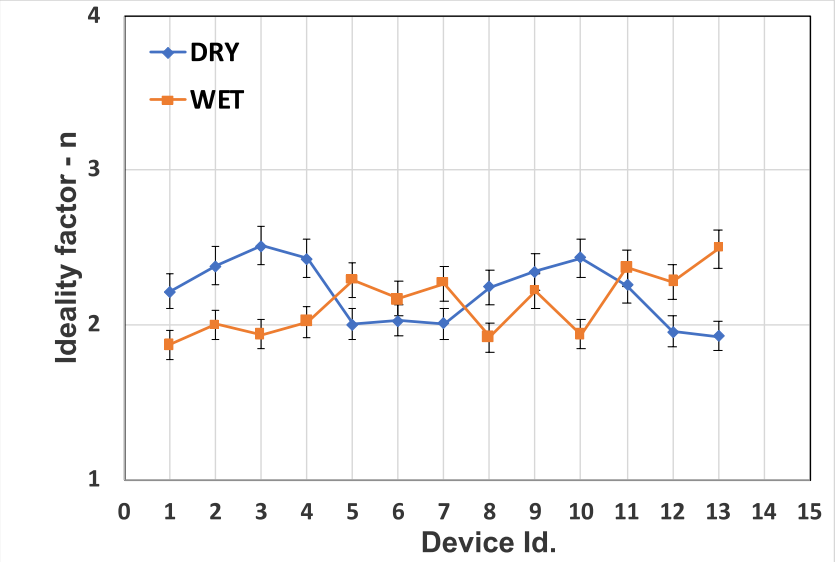

Figure 2.10: Plot of the ideality factor for WET (orange dots) and DRY (blue dots) Gr/Si diodes. The values plotted have been extracted working in the region of low forward voltage (n-low bias in Table 2.3). Similar values for WET and DRY diodes, slightly higher than 2, are obtained.

Table 2.3: Ideality factor extracted for WET (a) and DRY (b) diodes using the two methods described in the text.

a

device	n-low bias	n-Cheung
1	1,9	3,7
2	2,0	3,0
3	1,9	3,3
4	2,0	3,1
5	2,3	3,1
6	2,2	3,0
7	2,3	3,3
8	1,9	2,9
9	2,2	4,4
10	1,9	4,4
11	2,4	3,8
12	2,3	2,9
13	2,5	3,6
average	2,1	3,4
std dev	0,2	0,5

b

device	n-low bias	n-Cheung
1	2,2	3,0
2	2,4	5,1
3	2,5	4,6
4	2,4	5,4
5	2,0	3,6
6	2,0	2,2
7	2,0	3,7
8	2,2	3,6
9	2,3	4,5
10	2,4	4,0
11	2,3	4,0
12	2,0	2,5
13	1,9	3,9
average	2,2	3,9
std dev	0,2	0,9

Table 2.4: Values for the effective Richardson constant extracted for Gr/Si Schottky diodes fabricated with WET (a) and DRY (b) graphene transfer method. A_0^* is extracted for low forward applied voltage (near 0), while A^* aver(rev) is the average value of the Richardson constant extracted applying different reverse voltages (ranging from 1 to 5 V).

a

device	A^*_0 (forw)	A*aver. (rev)
	A/cm^2K^2	A/cm^2K^2
A7	1,4558E-07	8,47E-04
B7	2,9016E-07	1,37E-03
C7	5,875E-07	9,19E-04
F7	1,4374E-07	1,60E-03
G7	2,5014E-09	3,08E-03
J7	3,1543E-08	7,94E-03
A8	8,8506E-06	2,48E-03
B8	5,2038E-06	6,81E-03
C8	2,178E-07	7,45E-05
D8	2,0979E-06	4,39E-03
E8	1,5179E-08	3,31E-03
H8	1,1395E-06	2,38E-02
I8	2,7968E-11	2,99E-03

b

device	A^*_0 (forw)	A*aver. (rev)
	A/cm^2K^2	A/cm^2K^2
A3	5,5313E-07	2,73E-04
B3	5,2305E-07	5,24E-05
C3	1,8631E-06	7,19E-05
D3	3,9573E-07	3,73E-03
E4	1,0785E-06	1,17E-02
G5	4,2569E-06	3,35E-03
J5	1,2182E-07	2,63E-03
H5	3,1536E-06	9,86E-03
I5	1,8127E-06	5,32E-03
A8	2,163E-07	8,27E-05
B8	1,8114E-07	2,66E-04
C8	3,9733E-07	8,40E-04
D7	6,9388E-07	7,42E-04
F7	5,8374E-08	1,96E-04
J7	3,3111E-07	6,74E-03
H7	8,7183E-06	8,80E-03
F8	9,0521E-09	6,24E-06

0 V and V_{FB}, (V_{FB} is the voltage for flat band condition). As shown in Table 2.3, the Cheung method gives higher values for the ideality factor (≥ 3), outside the classic range of values expected for n, while the n value extracted using method 1 is ~ 2, very close to the expected value for non-ideal diodes. The higher value of n obtained using the Cheung method could be explained considering that this method operates in the high forward bias region of the GSJ (for $|V| > 0.5$ V), where the transfer of carriers across the Gr/Si junction does not follow the ideal thermionic emission. The value of n-low bias is therefore considered more relevant in describing the quality of the GSJ, because it's obtained in the region where the thermionic emission is dominant. Similar values for the ideality factor are obtained for WET and DRY diodes (Figure 2.10).

Richardson constant The effective Richardson constant is defined as:

$$A^* = 4\pi q m^* k^2 / h^3 \tag{2.20}$$

with m^* the electron effective mass, k the Boltzmann constant, q the electronic charge and h the Plank constant. For 3D-3D junctions the thermionic emission prefactor A^* is mainly fixed by the electronic properties of the semiconductor, while there is evidence

that Equation (2.20) is no more valid for GSJ, where the charge transport across the 2D-3D Schottky junction is mainly determined by the electronic properties of the 2D material. The effective Richardson constant A^{**} for GSJs is extracted from the Richardson plot (step 1, or step 4), where $\ln(I_S/T^2)$ is plotted versus $1/T$, (Equation 2.16), with temperature ranging between 300 K and 400 K. This plot reveals a straight line whose slope yields the mean SBH, and the intercept ($= \ln(AA^{**})$) at the ordinate permits to extract the value for A^{**} for a given diode area. Two different values are obtained for the Richardson constant: the A_0^{**}(forw) is obtained in the forward region for $V \to 0$, while A^* aver. (rev) is the average of the values obtained for the Richardson constant in high reverse bias conditions (at 1, 2, 3, 4 and 5 V applied). The choice to show a mean value for high reverse bias is due to the fact that the extracted values for the Richardson constant in this region are very similar. The values obtained are reported in Table 2.4. The very low values here extracted for the Richardson constant are in agreement with the experimental ones presented in literature and are at least 7 orders of magnitude smaller than the value obtained for 3D structures on P-Si substrate, where the Richardson constant is $\sim 32\,\mathrm{Acm^{-2}K^{-2}}$. This large variance will be discussed in the next section. The larger value obtained for A^* aver.(rev) has to be further investigated, and it's probably related to the presence of an inversion layer that forms at the silicon interface at high reverse bias. Indeed, this different and higher value for the Richardson constant is related to the SBH of the Gr/Si junction which moves from 0,25 V at zero bias, to $\sim 0,4$V for high reverse bias, and it could represent a different physical mechanism underlying the free carrier generation in these biasing conditions.

Interface oxide layer Concerning the interface oxide layer, recently x-ray photoelectron spectroscopy (XPS) has demonstrated the presence of a thin silicon dioxide layer at the Gr-Si interface. According to Equation (2.17), this oxide introduces a tunneling attenuation factor $\exp\left(\chi^{\frac{1}{2}}\delta\right)$ [36], which can be considered as a modification of the Richardson constant, that can be rewritten as in Equation (2.18) (valid for 3D/3D structures, its validity for 2D/3D structure has to be verified). The values for the oxide interface layer, obtained using Equation (2.18), are shown in Figure 2.11. They are in the range 10–13 Å, thinner than the typical thickness of native oxide on uncovered silicon, of 2–3 nm. From the conduction point of view, the presence of this interfacial oxide could affect the carrier conduction in the junction, reducing the thermionic emission current of majority carrier, and could increase the scattering at the interface, while the diffusion current (due to minority carrier) is not influenced. The values for the oxide thickness extracted for WET and DRY samples are similar, so the transfer process used does not seem to have a clear effect in determining the interface oxide thickness.

Rectification factor The rectifying ratio (RR) is another important parameter for the Schottky junction. This factor evaluates the ratio of on/off current in the diode, and

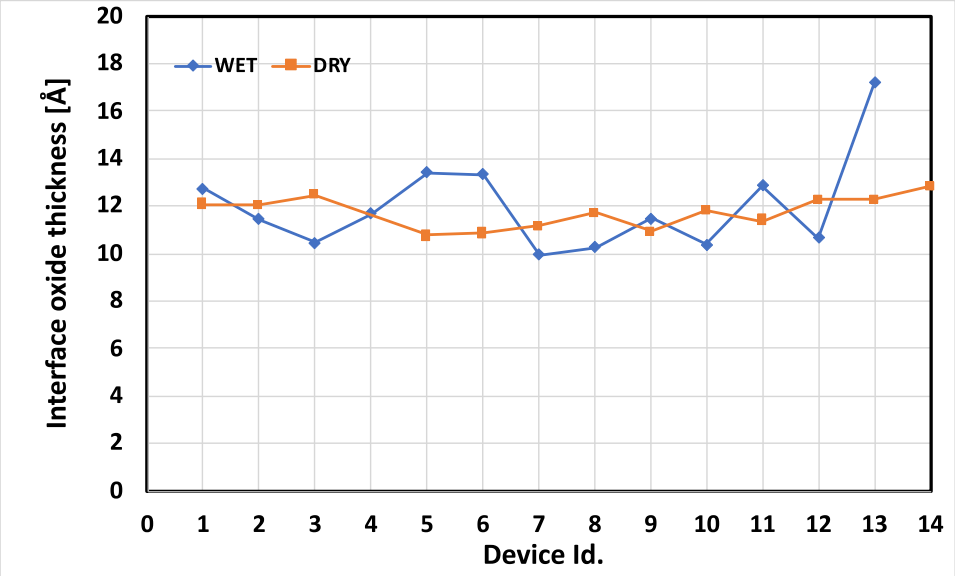

Figure 2.11: Thickness of the interface oxide layer obtained from the value of effective Richardson constant, using Equation 2.18. Dry and Wet diodes show similar thicknesses for the interface oxide layer.

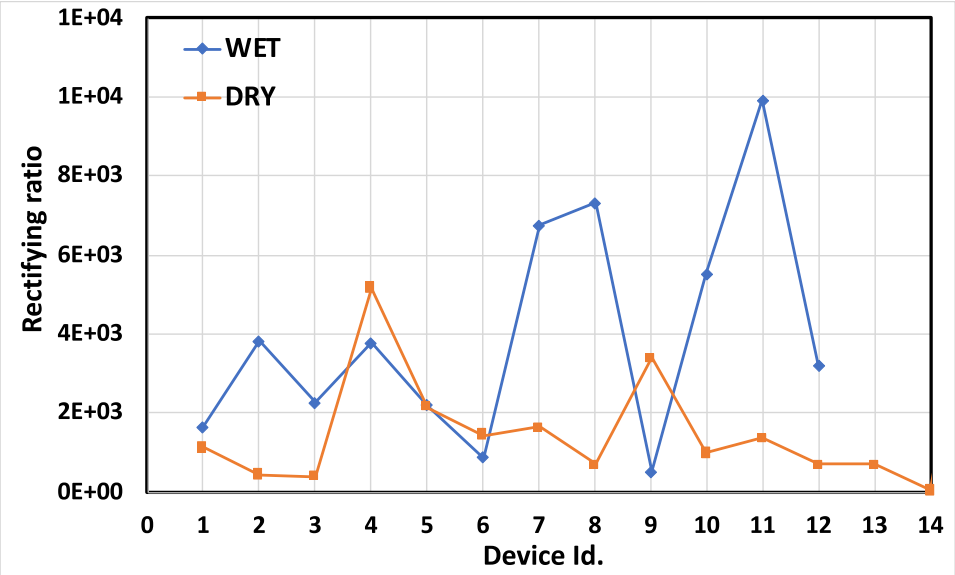

Figure 2.12: Comparison of rectification ratio for WET and DRY GSJ calculated at ∓ 2 V. The lower values obtained for DRY diodes are due to the higher reverse current.

large values define the good quality of the junctions. In this work, RR is defined as the ratio of the forward to the reverse current at $\mp 2\,\mathrm{V}$. Because the diode's reverse current increases with temperature (Figure 2.4), the rectification factor reduces increasing the temperature. For WET diodes the RR at room temperature is a quite good value, around some thousands. DRY diodes present higher reverse current, therefore their RR is often reduced to some hundreds (Figure 2.12).

2.4 Modeling the graphene/semiconductor junction

As explained in the previous paragraphs, the traditional Schottky diode equation derived for metal/semiconductor contact is not completely satisfactory to describe the behavior of Gr/semiconductor Schottky contact. A new equation, consistent with experimental measures, is proposed to account for the conduction mechanisms and variation in the graphene Fermi level that occurs applying positive and negative biasing to the Gr/Si device. The derivation of a diode equation can be carried out under a variety of approximations. Irrespective of the assumption that the mean free path of the charge carriers in the semiconductor be either much larger (thermionic regime) or much smaller than the thickness of the depletion layer, the same canonical form of the diode Equation (2.4) is found. In fact, Equation (2.4) can also be derived through the proper adaptation of general frameworks (such as that of Landauer) to the description of 2D/2D, 2D/3D or 3D/3D devices. This circumstance confers to this equation a sort of universality, which is the reason why it is widely adopted for first, coarse grain analyses. On the other hand, when specific systems have to be investigated in detail, deeper insights are usually needed. The initial step for the quantitative description of the $I-V$ characteristics of Graphene/oxide/P-Si system, is the derivation of the relationship between the Fermi levels of graphene (E_{Fg}), and P-Si (E_{Fs}), in the presence of a bias potential V_{bias}. This can be done with the help of the energy diagram reproduced in Figure 2.13 (in this case the presence of a single graphene layer is envisaged).

This scheme accounts for the relevance of donor surface states in Si, characterized by a constant density D_i (in units of $\mathrm{eV}^{-1}\,\mathrm{cm}^{-2}$), over an energy domain $E \leq q\phi_0$. Since $q\phi_0 > E_{Fs}$, a part of these donors releases their electrons to the bulk acceptors near the surface and, as a consequence, a positive charge surface density

$$Q_s = qD_i(q\phi_0 - E_{Fs}) \tag{2.21}$$

localizes at the surface, balanced by a negative charge distributed in a depletion layer, which already forms before the junction is made, due to the very low doping of bulk Si ($N_a \sim 10^{15}\,\mathrm{cm}^{-3}$). This interfacial layer supports a potential difference Δ_{int}, which is related through the Gauss theorem to the charge density Q_g localized on graphene sheet

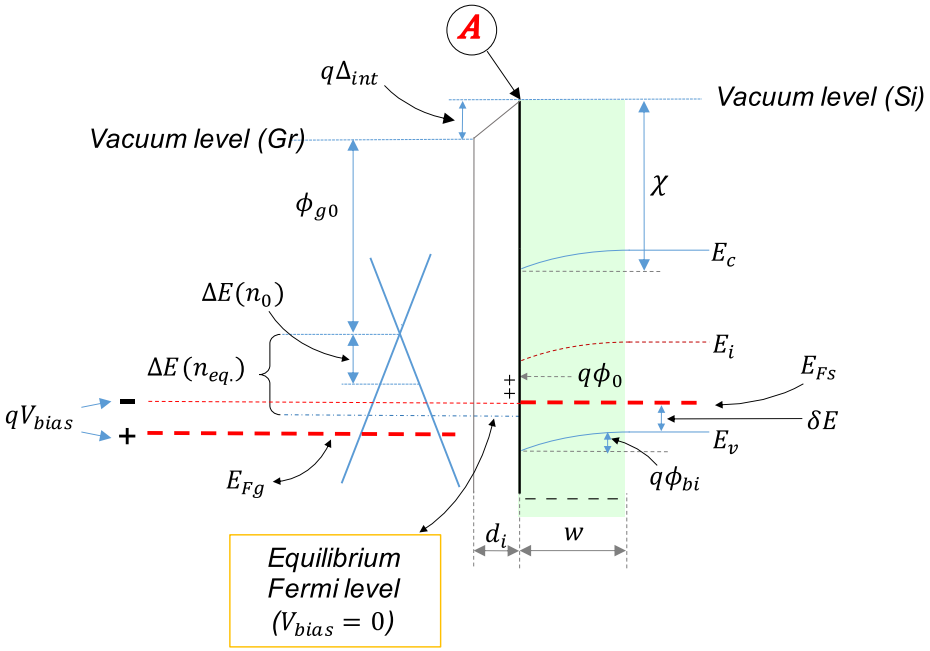

Figure 2.13: Energy diagram of a Gr/P-Si junction under moderate reverse bias ($V_{\text{bias}} > 0$, being Si the reference "electrode"). With $V_{\text{bias}} \neq 0$ both E_{Fs} and E_{Fg} shift with respect to the equilibrium level ($V_{\text{bias}} = 0$), due to the finite density of states in Gr as well as in P-Si. Localized donor surface states on P-Si, with energy $\leq q\phi_0$, are envisaged, as well as the presence of a d_i-thick oxide layer between Gr and Si, supporting a potential difference Δ_{int}. The point labelled with A is a reference that may be adopted for the derivation of Equation 2.25. The remaining quantities can be identified through the main text, for which this figure is a reference.

and due to the exchange of electrons with Si:

$$q\Delta_{\text{int}} = \frac{qQ_g}{\varepsilon_d} d_i \tag{2.22}$$

where ε_d is the dielectric permittivity of the oxide and d_i is the thickness of the interfacial layer; if $\Delta n(>0)$ is the number of electrons transferred to Si, the charge density in Gr is $Q_g = q\Delta n(>0)$. Both the Δn electrons transferred from graphene and those provided by donor states at the surface contribute to the formation of a built-in potential $\phi_{bi}(>0)$ that is solution of the Poisson equation

$$-\nabla^2\phi = \frac{1}{\varepsilon_s}\rho(\mathbf{r}) \tag{2.23}$$

where ε_s is the dielectric permittivity of Si and $\rho(\mathbf{r})$ is the charge density. Accounting also for the effect of the minority carriers [50, 49] the following relation between transferred charges and ϕ_{bi} can be derived [51]:

$$Q_g + Q_s = \text{sign}\left(\phi_{bi} - \frac{k_B T}{q}\right)\left[2q\varepsilon_s N_a \left|\phi_{bi} - \frac{k_B T}{q}\right|\right]^{1/2} \tag{2.24}$$

where N_a is the acceptor density in bulk Si.
At equilibrium the Fermi levels of graphene and P-Si line up; however, if an energy difference V_{bias} is applied, the following balance equation is established:

$$\Phi_{g0} + \Delta E + q\Delta_{\text{int}} = \chi + E_{\text{gap}} - \delta E - q\phi_{bi} + qV_{\text{bias}} \tag{2.25}$$

The energy level of point A in Figure 2.13, that is the vacuum level of Si, can be used as reference for its derivation. The left-hand side (l.h.s) of Equation (2.25) is the graphene Fermi energy E_{Fg} with respect to A and the right hand side (r.h.s.) is the Fermi energy of the semiconductor, E_{Fs}, shifted upwards by the potential energy $qV_{\text{bias}} > 0$ with respect to E_{Fg}. The Dirac point in Gr is at $\phi_{g0} = 4.5\,\text{eV}$, below the vacuum level of graphene [36] and $\Delta E \equiv \Delta E(n_0 + \Delta n)$ is the energy difference between the actual Fermi level of graphene and the Dirac point, n_0 being the surface density of carriers in graphene before the junction is made. In the r.h.s. χ is the affinity, E_{gap} the energy gap of Si and δE is the Fermi energy of Si with respect to the upper bound E_v of the valence band in the bulk ($\delta E \simeq 0.24\,\text{eV}$ for $N_a = 10^{15}\,\text{cm}^{-3}$). Depending on the number of piled up graphene layers adhering the interface oxide, the functional form of $\Delta E(n_0 + \Delta n)$ may vary in close proximity of the Dirac point. For a single graphene layer, the expression 2.26 holds [36]:

$$\Delta E = \hbar v_F \pi^{1/2}\sqrt{n_0 + \Delta n} \tag{2.26}$$

While for 2/3 layers graphene the proper expression is reported in Equation (2.27):

$$\Delta E = \frac{\hbar^2\pi}{2m}(n_0 + \Delta n) \tag{2.27}$$

where v_F is the carrier Fermi velocity ($10^8\,\mathrm{cm\,s^{-1}}$) and $m \simeq 0.04 m_e$ is the effective mass (m_e being the electron mass) [52]. Since the Graphene Fermi level will always be distant from the Dirac point in the experimental conditions considered, Equation (2.26) will be adopted. Equations 2.21 and 2.26 are the basis for the derivation of the functional dependence of SBH (i.e. ϕ_B) on V_{bias} and other parameters characterizing the Gr/Si diode. In fact, the unbalance between forward and backward currents at the junction is central in determining the overall current profile $I(V_{\mathrm{bias}})$ observed, and this unbalance depends on V_{bias} non-trivially.

The metal-P-Si junction In order to better understand this point, we start considering an unbiased metal/P-Si junction (without interfacial oxide and in absence of surface states), as illustrated in Figure 2.14. To have a Schottky contact, the work function Ψ_m of the metal is lower than that of the semiconductor and, once the junction is made, electrons transfer from the metal to a layer of the semiconductor next to the interface until E_{Fm} (which remains stable relative to the vacuum level, due to the high density of states in metals) and E_{Fs} line up. This charge transfer establishes a potential profile $\phi(x)$, the built-in potential being $\phi_{bi} \equiv \phi|_{x=0}$, and an electric field $E = -d\phi/dx$; the bands' bending is assumed not to induce inversion (see Figure 2.14).

Electron-hole pairs which form at the Si surface tend to separate due to the electric field; if the electron energy increases by more than the threshold Φ_B with respect to the top of the valence band at the interface, then it may transfer to the metal. At equilibrium, with $V_{\mathrm{bias}} = 0$, this process is exactly compensated by an opposite one in which another electron leaves the metal and crosses the interface, so that at equilibrium the overall current is zero. Applying a small forward polarization (the metal at a negative potential with respect to P-Si), the Fermi energy E_{Fm} in the metal rises above E_{Fs} by $|qV_{\mathrm{bias}}|$; the holes in P-Si are attracted to the surface, the depletion layer gets thinner and ϕ_{bi} decreases. The electrons at the Fermi level in the metal migrate toward P-Si if free holes are created at its surface for the effect of thermal generation and could be occupied by the electrons; this can happen if a valence electron at the surface gains an energy of at least $\phi_B = q\phi_{bi} + \delta E$. While the electrons generated at the P-Si surface would cross at least a barrier $\phi_B + qV_{\mathrm{bias}} (> q\phi_{bi})$ to tunnel towards free states in the metal. In these conditions the electron current from the metal overwhelms the electron current from the semiconductor. Under reverse polarization (the metal at a positive potential with respect to Si), holes in P-Si are repelled from the interface, that is, a thicker depletion layer establishes, in which bulk acceptors are ionized, without a corresponding number of holes generated in the same region and ϕ_{bi} increases. A metal-to-Si electron current may flow toward the holes formed by thermal excitation at the P-Si surface, that are available for recombination with the metal electrons tunneling to the surface. Vice versa, a Si-to-metal electron current may flow provided electron/hole pairs form at the Si surface with an energy larger than $q\phi_{bi} + \delta E - (E_{Fs} - E_{Fm}) = q\phi_{bi} + \delta E - qV_{\mathrm{bias}}$. These two current

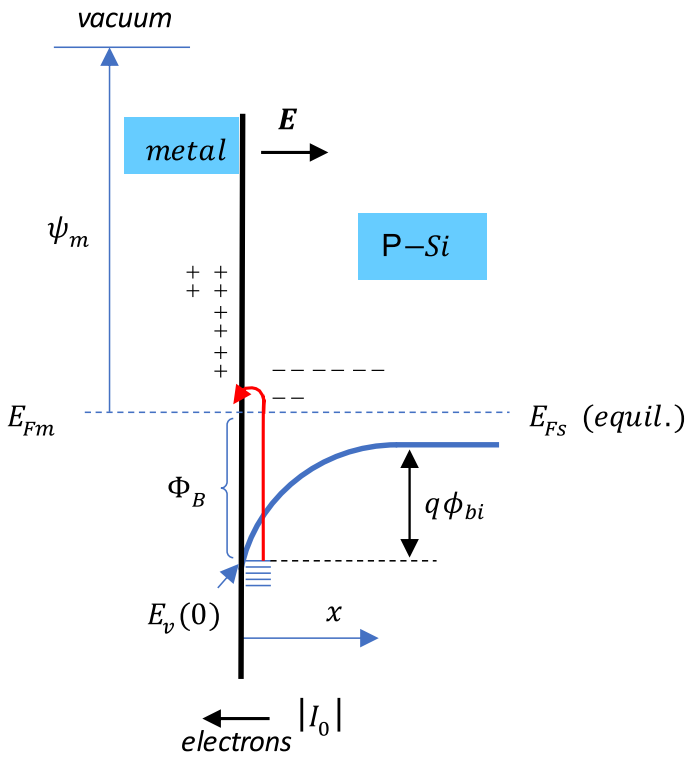

Figure 2.14: Metal/P-Si interface at equilibrium, upon formation of a Schottky barrier ($\psi_m < \chi + E_{\text{gap}} - \delta E$ before contact).

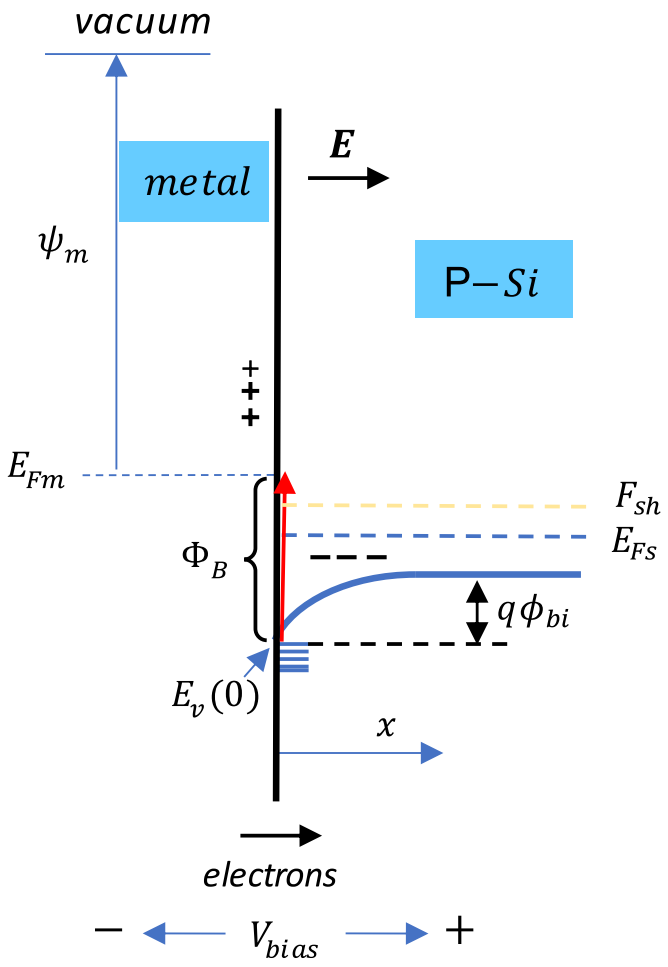

Figure 2.15: Low forward biased metal/P-Si junction in the case for Si bands still maintaining a downwards curvature (i.e. a depletion layer still exists). In presence of a current, the actual hole density would be described as at equilibrium condition by adopting a hole quasi-Fermi level $F_{sh} > E_{Fs}$.

contributions oppose each other, but the Si-to-metal electron current overwhelms the former. Figure 2.15 shows the case of a metal/P-Si junction with a constant applied forward bias, in a stationary, non-equilibrium condition.

The graphene/P-Si junction Coming back to the graphene/P-Si system envisaged in Figure 2.13, we have to take into account three issues in order to develop a proper analysis: the dependence of $E_{vacuum} - E_{Fg}$ on the number Δn of exchanged charge carriers, the finite surface density of states and the presence of an interfacial oxide (interfacial inhomogeneities will not be considered). The simple behavior described by Equation (2.4) is reasonably applicable only within a limited biasing interval, that is, when in direct polarization $|V_{\text{bias}}|$ does not exceed the flat-band potential $|V_{f-b}|$, and in reverse polarization it cannot exceed the potential range in which minority carriers start being relevant (inversion condition). At $V_{\text{bias}} = V_{f-b}$, indeed, the biasing exactly compensates the built-in potential established at equilibrium, when $E_{Fg} = E_{Fs}$; the energy bands' profiles flatten and the electric field is zero. Upon further increasing of $|V_{\text{bias}}|$, the bands tend to slightly bend upwards and holes then accumulate towards the surface (Figure 2.16), and are available to recombine with the electrons that tunneling from graphene, easily can occupy lower energy states. Strong reverse polarization, instead, causes a significant downwards bending of the energy bands in Si. When the intrinsic Fermi level E_{Fi} crosses E_{Fs}, a layer of electrons forms at the semiconductor surface and the mechanism of supplying the tunneling of charge carriers towards graphene changes (see Figure 2.17). Both situations are described in details in the following paragraphs.

2.4.1 Direct polarization beyond the flat-band potential

Figure 2.16 shows the case of a Gr/P-Si, with a single graphene sheet, under forward polarization, with $|V_{\text{bias}}| > |V_{f-b}|$. In these conditions $\phi_{bi} < 0$ and holes from the bulk tend to accumulate at the surface of the semiconductor. As a semi-phenomenological approach, it is assumed that the diode current is proportional to the number Δn_h of holes that accumulate at the Si interface (or to some power of it with an exponent α not larger than one, as it will be motivated below), which can host the electrons coming from Gr. Therefore, the current can be expressed using the following phenomenological equation:

$$I = AJ\Delta n_h^{\alpha} \tag{2.28}$$

where A is the area of the diode and J is a fitting parameter, accounting in particular for the tunneling attempt rate of the electrons. In order to calculate Δn_h as a function of V_{bias}, one proceeds by solving the 1-dimensional Poisson equation (see Equation (2.23)) for the associated potential ϕ, in which the source term is the excess charge density over

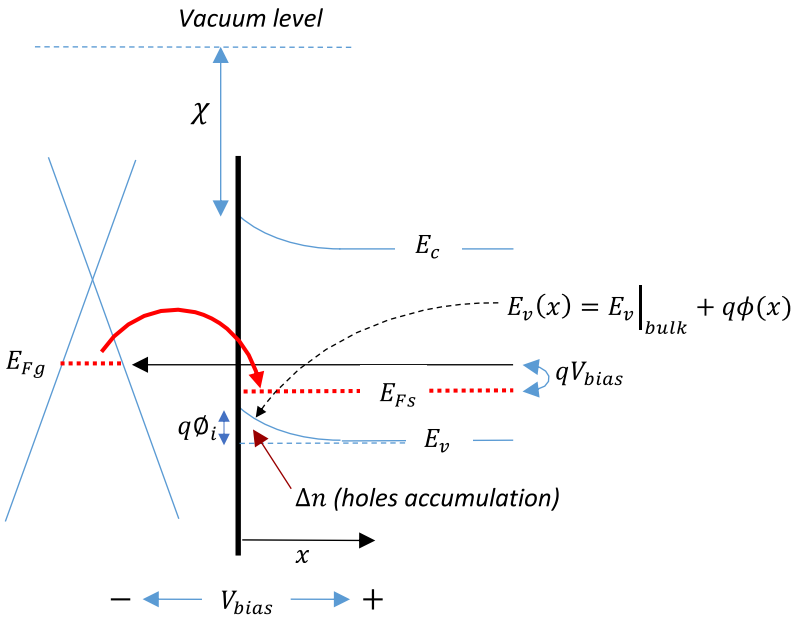

Figure 2.16: Energy diagram for a Gr/P-Si diode under direct polarization beyond the flat band potential.

p_0, being p_0 the un-perturbed (bulk) hole density:

$$\rho(x) = qp_0 \left[\exp\left(-\frac{q\phi(x)}{k_B T} - 1 \right) \right] , \tag{2.29}$$

adopting the conditions

$$\phi \to 0 \quad \text{and} \quad E = -\frac{\mathrm{d}\phi}{\mathrm{d}x} \to 0 \quad \text{for} \quad x \to \infty , \tag{2.30}$$

the solution yields for the electric field

$$E = -\frac{\mathrm{d}\phi}{\mathrm{d}x} = \pm \sqrt{\frac{2p_0 k_B T}{\varepsilon_s} \left(\frac{q\phi}{k_B T} + \exp\left(-\frac{q\phi}{k_B T} \right) - 1 \right)} \tag{2.31}$$

Since the potential $\phi \leq 0$, the derivative $\mathrm{d}\phi/\mathrm{d}x$ must be positive, so the solution with positive sign in Equation (2.31) must be discarded. The excess electric field consistently points from P-Si towards graphene (the potential $\phi(x)$ can be obtained by further integration of Equation (2.31), although in non-closed form). The carrier number Δn_h is then related to the electric field established at the surface of the semiconductor through the Gauss theorem:

$$\frac{q\Delta n_h}{\varepsilon_s} = \left. \frac{\mathrm{d}\phi}{\mathrm{d}x} \right|_{x=0} \equiv f(\phi_{bi}) \tag{2.32}$$

Equation (2.32) provides Δn_h as a function of ϕ_{bi}, since $\phi_{bi} \equiv \phi|_{x=0}$. It's important to notice that through Equation (2.32) the balance Equation (2.25) provides the dependence of excess carriers $\Delta n_h(\phi_{bi})$ on V_{bias}.

It's important to notice that the Δn_h vs. V_{bias} dependence thus found, strictly holds in the hypothesis that no current flows; indeed, all the equations above relate to the equilibrium case. When the current flows, one has to take into account some deviation from the "static" situation (as explained at the end of the previous section, with the introduction of the hole quasi-Fermi level to which Figure 2.15 refers). In particular, it is expected that the injection of electrons slightly reduces the number of holes Δn_h with respect to the equilibrium case, due to a finite hole refilling rate from the Si bulk; this circumstance supports the presence of an exponent $\alpha \leq 1$ in Equation (2.28). A further argument supporting an exponent lower than unity is the fact that electrons recombine mainly with holes sufficiently proximal to the Si surface (cf. Figure 2.16).

2.4.2 (Moderately) strong reverse polarization

Applying a reverse polarization, the energy bands of P-Si tend to bend downwards as ϕ_{bi} (now positive) increases. This mechanism proceeds on increasing $|V_{\text{bias}}|$ until the intrinsic Fermi energy E_{Fi} closely approaches and then crosses the P-Si equilibrium Fermi energy E_{Fs}. When this happens, a significant part of minority carriers is promoted to the conduction band, forming an inversion layer at the semiconductor surface. This layer is negatively charged and provides electrons which are more directly involved in reverse current. The following treatment is devoted to a semi-quantitative description of a conduction mechanism that is believed to be possibly responsible of the experimental observations (Figure 2.17 depicts this situation). No data fitting are performed in the strong reverse-biased region of these systems. When the intrinsic energy level E_i approaches E_{Fs}, the minority carriers only need to overcome an energy barrier $\delta\text{E} \ll \frac{1}{2} E_{\text{gap}}$ and the occupation of the conduction band by electrons is favored. The upper panel of Figure 2.17 schematically illustrates both the energy diagram of the system and the position of the inversion (negative) layer near the surface; the lower panel instead, shows the adopted absolute value of the charge density $|\rho(x)|$ with the square block approximation used for calculations. The potential $\phi(x)$ can be formally estimated from the Poisson equation with a source term described as in Figure 2.17, where w and d are the thicknesses of the depletion and of the inversion layers, respectively. The central quantity, however, will be ϕ_{bi}; so, afterwards, the charge density within the inversion layer will be expressed in terms of ϕ_{bi} and arriving at a self-consistent transcendental equation to be solved numerically for ϕ_{bi}. Setting $\phi(w) = 0$, $\frac{\mathrm{d}\phi}{\mathrm{d}x}|_{x=w} = 0$ and imposing continuity of the solution and of its derivative at $x = d$, one finds

$$\phi(x) = \frac{q}{2\varepsilon_S}\left\{n_i x^2 + 2[N_a(d-w) - n_i d]x + N_a(w^2 - d^2) + n_i d^2\right\} \tag{2.33}$$

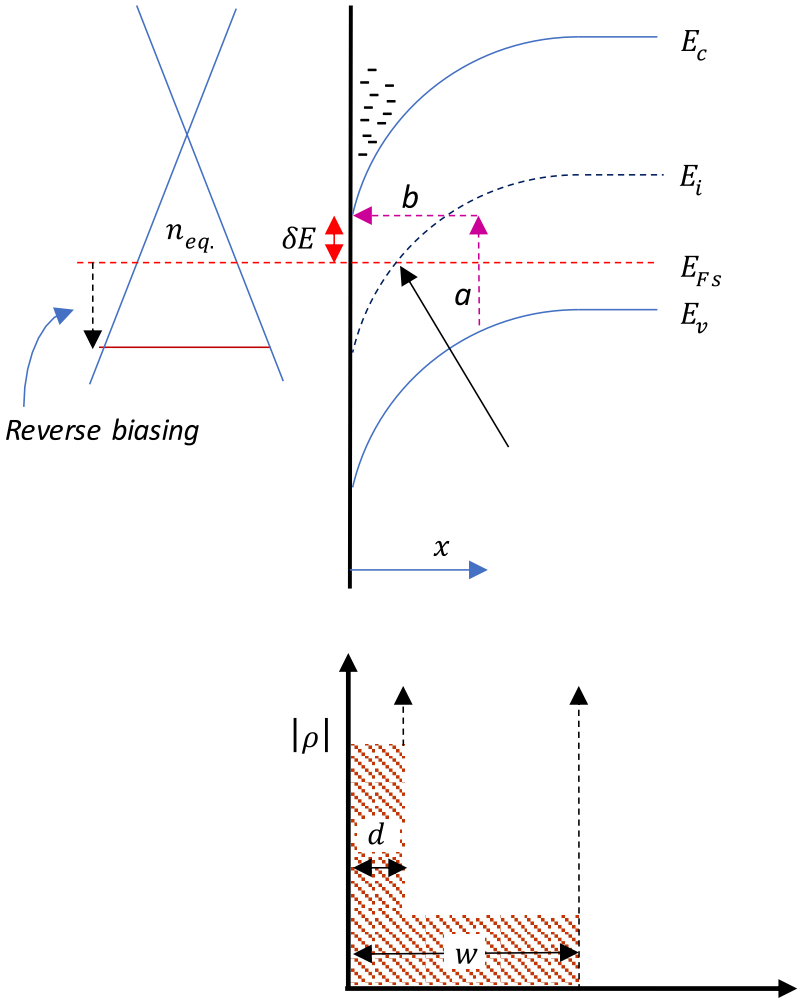

Figure 2.17: Energy diagram for the system Gr/P-Si in reverse polarization, with the illustration of the inversion layer that forms near the silicon surface (upper panel). Lower panel shows the square block approximation adopted for charge density in calculations.

where n_i is the electron density in the interval $0 < x \leq d$.
For the system Gr/Si considered here ($n_0 \sim 10^{13}\,\mathrm{cm}^{-2}$, $N_a = 10^{15}\,\mathrm{cm}^{-3}$ in Si), the condition for the onset of inversion ($\phi_{bi} \equiv E_{\mathrm{gap}}/2$) is reached at $|V_{\mathrm{bias}}| \sim 0.4\,\mathrm{V}$ in reverse polarization, with a thickness of the depletion layer $w \simeq 800\,\mathrm{nm}$ and $\phi_{bi} \simeq 0.56\,\mathrm{V}$. Figure 2.18 shows calculated $\phi(x)$ as a demonstrative example for $d \simeq 200\,\mathrm{nm}$ and considering 3 values for the electron density: $n_i = 10^{15}, 1.5 \times 10^{16}$ and $3 \times 10^{16}\,\mathrm{cm}^{-3}$. (In real samples the width of the inversion layer would be much smaller, also due to the very high density of states, $\sim 10^{19}\,\mathrm{cm}^{-3}$, at the conduction band edge of Si).
In order to find the built-in potential ($x = 0$) in the actual situation, one sets

$$n_i = N_c \frac{2}{\sqrt{\pi}} F(\xi) \quad \text{and} \quad \xi = -\frac{E_{\mathrm{gap}} - \delta E - \phi_{bi}}{k_B T} \tag{2.34}$$

in Equation (2.33), where N_c is the density of states at the edge of the conduction band ($N_c \simeq 10^{19}\,\mathrm{cm}^{-3}$ for Si) and $F(\xi)$ is the Fermi integral of order 1/2 [53]:

$$F(\xi) = \int_0^\infty \frac{x^{1/2}}{1 + \exp(x - \xi)} \mathrm{d}x\,. \tag{2.35}$$

Resorting to the Fermi integral is necessary because, within the inversion layer, the semiconductor is degenerate, that is, the Fermi level is close to (if not merged in) the energy interval occupied by the electrons.
As anticipated, the built-in potential is obtained numerically from the zeroes of the function.

$$\Psi(\phi_{bi}) \equiv \frac{q}{2\varepsilon_s}\left[N_a(w^2 - d^2) + d^2 N_c \frac{2}{\sqrt{\pi}} F\left(-\frac{E_{\mathrm{gap}} - \delta E - \phi_{bi}}{k_B T}\right)\right] - \phi_{bi} \tag{2.36}$$

Figure 2.19 reports the behavior of the function in Equation (2.36) in the interval $0 \leq \phi_{bi} \leq 1\,\mathrm{V}$, for $T = 27\,^\circ\mathrm{C}$ and $T = 120\,^\circ\mathrm{C}$ and for different values of w and d. The solution of interest for $\Psi(\phi_{bi}) = 0$ is the larger between the two possible ones, because the larger value corresponds to the case of large band bending, which guarantees the formation of the inversion layer. Of course, Equation (2.36) relies on the square charge profile approximation (Figure 2.17), so that functional behaviors similar to those represented in Figure 2.19 are expected to be found also for d values (much) smaller than those used for calculations and reported in the caption. Figure 2.19 shows that ϕ_{bi} changes only weakly upon reducing the thickness of the depletion layer at fixed T (solid black and dashed green curves at 27 °C , or dotted red and blue curves at 120 °C), while on increasing the temperature with constant w and d, ϕ_{bi} increases significantly (dashed green and dotted red curves).

Figure 2.20 shows the relevant solution ϕ_{bi} as a function of the inversion layer thickness at room temperature ($k_B T = 0.026\,\mathrm{eV}$), for different thickness values of the depletion layer, w. It can be noticed that ϕ_{bi} decreases from 0.82 V down to 0.7 V on changing d

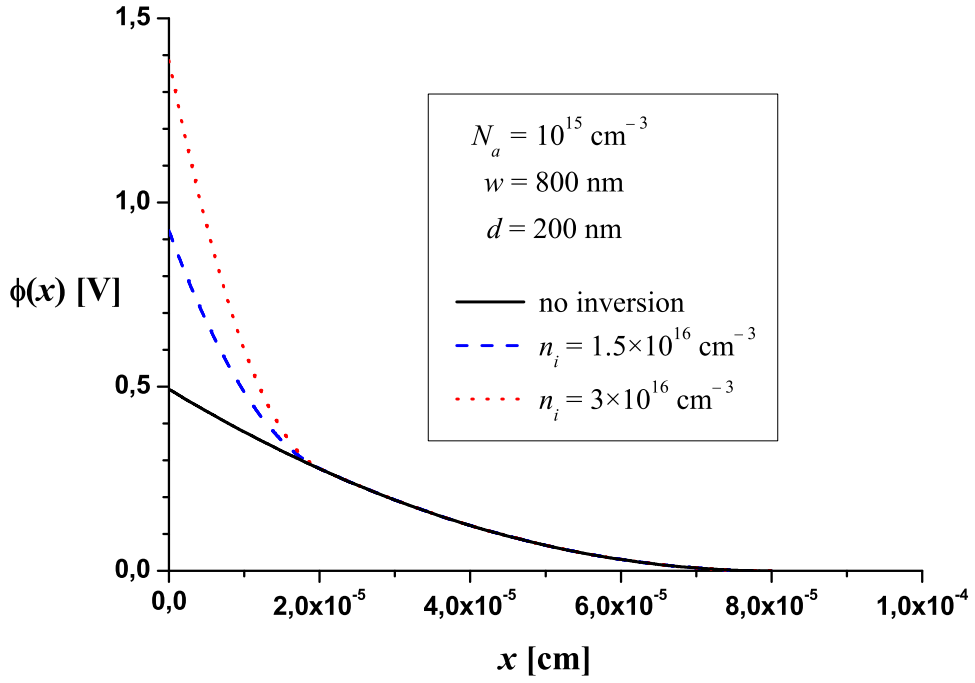

Figure 2.18: Excess potential $\phi(x)$ after Equation 2.33 calculated as an illustrative example in the three conditions reported in the legend.

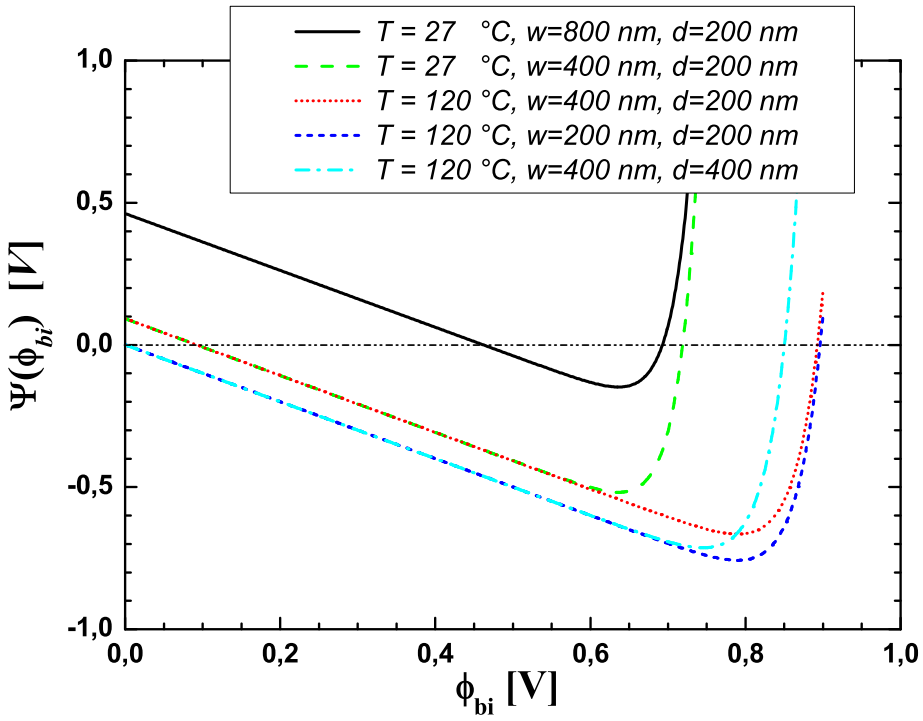

Figure 2.19: $\Psi(\phi_{bi})$ after Equation (2.36) for different values of the temperature (T), thickness of the depletion layer (w) and of the inversion layer (d), as reported in the legend.

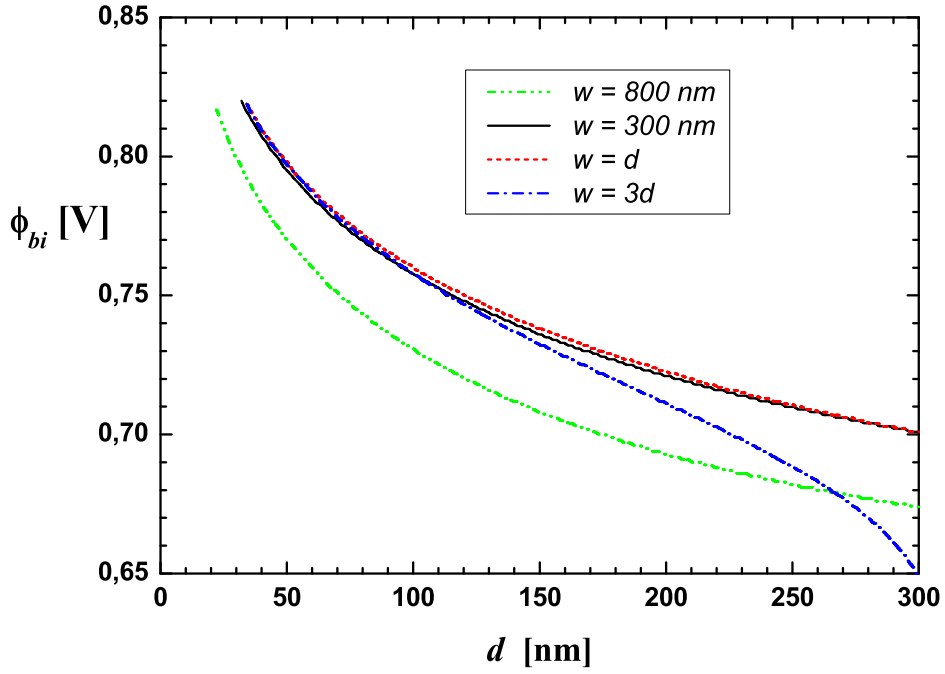

Figure 2.20: The relevant solution of Equation 2.36 as a function of the inversion layer (d) for different values of the depletion layer thickness w, at a temperature $T = 27\,^{\circ}\mathrm{C}$. The $w = 3d$ line is plotted just to show how the situation relative to small w merges into that of large w.

from 40 to 300 nm, while it's only slightly influenced by the thickness of the depletion layer (green dash-dotted and red dotted lines).

Considering all the results so far obtained, it seems likely that once the marginal conditions for inversion are reached, the formation of the inversion layer may rapidly come to completion. There is indeed a sort of self-sustainment of the field $\phi(x)$ due to the accumulation of the minority carriers towards the surface, which can also persist even if the thickness w of the depletion layer reduces to the inversion layer, d. In other words, the depletion layer that must necessarily develop to trigger inversion, may change afterwards without compromising the stability of the inversion layer itself. The problem of estimating the depth d to which the negative charge profile extends, depends on the amount of charge moving from graphene (on reverse polarization potential V_{bias}) and on the thermodynamic stability of the charge distribution in Si. Note indeed that ϕ_{bi} increases on rising k_BT (dashed green and dotted red lines in Figure 2.19) and decreases yet on increasing d, as illustrated in Figure 2.20. It's useful to underline that in this discussion the dependencies $\phi_{bi} \simeq \phi_{bi}(k_BT, d)$ are to be considered rather qualitative, given the approximation introduced with the assumed charge density profile reported in Figure 2.17. In conclusion, from above calculations, a built-in potential $\phi_{bi} \sim 0.7$–$0.8\,\text{V}$ may be expected to establish by inversion.

Under reverse polarization $E_{Fg} < E_{Fs}$ and, in the presence of an inversion layer, $E_{Fg} < |E_c|_{x=0}$. The electrons that more than others are available for tunneling are those already at the Si surface, i.e. those forming the inversion layer. Because of the self-sustainment of the potential profile, any electron tunneling away from Si needs to be replaced by another one formed as a consequence of an electron/hole pair formation close to the inner border of the inversion layer. In the upper panel of Figure 2.17 the arrows labelled as "a" and "b" indicate a possible path for the electron replacement. Electron migration through path "b" in Figure 2.17 is enhanced by the electric field $-\text{d}\phi/\text{d}x$, while the hole would drift towards the bulk of the semiconductor as the charge carrier of the reverse current in P-Si. The overall process would require an energy fluctuation $\phi \simeq E_{\text{gap}} - q\phi_{bi} \simeq 0.35 - 0.4\,\text{eV}$ and would represent the SBH in strong reverse polarization. It is worth to note that indeed the SBH values extracted from experimental I-V curves fall within this scale in the majority of cases (see Figure 2.8, yellow line).

2.4.3 Data analysis

The experimental $I - V$ curves obtained for the Gr/Si diodes fabricated in this thesis have been used for data analysis. When the experimental $I - V$ data obtained for a DRY Gr/P-Si diode (sample D3, at the temperature of $T = 80\,^{\circ}\text{C}$) are fitted using Eq. 2.4 (down triangles in Fig. 2.21), the following diode's parameters are obtained: n ~ 4, $A^* = 7 \times 10^{-7}\,\text{A}\,\text{cm}^{-2}\,\text{K}^{-1}$, and $\phi_{B0} = 0.21$ eV. The fitting is quite good, but only in the range where thermionic regime holds (cfr Fig. 2.22), and is stopped at $V = 0.1V$,

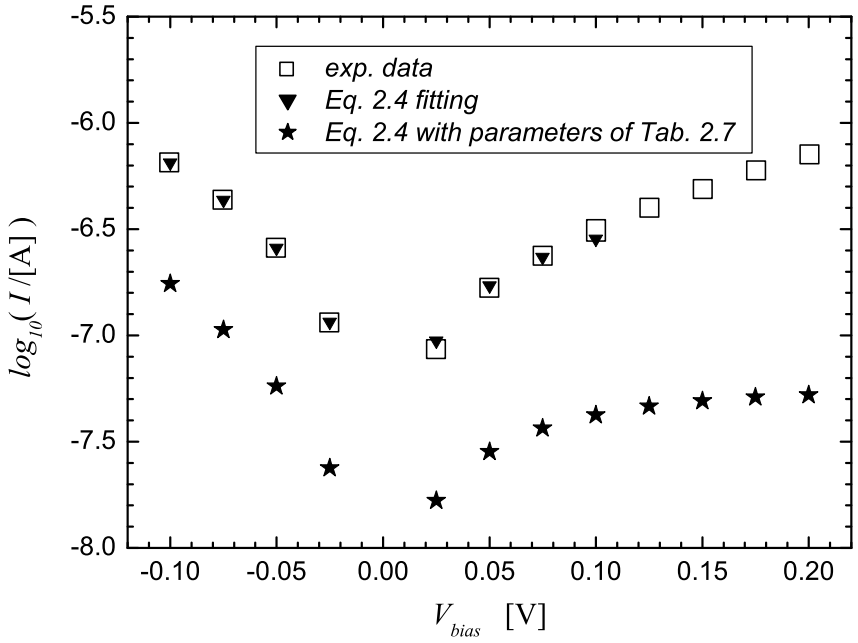

Figure 2.21: Experimental $I-V$ data (open squares) for a DRY Gr/P-Si diode (sample D3, $T = 80\,^{\circ}\mathrm{C}$) are fitted using Eq. 2.4 (down triangles), yielding the following parameters: n $\sim$ 4, $A^* = 7 \times 10^{-7}\,\mathrm{A\,cm^{-2}\,K^{-1}}$, and $\phi_{B0} = 0.21$ eV. The stars represent the I-V values obtained for the same device introducing in Eq. 2.4 the diode's parameters extracted using classical methods and reported in Tab. 2.7 (n $\sim$ 2.4, $A^* = 1 \times 10^{-7}\,\mathrm{A\,cm^{-2}\,K^{-1}}$, and $\phi_{B0} = 0.23$ eV).

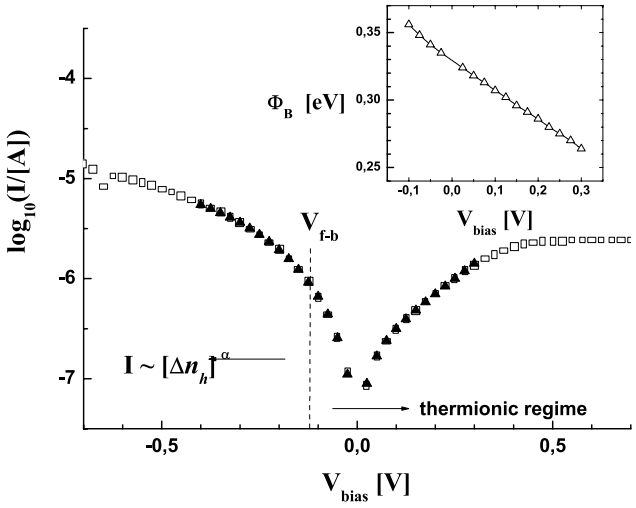

Figure 2.22: Fitting of experimental $I-V$ data for a DRY Gr/P-Si diode (sample D3, $T = 80\,^{\circ}\mathrm{C}$). Values $n_0 \simeq 10^{13}\,\mathrm{cm}^{-2}$ and $N_a = 10^{15}\,\mathrm{cm}^{-3}$, and an oxide thickness of 1 nm, are assumed for the fitting.

which suggests that the physics described by Eq. 2.4 is over-simplified. Eq. 2.4 is also used to calculate the diode $I-V$ behavior introducing the parameters reported in table 2.7, extracted with classical methods. The calculated $I-V$ values are represented by stars in Fig. 2.21. We can notice that in this case there is a great discrepancy between experimental and calculated $I-V$ data, mainly due to the fact that Eq. 2.4 does not include the effect of surface states. The high n values obtained so far is related to the V_{bias} dependence on Φ_B (this can be checked simply substituting $\Phi_B = \Phi_{B0} + \frac{V\partial\Phi_B}{\partial V}$ in place of Φ_{B0} in Eq. 2.4).

In Fig. 2.22 the same experimental data are fitted with the model illustrated in the previous paragraphs, mainly based on theoretical expression of Equations 2.25 and 2.28. The values $n_0 \simeq 10^{13}\,\mathrm{cm}^{-2}$ and $N_a = 10^{15}\,\mathrm{cm}^{-3}$ were assumed for doping of graphene and silicon respectively, and it is expected that $V_{f-b} \simeq -0.085\,\mathrm{V}$ in the hypothesis that no significant band-bending is caused by surface states. An effective oxide layer thickness $d = 1\,\mathrm{nm}$ was assumed, consistently with the presence of more than one graphene sheet piled up on the Si-surface to form the device. Given the relatively large carrier density n_0, Equation (2.26) was adopted. The analysis yields an optimal value of $D_i \approx 10^{12}\,\mathrm{cm}^{-2}\,\mathrm{eV}^{-1}$, while surface donor states are located in an energy interval $q\phi_0 - E_{Fs} \sim 0.2\,\mathrm{eV}$ as found from fitting. The electrons provided by the surface donor states contribute to the downwards bending of the valence band; this contributes to an increase of $|V_{f-b}|$. For larger values of forward bias, the thermionic model does

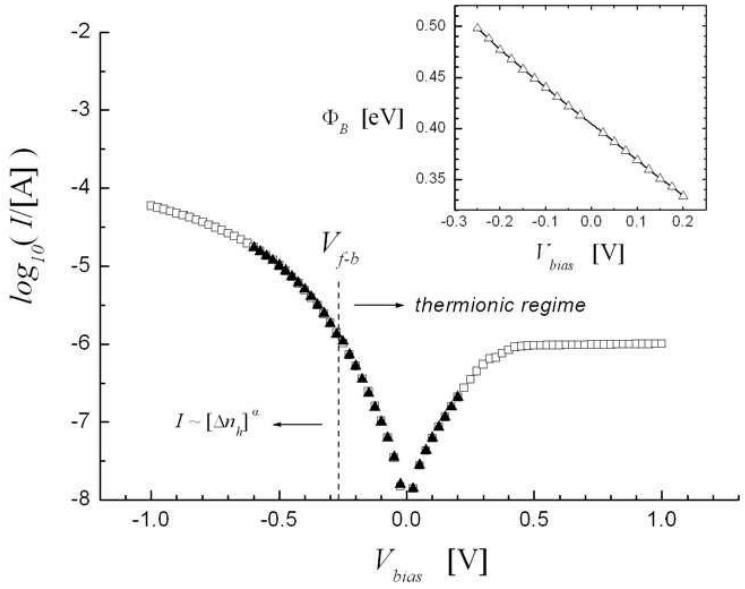

Figure 2.23: Fitting of experimental $I - V$ data for a WET Gr/P-Si diode (sample B7, $T = 80\,^{\circ}\mathrm{C}$). Values $n_0 \simeq 10^{13}\,\mathrm{cm}^{-2}$, $N_a = 10^{15}\,\mathrm{cm}^{-3}$, and an oxide thickness of 1 nm, are assumed for the fitting. (Note that, differently from the data reported in the following Table 2.6, here the interval of the fitting is extended up to $V_{\mathrm{bias}} = -0.6\,\mathrm{V}$ to better show the overall fitting quality; the values obtained for J and α differ very little from those reported in the table.)

Table 2.5: Fitting results for the DRY Gr/P-Si diode D3-sample obtained for the different temperatures T.

T [°C]	ΔV_{bias} [V]	V_{F-B} [V]	D_i [$cm^{-2}eV^{-1}$]	$q\phi_0 - E_{Fs}$ [eV]	Φ_{B0} [eV]	$\partial\Phi_{B0}/\partial V_{bias}$ [$eV\ V^{-1}$]	n	A^* [$Acm^{-2}K^{-2}$]	J [Acm^{-2}]	α
27	$-0.4 \div 0.1$	0.14	$(1.11 \pm 0.01)\times10^{12}$	0.32	0.34	-0.21	1.3	$(1.80 \pm 0.02)\times10^{-5}$	3.6×10^{-4}	0.78
60	$-0.4 \div 0.25$	0.12	$(1.27 \pm 0.01)\times10^{12}$	0.22	0.33	-0.23	1.5	$(1.46 \pm 0.02)\times10^{-5}$	1.3×10^{-3}	0.71
80	$-0.4 \div 0.3$	0.12	$(1.26 \pm 0.02)\times10^{12}$	0.22	0.33	-0.23	1.4	1.000×10^{-5}	1.1×10^{-3}	0.62
100	$-0.4 \div 0.3$	0.12	$(1.49 \pm 0.06)\times10^{12}$	0.19	0.33	-0.25	1.3	5.327×10^{-6}	1.7×10^{-3}	0.68
120	$-0.4 \div 0.3$	0.12	$(1.40 \pm 0.04)\times10^{12}$	0.20	0.33	-0.24	1.3	4.733×10^{-5}	2.0×10^{-3}	0.66

not apply anymore and the system enters an ohmic conduction regime described by Equation (2.28). Relevant quantities for the discussion are: the polarization interval ΔV_{bias}; the flat band potential V_{f-b}; the surface density of states D_i; the energy interval $q\phi_0 - E_{Fs}$ of the surface states above the Fermi energy of Si; the zero-bias SBH ϕ_{B0}; the ϕ_B vs. V_{bias} dependence (through $\phi_B \equiv \partial\phi_B/\partial V_{\text{bias}}$); the ideality factor n; the Richardson constant A^*; the ohmic regime current density factor J and the exponent α of Equation (2.28). As fitting strategy, the ideal diode Equation (2.4) is first adjusted in the domain $V_{\text{bias}} > V_{f-b}$, while being cautious in carefully limiting V_{bias} within suitable moderate reverse biases. To obtain a good fit, one sets starts with a low upper limit to $q\phi_0 - E_{Fs}$, then this constraint is progressively released upon successive fitting runs, until a stable value is obtained for $q\phi_0 - E_{Fs}$. In doing this, V_{f-b} is recalculated each time, as it depends on the number of ionized surface states; the fitting interval for Equation (2.4) is re-defined accordingly. In each iteration, the ohmic regime domain (for $V_{\text{bias}} < V_{f-b}$ is fitted after the balance Equation (2.25) is reset as a result of the previous ideal diode analysis performed in the interval $V_{\text{bias}} > V_{f-b}$; indeed, the function $\Delta n_h(V_{\text{bias}})$ is defined through the balance Equation (2.25). The above steps are iterated until a "fixed point" is reached for all parameters. Table 2.5 summarizes the fitting results obtained for measurements on sample D3, performed at different temperatures.

The values $n_0 \simeq 10^{13}\text{cm}^{-2}$ and an oxide layer thickness $d = 1\,\text{nm}$ have been assumed for the fitting. The values obtained for the ideality factor, n, indicate good quality devices. The zero-bias SBH, Φ_{B0}, is found by interpolation of the $\phi_B(V_{\text{bias}})$ values worked out from the fitting and reported in the inset of Figure 2.22 (note that the ϕ_B-domain is limited to $V_{\text{bias}} > V_{f-b}$, i.e. where Equation (2.4) holds). Differently from classical extraction methods, ϕ_{B0} is derived here from the analysis of the $I(V_{\text{bias}})$ behavior at just one temperature, and the results are quite independent of the temperature at which the data were collected. The barrier ϕ_{B0} depends on the band curvature that establishes at equilibrium when graphene and P-Si are put into contact: the larger the curvature, the larger ϕ_{B0}. The result of a fitting procedure with the present model is indeed sensitive to i) the charge carrier density n_0 assumed for the calculations and ii) the surface density of states and the energy difference $q\phi_0 - E_{Fs}$ between the highest occupied surface donor

Table 2.6: Fitting results for the WET Gr/P-Si diode B7-sample at different temperatures T[°C].

T [°C]	ΔV_{bias} [V]	V_{F-B} [V]	D_i [$cm^{-2}eV^{-1}$]	$q\phi_0 - E_{Fs}$ [eV]	Φ_{B0} [eV]	$\partial\Phi_{B0}/\partial V_{bias}$ [$eV\ V^{-1}$]	n	A^* [$Acm^{-2}K^{-2}$]	J [Acm^{-2}]	α
60	$-0.4 \div 0.3$	0.19	$(1.60 \pm 0.08)\times10^{12}$	0.38	0.37	-0.26	1.3	$(8.24 \pm 0.23)\times10^{-6}$	2.5×10^{-4}	0.84
80	$-0.4 \div 0.2$	0.26	$(2.62 \pm 0.05)\times10^{12}$	0.37	0.4	-0.35	1.2	$(1.17 \pm 0.04)\times10^{-5}$	1.2×10^{-3}	1.45
100	$-0.4 \div 0.25$	0.24	$(2.69 \pm 0.08)\times10^{12}$	0.32	0.39	-0.36	1.1	$(4.38 \pm 0.16)\times10^{-6}$	1.3×10^{-3}	1.37
120	$-0.4 \div 0.3$	0.21	$(2.47 \pm 0.13)\times10^{12}$	0.3	0.38	-0.34	1.1	$(2.08 \pm 0.14)\times10^{-6}$	1.3×10^{-3}	1.2

level and the Fermi energy in the semiconductor. Thus, a central issue is that n_0 must be known with a good degree of reliability. Note that $\alpha < 1$ is obtained at all temperatures. The same analyses have been carried out on WET graphene/P-Si diodes. Figure 2.23 refers to sample B7 at $T = 80\,°\text{C}$ and $n_0 \simeq 10^{13}\text{cm}^{-2}$. The worked out fitting results are collected in Table 2.6.

In general, good fittings for WET-samples are characterized by a larger number of surface states, compared to the DRY-samples (this can be seen from both the D_i and the $q\phi_0 - E_{Fs}$ fitting values). This circumstance is responsible of a somewhat enhanced downwards curvature of the valence and conduction bands in Si, which leads to an increase in both $|V_{f-b}|$ and Φ_{B0}. It is worth to notice that in WET-samples the exponent *alpha* may well reach values larger than unity. Considering that the meaning of the relation $I \propto (\Delta n_h)^\alpha$ is that the total current is proportional to the number of available recombination sites in Si for the electrons that tunnel from graphene, thus the obtained $\alpha > 1$ values seem to indicate that the effective number of recombination sites is larger than the totality of the holes accumulated at the interface. Considering the larger effect of the surface states in $I - V$ of WET-samples, these results suggest that the empty surface states may play a role as transient recombination sites that add to the Δn_h (the dynamic excess negative charge on these states would attract further holes from Si bulk). Note that the surface states are certainly accounted for in the "equilibrium" balance equation (Equation 2.25), while the phenomenological expression of the current (Equation 2.28) does not; nonetheless the application of the latter in the fitting procedure provides a suggestion of the role played by the large number of surface states. This theme, with all its effects, will be considered for further investigations.

2.5 Conclusions

Several batches of Gr/Si Schottky junctions have been fabricated and characterized using the current-voltage measurements. Classical methods, developed and commonly used for

metal/Si junctions, have been applied to Gr/Si diodes demonstrating their limit of applicability and defining an optimized procedure for the extraction of the main Gr/Si diode parameters. In particular, it was demonstrated that an accurate evaluation of the Gr/Si Schottky barrier height at zero bias (Φ_{B0}) and of the ideality factor (n), using classical methods can be obtained uniquely investigating the temperature behavior of the Gr/Si junctions, and working in the forward region of the diode, for $\mid V_{\text{bias}} \mid < \mid V_{f-b} \mid$, where the current is dominated by the thermionic mechanism. Conversely, the commonly used approach based on the Cheung method, that extracts these parameters from a single $I-V$ measurement performed at room temperature, produces an estimation for the SBH in Gr/Si diodes that does not refer to the zero-bias condition, but to the high forward bias one. Similarly, the Richardson plot constructed for reverse biasing can be used to obtain an estimation of the SBH in the high reverse bias condition.
In order improve the understanding of the conduction mechanisms in the Gr/Si junction, a simple equation, consistent with experimental measures, has been proposed to account for the variation in the graphene Fermi level that occurs applying positive and negative biasing to the Gr/Si device.

Table 2.7 shows the comparison between the main Gr/Si junction parameters obtained using this fitting model and employing the classical extraction method. Before proceeding with the discussion, it's useful to underline some features:

- both methods take advantage of the same experimental data;
- the fitting procedure works on a single experimental measurement (performed at one temperature), and the value of Φ_{B0} and of the ideality factor are extracted in the thermionic emission region of the diode. It's worth to notice that modeling the measurements at different temperatures, the same value is always obtained for these parameters, confirming the solidity and reliability of the model used;
- differently, using classical extraction methods, the values for Φ_{B0} and the ideality factor are obtained from the Richardson semilogarithmic plot, fitting the values of reverse current I_S/T^2 at a fixed voltage, as a function of $1/T$. Therefore, this method requires to execute $I-V$ measurements at different temperatures for each device.

Comparing the results reported in Table 2.7, we can notice that the Φ_{B0} values derived using the fitting procedure are always larger than those derived from the Richardson plots on the same systems. The latter method, requiring the analysis of the $I-V_{\text{bias}}$ behavior of single diodes at different temperatures, yields results characterized by a dispersion around the mean of $\pm 10\%$, that is compatible with the dispersion obtained by fittings (such as those reported in Figs. 2.22 and 2.23), for which the extraction of Φ_{B0} depends significantly on the n_0 value used. In fact, a 100 mV shift in fitted Φ_{B0} is obtained

Table 2.7: Comparison between the main diode's parameters extracted from experimental $I-V$ curves working in the low forward bias region (in red) and using the fitting procedure (in black).

Device	$\emptyset_{B0}$ [eV]	n	A^* [A/cm^{2}K^2]	
Dry-B3	0,33	1,2	1E-5	model
	0,24±10%	2,4	3E-8	extracted
Dry-D3	0,33	1,3	1E-5	model
	0,23±13%	2,4	1E-7	extracted
Dry-E4	0,34	1,2	9E-6	model
	0,28±11%	2	2E-7	extracted
Wet-A7	0,34	1,2	5E-6	model
	0,28±7%	1,9	8E-9	extracted
Wet-B7	0,38	1,1	1E-5	model
	0,3±7%	2	8E-9	extracted
Wet-F7	0,4	1,1	2E-5	model
	0,27±4%	2,0	5E-8	extracted

changing the graphene doping in the range 0.7–1 10^{13}. This suggests that the use of more accurate values for n_0 would be required for a deeper and thorough discussion of the observed systematic deviations. In the future, the measure of the doping level in graphene (n_0) would be performed both at the beginning and at the end of the fabrication process.

Concerning the Richardson constant, the values obtained with both methods are much lower (in the order 10^{-5} – 10^{-6}A cm^{-2} K^{-2}) than those expected for 3D/3D systems. As explained in [38, 39], this is peculiar of the 2D/3D systems in a vertical diode configuration, where the reverse saturation current is not anymore controlled solely by the semiconductor, but also by the out-of-plane velocity of the charge carriers that move from graphene to silicon. The mean cross velocity $v_\perp$ can be obtained using Equation (2.37) below, as suggested in [39], where the reverse saturation current of the diode is expressed through the kinetics of charge carriers and the interface barrier height:

$$I_S = A^* T^2 \exp\left(-\frac{\Phi_{B0}}{k_B T}\right) \approx 4q\bar{v}_\perp n \exp\left(-\frac{\Phi_{B0}}{k_B T}\right) \tag{2.37}$$

being n the density of charge carrier contributing to the current flow. For 3D/3D P-Si based diodes, n is determined by the effective density of states of silicon, $N_c \simeq 2.8 \times 10^{19}$cm^{-3}, and for an appropriate Richardson constant ($A^* \approx 30$A cm^{-2} K^{-2} for P-Si) one finds $\bar{v}_\perp \simeq 1.5 \times 10^5$cm s^{-1}. For the values of A^* extracted from the fittings of Gr/Si diodes, one would get $\bar{v}_\perp \simeq 0.05$ cm s^{-1}. In order to take into account the role that

electronic properties of the 2D material plays in determining the charge transport across a 2D-3D Schottky junction, Ang developed a new model [38] where the current across the vertical graphene-semiconductor Schottky junction depends on T, and the reverse saturation current is expressed as follows:

$$I_S = C_{\mathcal{G}} \Phi_{B0} \bar{v}_{\perp} T \exp\left(-\frac{\Phi_{B0}}{k_B T}\right) \tag{2.38}$$

being $C_{\mathcal{G}}$ a constant related to the electronic properties of graphene:

$$C_{\mathcal{G}} = \frac{g_{sv} q k_B}{2\pi \bar{l}_{\perp} \hbar^2 v_F^2} \simeq 0.06\,\mathrm{C\,eV^{-1}\,cm^{-3}\,K^{-1}} \tag{2.39}$$

with $g_{sv} = 4$ the spin-valley degeneracy and $\bar{l}_{\perp} \simeq 0.335\,\mathrm{nm}$ the thickness of the graphene sheet (single graphene sheet), and $v_F = 10^8\,\mathrm{cm\,s^{-1}}$ the Fermi velocity. From Equations 2.38 and 2.39 one finds $\bar{v}_{\perp} \simeq 0.14\,\mathrm{cm\,s^{-1}}$ using the Φ_{B0} and A^* values extracted from the fitting and reported in table 2.7. The cross velocity $\bar{v}_{\perp}$ here obtained is very close to that found for single-sheet/n-Si devices as reported in [39]. Note that in the present case $\bar{v}_{\perp}$ has been estimated directly from actual fitting parameters derived at a single temperature. Similarly, applying Equations 2.38 and 2.39 to the $I-V$ measurements, we obtain a Φ_B in reverse bias of 0.49 eV and $\bar{v}_{\perp} \simeq 0.7\,\mathrm{cm\,s^{-1}}$, in quite good agreement with theoretical and fitted values.

Finally, concerning the ideality factor (n), we can observe that the value obtained are quite good. In fact, the ideality factor is introduced in the diode equation to account for deviations from the pure thermionic transport that possibly occur in the Schottky junction. The value obtained for n using the fitting procedure is slightly larger than 1, indicating that the Gr-Si junction approaches an ideal behavior (in the framework of validity of the model used). A higher value, around 2 is extracted using the classical method previously described, that works in the forward region for $V \to 0$, (where the thermionic conduction in the junction is predominant), confirming the good quality of the hybrid Graphene/silicon junctions fabricated in this thesis. This higher value is mainly due to the fact that n so obtained implicitly includes also the bias dependence of the SBH when Equation (2.4) is used to model the diode I-V.

Chapter 3

Graphene integrated photodetectors

Introduction

Photodetectors play a crucial role in several applications, like image sensors, spectrometry, biomedical imaging, and manufacturing monitoring. The photodetector market is currently served by silicon photodetectors, based on CMOS technology, that guarantees low cost, high maturity, good reliability and reproducibility, and high integration with electronics. But many applications require components operating in the infrared regime, where the absorption of silicon is poor, due to its indirect bandgap of 1.12 eV. Currently, high performance infrared photodetectors are based on not usual semiconductors, such as germanium or III-V semiconductors, that have been integrated in the SOI platform, providing new functionalities and the fabrication of more flexible components, operating in the near-infrared (NIR) and mid-IR (MIR) regime for telecommunications applications. However, this hybrid platform has some technological limitations, like the expensive and complex epitaxial process required for the growth of high-quality semiconductor materials on bulk Si (to reduce the lattice mismatch with Si of 4.3%, that induces high leakage currents), and their hard integration with the use of extra bonding processes, which hugely increase the fabrication costs, limiting the final applications only to high-value markets. Considering this scenario, an all-Si approach with the integration of 2D materials in the silicon platform for the fabrication of photodetectors is gaining extensive interest and 2D/Si Schottky diodes are quite promising detectors for their broadband optical absorption and high carrier dynamics [54]. In particular, as already shown in the previous chapters, the graphene-silicon Schottky platform is simple and suitable for the integration in the back end-of-line (BEOL) CMOS fabrication process, enabling large scale fabrication.

3.1 Graphene-silicon Schottky photodetectors

Among the different type of graphene photodetectors, the Schottky diode structure represents one of the most promising approaches for fabrication of Si-based photodetectors with high performances. The use of graphene for fabrication of Schottky diodes is of great interest for the following reasons:

- graphene can be prepared at wafer scale by CVD, a well-known technique with high reproducibility and high throughput, and can be easily transferred to almost any substrate. In particular, graphene is suitable for the monolithic integration with CMOS technology, enabling the fabrication of Gr-Si Schottky detectors, without introducing costly steps in the process.

- the photodetection area is defined by the area where graphene is in contact with the silicon substrate, therefore is limited only by the dimensions of the CVD graphene. Therefore, large area photodectors can easily be fabricated.

- the Schottky configuration has better performances (higher speed and responsivity), compared to graphene-FET detectors. In fact, Gr-Si Schottky diodes have a vertical configuration and the photo-generated carriers pass through the thin graphene layer and are directly absorbed by Si. Instead, in a graphene-FET structure the photo-generated carriers are transported horizontally (from source to drain) and lot of them recombine before reaching the metal contact; therefore, the collecting mechanism is slow and reduces the absorption and therefore the responsivity of the detector. Moreover, graphene-FET based detectors suffer of high dark current, because they have a linear behavior, with current flowing when a voltage is applied between source and drain, even when the laser is off. For the Gr-Si Schottky detectors the dark current is the diode reverse saturation current, which is very low.

- The vertical configuration of Gr/Si Schottky diodes permits also to obtain high internal quantum efficiency (η_{int}). η_{int} is defined as the ratio between the number of photocarrier emitted from Gr and absorbed into silicon (N) and the number of the total photons absorbed in graphene, (graphene absorption is 2.3%):

$$\eta_{\text{int}} = \frac{N}{N_T} \tag{3.1}$$

To evaluate η_{int} for the graphene/Si Schottky junction, three important factors have to be considered: i) the photo-generated carriers move vertically, so that all the photo carriers in graphene have the same probability to be transferred and absorbed in Si, (as already mentioned, the effective detection area is the area where graphene and Si are

in contact, and is defined by graphene dimensions); ii) the relatively short lifetime of photogenerated carriers does not limit the number of carriers transferred to Si, because the mean recombination length of carriers is larger than the graphene thickness, therefore all photogenerated carriers can be absorbed before recombining; iii) graphene has π orbitals perpendicular to its surface, that are responsible of carrier conductivity. These orbitals provide only two directions for graphene carriers' momentum: towards silicon or in the opposite direction. Therefore, almost half of graphene's carriers have a chance to enter the Si. For all these reasons, the internal quantum efficiency of graphene Schottky diodes can be higher than that obtained for 3D materials, and can be expressed as [55]:

$$\eta_i = \frac{1}{2}\frac{(h\nu)^2 - (q\phi_B)^2}{(h\nu)^2} \tag{3.2}$$

where $h\nu$ is the photon energy and ϕ_B is the Schottky barrier height of the Gr/Si junction. Under a 1550 nm excitation laser, the energy of incident photon is 0.8 eV, therefore to have high internal quantum efficiency the Schottky barrier of Gr/Si diode must be low [56].

Table 3.1 allows a comparison of the main performances for the 2D materials-Si NIR photodiodes

3.2 Internal photoemission (IPE) in Schottky diodes

The absorption mechanism in Metal/Si Schottky junctions is based on the internal photoemission effect (IPE): the photons incident on a metal-Si interface, having an energy below the silicon bandgap, generate photo-excited carriers in the metal with an energy higher than the junction Schottky barrier. These carriers are injected into silicon substrate, where they are accelerated by the high electric field in the depletion region of the diode, generating a photocurrent [65, 66]. The photodetection mechanism is strictly related to the responsivity (R) of the photodetector, used to quantify the performance of the photodiode. Responsivity is defined as the ratio between the photogenerated current (I_{ph}) and the incident optical power (P_{inc}), and is strictly connected to the external quantum efficiency (η_{ext}) of the photodiode, that is defined as the number of charged carriers generated for each incident photon:

$$\eta_{\text{ext}} = \frac{N_{\text{inc}}}{N_{\text{Ph}}} = \frac{h\nu I_{ph}}{\lambda P_{\text{inc}}} \tag{3.3}$$

$$R = \frac{I_{ph}}{P_{\text{inc}}} = \frac{\lambda}{1242}\eta_{\text{ext}} \tag{3.4}$$

where λ is the wavelength of the incident light (in nanometer), and $h\nu$ is the photon energy ($= 1242$ eV). η_{ext} is related to the internal quantum efficiency by the equation:

Table 3.1: Comparison of the main electrical and optical parameters for 2D materials-Si NIR photodiodes [57].

Ref.	Type	Responsivity	λ (nm)	I_d	SBH (eV)	Config.
[55]	Exfoliated Graphite/P-Si	9.9 mA W^{-1} at -16V	1550	$\sim$ 2.4 µA at -16 V	0.44–0.46	Free-space
[58]	SLG/P-Si	370 mA W^{-1} at -3V	1550	$\sim$ 2.4 µA at -3V	0.34	WG
[59]	SLG/P-Si	20 mA W^{-1} at -10V	1550	$\sim$ 147 µA at -10V	0.46	Free-space
[60]	SLG/N-Si	83 A W^{-1}	1550	$\sim$ 0.1 µA at -1.5V	0.5	Free-space
[56]	SLG/P-Si	0.16 mA W^{-1} at -0V	2000	$\sim$ 3 µA at -6V	0.62	Free-space
[61]	MoS_2/P-Si	300 mA W^{-1}	808	-	0.33	Free-space
[62]	N-WS_2/P-Si	5–6 mA W^{-1}	420–1000	$\sim$ 0.1 µA (saturation current)	-	Free-space
[63]	WS_2/N-Si	10.4 mA W^{-1}	785	$\sim$ 0.1 µA at -6V	-	Free-space
[64]	PtS_2/N-Si	520 mA W^{-1}/ 0.57 mA W^{-1}	808/ 1550	$\sim$ 1.1 nA at -1V	-	Free-space
[*]	**a-Si:H/ FLG/P-Si**	**27 mA W^{-1} at -21V**	**1543**	**$\sim 1.9\mu$A at -21V**	**0.45**	**Free-space**

[*] the present thesis.

$\eta_{\text{ext}} = \alpha\eta_{\text{int}}$, being α the absorption coefficient of the active material. In the following sections, the expression of internal quantum efficiency for metal-Si and for graphene-Si Schottky junctions will be obtained.

3.2.1 IPE in metal-Si diodes

Following the approach of Elabd and Kosonocky [67], the total number of excited carriers (N_T) can be expressed as:

$$N_T = \int_0^{h\nu} D(E)\mathrm{d}E \tag{3.5}$$

where $h\nu$ is the incident photon energy, E is the carriers energy referred to Fermi level and $D(E)$ is the density of state in the absorber material. Not all these excited carriers will be emitted from metal to silicon, but only those carriers with an energy higher than the Schottky barrier would have a certain probability $P(E)$ to be emitted to silicon. Therefore the number of carriers emitted to silicon can be expressed as:

$$N = \int_{q\phi_{B0}}^{h\nu} D(E)P(E)\mathrm{d}E\,. \tag{3.6}$$

In metal-based junctions, with 3D materials, the internal quantum efficiency can be expressed with the following expression, obtained with the zero-temperature approximation [67]:

$$\eta_{\text{int}}^{3D} = \frac{N}{N_T} = \frac{1}{8q\phi_{B0}}\frac{(h\nu - q\phi_{B0})^2}{h\nu} \tag{3.7}$$

where ϕ_{B0} is the Schottky barrier height at zero bias (in eV), $h\nu = 1242\lambda_0^{-1}$ is the photon energy in nm, being λ_0 the wavelength in vacuum condition, and q is the electron charge. In their work, Elabd and Kosonocky outlined that reducing the thickness of the metal, the emission probability $P(E)$ is increased and therefore the efficiency is enhanced.

3.2.2 IPE in graphene-Si diodes

Equation (3.7) does not properly describe the behavior of graphene-Si Schottky junction (or in general of junctions with 2D materials), because both the density of state and the emission probability function have a different expression for 2D materials. In particular, for graphene $P(E)$ can be taken equal to 1/2 (as explained in Section 3.1), while the density of state in graphene is related to energy with the expression [67]:

$$D(E) = \frac{2|E|}{n\hbar^2 v_F^2} \tag{3.8}$$

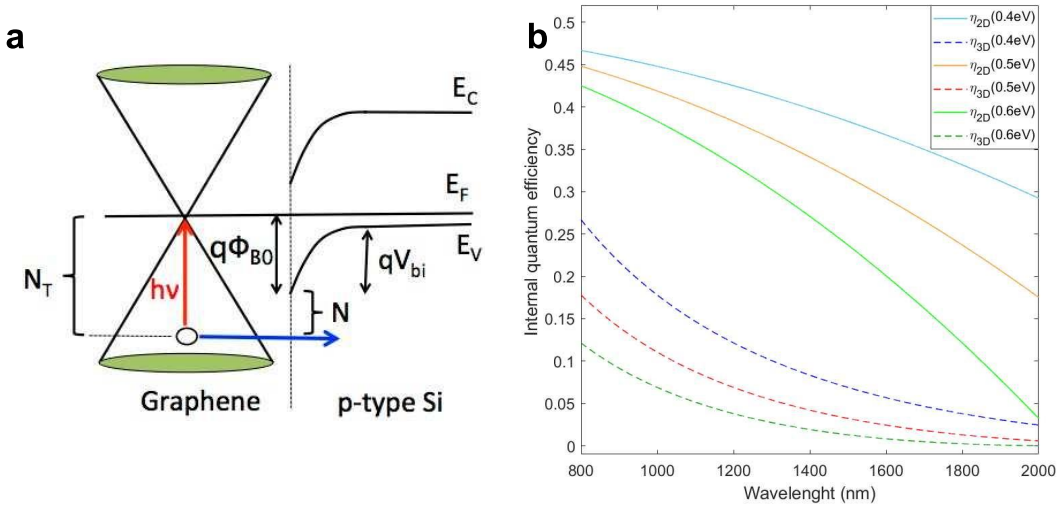

Figure 3.1: (a) band diagram for graphene/P-Si Schottky junction. E_F is the Fermi level, E_V (E_C) is the silicon valence (conduction) band, $q\phi_{B0}$ is the zero bias Schottky barrier height, qV_{bi} is the built-in potential, N_T and N are the total number of excited hole and the number of holes having the probability to be emitted to Si, respectively; (b) comparison between internal quantum efficiency obtained for 3D (dashed lines) anf for 2D (continuos lines) active materials as a function of the wavelength. Three values have been considered for the Schottky barrier: 0.4, 0.5 and 0.6 eV [57].

where $\hbar$ is the reduced Plank constant, and v_F is the Fermi velocity, n is the graphene doping. Therefore Equation (3.7) for internal quantum efficiency is modified for graphene/Si junctions as follows:

$$\eta_{\text{int}}^{2D} = \frac{N}{N_T} = \frac{1}{2}\frac{(h\nu)^2 - (q\phi_{B0})^2}{(h\nu)^2} \tag{3.9}$$

Internal quantum efficiency for 3D- and for 2D-Schottky junction has been calculated using Equations (3.7) and (3.9), respectively. The trends obtained for η_{int} versus the wavelength, are shown in Figure 3.1b, for three different values of the barrier height: 0.4, 0.5 and 0.6 eV. We can notice that η_{int} is improved in Schottky junction with 2D material.

3.3 The REVEAL project: NeaR-infrarEd resonant caVity enhancEd grAphene/siLicon photodetectors

Reveal is a one-year proof-of-concept technology project developed with support from ATTRACT [68], a €20 million EU-funded, CERN-led consortium, which has awarded 170 grants worth €100000. Two are the main objectives of the REVEAL project [69]: 1) integration of graphene in Si-technology for the development of components for photonic and optoelectronic applications; 2) proof-of-concept of high-performance hybrid graphene-based Si photodetectors (PDs) operating at 1550 nm. The wavelength of 1550 has been chosen because of its importance in modern telecom systems. In fact, operation at 1550 benefits of reduced light absorption in optical fibers, while in free-space optical (FSO) communications and in light radars (LIDARs) working at 1550 nm minimizes the propagation losses in fog and humid conditions, due to a reduced optical absorption and scattering, compared to wavelengths $\leq 1\,\mu$m. Another important aspect is the fact that eye safety is improved, because the cornea absorbs light at 1550 nm, avoiding detrimental effects on the retina. From simulation reported in Figure 3.1(b), graphene-Si Schottky diodes show increased IPE, thanks to the low dimensionality of graphene. The absorption coefficient of graphene is quite high ($\alpha = 2 \times 10^5\,\text{cm}^{-1}$), but graphene is very thin and therefore its absorption is low ($\sim$ 2.3% for a monolayer graphene). Therefore a large part of the incident optical power does not contribute to photodetection and the responsivity of the detector is low. But light absorption can be improved embedding graphene into an optical or photonic crystal cavity, by placing the graphene layer in the position where the stationary optical field is maximum. An optical cavity consists in a thin dielectric layer incapsulated between two mirrors, that can be Bragg or metallic reflectors [70]. Designing the cavity with an optical thickness of a quarter of the resonant wavelength, the optical field is trapped inside the cavity and the light passes through graphene several times, so that the light absorption is increased. The REVEAL project

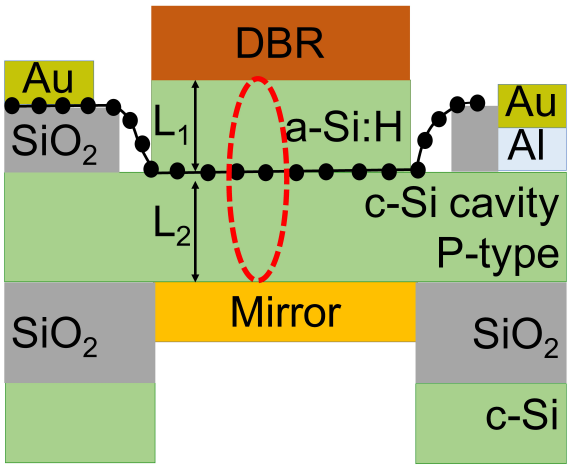

Figure 3.2: Section sketch of the proposed RCE photodetector. Thanks to the vertical structure, photogenerated carriers move through a very short path. L_1 and L_2 are the separations between the active layer (Gr) and the mirrors, and are calculated in order to maximize the stationary optical field at the graphene layer.

follows this approach [71]. The photodetector is based on the graphene/Si Schottky junction, and it is integrated in a Fabry-Pèrot optical microcavity designed to operate at 1550 nm. The following sections will describe the device fabricated in this work and the related characterization, as well as the problems encountered.

3.4 Vertical RCE photodetectors based on thin Gr/Si Schottky diodes

This activity has been developed in the framework of the REVEAL project funded by EC (Grant agreement n. 777222, in the Horizon 2020 Framework Programme for Research and Innovation). The proposed resonant cavity enhanced (RCE) graphene/Si photodetector is based on a Fabry-Pèrot structure formed by input and ouput mirrors, with an optical microcavity in between constituted by crystalline silicon-graphene-amorphous silicon (c-Si/Gr/a-Si:H, in Figure 3.2). The detection mechanism is based on IPE through the Gr/c-Si Schottky junction, while the a-Si:H layer works as buffer layer used to accommodate the localization of the optical field on the thin graphene layer. Working at 1550 nm, the refractive index of c-Si ($n_{cSi} = 3.47$) is very close to that of amorphous silicon ($n_{aSi} = 3.58$), therefore the reflections between the two materials are negligible. The operating wavelength is fixed to 1550 nm, but thanks to the wide band of graphene absorption, the proposed structure can work at longer wavelength (Mid-IR) if properly designed (that is changing the resonance wavelength of the microcavity). Moreover, it

Table 3.2: Main parameters extracted from the measurements of circular TLM structures fabricated using ITO to contact low doped silicon substrates ($\rho = 5$–$10\,\Omega\,\mathrm{cm}^{-1}$). The lowest values are obtained depositing ITO at higher temperature, or after an annealing at 300 °C for 1 hour.

Sample name	**ITO thickness [nm]**	**Deposition Temperature [°C]**	**Contact resistance - R_c [Ω]**	**Specific contact resistance - ρ_c [Ω/cm^2)**	**Transfer length - L_t [µm]**
Dep. **IT905**	80	350	4.4	3.9E-4	29
Dep. **IT905 + anneal**	80	350	2.1	1.2E-4	18.6
Dep. **IT914**	150	350	4.3	6E-5	4
Dep. **IT921**	88	380	1.5	1.8E-5	3.9

is important to notice that the proposed structure of Figure 3.2 has a vertical RCE configuration, where the photogenerated carriers have to move through a very short path (~ 220 nm, the c-Si thickness), before being collected.

The project of the optical Fabry-Pèrot cavity (made with c-Si/Gr/a:Si-H) is based on the analytical formula of the absorption of the graphene layer (A_G), reported in [71], and obtained applying the RCE theory [72].

3.4.1 Fabrication of vertical RCE photodetectors

The fabrication of the RCE Gr/Si photodetector with the MESA structure of Figure 3.2, is a quite complex technological process. Four main fabrication items can be identified:

Fabrication of the thin c-Si membranes

The process starts from a 6 inches SOI wafer, with 220 nm thick c-Si, and 3 µm buried oxide. The thickness of bulk silicon is reduced to 300 µm using a lapping procedure, and then membranes are obtained using anisotropic DRIE etching of silicon (Bosch process, with a thick oxide layer as mask during the silicon etching process). The buried oxide is used as etch stop layer, and it is finally removed wet in a BOE solution. Unfortunately, after the etching of bulk silicon, most membranes are characterized by large deformations, due to the compressive stress developed at the oxide/c-Si interface, which results in large buckling. Removing the buried oxide from the membrane area, does not completely solve this issue, in fact the membranes are often rippled, due to the stress released at the edge of the membrane (see Figure 3.3).

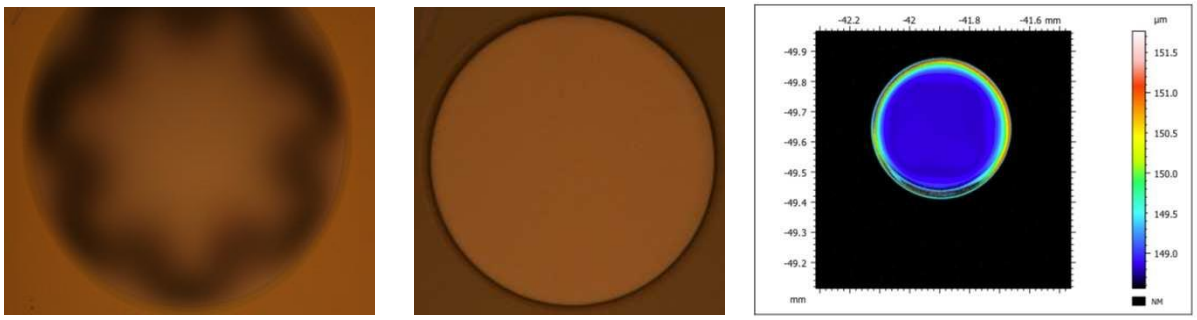

Figure 3.3: Microscope optical images of a 220 nm thick membrane made by direct SOI etching, (a) after bulk silicon etching, and (b) after etching of the 3 µm thick buried oxide; (c) optical interferometry image of the same membrane. The membrane is planar in the central part, but with a 2 µm bulge with respect to its edges.

Fabrication of the high reflectivity mirror on the back side of the membrane

A high-reflectivity distributed Bragg reflector (DBR) and a mirror surround the optical cavity to increase the number of round-trips for the radiation that cross multiple times the graphene layer, strongly increasing its absorption, and providing a 100% maximum graphene absorption [71]. The mirror on the backside of the membrane must accomplish a double function: to maximize the reflection of the signal into the microcavity and to make an ohmic contact to bulk silicon of the GSJ. Both aluminum and gold have high reflectivity, but they form a Schottky contact to low doped silicon. Therefore, a layer of indium tin oxide (ITO) has been deposited directly onto silicon in order to achieve the ohmic contact. ITO has been selected because it is usually used in heterojunction solar cells as the transparent conducting oxide layer. The best deposition conditions have been found by means of electrical characterization using circular TLM (transmission line model) structures. Before ITO deposition the substrates were dipped in a 1% HF solution for 30 s, and immediately put inside the evaporation system, in order to avoid the formation of a native oxide and to reduce the density of surface states at the Si/ITO interface. ITO was deposited setting the temperature to 350 °C or 380 °C, but the temperature on the sample would be lower, around 200–230 °C, respectively, because the sample is suspended during the process. A comparison of the results obtained with the different processes are reported in Table 3.2. The best results are obtained for the 80 nm thick ITO, deposited at higher temperature. Therefore, the back mirror in the structure of Figure 3.2 would be a multilayer, with ITO in direct contact to the Si substrate, covered with one or more metallic films, in order to obtain a high reflectivity. Simulations of the reflectivity for a metallic multilayer have been performed, in order to select the composition of the mirror that maximizes reflectivity at 1550 nm (Figure 3.4).

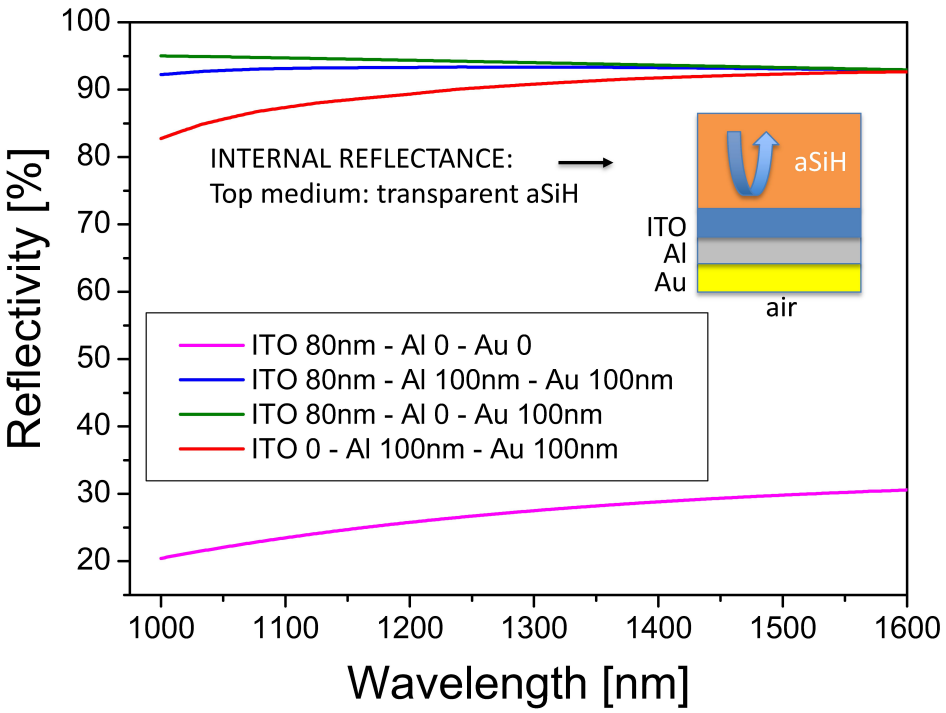

Figure 3.4: Simulation of the reflectivity versus wavelength for the mirror, considering different structures: only ITO (pink line), ITO and one or more metals (blue and green lines), only metals (red line).

Both ITO/Al/Au and ITO/Au (ITO is in contact with the silicon membrane), show a reflectivity of 0.95 at 1550 nm, a bit lower than the value of 0.98 obtained using Al/Au.

Fabrication of the optical microcavity a-Si:H/Gr/Si working at 1550 nm

With the aim of determining the optimized structure, the analytical formula for the absorption of graphene (A_G) has been used (a detailed description is reported in [71]). Since at 1550 nm the refractive index of crystalline Si layer ($n_{c-Si} = 3.47$) is very similar to that of amorphous silicon ($n_{a-Si} = 3.58$), the reflections at the interface between the two materials are negligible. The design of the optical microcavity must take into account two issues: a) once fixed the DBR on the front of the structure, the presence of the sandwich ITO/Au on the back of the optical cavity affects the resonance wavelength. Therefore, the thickness of the a-Si:H layer has to be modeled in relation to the thickness of ITO; b) the peak absorption of the structure is maximum in absence of ITO, so the thickness of ITO plays an important role. Table 3.3 shows the different combination of thicknesses for ITO and a-Si:H in order to obtain a high peak of absorption (values are obtained considering thickness of 3 nm for the graphene film and 200 nm for c-Si, and a

Table 3.3: Calculated peak absorption for the proposed structure varying the thickness of ITO deposited on the back of the membrane and of a-Si:H layer on the front.

Th(ITO) [nm]	**Th(a-Si:H)** [nm]	**A(peak)**
0	298.5	0.87
10	290.5	0.87
20	282.5	0.86
40	270	0.83
70	256.5	0.76

diffraction index $n = 0.65 - 0.38$i for ITO).

Fabrication of the DBR on the front of the structure

The fabrication of the input insulating DBR on top of the optical cavity containing graphene, is the last technological step. Processes have been selected in order to maintain full compatibility with Si photonics and with CMOS technology, and paying attention to full preservation of the graphene properties and of the interface between graphene and Si, because the GSJ has been already fabricated. For this reason, a quarter-wave stack of a-Si:H and a-SiN:H layers deposited at low temperature by plasma enhanced chemical vapor deposition (PECVD) process, have been selected. As reported in [71], the maximum efficiency for the cavity can be achieved maximizing the reflectivities R_1 and R_2 of the two mirrors. The reflectivity of the metal mirror R_2 on the back is ~ 1. In order to maximize R_1, the Bragg condition: $nd = \lambda/4$, will be applied to determine the optical path for both materials of the DBR, where n is the refractive index and d is the thickness of each material. Given the refractive index of a-Si:H and a-SiN:H layers of 3.58 and 1.82 respectively, the optimized thickness of 108 nm and 213 nm are obtained for the two layers. In order to limit the technological impact of the DBR fabrication on the final structure, the number of pairs will be limited to 3, obtaining a predicted value for $R_1 \sim 0.94$. Moreover, the layers used for the fabrication of the input DBR, do not affect the design of the resonant cavity.

3.4.2 Process flow and design of the photolithographic masks

The fabrication flow chart is the sequence of processes (deposition of layer, photolithographic processes, etching, annealing, etc.) required for the fabrication of the microelectronic devices. The flowchart has been defined in order to maintain the full compatibility with standard CMOS Si technology and paying large attention to preserve quality and

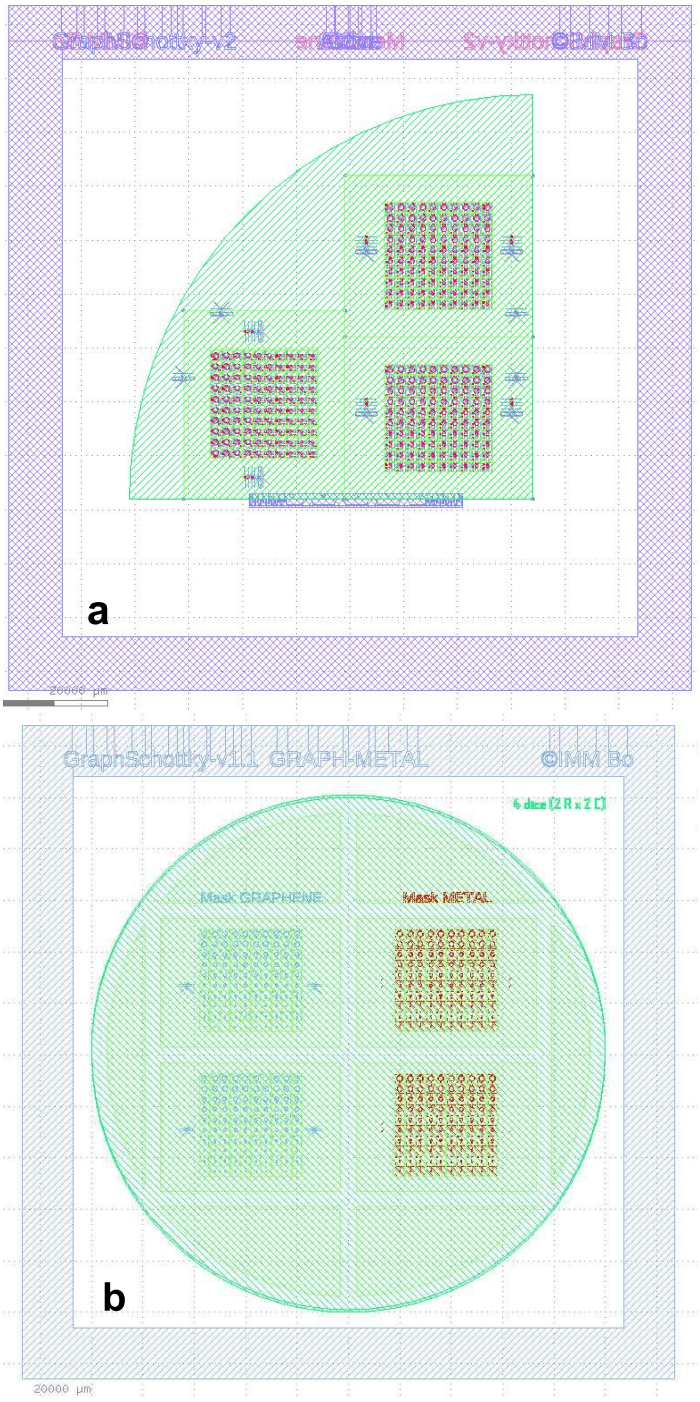

Figure 3.5: Mask layout for the fabrication of graphene/Si photodetectors. The different masks are superimposed and of different colors. (a) mask layout for fabrication of membranes (on the back side of the wafer), diode active area, opening for contact to silicon and metal definition; (b) mask layout for graphene patterning and definition of the metal contact to graphene. The mask for the definition of a-Si:H is not reported.

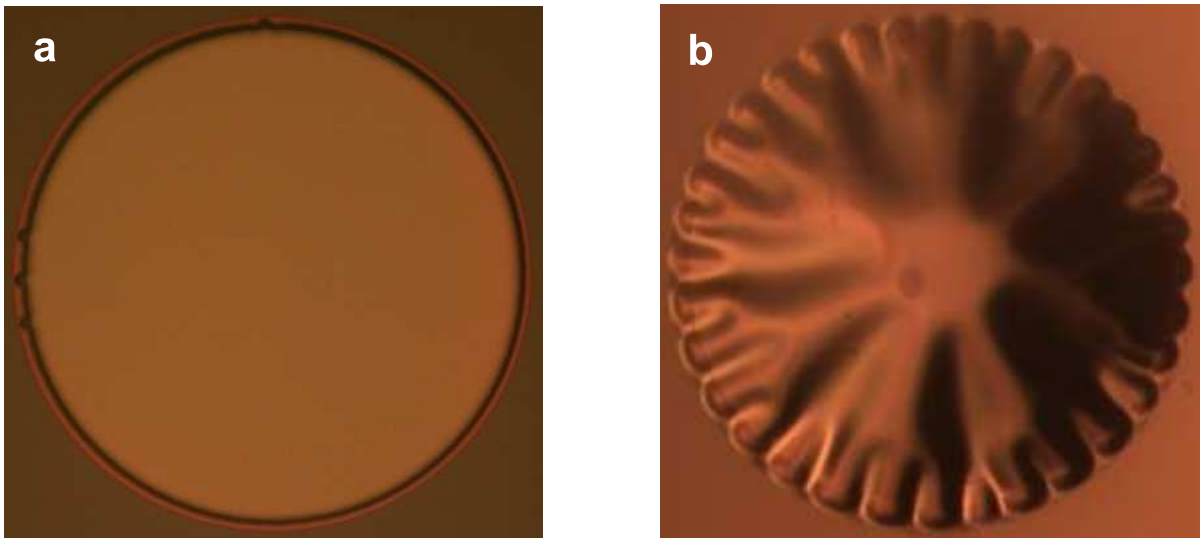

Figure 3.6: Optical image of a silicon membrane (1 mm diameter), before (a) and after (b) the deposition of 80 nm of ITO on the back side. Most part of the membranes are convex, with a great bulge in the central part.

electrical properties of the graphene layers. The main technological steps for the integration of the graphene layer in the CMOS planar technology has been developed at the beginning of this thesis and are described in Chapter 1. The photolithographic masks are designed based on the fabrication flowchart, taking into account the alignment tolerances between the different masks. The mask layout has been designed using the SW LayoutEditor©. An array of 10x10 circular diode structures, with radius in the range 250–500 µm has been designed. The masks (Figure 3.5) are designed to work on the full substrate (a 6" wafer quarter) for the fabrication of the bulk part of the device and of the silicon membranes. The process steps related to graphene (graphene patterning, contact, and a-Si:H definition) are executed on small pieces (3.5 cm × 3 cm), in order to prepare Gr/Si diodes using different procedures. The detailed description of the technological process flow used for the fabrication of vertical RCE photodetectors is reported in Appendix A.

3.4.3 Characterization of the RCE thin Gr-Si photodetectors

Unfortunately, the deposition of ITO on the back side of the membrane introduces a large bulge in the thin silicon membrane, which hinders the fabrication of the full RCE structure (Figure 3.6). Anyway, a graphene foil has been transferred on top of the thin silicon membranes, and then patterned, obtaining a set of vertical GSJ, with the simple architecture shown in Figure 3.7a.

Due to the large bulge, only few GSJ devices have a quite planar membrane and show

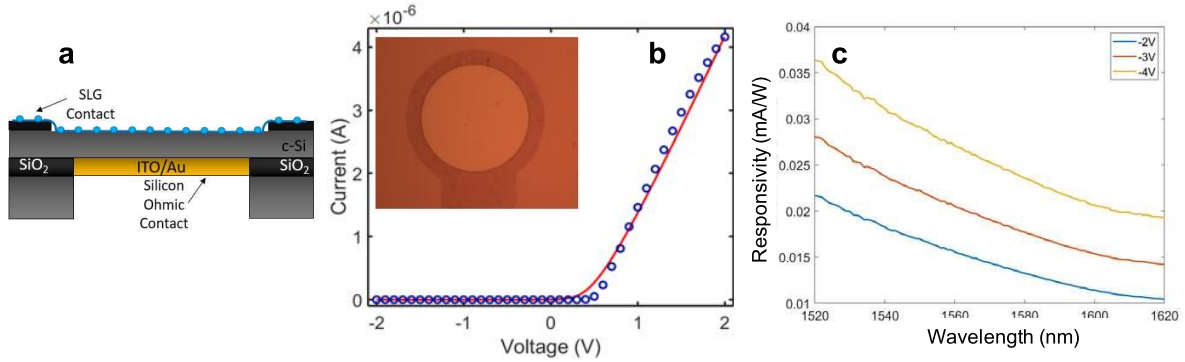

Figure 3.7: (a) section sketch of the MESA simplified structure for the graphene silicon photodetector fabricated. ITO on the backside of the membrane is used as contact to diode bulk Si, while graphene is contacted on the front side. The mirror on the back of the structure is obtained using 80 nm of gold; (b) I-V characteristic of the GSJ; in the inset is shown the microscope image of the measured device; (c) responsivity of the GSJ photodiode applying different bias voltages.

the expected rectifying behavior. It is important to notice that the Schottky junctions obtained are forward biased applying a positive voltage to the graphene layer, while a forward behavior of the diode was expected for negative applied bias. This is probably related to the deformation of the bulk silicon that modifies the contact interface between graphene and Si, flipping its polarity. The flip of polarity of graphene upon junction formation is a known phenomenon when a low doped graphene ($n \leq 10^{12}\,\mathrm{cm}^{-2}$) is put in contact with Si with an opposite doping concentration around $N = 10^{15}\,\mathrm{cm}^{-3}$. The extraction of some important diode's parameters has been performed working in the forward part of the I-V measurement at very low voltages. The diodes show a potential (Schottky) barrier $\Phi_B \sim 0.72\,\mathrm{eV}$, lower than the photon energy at 1550 nm (0.8 eV), an ideality factor of ~ 3, and a series resistance in the order of some tens of kW. The electro-optical measurements prove that the structure is able to detect wavelength around 1550 nm, as shown in Figure 3.7c. Measured devices show a best value of responsivity $R \sim 0.04\,\mathrm{mA\,W}^{-1}$ at 1520 nm, applying a reverse bias voltage of $-4\,\mathrm{V}$. Due to the absence of the F-P cavity coupled to the PD, the measured responsivity decreases at higher wavelength.

3.4.4 Conclusions

The single technological steps required for the fabrication of vertical GSJ in a RCE structure, have been studied and developed. The fabrication of the complete RCE structure is inhibited by the great deformation that affects the thin silicon membrane after ITO deposition on the back side. The bulged substrate (the silicon membrane) greatly

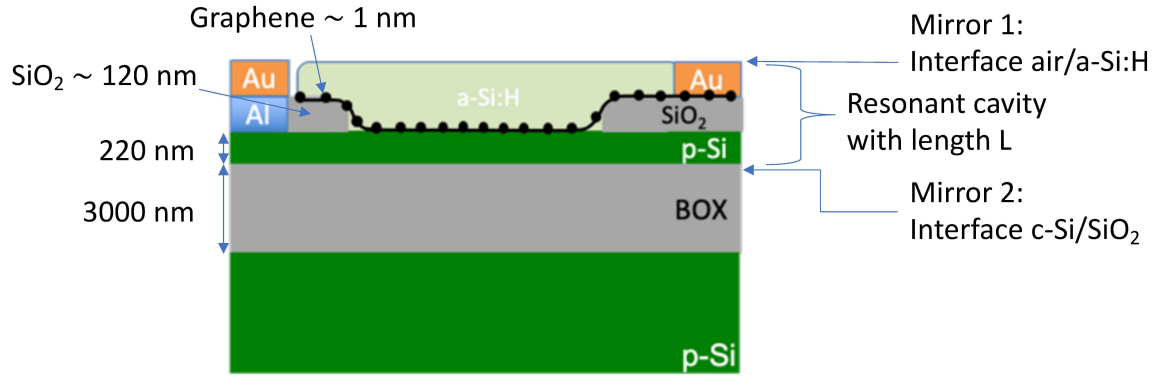

Figure 3.8: section sketch of the planar structure for the graphene silicon photodetector.

modifies the proper operation of the graphene/Si Schottky diodes. In fact, diodes show a high reverse current, and therefore a low rectification factor. The value obtained for responsivity is low, because the structure with the F-P cavity coupled to the PD was not completed due to the great bulge of the membranes.

3.5 RCE photodetectors based on thick Gr/Si Schottky diodes

Considering the technological problems encountered during the fabrication of the thin vertical RCE structure, the idea of coupling PD inside a resonant cavity has been continued, taking into account a planar structure. Devices are fabricated on a SOI wafer substrate and the resonant cavity consists of a $\lambda/2$ Schottky PDs incorporated into a Fabry-Pèrot optical microcavity with length L, where a-Si:H on top and the interface SiO_2/c-Si at the bottom are used as mirrors.

3.5.1 Design of the resonant cavity

The length of the resonant cavity, L, is calculated in order to maximize the light absorbance in the graphene layer at the wavelength of 1550 nm. Two different SOI wafers have been considered: the first one has the top silicon layer of 220 nm and buried oxide of 3 µm; while the other one has a top silicon layer of 1500 nm and buried oxide of 3 µm. Top Si is P-type, low doped, with a resistivity of 14–22 Ω cm in both cases. Being the thickness of both the graphene layer and the c-Si fixed, the thickness for the a-Si:H layer will be optimized in order to satisfy the following equation, that maximizes the light absorbance in the graphene layer:

$$n_{\text{c-Si}} \cdot th(c-Si) = n_{\text{a-Si}} \cdot th(a-Si) \tag{3.10}$$

where $n_{\text{c-Si}} = 3.48$ and $n_{\text{a-Si}} = 3.58$ at 1500 nm.
Because the refractive index of c-Si and a-Si:H are quite similar, the thickness of the Si part in the two mirrors would be similar. In fact, considering the c-Si thickness of 220 nm, we obtain:
th(a-Si:H) = (3.48 × 220 nm)/3.58 = 213 nm.
While considering the c-Si thickness of 1500 nm, we obtain:
th(a-Si:H) = (3.48 × 1500 nm)/3.58 = 1458 nm.
Therefore, the a-Si:H layer that optimizes the structure in case of the thicker SOI substrate is very thick, and even if it could be deposited using the PECVD system, it would have large intrinsic stress. Thus, only the SOI wafer with the thin 220 nm c-Si would allow the fabrication of the Fabry-Pèrot cavity around the graphene/Si photodetector.

Calculated absorption in the graphene layer

The absorption in graphene for the three-layer c-Si/Gr/a-Si:H has been simulated at 1550 nm using the transfer-matrix method (TMM) [73]. The structure analyzed is a low finesse cavity, with a quite good wavelength selectivity. Calculations have shown that the peak of amplitude of the optical field in the Fabry-Peròt detector can be localized to the a-Si:H/Gr interface by a 208 nm-thick a-Si:H layer, as shown in Figure 3.9a, with the resonance wavelength of 1550 nm, and the c-Si top layer 220 nm thick. In Figure 3.9b the corresponding Gr optical absorption at 1550 nm as function of the a-Si:H thickness is also reported, while Figure 3.9c shows the Gr spectral absorption as function of the wavelength for various a-Si:H thicknesses. Both optical field distribution and spectral optical absorption of Figure 3.9 have been calculated by means of the Generalized Scattering Matrix method using the code 'Optical' [20] and by taking into account the complex refractive index dispersion of all the involved materials. The refractive index of Gr (n_g) in the range of interest can be written as [74]:

$$n_{\text{g}} = \sqrt{\varepsilon_g} = \sqrt{5.7 + j\frac{\alpha\lambda}{2d_g}} \tag{3.11}$$

where λ is the wavelength, $d_g = 0.335$ nm is the monolayer Gr thickness, ε_g is the relative permittivity of Gr, and $\alpha = \frac{1}{4\pi\varepsilon_0}\frac{q^2}{\hbar c} = 0.0073$ is the fine structure constant [4] in SI base units (where $\varepsilon_0 = 8.854 \times 10^{-12}\,\text{F m}^{-1}$ is the vacuum permittivity, $c = 3 \times 10^8\,\text{m s}^{-1}$ is the speed of light in vacuum and $\hbar = 1.055 \times 10^{-34}\,\text{J s}$ is the reduced Planck constant). By Equation (3.11), the complex refractive index of Gr results $n_g = 3.43$ - $j2.46$ at 1550 nm.

Figure 3.9b shows that the absorption in our few layer graphene (∼ 3–4 layer) has a maximum larger than 9%. Fixing to 220 nm the thickness of the top silicon in the SOI wafer, we obtain the graph of graphene absorption varying the thickness of the a-Si:H layer (Figure 3.9c). The graphene absorption has a periodic structure, therefore there are several values for the a-Si:H layer thickness which maximize the absorption (as shown in

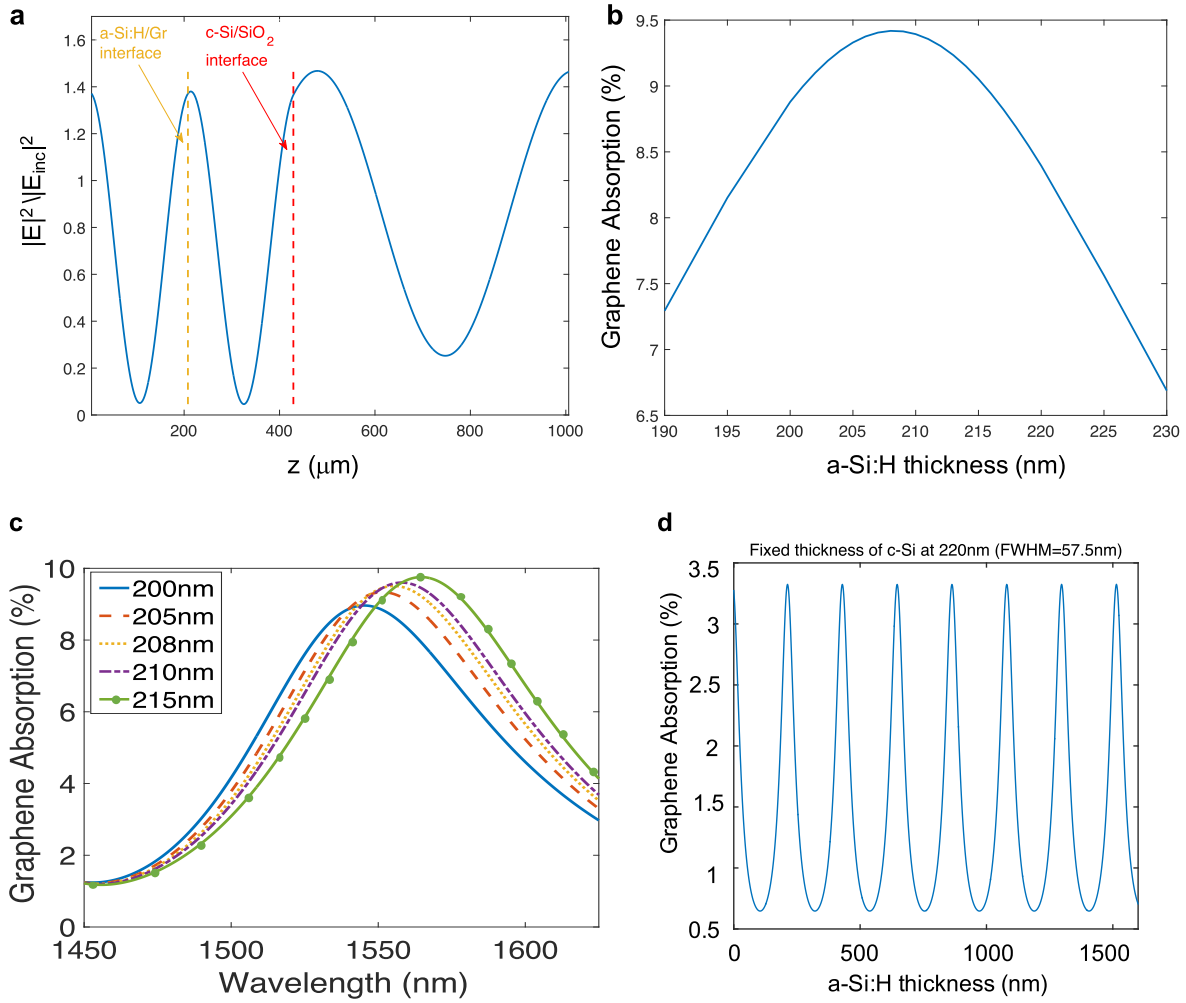

Figure 3.9: (a) optical field distribution as a function of position in the proposed photodector, considering a thickness of 208 nm for the a-Si:H layer, that maximizes the absorption at the interface between graphene and a-Si:H (b); (c) theoretical graphene optical absorption as a function of the wavelength, for different thicknesses of the a-Si:H layer; (d) calculated absorption in single layer graphene at 1550 nm wavelength, for c-Si thickness of 220 nm and varying the thickness of the a-Si:H layer.

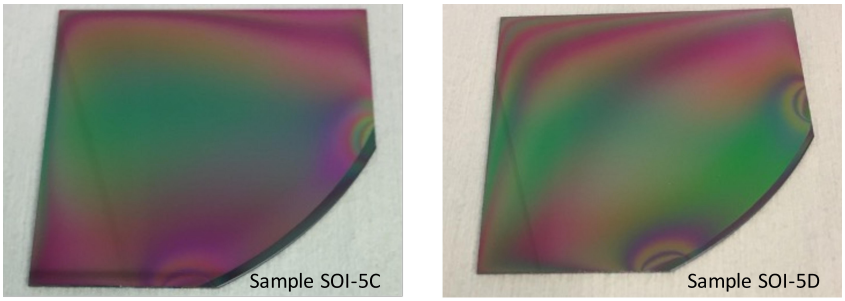

Figure 3.10: Images of the two SOI substrates used for fabrication of photodetectors. Both samples have 570 nm of oxide deposited on the surface, as field oxide.

Figure 3.9d for a single layer Gr). The peaks show a full width at half maximum (FWHM) of 57.5 nm. Therefore, there is a reduction of the graphene absorption if the thickness of the deposited a-SI:H layer differs from the optimized value. In particular, considering a reduction in its thickness of 57 nm (the FWHM) the absorption is halved. Similarly, the absorption in Gr reduces if the thickness of the c-Si is different from the nominal value used in calculations to maximize the absorption in the Gr layer (for example reducing the thickness of top-Si to 180 nm, simulations show that the absorption in graphene is reduced $\sim$ 2.7%). Therefore, the fabrication process must be carefully defined, having in mind not to modify the thickness of the top Si layer. In particular, the field oxide usually grown on the surface of the wafer, could not be obtained using the standard thermal oxidation process, because for the growth of an oxide layer with thickness d, a silicon layer with thickness of $0.44d$ is consumed, hence reducing the thickness of the top silicon layer. Instead, an oxide deposition process would be preferred.

Thickness of the resonant cavity

Another important aspect to take into account, is the system that would be used for the optical characterization. The resonance wavelength of the fabricated Fabry-Pèrot photodetector is 1550 nm, and a laser centered at 1550 nm, with 100 nm of tuning window will be used for the optical characterization. In order to guarantee the presence of an absorption maximum in this wavelength range, the minimum cavity thickness can be calculated by setting the free spectral range (FSR) equal to the tuning window. Therefore, the minimum thickness of the cavity must satisfy the equation:

$$\mathrm{FSR} = \frac{\lambda^2}{2nL} \tag{3.12}$$

where λ is the laser wavelength, n is the cavity refractive index and L is the cavity length. The cavity refractive index can be evaluated as the average value of the refractive indexes of c-Si and a-Si:H. From Equation (3.12), the minimum thickness for the cavity (that is

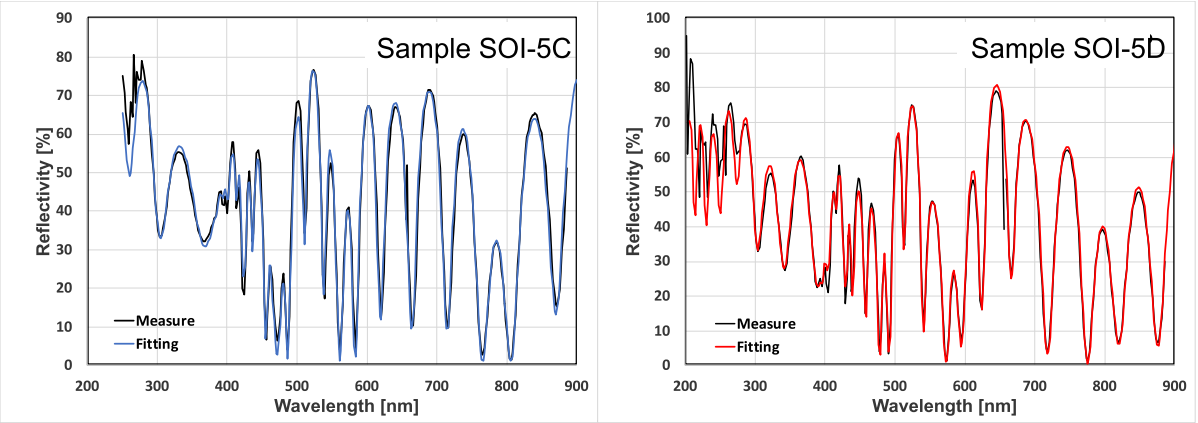

Figure 3.11: Spectrophotometer spectra (black lines) obtained for the two samples SOI-5C (left) and SOI-5D (right). From simulation (blue line for the left graph and red line for the right graph) the thickness of the different layers can be extracted with high precision.

the cavity length, L), can be obtained from Eq. 3.12:

$$L = \frac{1550^2}{2 \times 3.53 \times 100} = 3403\,\text{nm} \tag{3.13}$$

Having a cavity with this thickness, at least one absorption peak is fitted in the tuning window. However, the fabrication of a cavity having this large thickness is technologically demanding. Moreover, we have chosen to fabricate the resonant cavity starting from a SOI wafer, with a thin c-Si layer, 220 nm thick. Therefore, the thickness of the layers for the cavity fabrication will be carefully defined, to be sure to have an absorption maximum centered around 1550 nm. In particular, it is important to know with high precision the thickness of the c-Si in order to finely evaluate the thickness of the a-Si:H layer, obtaining the optimization of the complete structure. From SOI datasheet, the top silicon layer has a target value of 220 nm, with minimum and maximum values of 198 and 242 nm, respectively. The actual thickness of the top Si layer has been evaluated by simulation of the spectral reflectance, measured in the UV-visible by means of an Avantes fiber optics spectrophotometer. The simulation has been done by means of the software Optical [20, 73]. The two SOI substrates used for the fabrication of photodetectors are shown in Figure 3.10. The samples have an oxide layer (deposited by LTO) on their surface, as field oxide. From simulations of the measured spectra (Figure 3.11), the following thickness for the different layers in the substrates are obtained: LTO = 570 nm, buried oxide = 2971 nm, top-Si in SOI-5C is in the range 212–218 nm, and top-Si in SOI-5D ranges from 215 to 218 nm.

3.5.2 Fabrication of planar hybrid Gr/SOI Schottky diodes

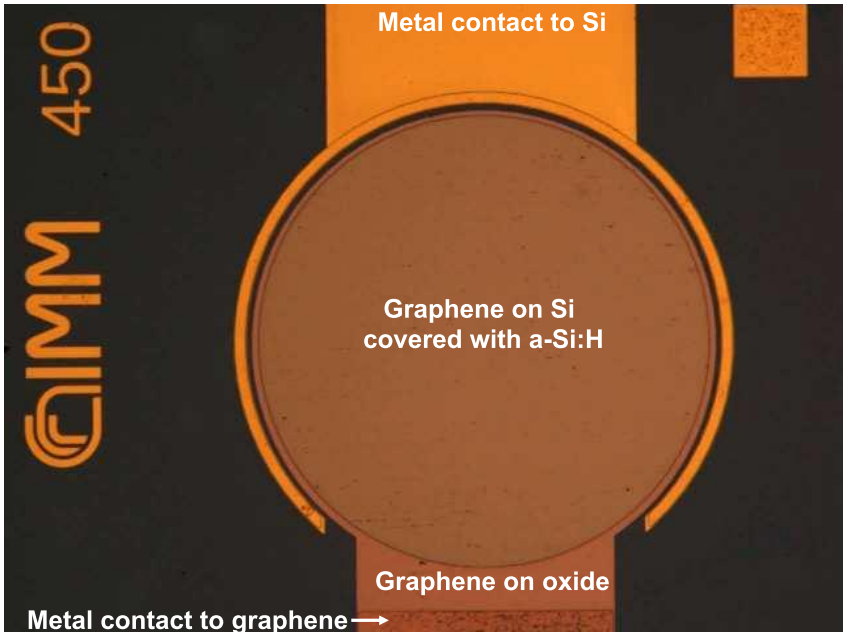

Figure 3.12: Micrograph of the fabricated photodetector. The device active area, with radius of 450 µm, is covered transfering a few layers graphene, finally a PECVD a-Si:H layer is deposited on top.

The substrate used is a 6 inches SOI wafer from Soitec, with 220 nm top crystalline Silicon, boron doped, with resistivity of 14–22 Ω cm; buried oxide is 3 µm thick and bulk silicon is 675 mm thick, Boron doped, with resistivity of 14–22 Ω cm. The fabrication process is the same described in Section 2.2, with 140 nm of oxide (LTO) deposited on the front as insulating layer. A rectangular graphene foil 3 cm x 2.5 cm is transferred on the patterned SOI substrates, using a semi-dry transfer process (Section 1.4.4). The amorphous silicon (a-Si:H) layer has been deposited on top of the chip by using a PECVD system, whose low thermal budget is compatible with the back end of line (BEOL) semiconductor device fabrication. Deposition of a-Si:H is obtained working at 13.56MHz, with 4W SiH_4 plasma, and temperature of 170 °C. Then, a-Si:H is photolithographically patterned, and dry etched in a SF_6 plasma. The detailed description of the process-flow used for the fabrication of the Gr/SOI photodetectors is reported in Appendix A. A top view of the device taken by an optical microscope is reported in Figure 3.12. The quality of Gr is examined by Raman spectroscopy under 785 nm laser excitation. Raman spectra are measured at room temperature with a Renishaw InVia micro- spectrometer. Measurements are executed with 10% power, with a 50x objective, and in this condition the spot is ~ 2 µm width and 25 µm length, and the spectral resolution is 2 cm^{-1}. Raman

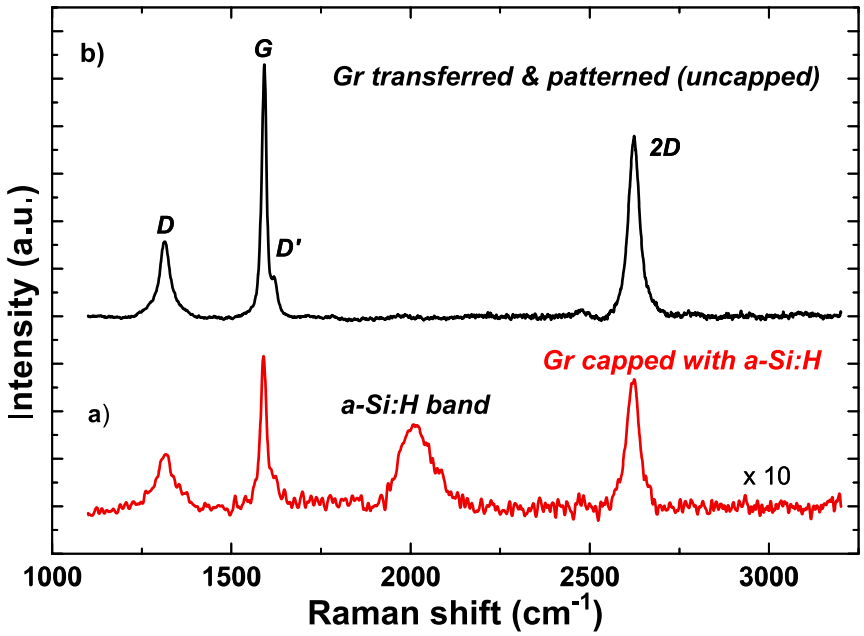

Figure 3.13: Characteristic Raman spectra of bare graphene on silicon oxide (black spectrum, curve b), and capped with amorphous silicon (red spectrum, curve a).

Table 3.4: Frequency of D, G, D' and 2D phonon modes and ratio of the D and G peak intensity, and of 2D and G peak intensity for bare and embedded graphene, and for graphene after the removal of the aSi:H layer by RIE process.

	X_D [cm^{-1}]	X_G [cm^{-1}]	X_{2D} [cm^{-1}]	$X_{D'}$ [cm^{-1}]	$FWHM_G$ [cm^{-1}]	I_D/I_G	I_{2D}/I_G
uncapped Gr	1312	1592	2623	1620	15	0,29	0,7
Gr capped with a-Si:H	1314	1590	2625	1621	22	0,41	0,9
Gr after plasma etching	1310	1592	2621	1624	22	1,1	0,5

measurements on graphene are executed on different devices, both before (bare graphene) and after the deposition of the amorphous silicon layer. During the technological process, the Gr layer is exposed to plasma twice: during the a-Si:H deposition process, and during the subsequent etching of the a-Si:H (in a RIE system), so that the worsening of graphene properties could arise due to ion bombardment. In fact, in a previous work [75] was shown a strong correlation between the energy of impinging ions and the intensity of the defect-related Raman D band. As already reported [76], the characteristic Raman peaks of graphene can be hardly detected when graphene leans on flat silicon, as in the case of Gr on the active Schottky diode area. Therefore, the Raman spectra have been obtained in the region immediately outside the active diode area, where Gr is on oxide (see Figure 3.12). The characteristic phonon modes are well observed for uncapped graphene (black spectrum (b) in Figure 3.13), while in graphene capped with a-Si:H, we can notice a pronounced decrease of the intensity of the graphene related phonon modes (red spectrum (a) in Figure 3.13). This behavior was ascribed to the optical absorption of the a-Si:H layer through which the phonon modes of graphene were measured. Raman spectrum for bare graphene shows a small D band at $1312\,\mathrm{cm}^{-1}$, together with the D' peak at $\sim 1620\,\mathrm{cm}^{-1}$, which are mainly related to defects introduced with transfer and patterning of Gr, and two strong peaks at $1592\,\mathrm{cm}^{-1}$ and $2623\,\mathrm{cm}^{-1}$, assigned to G and $2D$ band, respectively. The deposition of the a-Si:H layer introduces the broad peak centered at $2011\,\mathrm{cm}^{-1}$, associated with Si-H bond vibrations, but the characteristic Raman spectrum of Gr is preserved, and only a slight shift of the frequencies (in the order of spectral resolution) for D, G and $2D$ modes was detected (Table 3.2). The low signal intensities obtained for D and D' peaks (red spectrum a) in Figure 3.13) make difficult a reliable evaluation of the effect of the a-Si:H deposition on Gr quality. To estimate the level of induced damage, the ratio I_D/I_G can be used, as suggested by Cançado [35, 75]. In particular, for large graphene crystals ($\gg 30\,\mathrm{nm}$), the mean distance between defects in the graphene film can be obtained using the simplified Equation (1.8), valid using excitations in the visible range:

$$\frac{I(D)}{I(G)} = (1.8 \pm 0.5) \times 10^{-9} \frac{\lambda^4}{L_D^2} \tag{3.14}$$

where λ is the Raman wavelength, 785 nm, and L_D is the mean distance between defects in the graphene film. Using this equation we obtained $L_D = 48\,\mathrm{nm}$ for bare graphene, and L_D slightly reduces to 39 nm for graphene covered with a-Si:H. Considering all the reported results extracted from Raman measurements, it's just possible to say that deposition of the a-Si:H layer introduces some changes in Gr, but it's not possible to quantify it. An accurate evaluation of the strain introduced by the a-Si:H layer should be obtained from Raman maps executed on a large Gr area, before and after the a-Si:H deposition and using a correlation analysis of the G and 2D peak positions, as suggested by Lupina [77] (this analysis is not possible with the Raman system used in the thesis).

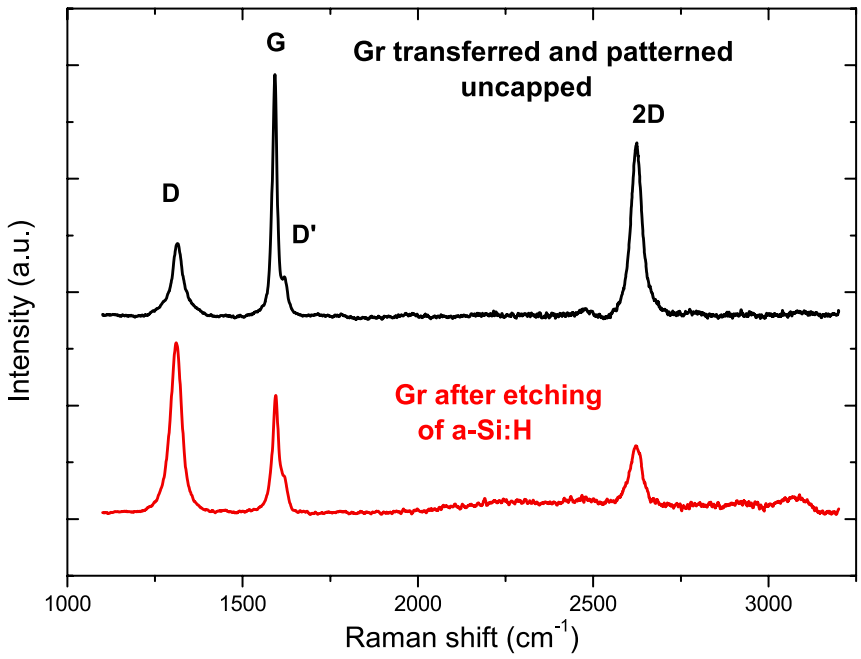

Figure 3.14: Raman spectra of bare and patterned graphene on silicon oxide before a-Si:H deposition (black spectrum on top) and on the same structure after a-Si:H deposition and RIE etching (red spectrum at the bottom).

Beside the effect of a-Si:H deposition, also the effect of the plasma process used to remove a-Si:H from some graphene structures (such as van der Pauw structure), has been studied. Raman measurements on graphene, before and after the a-Si:H removal (a-Si:H is etched using a RIE process in SF_6), are reported in Figure 3.14. As shown in Table 3.4, a small shift of the frequencies (in the order of spectral resolution) for D, G and $2D$ modes was detected. After plasma etching of a-Si:H, the intensity of $2D$ peak is decreased, while that of D peak is largely increased. The G peak intensity decreases while that of D' peak, centered at slightly higher wavenumbers, increases after the plasma etching. The D' peak is due to a double resonance intravalley process which is active in the presence of a defect and becomes detectable after reaching a certain defect level in graphene layers. Therefore, the plasma etching of a-Si:H affects the quality of not covered graphene, introducing defects in graphene, as confirmed also by the higher value of $I(D)/I(G)$ ratio that increases from 0.3 before a-Si:H deposition, to more than 1.1 after a-Si:H etching (Table 3.4). Moreover, the amount of defects introduced by the etching process starts affecting the crystalline quality of graphene layers, as demonstrated by the reduced intensity obtained for the $2D$ peak. This result indicates that the graphene layer structure is becoming polycrystalline, which is the first step of the amorphization process. As previously reported, Equation (3.14) is used to have an estimation of the level of induced damage, obtaining that the mean distance between defects in graphene reduces from 48 nm (for pristine graphene) to 25 nm, for graphene after plasma etching of the a-Si:H layer. Introduction of defects in graphene is confirmed also by measurements of the graphene sheet resistance, executed on the same van der Pauw structures used for Raman measurements. The plasma process introduces a large change in the value of graphene mean sheet resistance, that increases from 730 Ω/sq to 1.1 Ω/sq, with an increase $\sim 66\%$.

3.5.3 Electrical characterization of the photodetector

As already reported, the Gr-Si photodetectors are fabricated on a SOI substrate, with a 220 nm thick top silicon layer. The comparison between diodes on bulk Si and on SOI substrate is reported in Figure 3.15, showing that the thin silicon bulk (SOI substrate) affects the diode I-V characteristics, which present a higher series resistance and a higher Schottky barrier height. This results in an effective voltage drop on diode at higher currents, and in a lower current density in the region of thermionic emission, near zero bias. The main parameters extracted for these "thin" Schottky diodes are: $\phi_{B0} = 0.4\,\mathrm{V}$, ideality factor ~ 4, $R_s \sim 1 \times 10^6\,\Omega$, $I_s \sim 5 \times 10^{-9}$. The model developed and previously described cannot be used for fully depleted SOI diodes, because the boundary conditions for the potential and for the electric fields are completely different. A new model is under development taking into account the different working conditions.

Given the estimated locations of Fermi levels for graphene ($\sim 0.42\,\mathrm{eV}$ for P-doped graphene with an estimated hole concentration of $\sim 1 \times 10^{13}\,\mathrm{cm}^{-2}$ [45]), P-Si and alu-

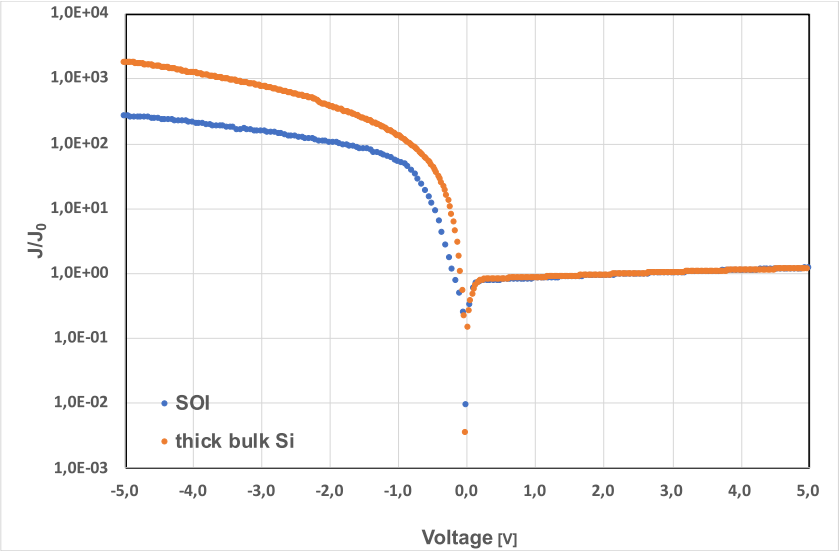

Figure 3.15: Dark I-V curves obtained for Gr-Si diodes fabricated on thick Si substrate (orange curve) and on SOI substrate with thin top silicon layer (blue curve).

minum (its Fermi level is pinned at the charge neutrality level of silicon, $\sim 1/3$ of the silicon bandgap $= 0.37\,\text{eV}$), we obtain that the depletion regions for both Gr-Si and Al-Si Schottky junctions, are in the order of $1\,\mu\text{m}$, and therefore they expand throughout the entire $220\,\text{nm}$ thick silicon layer, leading to fully depleted devices.

An estimation of the built-in potential for the two diodes gives:
$V_{bi}(\text{Gr-Si}) = \Phi_{\text{Gr}} - \Phi_{\text{Si}} = ((4.5 + 0.42) - 4.52)\,\text{eV} = 0.4\,\text{eV}$
$V_{bi}(\text{Al-Si}) = \Phi_{\text{Al}} - \Phi_{\text{Si}} = ((5.17 - 0.37) - 4.52)\,\text{eV} = 0.28\,\text{eV}$
The calculated built-in potential for Gr-Si junction is in agreement with the value of $0.4\,\text{eV}$ extracted for Φ_{B0} from experimental measurements.

The deposition of the amorphous silicon layer on top of the graphene diode, for the fabrication of the resonant cavity, introduces important changes in the electrical $I - V$ characteristics of the diodes, as shown in Figure 3.16. The main effect is the increase of the reverse diode current of more than two orders of magnitude. The modified I-V characteristic, highlights that the photodetector behaves like a metal-semiconductor-metal (MSM) structure, with two asymmetric rectifying junctions: the Gr-Si junction with an exponential behavior for the current under negative bias, and the Al-Si junction that is responsible for the current path in the opposite direction. Therefore, the photodetector can be modeled as reported in Figure 3.17, with two back-to-back Schottky diodes connected in series (the Al/Si junction is due to the Schottky contact formed by Aluminum with the low doped P-Si, as shown by $I - V$ measurements in Figure 3.16b). Moreover, we can notice that after the deposition of the amorphous silicon layer, the thermionic forward current of the Gr/Si junction is increased at low forward bias, indicating that

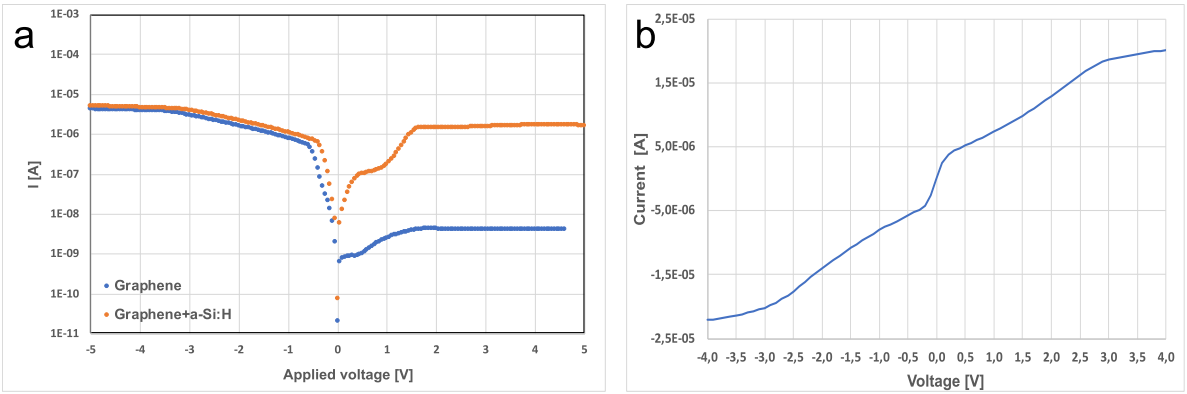

Figure 3.16: (a) Electrical $I-V$ characteristics for the Gr-Si junction on SOI substrate (blue curve), and for the same diode after deposition of the a-Si:H layer in the diode active area (orange curve). Measurements are performed at room temperature and in the dark. (b) $I-V$ measurement obtained contacting two adjacent Aluminum contacts to the thin silicon substrate; the curve shows the rectifying behavior for the Al-Si contact.

the SBH of this junction has lowered. In fact, from experimental $I-V$ measurements the following parameters are obtained for the Gr/Si junction: $\phi_{B0} = 0.2\,\mathrm{V}$, ideality factor ~ 2.5, $R_s \sim 1.5 \times 10^6\,\Omega$.
Applying a sufficiently high external voltage to the structure, the voltage drops onto the two Schottky diodes, and whether positive or negative, one Schottky junction is forward biased and the other one is reversed biased. As a result, the reverse saturation current of the reversed biased junction always limits the current in the whole structure. The following relations can be written for the MSM structure:
$V_{\mathrm{MSM}} \simeq V_1 + V_2$
and for the current continuity requirement, the total current in the MSM structure must equal the currents flowing through the two junctions:
$I_{\mathrm{MSM}} = I_1 = I_2$
In particular, when a positive voltage is applied to the graphene contact, with respect to the aluminum contact, the Al/Si junction is forward biased, while the Gr/Si junction is reversed biased, and therefore limits the maximum circulating current. The same situation is obtained applying a negative voltage to graphene, when the maximum circulating current is limited by the reverse current in the Al/Si junction.

Dependence of current on time in the photodetector

As shown in Figure 3.18, these devices show a dependence on time of the current under the fixed voltage of $-21V$, that was not observed on the same devices prior to the a-Si:H deposition (silicon is grounded, and measurements are executed at room temperature and under dark condition). This time dependence must be ascribed to the presence of

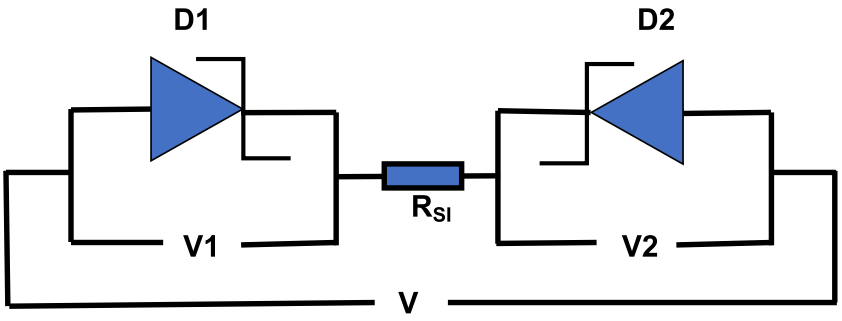

Figure 3.17: Schematic electrical circuit for the back-to-back connected diodes. $D1$ represents the Gr/Si junction, $D2$ is the Al/Si junction and R_{Si} is the resistance of the Si substrate, (voltage drop across Si can be neglected) [78].

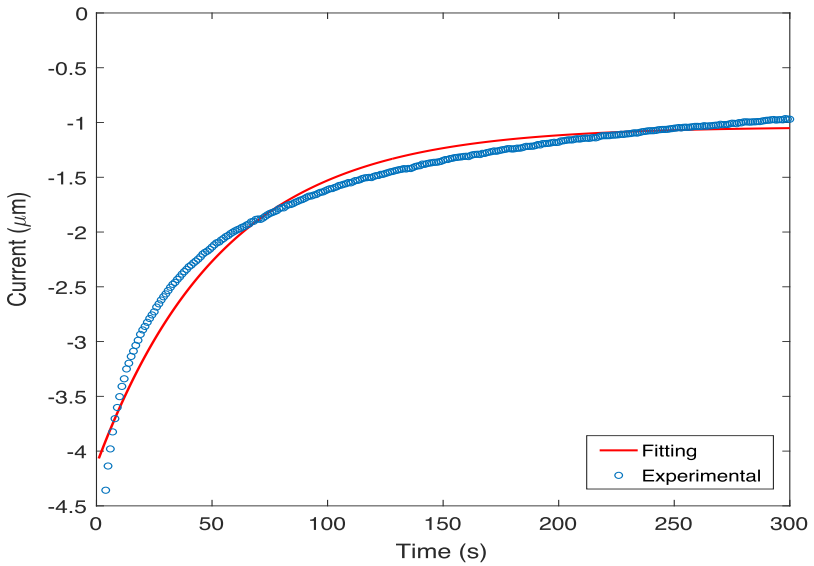

Figure 3.18: Dependence on time for the current flowing in the photodetector upon biasing graphene with a fixed voltage of $-21V$. Measurements are performed at room temperature and under dark condition.

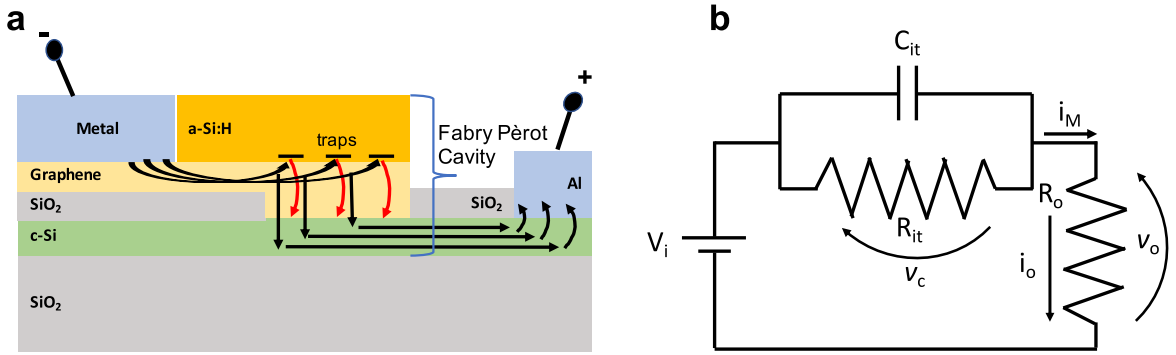

Figure 3.19: (a) sketch of the device showing the path of carriers moving from the Gr contact to the ground electrode, under a negative voltage applied to the graphene contact; (b) equivalent electrical circuit that represents the electrical behavior of the device under negative bias shown in (a).

a parasitic capacitance originating from the deposition of a-Si:H and to the presence of interface traps at the a-Si:H/Gr interface. Indeed, under the negative biasing conditions, the Gr/c-Si and the Al/c-Si junctions are forward- and reverse-biased, respectively, and the charge carriers travel in Gr before being injected into Si through the Gr/c-Si Schottky barrier. During their path in Gr the charge carriers interact with the interface traps, that could have a double effect. Traps could act as defects, increasing the scattering phenomena and introducing a degradation in mobility (as widely reported in literature for the top gated Gr field effect transistor (G-FET) [79]), that reflects in an increased resistance R_{it}. Moreover, during their path the charge carriers can be trapped in these defects giving rise to a capacitance C_{it}. Finally, the charge carriers are injected over the Gr/c-Si Schottky barrier (which can be represented as a resistance R_j) and, after moving through the resistance R_s of the Si substrate, they are collected by the Al contact. The simplified electrical circuit of Figure 3.19b takes into account all these phenomena that could affect the conduction mechanism ($R_o = R_j + R_s$ in Figure 3.19b). The complete description and solution of the circuit is reported in the next section.

3.5.4 Electro-optical characterization of Gr-photodetector

The parameter usually used to quantify the detector efficiency is the responsivity, defined as the ratio between the photoinduced current and the incident optical power on the device. Responsivity measurements have been performed at CNR-ISASI, using a CW laser at 1543 nm (ANDO AQ4321D) and measuring the IV curves of the device by a source-meter (Agilent B2902A) in dark condition (i_D) and under illumination (i_L). i_D and i_L were measured alternatively for ten times and then the net current $i_{ph} = i_L - i_D$ was calculated as the average value. The NIR beam was aligned to the active area using

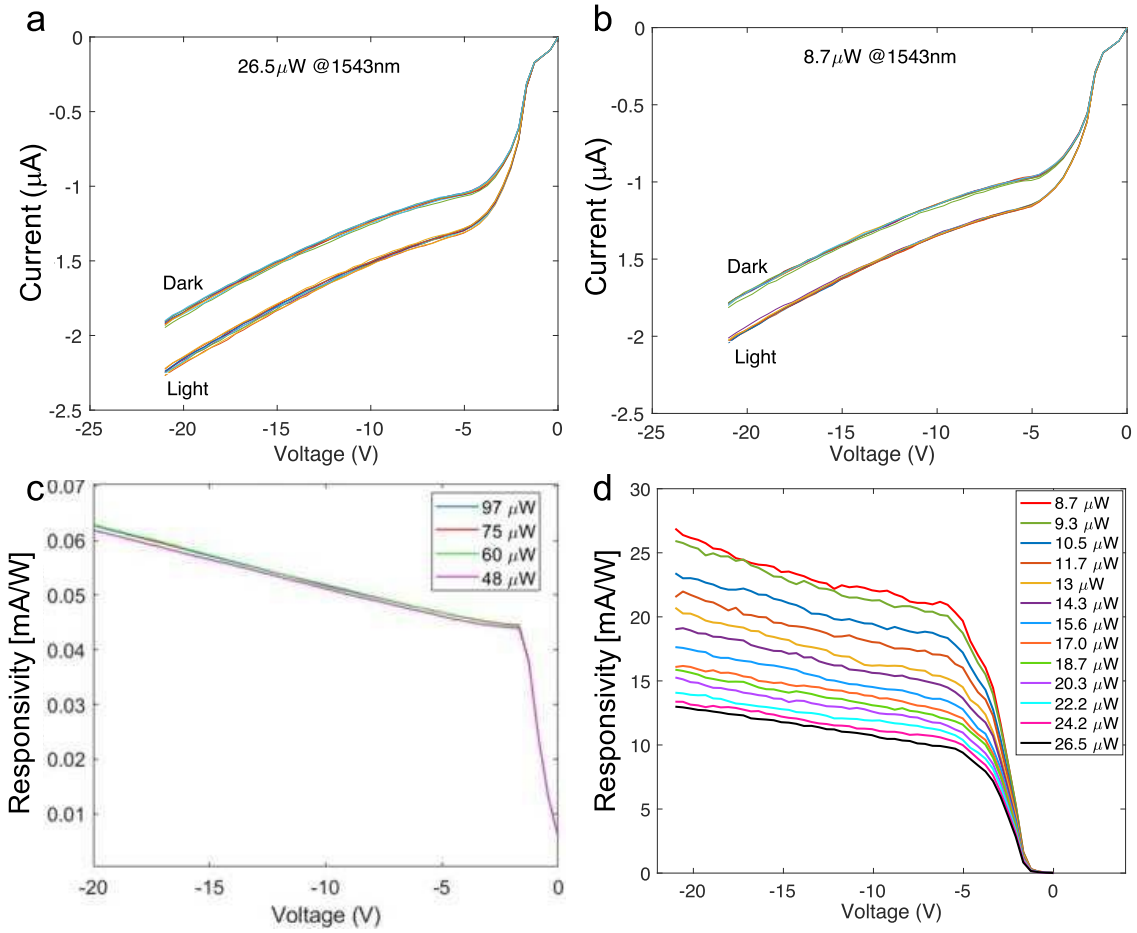

Figure 3.20: Dark and photogenerated currents with a laser at 1543 nm measured for an optical power of 26.5 µW (a) and 8.7 µW(b). Each $I-V$ measurement has been repeated 10 times under the same working conditions; (c) responsivity measured around 1550 nm vs negative voltage applied for various optical powers incident on the Gr/c-Si Schottky junction before the a-Si:H deposition; (d) responsivity versus the applied negative voltage, for different optical powers incident on the MSM device.

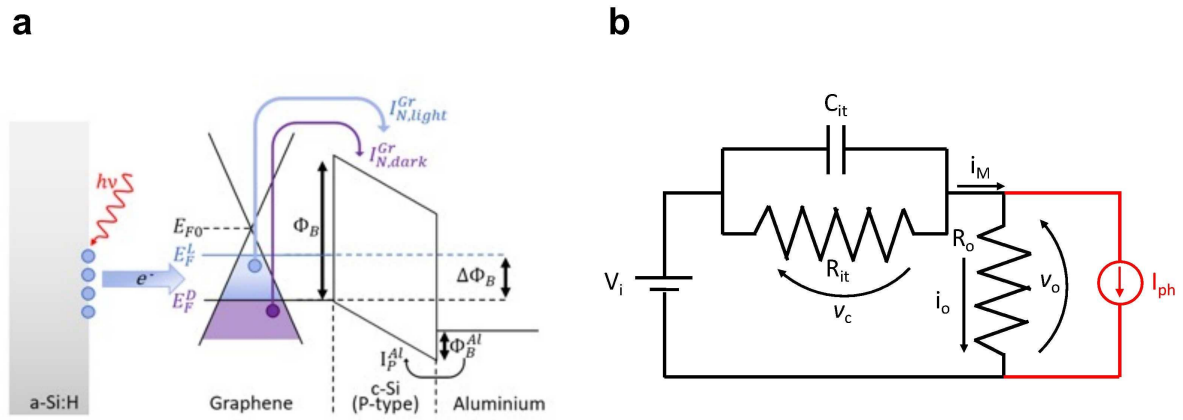

Figure 3.21: (a) device sketch to describe the detection mechanism in the a-Si:H/Gr/Si detector: under NIR illumination charge carriers are released from the traps at the a-Si:H/Gr interface to the graphene layer, changing the Gr-Si Schottky barrier; (b) the equivalent electrical circuit shown in Figure 3.19b has been modified introducing a current generator (in red), that represents the photogenerated current in the device under NIR illumination.

an IR microscope provided with an IR CCD. The incident optical power P was separately measured by a commercial calibrated InGaAs PD and normalized to the active area of the device under test. Finally, the responsivity was calculated as $R = i_{ph}/P$. Optical measurements have been performed after maintaining the device at the fixed bias of $-21\,\mathrm{V}$ for 20 minutes, in order to fill all the traps, thus minimizing the dark current in the device. NIR illumination is applied for $1s$ in all measurements. The experimental results are shown in Figure 3.20.
To explain what happens in the Gr/Si device upon illumination, it is useful to refer to the sketch and to the equivalent electrical circuit, reported in Figure 3.21. The circuit shown in Figure 3.21b is the same reported in Figure 3.19b, modified introducing a current generator (in red) that represents the photogenerated current in the device under NIR illumination. The modified circuit can be described by the following first order differential equation:

$$\frac{\mathrm{d}v_c}{\mathrm{d}t} + \frac{v_c}{(R_{it}//R_o)C_{it}} = \frac{V_i}{R_o C_{it}} + \frac{i_{ph}}{C_{it}} \tag{3.15}$$

Equation (3.15) has the following solution:

$$v_c(t) = \exp\left(-\frac{t}{\tau_{it}}\right)\left[v_c(0) + \int_0^t \left(\frac{V_i}{R_o C_{it}} + \frac{i_{ph}}{C_{it}}\right)\exp\left(\frac{s}{\tau_{it}}\right)\mathrm{d}s\right] \tag{3.16}$$

where V_i is the constant bias applied to the device at the initial time $t = 0$, v_c is the voltage drop on the capacitance C_{it} in parallel with the resistance R_{it}, v_o is the voltage

drop on the resistance R_o, while the time constant is $\tau_{it} = (R_{it}//R_o)C_{it}$.
Considering that the device is NIR illuminated starting from a time t_0, the photogenerated current can be expressed as $i_{ph}(t) = I_{ph}u(t - t_0)$, where I_{ph} is the photogenerated current originating by a continuous optical power impinging on the Gr/c-Si junction, while $u(t)$ is a step function, that considers if NIR illumination is on or off. In this condition Eq. 3.16 can be rewritten as follows:

$$v_c(t) = v_c(0)\exp\left(-\frac{t}{\tau_{it}}\right)+\frac{V_i\tau_{it}}{R_oC_{it}}\left(1-\exp\left(-\frac{t}{\tau_{it}}\right)\right)+\frac{I_{ph}\tau_{it}}{C_{it}}\left(1-\exp\left(-\frac{t-t_0}{\tau_{it}}\right)\right)u(t-t_0) \tag{3.17}$$

where $v_c(0)$ is the voltage drop on the capacitance for $t = 0$. Therefore, the current flowing through the resistance R_o can be written as:

$$\begin{aligned} i_o = \frac{V_i - v_c}{R_o} = \frac{V_i}{R_{it}+R_o}\left(1+\frac{R_{it}}{R_o}\exp\left(-\frac{t}{\tau_{it}}\right)\right) \\ - \frac{I_{ph}R_{it}}{R_o+R_{it}}\left(1-\exp\left(-\frac{t-t_0}{\tau_{it}}\right)\right)u(t-t_0) - \frac{v_c(0)}{R_o}\exp\left(-\frac{t}{\tau it}\right) \end{aligned} \tag{3.18}$$

and the current measured under NIR illumination $i_M = i_{ph} + i_o$, becomes:

$$\begin{aligned} i_M = \left[I_{ph}\left(1-\frac{R_{it}}{R_o+R_{it}}\left(1-\exp\left(-\frac{t-t_0}{\tau_{it}}\right)\right)\right)u(t-t_0)\right] \\ + \left[\frac{V_i}{R_o+R_{it}}\left(1+\frac{R_{it}}{R_o}\exp\left(-\frac{t}{\tau_{it}}\right)\right) - \frac{v_c(0)}{R_o}\exp\left(-\frac{t}{\tau_{it}}\right)\right] = i_L + i_D \end{aligned} \tag{3.19}$$

Thus, the measured current has two contributions: one due to the impinging light (in the first bracket), while the second contribution can be considered as a dark current, since not depending on the photogenerated current. By considering the capacitance completely discharged at $t = 0$, ($v_c(0) = 0$), the dark current i_D reduces to the following:

$$i_D = \left[\frac{V_i}{R_{it}+R_o}\left(1+\frac{R_{it}}{R_o}\exp\left(-\frac{t}{\tau_{it}}\right)\right)\right] \tag{3.20}$$

where $\tau_{it} = C_{it}(R_o//R_{it})$. Equation 3.20 is the solution of the circuit reported in Fig. 3.21b, when the PD is working in dark condition. The current obtained depends on time, as shown in Fig. 3.18 and can be reduced to the minimum value $i_D = V_i/(R_{it} + R_o)$ if $t \gg \tau_{it}$, i.e., if sufficient time has elapsed before the light is applied. By taking advantage of Eq. 3.20, it is also possible to extract R_{it},R_o and C_{it} by a fitting procedure (red line in fig. 3.18, R-square of 0.93). The resulting fitting parameters are: $R_o = 5.1\,\mathrm{M\Omega}$, $R_{it} = 15.1\,\mathrm{M\Omega}$ and $C_{it} = 14.3\,\mu\mathrm{F}$. By considering the active area of the Gr/c-Si junction (A_{Gr}) of $1.26\times10^{-3}\,\mathrm{cm}^2$, the capacitance due to the traps per unit of area results $11.35\,\mathrm{mF\,cm}^{-2}$.

The results of the fitting parameters can be used to evaluate the transitory, as well as the total charge trapped in this time. Indeed, the time constant $\tau_{it} = C_{it}(R_{it}//R_o)$ can be calculated as 54 s, while the trapped charge Q_t in the a-Si:H layer can be calculated as 0.015 C, that corresponds to a total number of trapped charges of $N_t = 9.46 \times 10^{16}$.

The contribution of the measured current originating from the NIR illumination is reported in the first bracket of equation 3.19:

$$i_L = \left[I_{ph} \left(1 - \frac{R_{it}}{R_o + R_{it}} \left(1 - \exp\left(-\frac{t - t_0}{\tau_{it}} \right) \right) \right) u(t - t_0) \right] \tag{3.21}$$

From the equation above, to increase i_L the condition $t - t_0 \ll \tau_{it}$ should be fulfilled. Therefore, the time $t - t_0$ defines the measurement time (t_M), that is the time during which the optical power is applied to the Gr/c-Si junction. If $t_M \ll \tau_{it} = 54$ s, the expression of i_L in equation 3.21 reduces to:

$$i_L = I_{ph} \left(1 - \frac{t_M}{R_o C_{it}} \right) \simeq I_{ph} \tag{3.22}$$

It is worth noting that $R_o C_{it} \gg \tau_{it} = C_{it}(R_o//Rit)$, therefore if the measurement time is low ($t_M \ll \tau_{it}$), the condition $t_M \ll R_o C_{it}$ is certainly fulfilled and $i_L \simeq I_{ph}$. Measurements reported in Figure 3.20a and b, were performed by maintaining the device at the constant bias $V_i = -21\,\mathrm{V}$ for 20 min ($\gg \tau_{it}$), and only after this time NIR illumination is applied for 1 sec ($\ll \tau_{it}$), alternating dark and light for 10 times. In these working conditions, the current measured under NIR illumination should be expressed as $I_{ph} + V_i/(R_{it} + R_o)$, being $V_i/(R_{it} + R_o)$ the current in stationary conditions and in dark. Therefore, under the selected working conditions, the difference between i_L and i_D gives the photogenerated current (I_{ph}), useful for the responsivity evaluation.

Responsivities measured at 1543 nm are shown in Figure 3.20 for the Gr/c-Si junction before (Figure 3.20c) and after (Figure 3.20d) the deposition of the a-Si:H layer. We can notice that before the a-Si:H deposition, the Gr/c-Si Schottky junction shows a limited responsivity of only $0.06\,\mathrm{mA\,W^{-1}}$ at 1550 nm, and no dependence on the incident optical power, as predicted by the IPE theory [66]; while adding the a-Si:H layer, the device responsivity increases by more than one order of magnitude, evidencing the clear dependence on the incident optical power shown in Figure 3.20d which is typically associated to the presence of traps [80]. In order to clarify the photoconduction mechanism in these devices, in the following the photocurrent will be derived. From Figure 3.20a and b, we notice that the photogenerated current increases its value with respect to the dark current by translating rigidly downwards. This suggests that the photogenerated current is nothing more than a thermionic current, flowing through a reduced Gr/c-Si Schottky barrier. The Gr/c-Si Schottky barrier reduction could be attributed to the electrons trapped in the defects at the a-Si:H/Gr interface which are released into Gr under illumination, reducing the hole concentration in the graphene layer.

By following this line of reasoning, we derive how the thermionic current is supported by the device changes passing from dark condition to NIR illumination. The following assumption have been considered: (a) the dark current is primarily due to thermionic emission, (b) the applied bias is greater than the flat-band voltage, and (c) recombination in the space charge region, breakdown effects, and surface state transport can be neglected. Applying a negative voltage to the Gr contact with respect to grounded Al contact, the Gr/p-Si junction is forward-biased whereas the Al/p-Si junction is reverse-biased, providing the energy band-diagram shown in Figure 3.21a under dark condition (E_F^D). Considering the structure reported in Figure 3.21a for the detector, the total current flowing through the device in dark condition (I_{TD}) is the sum of the dark current I_N^{Gr} due to thermionic emission of electrons overcoming the potential barrier Φ_B^{Gr} from the Gr contact, and the thermionic emission of holes I_P^{Al} overcoming the potential barrier (Φ_B^{Al}) from the Al contact:

$$I_{TD} = I_{N,dark}^{\mathrm{Gr}} + I_P^{\mathrm{Al}} = A_{\mathrm{Gr}} A_N^* T^2 \exp\left(-\frac{q\phi_B^{\mathrm{Gr}}}{k_B T}\right) + A_{\mathrm{Al}} A_P^* T^2 \exp\left(-\frac{q\phi_B^{\mathrm{Al}}}{k_B T}\right) \tag{3.23}$$

where A_{Gr} and A_{Al} are the areas of Gr and Al in contact with Si, respectively, T is the absolute temperature, k_B is the Boltmann constant and A_P^* and A_N^* are the Richardson constants for P-type and for N-type silicon, respectively. Indeed, as reported in [81], the current continuity requirement dictates that the total current in the MSM structure must equal the sum of the thermionic current which flows through the two junctions. Under NIR illumination of the Gr active area, the increase in total current flowing through the device (I_{TL}) suggests a reduction $\Delta\Phi_B$ of the Gr/Si Schottky barrier Φ_B^{Gr}, therefore the current under illumination can be expressed as:

$$I_{TL} = I_{N,light}^{\mathrm{Gr}} + I_P^{\mathrm{Al}} = A_{\mathrm{Gr}} A_N^* T^2 \exp\left(-\frac{q(\phi_B^{\mathrm{Gr}} - \Delta\phi_B)}{k_B T}\right) + A_{\mathrm{Al}} A_P^* T^2 \exp\left(-\frac{q\phi_B^{\mathrm{Al}}}{k_B T}\right) \tag{3.24}$$

Defining the photogenerated current as: $I_{ph} = I_{TL} - I_{TD}$, I_{ph} can be expressed as follows:

$$I_{ph} = I_{TL} - I_{TD} = A_{\mathrm{Gr}} A_N^* T^2 \exp\left(-\frac{q\phi_B^{\mathrm{Gr}}}{k_B T}\right)\left(\exp\left(\frac{q\Delta\phi_B}{k_B T}\right) - 1\right) \tag{3.25}$$

In dark condition, the decrement of the Gr/Si Schottky barrier can be ascribed to an upward shift of the graphene Fermi level towards the Dirac point, which depends on the charges stored in the Gr layer, and can be expressed as:

$$\Delta E_F^D = E_F^D - E_{F0} = \hbar v_F \sqrt{\pi \left| n_0 + \sqrt{\frac{2\varepsilon}{q} N (V_{bi} - V_F)} \right|} \tag{3.26}$$

where E_{F0} is the Dirac point, E_F^D is the Gr Fermi level, N is the doping of the crystalline silicon substrate, v_F is the Fermi velocity, V_{bi} the built-in potential, V_F the voltage

drop through the Gr/c-Si junction and n_0 the Gr doping after a-Si:H deposition. If the Al contact is strongly positively polarized with respect to the Gr contact, the Gr/c-Si junction is forward biased and the external voltage V_F dropping across the Gr/c-Si junction tends to approach to the built-in potential of the Gr/c-Si junction ($V_F \rightarrow V_{bi}$). In other words only a small depletion region is due to the Gr/c-Si junction. Thus, the term $\sqrt{\frac{2\varepsilon}{q}N(V_{bi}-V_F)}$ can be neglected, providing $\Delta E_F^D = \hbar v_F \sqrt{\pi\,|n_0|}$.

Under illumination, the a-Si:H/Gr interface traps release into Gr some charges per unit of area N_c, that are added to the initial doping n_0, and therefore the Gr Fermi level is shifted by a ΔE_F^L amount up to the level E_F^L:

$$\Delta E_F^L = E_F^L - E_{F0} = \hbar v_F \sqrt{\pi |n_0 + N_c|} \tag{3.27}$$

where N_c represents the charges trapped in the defects at the a-Si:H/Gr interface which are released into Gr under illumination. The value of N_c is completely determined by the generation rate of charges released into Gr from the a-Si:H interface. Defining the flux of photons as:

$$F_{ph} = \frac{P}{h\nu \times A_{\mathrm{Gr}}} \tag{3.28}$$

where P (expressed in eV/sec) is the constant incident optical power, A_{Gr} is the illuminated active area of a-Si:H/Gr interface in cm^2, $h\nu$ is the photon energy, N_c can be linked to the photon flux by means of this relation:

$$N_c = \tau \eta F_{ph} \tag{3.29}$$

where τ can be physically view as a carrier lifetime, while η is the conversion efficiency (adimensional), i.e., the number of charges trapped at the a-Si:H/Gr interface which are released into graphene per incident photon. The conversion efficiency depends on the interaction between photons and traps and, because the number of traps is fixed while the number of photons depends on the optical power intensity, a dependence of η on P is expected and made explicit in Eq. 3.30. The change in Schottky barrier $\Delta\phi_B$ under illumination can be expressed as:

$$q\Delta\phi_B = E_F^L - E_F^D = \Delta E_F^L - \Delta E_F^D = \hbar v_F \sqrt{\pi \left| n_0 + \tau\eta \frac{P}{h\nu A_{\mathrm{Gr}}} \right|} - \hbar v_F \sqrt{\pi |n_0|} \tag{3.30}$$

For our devices, the reduction of the Gr/c-Si Schottky barrier under illumination suggests that the charges released into Gr are electrons, therefore N_c can be considered with a negative sign. In addition, by Hall measurements we have found that transferred Gr presents a natural P-type doping of $9 \times 10^{12}\,\mathrm{cm}^{-2}$ and that the P-type doping reduces to $n_0 = 3.5 \times 10^{12}\,\mathrm{cm}^{-2}$ after the deposition of the a-Si capping layer, as also reported in literature [77, 82]. Therefore, n_0 can be considered with a positive sign and under the

assumption that no doping inversion in graphene occurs by NIR illumination ($|N_c| < |n_0|$), introducing Equation (3.30) in the expression of the photocurrent (Equation 3.25) we obtain:

$$I_{ph} = A_{\mathrm{Gr}} A_N^* T^2 \exp\left(-\frac{q\phi_B^{\mathrm{Gr}}}{k_B T}\right) \left\{\exp\left[\frac{\hbar v_F}{k_B T}\left(-\sqrt{\pi\left|n_0 - \tau\eta(P)\frac{P}{h\nu A_{\mathrm{Gr}}}\right|} + \sqrt{\pi|n_0|}\right)\right] - 1\right\} \quad (3.31)$$

Therefore, the responsivity for the photodetector becomes:

$$\mathrm{Resp} = \frac{I_{ph}}{P} = \frac{A_{\mathrm{Gr}} A_N^* T^2}{P} \exp\left(-\frac{q\phi_B^{\mathrm{Gr}}}{k_B T}\right) \left\{\exp\left[\frac{\hbar v_F}{k_B T}\left(-\sqrt{\pi\left|n_0 - \tau\eta(P)\frac{P}{h\nu A_{\mathrm{Gr}}}\right|} + \sqrt{\pi|n_0|}\right)\right] - 1\right\} \quad (3.32)$$

Equation 3.32 expresses the responsivity as a function of the incident power, and can be used to fit the experimental results reported in Figure 3.22, derived from Fig. 3.20(d) at $-21V$ by modelling the efficiency-lifetime carrier product as the power function $\tau\eta(P) = \tau\eta_o/P^\beta$. From the fitting procedure the following values have been extracted: $\tau\eta_0 = 3.0 \times 10^{-9}\,\mathrm{sW}^\beta$, $\beta = 0.79$ and a graphene/c-Si Schottky barrier for electrons $q\phi_B^{\mathrm{Gr}} = 0.67\,\mathrm{eV}$ (R-squareof 0.99). The fitting procedure was carried out with: $A_{\mathrm{Gr}} = 0.0038\,\mathrm{cm}^2$, $A_N^* = 112\,\mathrm{A\,cm^{-2}\,K^{-2}}$, $T = 300\,\mathrm{K}$, $k = 8.6 \times 10^{-5}\,\mathrm{eV\,K^{-1}}$, $\hbar = 6.58 \times 10^{-16}\,\mathrm{eV\,s}$, $v_F = 1.1 \times 10^8\,\mathrm{cm\,s^{-1}}$, $h\nu = 0.8\,\mathrm{eV}$ and a doping for capped graphene $n_0 = 3.5 \times 10^{12}\,\mathrm{cm^{-2}}$. The extracted potential barrier $q\phi_B^{\mathrm{Gr}}$ is in quite good agreement with the value predicted by theory: $q\Phi_{B0} = E_g - q(\Phi_{\mathrm{Gr}} - \chi_{\mathrm{Si}}) = 0.67\,\mathrm{eV}$ (being the Si electron affinity $q\chi_{Si} = 4.05\mathrm{eV}$, the graphene work function $q\Phi_{\mathrm{Gr}} = 4.5\,\mathrm{eV}$, and the Si bandgap $E_g = 1.12\,\mathrm{eV}$). The resulting $\tau\eta(P)$ behavior is reported in inset of Fig.3.22. It is widely reported in literature that graphene photodetectors, whose detection mechanism is assisted by traps, provide a photocurrent that can be expressed by the simple power law $I_{ph} \propto P^\beta$, where β is a non-unity exponent with values between 0 and 1, as a result of the complex process of carrier generation, trapping, and recombination within the involved materials [80]. This dependence can be easily made explicit under the assumption $|N_c| << |n_0|$, and Eq.3.32 can be approximated providing the following photocurrent:

$$I_{Ph} \simeq \left[A_N^* T^2 \exp\left(-\frac{q\phi_B^{\mathrm{Gr}}}{k_B T}\right)\left(\frac{\pi}{2} \cdot \frac{\hbar v_F}{k_B T} \cdot \frac{\tau\eta_o}{\sqrt{\pi n_0} \cdot h\nu}\right)\right] \cdot P^{1-\beta} \quad (3.33)$$

Therefore, considering that the photoinduced current can be expressed as $I_{Ph} = G \cdot P$ we obtain:

$$G \simeq \left[A_N^* T^2 \exp\left(-\frac{q\phi_B^{\mathrm{Gr}}}{k_B T}\right)\left(\frac{\pi}{2} \cdot \frac{\hbar v_F}{k_B T} \cdot \frac{\tau\eta_o}{\sqrt{\pi n_0} \cdot h\nu}\right)\right] \cdot P^{-\beta} \quad (3.34)$$

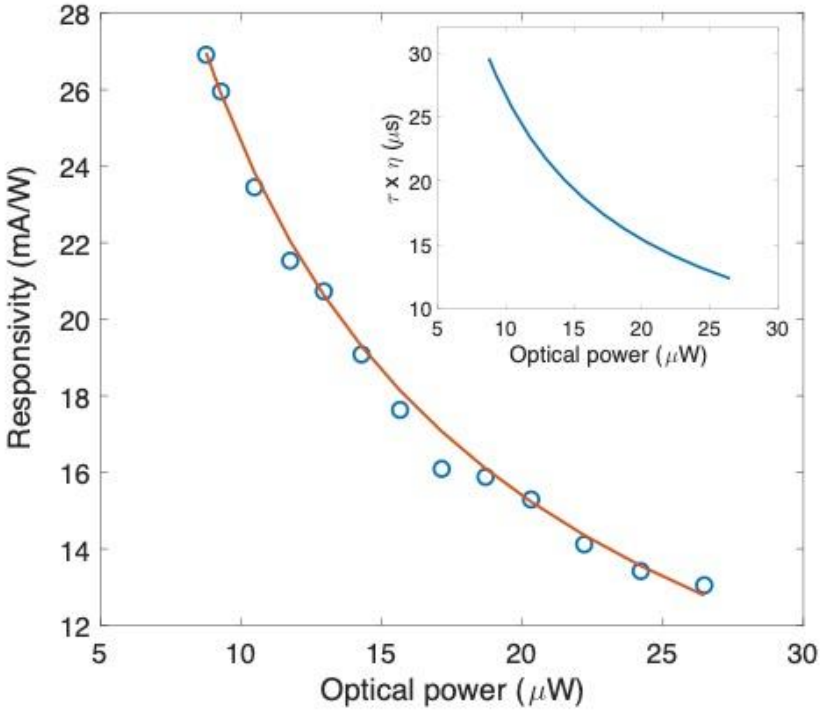

Figure 3.22: Graph of the responsivity obtained at 1543 nm and −21 V vs the applied optical power.

G represents the photo-gain of the detector, and it's related to the change of the thermionic current due to the shift of the graphene Fermi level, as a result of the carriers released in graphene by the interfacial traps under illumination. From Eq. 3.33 we can notice that the photo-gain is strongly related to the Gr Schottky barrier $q\phi_B^{\mathrm{Gr}}$, and that it decreases by increasing the applied optical power P.

3.5.5 Conclusions

Near-infrared resonant cavity photodetectors based on graphene and embedded between amorphous and crystalline silicon, have been fabricated and characterized, obtaining a a responsivity of 27 mA W^{-1} at 1543 nm, applying an optical power of 8.7 µW (the minimum available value for the equipment used). The results obtained in the thesis are reported in Table 3.1 for comparison with other 2D materials-Si photodiodes working in the NIR. The fabricated devices are based on the a-Si:H/Gr/c-Si/Al structure, where the Gr/c-Si/Al junction behaves like a MSM structure, and support the current flowing in the device, while the a-Si:H/Gr part is not involved in the transport of charge carriers. Nevertheless, performed measurements highlighted the important role of the a-Si:H on the device performances. In particular, traps located at the interface between a-Si:H

and graphene play a key role determining the dependence of the device dark current on time, and of the responsivity on the incident optical power. The photodetection mechanism can be ascribed to the thermionic current modulation of the Gr/c-Si junction, induced by the charge carriers released from traps localized at the a-Si:H/Gr interface under illumination. The physics behind the operation of these devices was derived and discussed, demonstrating a good agreement with the experimental results. The value obtained for responsivity can be further improved by using a higher-finesse cavity that may lead to an enhancement in the interaction between photons and interface traps, and consequently to an increase in the conversion efficiency. Furthermore, as demonstrated by 3.32, the responsivity of the PD can also be improved by lowering the incident optical power. Therefore, the better performance at low optical power makes this device useful in power monitoring within photonic integrated circuits, allowing non-invasive analysis in complex systems, where the stabilization and control of several of the components is crucial [83].

Chapter 4

Summary and outlook

Summary

The activity of this thesis has been developed at the CNR Institute for Microelectronics and Microsystems, Section of Bologna, where I work and where a technological Si platform for the fabrication of Si-based sensors and MEMS devices operates on a daily basis. The purpose that guided this work was to enlarge the platform of classical working 3D materials for Si technology, introducing 2DMs, starting from graphene, for the fabrication of new hybrid Gr devices. The aim was also to study how the applied technological processes and materials used could affect the electrical and structural properties of the 2D material and more widely the final device performances, since in a 2D material everything happening at its surface affects the material properties. The introduction of graphene (and more generally of a new material) into a standard platform faces several challenges and has required the development and implementation of new reliable and reproducible processes to maintain and use the physical properties of the new material in an efficient way. In the following, the main activities developed with the main results obtained in this thesis are reported.

Integration of graphene into the Si platform

A robust route to transfer and integrate few layer graphene films to a silicon substrate for the fabrication of hybrid devices has been demonstrated. The proposed fabrication process based on Si wafer technology is scalable, flexible, and compatible with a BEOL approach. Electrical and structural characterization have been defined and used to test the Gr quality related to the CVD deposition process and to select the high-quality graphene foil for the fabrication of hybrid devices. The developed technological process flow is robust and with high yield.

Graphene/ Silicon Schottky junction

Several batches of graphene/Si Schottky junctions have been fabricated, (testing different transfer procedures), and characterized, demonstrating a high reproducibility. Current-voltage measurements have been used to characterize the quality of Gr/Si interface through the extraction of the main diode parameters. In particular, it's demonstrated that an accurate evaluation of the Gr/Si Schottky barrier height at zero bias (Φ_{B0}) and of the ideality factor (n), can be obtained uniquely investigating the temperature behavior of the Gr/Si junctions, and working in the forward region of the diode, for $\mid V_{bias} \mid < \mid V_{f-b} \mid$, where the current is dominated by the thermionic mechanism. Other commonly used approaches, which work in high forward or reverse voltage, produce an estimation for the SBH that does not refer to the zero-bias condition, due to the Fermi level shift in graphene during charge transfer across the Gr/Si barrier height. A complete discussion of the validity of the different methods is presented.

Modeling the Graphene/Silicon junction

Due to the low density of states close to the Dirac point, the graphene Fermi level is extremely sensitive to the amount of carriers injected into or from the semiconductor, determining a tunable Schottky barrier height (SBH), which in turn controls the current-voltage relationship of the GSJ. These features make the Gr/Si junction an excellent platform for the study of interface transport mechanisms. For this reason, a model was proposed, in order to account for the conduction mechanisms and shifts in Gr Fermi level that occurs applying positive and negative bias to the GSJ. In particular, a new equation, working in the region near that of thermionic conduction and consistent with experimental results, was introduced. The model is used to fit the experimental measurements, extracting the main diode parameters. The model has allowed to demonstrate the fundamental role played by charge surface density in forward bias, and by the inversion layer in reverse bias, in defining the value of the Gr/Si SBH that establishes at the interface.

Fabrication of Graphene/Silicon Photodetectors

In the framework of a financed Attracts project, near-infrared resonant cavity photodetectors based on graphene and embedded between amorphous and crystalline silicon, have been fabricated and characterized, obtaining a responsivity of $27\,\mathrm{mAW}^{-1}$ at 1543 nm, applying an optical power of $8,7\,\mu\mathrm{W}$. The fabricated devices are based on the a-Si:H/Gr/c-Si/Al structure, where the Gr/c-Si/Al junction behaves like a metal-semiconductor-metal structure, and supports the current flowing in the device, while the a-Si:H/Gr part is not involved in the transport of charge carriers. The important role of the a-Si:H layer on the device performances has been highlighted by the measurements performed. In fact, the current of Gr/Si junction is influenced by the traps located at the interface

between a-Si:H and graphene. The physics behind the operation of these devices was derived and discussed, demonstrating a good agreement with the experimental results. The photodetection mechanism has been ascribed to the thermionic current modulation in the Gr/c-Si junction induced by charge carriers that under illumination are released from traps at the a-Si:H/Gr interface and move to graphene layer.

Outlook

The work reported in this thesis has permitted to develop the basic building-blocks (growth – transfer – quality control – electrical characterization - modeling) for the integration of graphene with the existing CMOS platform running at CNR-IMM on a daily basis. The expertise gained on graphene integration could be also applied to other 2D materials, opening to the fabrication of several hybrid electronic devices in the fields of optoelectronics, photonics and electronics. The next step would be the evaluation and fabrication of other electronics devices of interest, whose performances could be improved by the insertion of 2D material, preferably graphene, but opening to other 2D materials.

Concerning the technological processes, some more work would be dedicated to improve the graphene growth process and to optimize the fabrication of metal contact to graphene. In fact, Hall measurements performed on transferred CVD graphene demonstrated that our graphene foils present a quite high inhomogeneity, probably related to gas flow inhomogeneity along the tube (Gr is hole doped, with a quite high doping, in the range 0.6–1 $10^{13}\mathrm{cm}^{-2}$, a sheet resistance in the range 600–1000 Ω/sq, and a quite low mobility value, $\leq 1000\,\mathrm{cm}^2\mathrm{V}^{-1}\mathrm{sec}$). Therefore, some efforts will be dedicated to improve the synthesis process optimizing the uniformity and increasing the grain dimension, trying to reduce the sheet resistance and to increase the mobility. Moreover, an extensive study will be developed, testing different metals to contact graphene, and fabricating test structures to measure the contact resistance (i.e. cTLM).

The model adopted so far for the description of the $I-V$ behavior in the thermionic regime relies on equilibrium concepts. For this reason, its implementation in the presence of current flow is an approximation and will be improved in future work, possibly exploiting the concept of quasi-Fermi level in the appropriate form. The deviation from equilibrium is even better pointed out by the semi-phenomenological model for the behavior in strong direct polarization, i.e. beyond the flat-band potential, where the effect of the diode series resistance on conduction will also be introduced. Regarding the reverse polarization regime, the proper description of the transition towards the formation and maintenance of an inversion layer will be explored.

Appendices

Appendix A

The detailed description of the technological process flow used for the fabrication of Gr/Si Schottky diodes described in Chapter 2 and of photodetectors studied in Chapter 3 are reported in this Appendix. For device fabrication a set of photomasks has been designed. A photomask is a master template containing all the devices and structures that have to be fabricated. A picture of the photolithographic mask-set used in the technological process is reported in Fig. A.1. The mask-set is designed using the CAD LayoutEditor©, and contains 3 matrices, each with 100 circular diodes. Diodes are organized in rows, and have different diameters (D):
row A and B: D = 1 mm
row C and D: D = 0.9 mm
row E and F: D = 0.7 mm
row G and H: D = 0.5 mm
row I and J: D = 0.4 mm

A.1 Process flow for the fabrication of Gr/Si diodes

1. Substrate: low doped P-type Si wafer: 300 µm thick, $\rho = 4 - 10\,\Omega \cdot \mathrm{cm}$;
2. RCA cleaning;
3. Field oxide deposition: low temperature oxide deposition process (LTO), $T = 420\,^{\circ}\mathrm{C}$, time= 10 min, obtained oxide thickness = 118 nm;
4. Photolithographic process for the formation of Si contact areas in the oxide layer:
   (a) spinning of resist: ma-N-1420 (Microresist Technology), 3000 rpm, thickness = 2.1 µm
   (b) PR exposure in Karl Süss MA4: mask-1: SiCon (Fig. A.2(a)); exposure time: 35 s, hard contact;

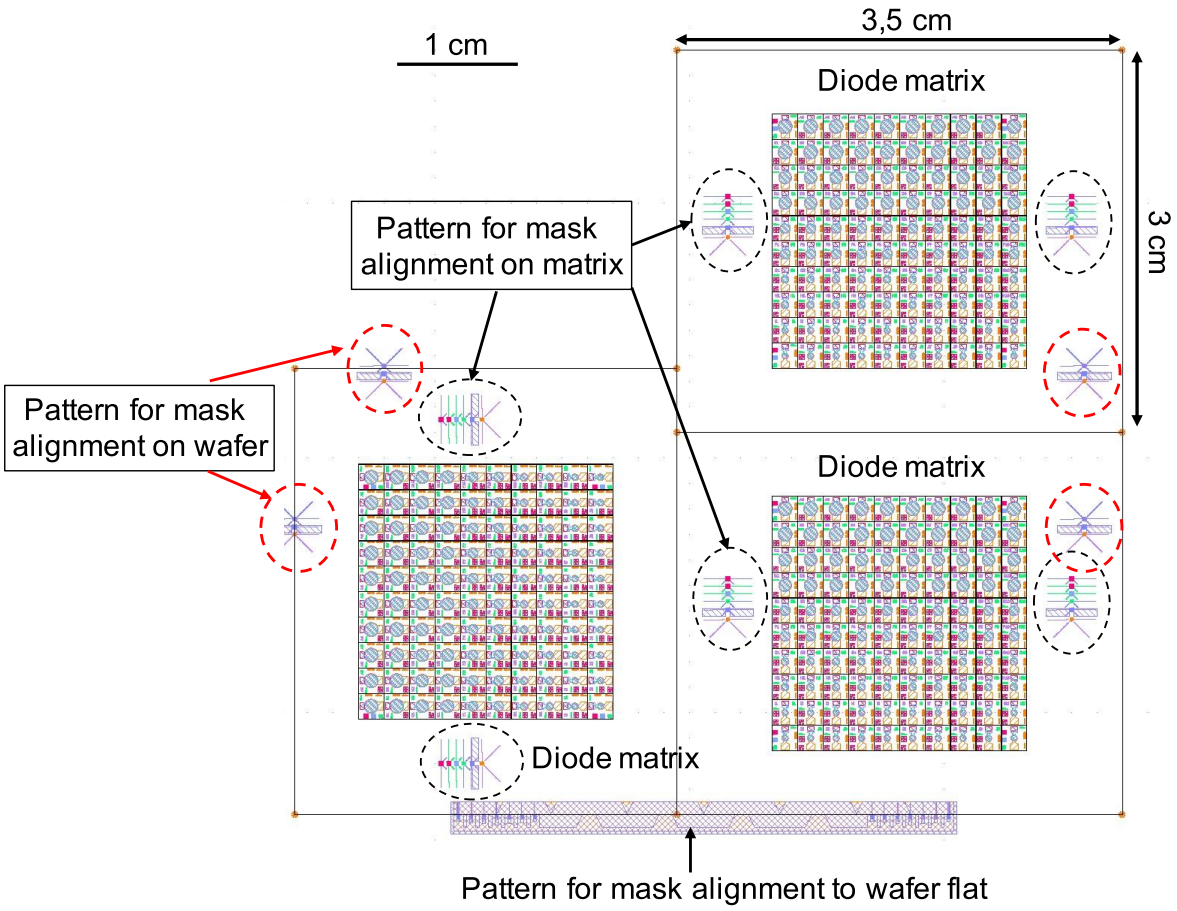

Figure A.1: Plot of the mask-set. All the photolithographic masks used in the technological process for the fabrication of Gr/Si diodes are superimposed in the plot. The mask contains three diodes matrices and is designed to fit the 3 matrices in a quarter of 6" wafer.

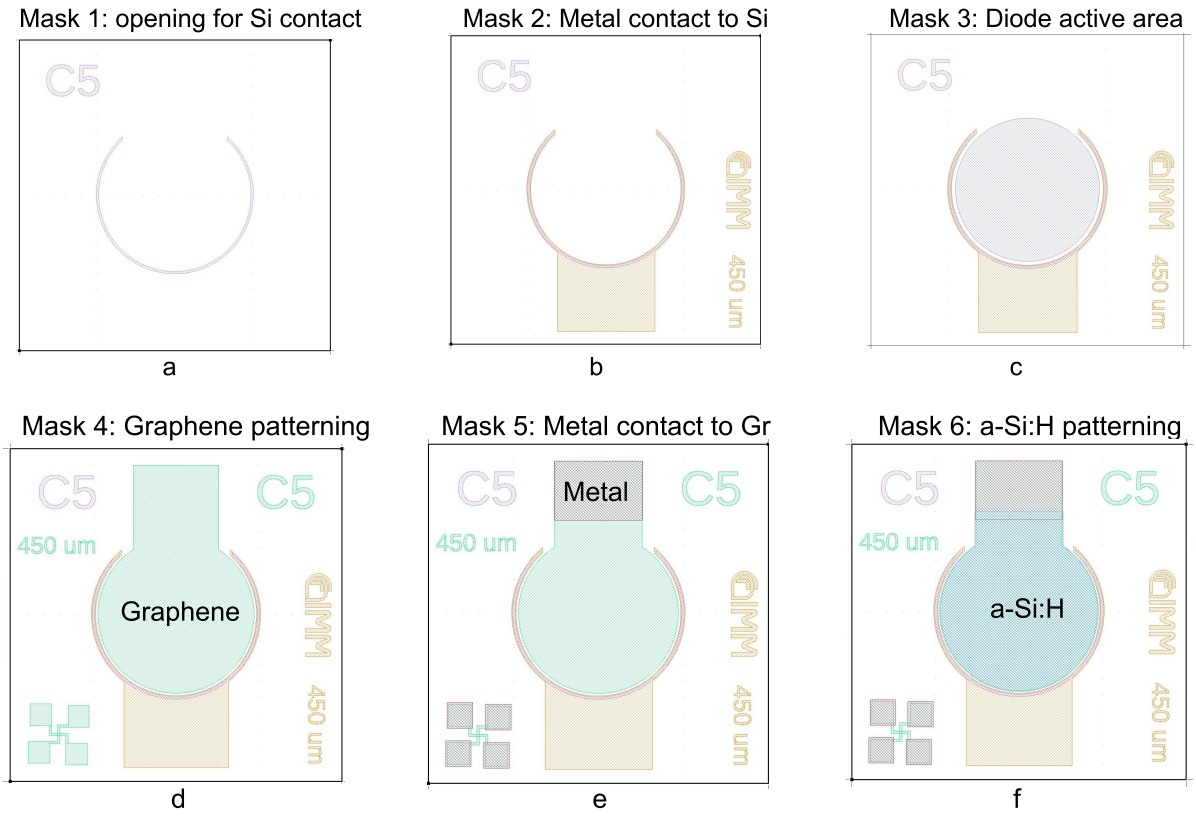

Figure A.2: Layout of the different layers in the mask-set: Si contact (a), metal contact to Si (b), active area (c), graphene (d), metal contact to Gr (e), and a-Si:H (f). Each layer is represented for a single diode of the mask.

(c) developing process of exposed PR (developer ma-D 533, Microresist Technology) for 95 s;

(d) oxide etching in BOE solution (buffered etch of fluoridric acid and ammonium persulfate, 7:1, from Fujifilm), for 50 s (etching rate $\sim 220\,\mathrm{nm\,min^{-1}}$);

(e) sputtering deposition of the Aluminum film, 50 nm thick;

(f) definition of Al using the lift-off process. Lift-off is performed in Microstrip 3001 (Fujifilm), at 85 °C, with ultrasounds, time used 3 hours.

5. Aluminum annealing in furnace: 400 °C, 20 minutes, in $N_2 + 10\%H_2$;

6. Photolithographic process for Cr-Au lift-off:

(a) spinning of resist: ma-N-1420 (Microresist Technology), 3000 rpm, thickness = 2.1 µm

(b) PR exposure in Karl Süss MA4: mask-2-Gold (Fig. A.2(b)); exposure time: 35 s, hard contact;

(c) developing process of exposed PR (developer ma-D 533, Microresist Technology) for 95 s;

(d) evaporation of Cr (adhesion layer): thickness = 10 nm;

(e) sputtering deposition of Au: thickness = 70 nm;

(f) lift-off of Cr/Au performed in Microstrip 3001 (Fujifilm), at 85 °C, applying ultrasounds, time used 3 hours.

7. Photolithographic process for the opening of the diode's active areas:

(a) spinning of resist: HPR-504 (Fujifilm), 2000 rpm, thickness = 1.2 µm;

(b) PR exposure in Karl Süss MA4: mask-3 - Active (Fig. A.2(c)); exposure time: 2 s, hard contact;

(c) developing process of exposed PR in AZ 400 K Developer (Merck) for 70 s;

(d) oxide etching using BOE solution for 50 s (etching rate $\sim 220\,\mathrm{nm\,min^{-1}}$);

(e) removal of PR in plasma stripper (in O_2);

8. Dicing of the 3 matrices of diodes using the dicing saw ADT Vectus 7100:

(a) spinning of resist: HPR-504 (Fujifilm), 2000 rpm, thickness = 1.2 µm, to protect the wafer's front during dicing;

(b) dicing in ADT Vectus 7100

(c) stripping wet of the PR in Microstrip 3001 (Fujifilm), 90 °C, for 20 minutes

All the following technological steps are executed on each single diode matrix, with dimension of 3.5 cm × 3 cm (see Fig. A.1).

9. Graphene transfer onto the silicon diode matrix following one of the polymer-based transfer process explained in section 1.4.
   (a) graphene transfer on the diode matrix;
   (b) PMMA removal in acetone vapors;
   (c) SEM observations to verify the uniformity of transferred graphene and the presence of residues and cracks;
   (d) 4-point electrical measurements on continuos Gr (before patterning);
10. Photolithographic process for Gr patterning
   (a) cleaning in hot acetone for 5 minutes;
   (b) dehydration in oven: 110 °C, 15 min
   (c) spinning of resist: HPR-504 (Fujifilm), 2000 rpm, thickness = 1.2 µm;
   (d) PR exposure in Karl Süss MA4: mask-4 - Graphene (Fig. A.2(d)); exposure time: 2 s, hard contact;
   (e) developing process of exposed PR in AZ 400 K Developer (Merck) for 70 s;
   (f) blanket PR exposure in Karl Süss MA4, exposure time = 8 seconds;
   (g) dry etching of Gr in Oxygen plasma: used Fischione plasma etcher, with $25\%O_2 + 75\%N_2$, etching time = 270 seconds;
   (h) removal of PR in AZ 400 K Developer (Merck) for 3 minutes;
11. Photolithographic process for fabrication of metal contact to Graphene
   (a) cleaning of substrates in hot acetone for 5 minutes;
   (b) dehidration in furnace: 110 °C, 15 minutes;
   (c) spinning of resist: 950 PMMA A7 in Anisole, 2500 rpm, thickness ∼ 0.85 µm;
   (d) PMMA exposure in Süss MicroTec mask aligner MA6: mask-5-Metal (Fig. A.2(e)), exposure using DUV (see section 1.5.1): wavelength = 248 nm, total dose = 22500 mJ cm^{-2};
   (e) developing in MIBK:IPA solution 1:3 (MicroChem Corporation), at room temperature for 6 minutes;
   (f) rinse in IPA for 3 minutes;
   (g) evaporation of Cr (adhesion layer): thickness = 10 nm;
   (h) sputtering deposition of the Au: thickness = 70 nm;
   (i) lift-off of Cr/Au performed in hot acetone, at 65 °C, time used 1 hour

A.2 Process flow for the fabrication of Gr integrated photodetectors

The Gr integrated photodetectors reported in section 3.5 are fabricated starting from a SOI wafer from Soitec (6 inches), with 220 nm top crystalline Si, boron doped, with resistivity of $14-22\,\Omega\cdot$cm, buried oxide is 3 µm thick, and bulk Si is 675 µm thick. Steps from 2 to 11 reported in the previous section A.1 are used also for the fabrication of Gr photodetectors, therefore the description of technological process flow will start from the deposition of the a-Si:H layer (step 12).

12. amorphous silicon (a-Si:H) deposition in PECVD system: P = 4 W, applied frequency = 13.56 MHz MHz, pressure = 0.6 mbar, T = 350 °C ($\sim$ 170 °C on the sample), SiH_4 = 20 sccm, deposition time = 1983 s, deposition rate = 1.1 Å/s, obtained thickness = 230 nm;

13. Photolithographic process for patterning of a-Si:H

    (a) dehydration in oven: 80 °C, 30 min;

    (b) spinning of resist: HPR-504 (Fujifilm), 2000 rpm, thickness = 1.2 µm;

    (c) PR exposure in Karl Süss MA4: mask-6 - Amorfo (Fig. A.2(f)); exposure time: 3 s, hard contact;

    (d) developing process of exposed PR in AZ 400 K Developer (Merck) for 70 s;

    (e) blanket PR exposure in Karl Süss MA4, exposure time = 8 seconds;

    (f) dry etching of a-Si:H in RIE Sentech SI 591, SF_6 = 60 sccm, P = 40 W, pressure reactor = 150 mTorr, etch rate = 3.66 nm s^{-1}, etching time = 66 s;

    (g) removal of PR in AZ 400 K Developer (Merck) for 3 minutes;

A.3 Process flow for the fabrication of vertical RCE photodetectors

The vertical RCE Gr/Si photodetectors described in section 3.4 are based on the MESA structure reported in fig. 3.2. The main fabrication steps are presented and discussed in section 3.4.1, while the detailed process flow is reported here. The substrate is a SOI wafer from Soitec (6 inches), with 220 nm top crystalline Si, boron doped, with resistivity of $14-22\,\Omega\cdot$cm, buried oxide is 3 µm thick, and bulk Si is 675 µm thick. The process begins with the fabrication of the thin Si membranes. Two are the main steps: the lapping procedure to reduce the thickness of bulk Si to 400 µm, in order to reduce the etching time for the membrane formation; and the anisotropic etching for the formation of the Si membranes.

1. RCA cleaning;
2. oxide deposition (only on wafer front): low temperature oxide deposition process (LTO), $T = 420\,^{\circ}\mathrm{C}$, time= 33 min, obtained oxide thickness = 520 nm;
3. Lapping of bulk Si: anisotropic Si wet etching in TMAH solution (40% in water, adding PSA to reduce the formation of hillocks on Si), T = 90 °C, etching rate $\sim 1.9\,\mu\mathrm{m/min}$, time used = 270 min, bulk Si thickness obtained =400 µm;
4. RCA cleaning;
5. oxide deposition (only on wafer backside): low temperature oxide deposition process (LTO), $T = 420\,^{\circ}\mathrm{C}$, time= 124 min, obtained oxide thickness = 1.9 µm;
6. Photolithographic process on the back side of the wafer for membrane patterning:
   (a) dehydration in oven: 110 °C, 30 min;
   (b) spinning of resist: OIR-908 (Fujifilm), 2000 rpm, thickness = 4.1 µm, spinning is performed on both sides of the wafer;
   (c) PR exposure in Karl Süss MA4 on the wafer backside: mask-0 - Membrane; exposure time: 20 s, hard contact;
   (d) developing process of exposed PR in AZ 400 K Developer (Merck) for 90 s;
   (e) oxide etching using BOE solution (Fujifilm) for 11 min (etching rate $\sim 220\,\mathrm{nm\,min^{-1}}$);
   (f) anisotropic etching of Si (in Alcatel DRIE A601E, BOSCH low roughness process): etching rate $\sim 5.5\,\mu\mathrm{m\,min^{-1}}$, etching time = 75 min;
   (g) buried oxide etching using BOE solution (Fujifilm) for 36 min (etching rate $\sim 220\,\mathrm{nm\,min^{-1}}$);
   (h) stripping wet of the PR in Microstrip 3001 (Fujifilm), T= 90 °C, for 20 min;

At this stage Si membranes 220 nm thick have been fabricated on the SOI substrate. Then, the technological process goes on with the fabrication on the front side of the metal contacts to Si and the opening of the diodes' active areas (steps from 4 to 7 in section A.1). The following steps describe to the fabrication of the metallic mirror on the backside of the membranes and the fabrication of the optical microcavities a-Si:H/Gr/Si.

1. Fabrication of the metallic mirror
   (a) dehydration in oven: 110 °C, 30 min;
   (b) etch of native oxide from diode active area: dip in HF: H_2O (1:50) solution for 30 s

(c) evaporation of ITO on the backside of the membrane: T=80 °C, thickness = 80 nm;

(d) sputtering deposition of Au: thickness = 100 nm;

2. Graphene transfer on the wafer frontside, following one of the polymer-based transfer process explained in section 1.4

   (a) graphene transfer on the diode matrix;

   (b) PMMA removal in acetone vapors;

   (c) SEM observations to verify the uniformity of transferred graphene and the presence of residues and cracks;

   (d) 4-point electrical measurements on continuos Gr (before patterning);

3. Photolithographic process for Gr patterning

   (a) dehydration in oven: 80 °C, 30 min

   (b) spinning of resist: HPR-504 (Fujifilm), 2000 rpm, thickness = 1.2 µm;

   (c) PR exposure in Karl Süss MA4: mask-4 - Graphene (Fig. A.2(d)); exposure time: 2 s, hard contact;

   (d) developing process of exposed PR in AZ 400 K Developer (Merck) for 70 s;

   (e) blanket PR exposure in Karl Süss MA4, exposure time = 8 seconds;

   (f) dry etching of Gr in Oxygen plasma: used Fischione plasma etcher, with $25\%O_2 + 75\%N_2$, etching time = 270 seconds;

   (g) removal of PR in AZ 400 K Developer (Merck) for 3 minutes;

4. Amorphous silicon (a-Si:H) deposition in PECVD system: P = 4 W, applied frequency = 13.56 MHz, pressure = 0.6 mbar, T = 350 °C($\sim$ 170 °C on the sample), SiH_4 = 20 sccm, deposition time = 1983 s, deposition rate = 1.1 Å/s, obtained thickness = 230 nm;

5. Photolithographic process for patterning of a-Si:H

   (a) dehydration in oven: 80 °C, 30 min;

   (b) spinning of resist: HPR-504 (Fujifilm), 2000 rpm, thickness = 1.2 µm;

   (c) PR exposure in Karl Süss MA4: mask-6 - Amorfo (Fig. A.2(f)); exposure time: 3 s, hard contact;

   (d) developing process of exposed PR in AZ 400 K Developer (Merck) for 70 s;

   (e) blanket PR exposure in Karl Süss MA4, exposure time = 8 seconds;

(f) dry etching of a-Si:H in RIE Sentech SI 591, SF_6 = 60 sccm, P = 40 W, pressure reactor = 150 m Tr, etch rate = 3.66 nm s^{-1}, etching time = 66 s;

(g) removal of PR in AZ 400 K Developer (Merck) for 3 minutes;

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Il tuo indirizzo e-mail

piera.maccagnani@edu.unife.it

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Ferrara

Provincia:

Ferrara

Il giorno:

07/07/1963

Avendo frequentato il Dottorato di Ricerca in:

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Titolo della tesi (traduzione):

Integrazione del grafene nella tecnologia planare del silicio per la fabbricazione di dispositivi ibridi

Tutore: Prof. (Cognome e Nome)

Bisero Diego

Settore Scientifico Disciplinare (S.S.D.)

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