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Development of an innovative hybrid single-photon imaging detector based on a Timepix4 CMOS ASIC embedded as pixelated anode

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Ph.D. Candidate

Dott. Riccardo Bolzonella

Supervisor

Prof. Massimiliano Fiorini

Thesis co-supervisor

Prof. Jerzy Wojciech Mietelski

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Development of an innovative hybrid single-photon imaging detector based on a Timepix4 CMOS ASIC embedded as pixelated anod

Riccardo Bolzonella

Abstract

An innovative single-photon detector is presented, based on a vacuum tube containing a photocathode, a microchannel plate, and a Timepix4 CMOS application-specific integrated circuit (ASIC) as its readout anode. This detector has been developed to detect up to 1 billion photons per second over a $7\,\mathrm{cm}^2$ active area, while achieving exceptional position resolution of $5 - 10\,\mu$m and timing resolution below 50 ps. The Timepix4 ASIC, which features approximately 230 thousand pixels equipped with both analog and digital front-end electronics, operates on a data-driven architecture, and it allows data transmission with bandwidth reaching up to 160 Gb/s.

The configuration and readout of the Timepix4 are controlled by FPGA-based external electronics, either the SPIDR4 DAQ system or the custom DAQ system developed by INFN Ferrara.
The DAQ system, the DAQ software and the analysis software developed are presented.
A characterization of a Timepix4_v2 assembly bonded to a 100 µm thick planar n-on-p Si detector has been performed. The presented characterization includes charge calibration and charge resolution estimation, as well as estimation of the timing performance.
A picosecond laser setup has been used to illuminate the sensor and generate electron-hole pairs in the silicon bulk, controlling the amount of charge, and the time and position of the generated signal.
The timing resolution per single pixel hit was measured at 107 ps, taking into account the silicon's contribution as well. When considering pixel clusters, the timing resolution improves to below 50 ps.

The ceramic carrier quality tests will be presented too, consisting of mechanical and electrical measurements, as well as a diagnostic of the basic operation of the Timepix4 ASIC mounted on the ceramic.

Furthermore, the characterization procedure of the first prototypes of the photo-

tubes will be discussed. It includes dark count rate and gain measurements, as well as timing resolution estimation.
Currently, a single prototype has been tested; the characterization and comparison of the other prototypes is ongoing.
Regarding the prototype tested, the expected dark count rate and gain trends have been obtained. The dark count rate results to be in the range between $\sim 1\,\mathrm{Hz/cm^2}$ and $\sim 30\,\mathrm{Hz/cm^2}$, depending on the MCP bias. The gain ranges from $\mathcal{O}\left(10^3\right)$ to $\mathcal{O}\left(10^5\right)$, depending on the MCP bias.
A non-uniform dark count structure has been observed across the matrix, and further studies are ongoing to better understand its source.
The timing resolution has been estimated with a method analogous to the one used to estimate the one of the assembly bonded to a Si detector. The single pixel timing resolution obtained is (107 ± 6) ps, while the cluster timing resolution reaches (88 ± 5) ps.

Eventually, a testbeam organized to characterize the developed phototubes with a Cherenkov setup is described.

Contents

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The LHCb experiment

The LHCb experiment is one of the four large experiments active at the Large Hadron Collider (LHC) accelerator complex, together with ALICE, ATLAS and CMS. Its main purpose is looking for new physics studying CP-violation and heavy-flavours hadrons decay [1].

It is operating since 2010: during the first two LHC runs (Run 1 from 2010 to 2012 and Run 2 from 2015 to 2018), it collected a total of $9\,\text{fb}^{-1}$ of proton-proton (pp) collisions, $30\,\text{nb}^{-1}$ of lead-proton, $200\,\text{nb}^{-1}$ of lead-lead and $200\,\text{nb}^{-1}$ of fixed target collisions. The detector has been originally designed to reach a maximum luminosity of $\mathcal{L} = 2 \times 10^{32}\,\text{cm}^{-2}\text{s}^{-1}$, but it has been successfully operated at twice the designed luminosity proving the feasibility to run LHCb at higher pile-up than the pile-up foreseen.

After LHC Run 2 a first upgrade, the LHCb Upgrade I, has been performed, to run at a nominal instantaneous luminosity of $\mathcal{L} = 2 \times 10^{33}\,\text{cm}^{-2}\text{s}^{-1}$ and to collect the full LHC bunch crossing rate of 40 MHz. During the LS4 another upgrade (LHCb Upgrade II) will be performed to allow LHCb to successfully operate to run with an instantaneous luminosity increased between a factor 5 and 7 with respect to Upgrade I, corresponding to a pile-up of approximately 40.

The foreseen upgrades and the proposals for LHCb Upgrade II will be presented in Section 1.3.

1.1 LHCb detector architecture

In this section the current status of LHCb detector, namely the one following the Upgrade I, is described.

LHCb is a single-arm forward spectrometer with a forward angular acceptance covering the range $10 - 300\,\text{mrad}$ in the horizontal plane, and $10 - 250\,\text{mrad}$ in the vertical plane, corresponding to a pseudorapidity range $2 < \eta < 5$ [2].
Since the main purpose of the experiment is the study of CP-violation and of rare decays of beauty and charm hadrons, the detector is optimised to measure decays of heavy-flavour hadrons at high energies.
Considering a right-handed coordinate system with the origin in the nominal pp interaction, the y-axis pointing vertically upward and the z-axis directed along the beam-line, pointing towards the muon system, a schematic of the z-y section of LHCb layout is shown in Figure 1.1. Tracks produced in LHCb are bent by a dipole magnet generating a magnetic field along y direction.
Most of the subdetectors element are split into two, which are mechanically independent to allow for easier maintenance operations.

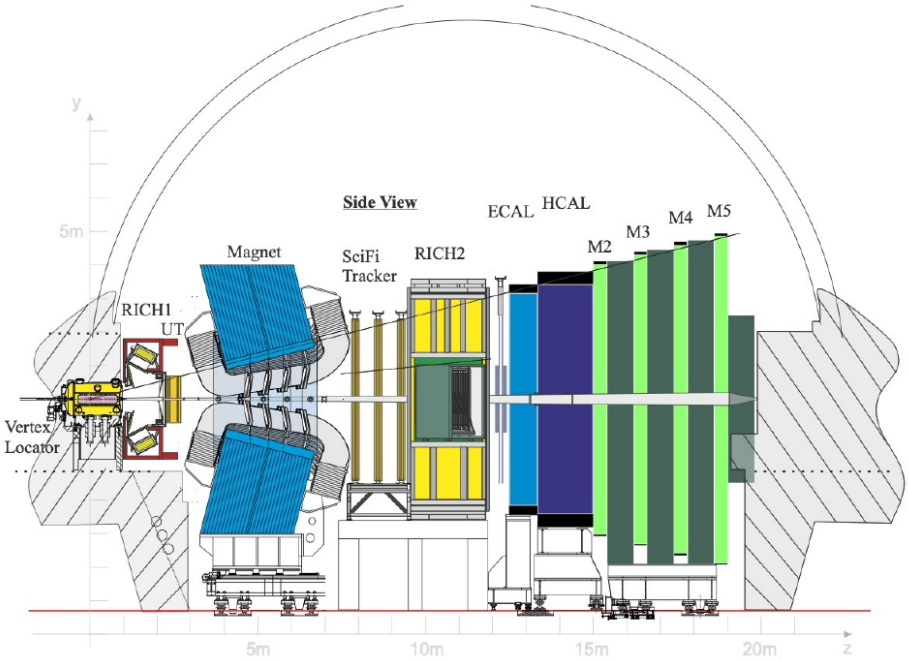


Figure 1.1: Current layout of LHCb detector, after Upgrade I [2].

The detector includes three main systems:

- **tracking system**: it is dedicated to the tracks reconstruction, based on

the positions of particle interactions with the detector; it is composed by several sub-detectors, including an array of pixel silicon detectors as vertex locator (VELO), the upstream-tracker (UT) in front of the bending magnet and three scintillating fibre-tracker stations (SciFi) placed downstream of the magnet [2]; this system will be further described in Subsection 1.1.1;

- **particle identification system**: charged-hadron identification is performed by two Ring Imaging Cherenkov (RICH) detectors, placed upstream and downstream of the magnet, respectively; an electromagnetic and a hadronic calorimeter (ECAL and HCAL) following the second RICH detector provide information on electrons, photons and hadrons energy and position; lastly, four muon stations (M2-M5) allow to detect the muons [2]; this system will be further described in Subsection 1.1.2, except for the RICH detectors description, that will be treated in more detail in Section 1.2;
- **trigger system**: responsible of selecting interesting events for offline analysis; originally it was based on a low-level hardware trigger (L0) partially processing information to make a first selection of data with an output rate of 1.1 MHz, which are then subject to a more complex processing by a high-level software trigger (HLT). One of the key elements of Upgrade I, together with the continuous readout of all subdetectors at 40 MHz, is the removal of the L0 trigger. The trigger system, fully implemented in software, processes 40 Tb/s of data and write 10 Gb/s on storage. The readout and trigger strategy allows to increase the efficiency in fully hadronic channels by at least a factor two [2].

1.1.1 Tracking system

This system is responsible for the reconstruction of the trajectories of the particle tracks. The momentum is derived from its deflection angle after passing through the magnet. It is composed by a vertex locator, silicon strips tracker stations and scintillating fibre-tracker stations.

The Vertex Locator (VELO)

The first sub-detector is the Vertex Locator (VELO), which measures the vertex positions and seed them to the reconstruction algorithm of LHCb spectometer. The current VELO [3], having a total Silicon active area of $0.12\,\mathrm{m}^2$, is based on silicon n-on-p pixel detectors with dimensions of $55\,\mu\mathrm{m} \times 55\,\mu\mathrm{m}$, read out by the VeloPix ASIC [4] at a frequency of 40 MHz with a 20.4 Gb/s bandwidth. The inner radius between the beam and the silicon detector is 5.1 mm when the detector is closed.

The forward geometry is ideal for fixed-target experiments as well, due to the high boost acquired by the produced particle in the laboratory frame.
A gas injection system, called System for Measuring the Overlap with Gas (SMOG), is used to inject noble gases (e.g. Helium, Argon and Neon) into the VELO vessel, allowing to perform fixed-target physics within LHCb [5].
After LHCb Upgrade I the gas is injected into a storage cell instead of injecting it directly into the vessel, to increase the areal density keeping the same injected flux, resulting in integrated luminosity orders of magnitude larger than before.

The upstram-tracker (UT)

The second element of the tracking system is the UT, located between the RICH1 detector and the bending magnet [2, 6]. It is fundamental to significantly reduce the ghost tracks rate, to improve the invariant mass resolution by about 30%, and to perform downstream tracking of particles decaying after the VELO, such as the K_S^0 or the Λ^0.
This detector comprises four planes of silicon detectors organised in two stations, where the strips are arranged in units called staves. The first station ("a") is composed by a layer of vertical strips (UTaX) measuring the x coordinate, and a layer of stereo strips tilted by 5° (UTaU). Similarly, the second station is composed by a first layer of stereo strips tilted by $-5°$ (UTbV) and a layer of vertical strips (UTbX), further from the nominal interaction point.
The gap between UTaU and UTbV is 205 mm, while the one between two planes of each station is 55 mm. A schematic of this detector is shown in Figure 1.2.

The scintillating fibre tracker (SciFi)

Lastly, a scintillating fibre tracker, shown in Figure 1.3, is located downstream of the dipole magnet, and it is responsible for tracking charged particles and measuring their momentum [2, 7]. The aim of this detector is achieving momentum resolution and tracking efficiency for beauty and charm hadrons comparable with the ones obtained during Run1 and Run2.

The detector uses 2.4 m long plastic scintillating fibres with a diameter of 250 µm. Its acceptance extends from about 20 mm from the beam pipe edge, to 3186 mm in the horizontal direction and 2425 mm in the vertical one.
The detector is composed of 3 stations (T1, T2, T3), each one comprising 4 detection layers, arranged in $x - u - v - x$ configuration, similarly to the UT tracker. Each layer is composed by 8 sub-layers of fibres, for a total surface of about 6 m × 5 m, and a total thickness of 1.35 mm.
The optical signals generated by the scintillating fibres are detected by 128-channel

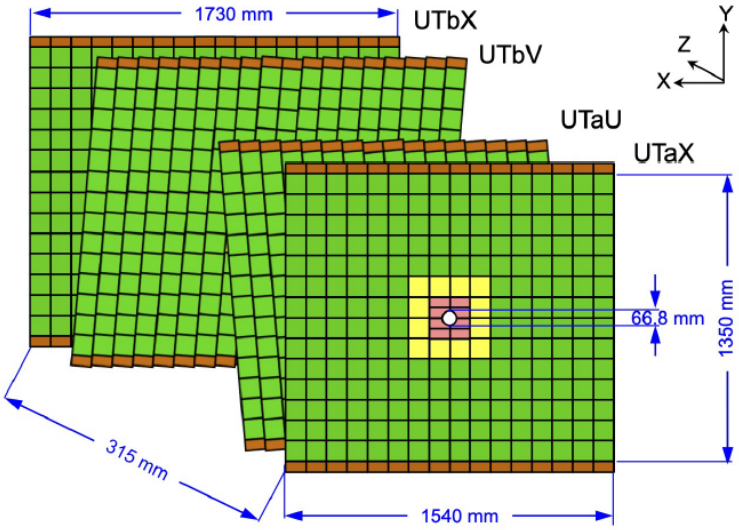


Figure 1.2: Schematic of upstream tracker, consisting of four planes of silicon strips, two of them comprising vertical strips, and the other two composed by stereo strips tilted by ±5° [2].

arrays of Silicon Photomultipliers (SiPMs) with a channel pitch of 250 µm, placed on one side of the fibres; a thin mirror is placed on the other fibre end, to reflect additional light to the readout array.

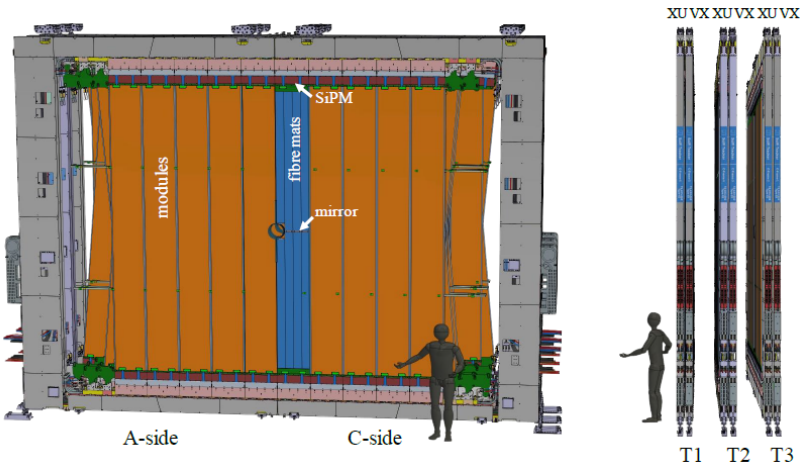


Figure 1.3: Schematic of the scintillating fibre tracker, consisting of 3 stations, each one including 4 layers of scintillating fibres oriented vertically or tilted by ±5° [2].

1.1.2 Particle identification system

Particle identification consists of categorising particles based on their tracks characteristics (mass, charge, momentum), and it is fundamental for flavour physics. Within the LHCb experiment, the PID system consists of three sub-detectors: the RICH detectors, the electromagnetic and hadronic calorimeters, and the muon stations [2]. In this subsection the latter subdetectors will be described, while the RICH detectors will be described in more detail in Section 1.2.

Calorimeters

The calorimeter system is composed by an electromagnetic calorimeter shashlik type (ECAL) [8] and an hadronic calorimeter (HCAL).

The ECAL, composed by a sampling scintillator and a lead structure, has a lateral segmentation, which is organised in three different sections [9]. Their transverse dimensions scale with the distance from the nominal interaction point, to take into account hit density variations over the surface. The main section allows to reduce the background from charged pions by measuring the longitudinal spread of electromagnetic showers. The outer acceptance matches the one of the tracking system, while the inner one is limited at a higher polar angle ($\theta > 25\,\text{mrad}$) by the squared hole surrounding the beamline. The ECAL has a total thickness of $25\,X_0$. The schematic of a cell of the ECAL is shown in Figure 1.4

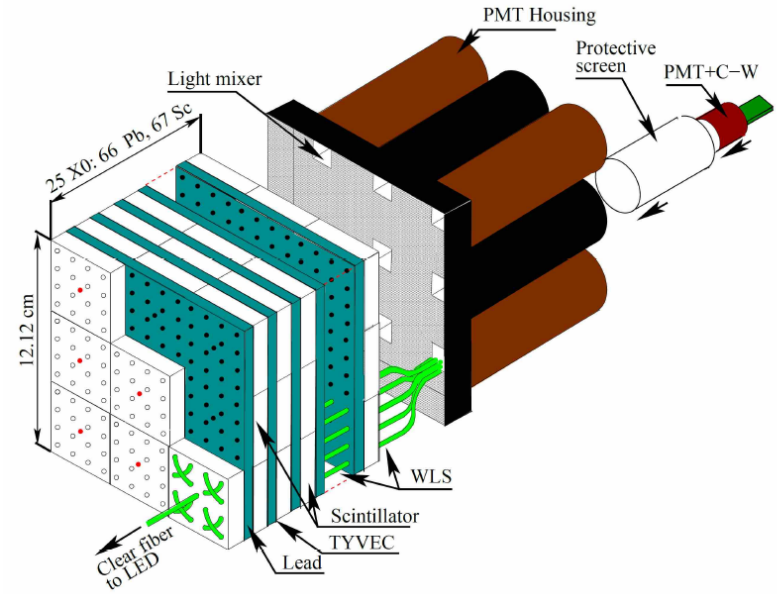


Figure 1.4: Schematic of a cell of the electromagnetic calorimeter [2, 10].

The HCAL is segmented into two zones, having different lateral dimensions, and it uses iron as absorbing material and scintillating tiles parallel to the beam axis as active material [9].
Its thickness is 5.6 nuclear interaction lengths (λ_i).

Differently from most of others sub-detectors, both the ECAL and HCAL have not been upgraded during LHCb Upgrade I, since they already had sufficiently high granularity to operate in higher luminosity conditions.

The muon detector

The muon detector is responsible for muon identification. Originally, it was composed by five stations (M1-M5) [11]; however, during the LHCb Upgrade I the first station, used in the hardware trigger L0, has been removed [2, 12].
Thus, the muon system is currently composed by four stations (M2-M5), equipped with 1104 multi-wire proportional chambers (MWPC) for a total area of $385\,\mathrm{m}^2$.
The stations are interleaved with 80 cm thick iron absorbers which filter out low energy particles.
Each station is divided into four regions (R1-R4) with increasing area moving out from the beam axis, in order to uniformly distribute the occupancy across the surface.

The MWPC comprises four independent layers, each one consisting of anode wires between two cathode planes. This organization allows to achieve both high efficiency and high redundancy.

1.2 RICH detectors

A crucial aspect of the LHCb physics program is the discrimination of charged hadrons, consisting of the recognition of pions, kaons and protons.
In LHCb hadrons identification is performed by the RICH system in the momentum range of $2.6 - 100\,\mathrm{GeV/c}$ [13].
This system allows to reduce the background of decays involving hadrons, and to distinguish between final states of decay modes that otherwise would have identical topologies. Moreover, it allows to flavour tag the $B^0_{(s)}$ identifying charged kaons.

1.2.1 Cherenkov effect

The working principle of the RICH detectors is based on the Cherenkov effect: a charged particle passing through a dielectric medium of refractive index n with a velocity $\beta = \frac{v}{c} > 1/n$ emits Cherenkov photons. As shown in Figure 1.5, the

photons are emitted at a characteristic angle with the particle direction, called Cherenkov angle θ_c, related to the particle velocity as

$$\cos(\theta_c) = \frac{1}{\beta n} \tag{1.1}$$

Thus, the minimum particle velocity needed to emit Cherenkov radiation is the one corresponding to $\theta_c = 0°$, that is

$$\beta_{th} = \frac{1}{n} \tag{1.2}$$

Conversely, the maximum Cherenkov angle is reached when the velocity approaches the speed of light in vacuum ($\beta \to 1$), given by

$$(\theta_c)_{max} = \arccos\left(\frac{1}{n}\right) \tag{1.3}$$

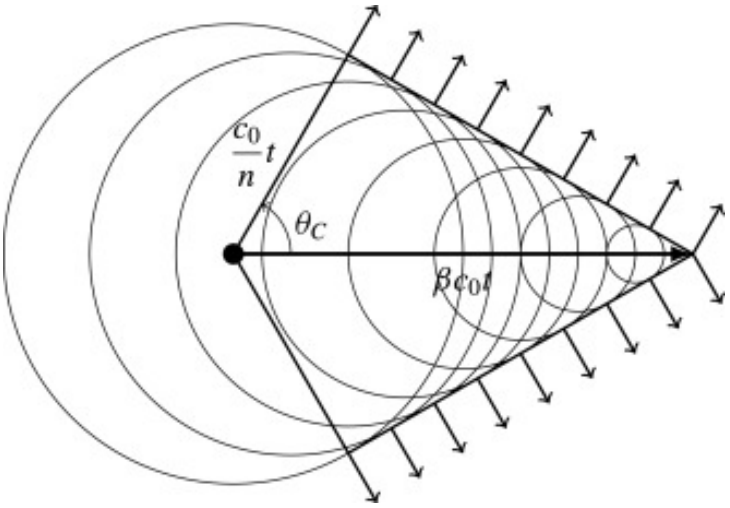


Figure 1.5: Schematic of the Cherenkov radiation emission of a particle with velocity βc_0 passing through a medium with refractive index n [14].

The particle velocity estimation provided by the RICH and the estimation of the particle momentum p performed by the tracking system allow to evaluate the particle mass m, as $m = p/(\beta\gamma)$.

If the particle velocity is high enough to saturate the Cherenkov angle close to its maximum value, it's not possible to experimentally distinguish different charged particles. Besides, these saturated tracks can be used to determine the Cherenkov angle resolution of a RICH detector, by comparing the measured angle with the

expected one.

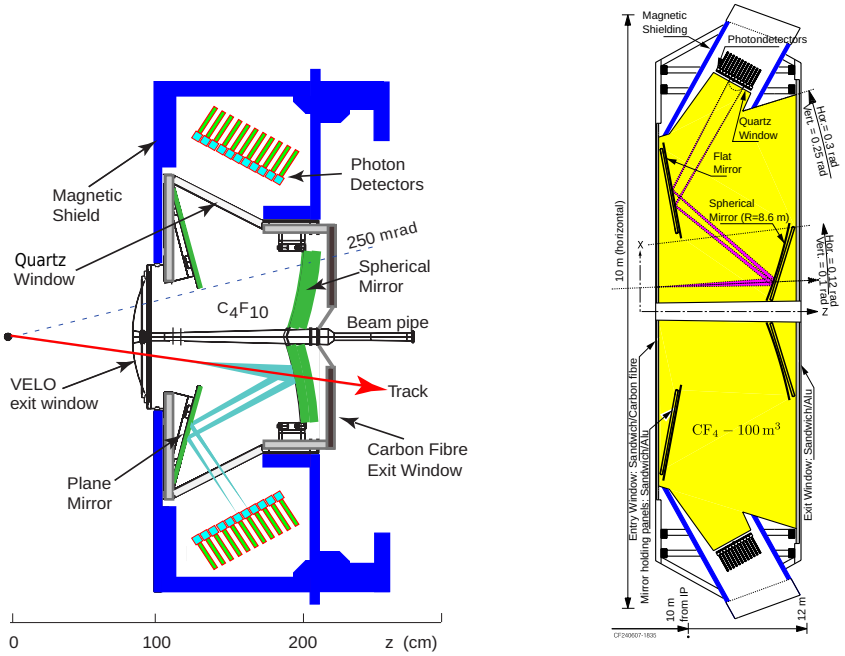
The yield of photons emitted per unit of wavelength in a unit length of the particle's path in the radiator is

$$\frac{d^2N_\gamma}{dxd\lambda} = \frac{2\pi z^2 \alpha}{\lambda^2}\left(1 - \frac{1}{\beta^2 n^2}\right) \tag{1.4}$$

where z is the particle charge in number of electrons and α is the electromagnetic coupling constant [15]. Equation 1.4 shows that the Cherenkov radiation is dominated by short wavelengths.
Thanks to the prompt emission of the Cherenkov radiation and to the focusing optics of the RICH system, signal photons from the same bunch crossing reach the photon detection plane with a time spread of a few hundreds of picoseconds.

1.2.2 RICH detector system layout

The RICH detectors system consist of two detectors, RICH1 and RICH2. A schematic of the detectors, including their optical systems, is shown in Figure 1.6.



(a) (b)

Figure 1.6: Schematics of **(a)** RICH1 and **(b)** RICH2 detectors [16].

The RICH1 detector, located upstream of dipole magnet, covers an angular acceptance ranging from 25 mrad to 300 mrad on the horizontal plane, and from

25 mrad to 250 mrad on the vertical plane. The photon detector planes are placed above and below the beam pipe.
A series of spherical and planar mirrors carry the Cherenkov photons produced in the fluorocarbon gaseous radiator to the photon detectors, focusing them on the detector planes. The gaseous radiator used is C_4F_{10}, which allows to provide PID in the momentum range $2.6 - 60\,\mathrm{GeV/c}$.

RICH2 is located downstream of the magnet, covering an acceptance in the range $15-120$ mrad in the horizontal plane, and $15-100$ mrad in the vertical one. In this system, the photon detectors are placed at the RICH sides. Similarly to RICH1, photons are directed to the detectors through spherical and planar mirrors.
Using CF_4 as gaseous radiator, RICH2 can provide PID at higher momentum with respect to RICH1, since the refractive index is lower at $\lambda = 400\,\mathrm{nm}$, allowing to recognize particles with a momentum from $15\,\mathrm{GeV/c}$ to $100\,\mathrm{GeV/c}$.

The RICH system has been designed to avoid occupancies exceeding 30%, to optimize the efficiency of the RICH reconstruction algorithm. The occupancy is not uniform, going from about 30% in the RICH1 central region, to 5% in the RICH2 outer region.

1.2.3 The RICH system photon detectors: the MaPMTs

The photon detectors are required to have a good spatial resolution on a large active area, to have a low noise, and to grant high efficiency in the range $200 - 600\,\mathrm{nm}$.
The solution selected consists of multi-anode photomultiplier tubes (MaPMTs), read out by front-end electronics allowing to sustain the required 40 MHz LHC crossing rate [17].

The MaPMTs of both RICH1 and RICH2, shown in Figure 1.7, consist of matrices of 8×8 anodes, with a fill factor higher than 80%.
The model used in RICH1 and the central region of RICH2 is a 1-inch MaPMT module, with a pixel size of $2.88\,\mathrm{mm} \times 2.88\,\mathrm{mm}$, with a higher segmentation ideal for the high occupancy expected. The RICH2 external region is instead equipped with a 2-inches module with pixel size $6\,\mathrm{mm} \times 6\,\mathrm{mm}$, since a lower occupancy is expected.

The MaPMT modules have gain larger than 10^6 and a dark-count rate lower than $2.5\,\mathrm{kHz/cm^2}$. A total of 1888 modules have been installed in RICH1, while RICH2 is read out by 768 1-inch modules and 384 2-inch modules.

Figure 1.7: MaPMTs models used in the LHCb RICH Upgrade I: the model on the left is the 2-inches one used in the RICH2 low occupancy regions, while the right model is the 1-inch model used in the RICH1 and RICH2 high occupancy regions [17].

1.2.4 Front-end electronics: CLARO and elementary cells

The hit rate in high occupancy regions of RICH1 can reach up to 10^7 hits/s per pixel, and the dose integrated over the detectors lifetime will be about 2 kGy; hence, a radiation-hard fast electronics with low power consumption is needed, and this requirement lead to development of an 8-channel front-end, named CLARO [18, 19].

CLARO is designed in the 350 nm CMOS Austria Micro System (AMS) [20] technology. Each channel includes an analogue amplifier and a discriminator.
Single channel configuration can be performed through a 128-bit register. In particular, it allows to individually tune the channel threshold and input signal attenuation, to compensate both for gain differences and discriminator offsets.

The number of channels matches the MaPMT modularity, allowing to place the ASIC close to the anodes to reduce the parasitic capacitance.
The readout system is arranged in modules named elementary cells (ECs): an R-type elementary cell (EC-R) is designed to read out four 1-inch MaPMTs, while H-type elementary cells (EC-H) read out a single 2-inches MaPMT.
The EC-Rs include cross-shaped magnetic shields, as visible in Figure 1.8, to attenuate the magnetic field reaching the MaPMTs.

The CLARO ASICs is connected to front-end boards (FEBs) routing the output signals to photon detector module digital boards (PDMDBs), which are also

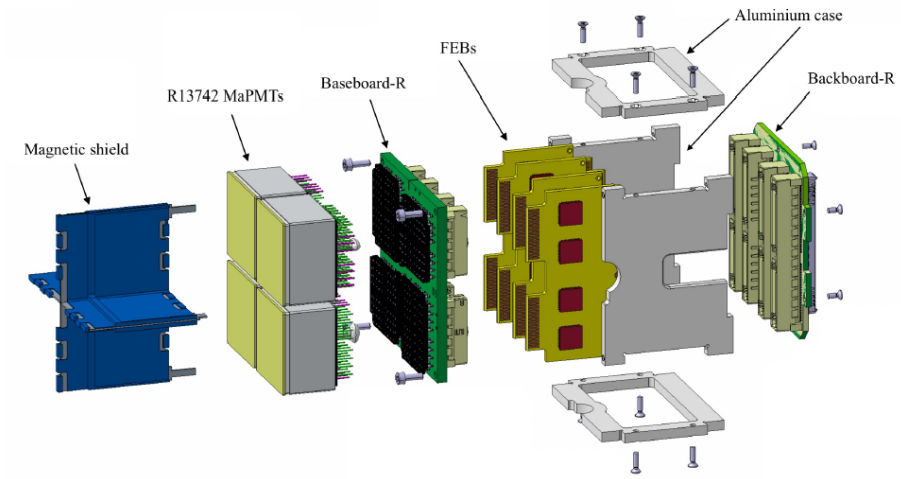


Figure 1.8: Schematic of the R-type elementary cell, designed to host and read out four 1-inch MaPMT [17].

responsible for the CLARO configuration and power supply control.

1.3 LHCb Upgrade II

The LHCb Upgrade II aims to fully exploit the High Luminosity LHC environment, allowing operations up to an instantaneous luminosity of $1.5 \times 10^{34}\,\mathrm{cm}^{-2}\mathrm{s}^{-1}$ [21]. The installation will take place during the Long Shutdown 4 (LS4), and the upgraded detector is supposed to start taking data in 2036, reaching an integrated luminosity of at least $300\,\mathrm{fb}^{-1}$ [22, 23].

The LHCb Upgrade II program [21] aims to:

- precisely measure CKM matrix mixing coefficients and CP violation in B^0, $B^0_{(s)}$ and D^0 with uncertainties below the theoretical uncertainties;
- study rare decays, such as $B^0_{(s)} \to \mu^+\mu^-$, $b \to sl^+l^-$ or $b \to dl^+l^-$, including also muon and electron decays;
- spectroscopy studies, including studies of tetraquarks, pentaquarks and heavy baryons;
- further studying production and properties of Z, W and H bosons, as well as searching dark-photons and particles beyond the Standard Model;
- perform new studies of heavy ion collisions through fixed target experiments.

1.3.1 Scoping scenarios

In the baseline proposal, the LHCb detector will be able to operate at a maximum peak luminosity of $1.5 \times 10^{34}\,\mathrm{cm}^{-2}\mathrm{s}^{-1}$, allowing to fully exploit the $50\,\mathrm{fb}^{-1}$/year delivered by HL-LHC.
However, two descoped scenarios, Middle and Low, have been identified to envelope the upgrade costs [24].
For this thesis purpose, the focus will be on the baseline scenario description, while a brief description of the low cost scenarios will be provided in this subsection.

Baseline scenario

The spectrometer acceptance will be maintained with respect to LHCb Upgrade I, slightly decreasing at low angles from 5.0 to 4.8 coverage in pseudorapidity.
The tracking system will consist of a Vertex Locator (VELO) and tracking stations upstream (Upstream Pixel tracker UP) and downstream (Mighty-Tracker, MT) the bending magnet. The MT will consist of silicon tracker in the inner region and scintillating fibres in the outer region. An additional tracking station with respect to the Upgrade I, called Magnet Station (MS), will cover the magnet sides.
The PID system will consist of the two RICH detectors, a new electromagnetic calorimeter (PicoCal) and the four muon station M2-M5. A new time-of-flight detector, TORCH, will be placed upstream of RICH2.
A schematic view of the baseline scenario LHCb Upgrade II is presented in Figure 1.9.

The tracking system will need to sustain radiation damage much higher than now, reaching a fluence of $6 \times 10^{16}\,1\,\mathrm{MeV}\,n_{eq}/\mathrm{cm}^2$ in the inner VELO sections.
New detectors are under development to be used in the VELO system, providing simultaneously information with high timing and spatial resolution. To meet these requirements, the VELO ASIC will be designed in a 28 nm technology, and new radiation-hard silicon sensors are under development as well.
Regarding the tracking stations, high-granularity pixel detectors are required. A strong candidate is the radiation-hard Depleted Monolithic Active Pixel Sensor (DMAPS) technology [25].
Eventually, the Magnetic Station will detect particles hitting the side walls of the magnet, extending the acceptance to lower momentum.

The RICH system will be an evolution of the current one, with new detectors with high granularity and excellent timing performance (e.g., SiPM or Micro-Channel Plates) replacing the MaPMTs. The electromagnetic calorimeter will be improved, implementing a new SpaCal design [26] for the inner part, and keeping a Shashlik design for the outer parts [22, 23].

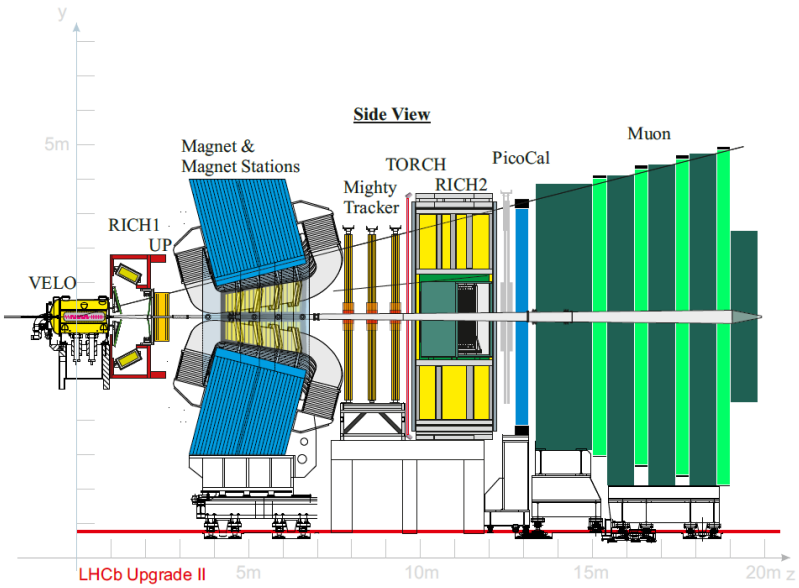


Figure 1.9: Schematic side-view of the LHCb detector as designed in the baseline scenario of Upgrade II [24].

In the innermost region of the muon stations, the multi-wire proportional chambers will be replaced by designs with both high granularity and high rate capabilities [21, 22, 23]. A good candidate technology would be the $\mu-$RWELL [27], a Micro-Pattern Gaseous Detector based on the principle of Gas Electron Multiplier detectors.

Low cost scenarios

A common point for both the low cost scenarios is the reduction of the luminosity from 1.5 to $1.0 \times 10^{34}\,\mathrm{cm}^{-2}\mathrm{s}^{-1}$ [24]. The reduction in luminosity will be achieved by reducing the pile-up, leading to a decrease of the peak of detector occupancy. Operating at lower peak luminosity would increase the leveling time, improving the stability of the detector-related systematics.

For the Middle scenario, the luminosity peak reduction would relax the granularity requirements, in particular on the silicon pixels of the Mighty-Tracker.
Both the muon and RICH detectors would have a consistent reduction in granularity, while the TORCH active area would be reduced, reducing the acceptance by $\sim 25\%$. This reduction has less redundancy with respect to the baseline one; still, thanks to the good balance between the granularity and peak luminosity reductions, robust performance are expected.

For the Low scenario, the proposed new detectors, as the TORCH and the Magnet Station, are eliminated. The outer acceptance of the Mighty-SciFi will be reduced. The current optical system of RICH2 will be maintained as it is.

1.3.2 New instrumentation development and ongoing research

Collecting data in the HL-LHC environment will be challenging: the instantaneous luminosity will be $\mathcal{L} = 1.5 \times 10^{34}\,\mathrm{cm}^{-2}\mathrm{s}^{-1}$ in the forward direction, corresponding to a pile-up of 42, meaning that about 2000 charged particles would be generated per LHC bunch crossing.
Moreover, the aimed integrated luminosity of $300\,\mathrm{fb}^{-1}$ corresponds to an absorbed dose such that radiation-hardness is a fundamental requirement, especially for the VELO [21].
PID detectors are required to cope with high occupancy.
The calorimeters have to keep resolution performance compatible with the current one while receiving an integrated dose of about 200 MRad.
Eventually, the trigger and data acquisition system (TDAQ) is required to be able to process up to $400 - 500\,\mathrm{Tb/s}$ and reduce the amount of data by 4-5 orders of magnitude before storing them.

In this section, several proposals for each system upgrade will be presented. The proposals for the RICH detectors upgrade will be treated in more detail in Section 1.4 and in Chapter 2.

1.3.3 Tracking system upgrade

The tracking system upgrade must be designed in order to increase its resolution, while keeping the occupancy at a level close to the current occupancy. Thus, the granularity will be increased, and the material budget will be reduced to decrease multiple scattering.
In order to correctly associate decays to their primary vertex, fast-timing information is required. Such information will also improve particle tracks reconstruction.

Practically, this leads to requirements for VELO sensors specification, namely pixel size $\lesssim 55\,\mu\mathrm{m}$, timing resolution $\lesssim 100\,\mathrm{ps}$ and good radiation hardness.

The downstream tracking stations will be updated following an analogous strategy, increasing the granularity, reducing the material and using timing information. In particular, silicon pixel detectors based on CMOS technology with dimension $100\,\mu\mathrm{m} \times 1\,\mathrm{cm}$ are candidates under investigation [21].

1.3.4 PID system upgrade

Improving PID performance is crucial to reach the physics goals proposed for Upgrade II. This improvement requires an update of most of PID system sub-detectors.

A possibility to improve PID performance at low momentum is the use of a TORCH (Timing of internally Reflected Cherenkov photons) detector to be installed upstream RICH2 [21].
TORCH detectors combine Micro-Channel Plate (MCP) PMTs with thin quartz plates used as Cherenkov radiators to provide precise time-of-flight (ToF) measurements, allowing to achieve a timing resolution of about 70 ps per photon [28, 29]. Exploiting the ToF measurement, proton-kaon identification can be extended in the region below 10 GeV/c.

The ECAL upgrade is crucial for the identification of electrons, photons and π^0; the main challenge is given by the expected rate and integrated dose.
The technology that will be chosen has to be radiation hard to survive the high integrated dose, and it has to have small size cells (for) to maintain the occupancy similar to the current occupancy. The scintillator has to be fast and have a high timing resolution, to reduce pile-up.
Currently, several technologies are being considered, such as homogeneous crystal calorimeter with longitudinal segmentation, as for instance multi-doped GAGG crystals, or sampling calorimeters with a crystal component for fast-timing, either Shashlik or SpaCal.

The hadronic calorimeter will be removed, since it will not be required anymore by the upgraded trigger [22]. Besides, an extra iron shielding will be introduced at its place, to reduce the flux of pions reaching the muon system, and increasing the muon reconstruction performance.

1.4 Overview on LHCb RICH Upgrade II

The requirements on the main specifications of the Upgrade II RICH system are based on studies on simulation and experimental data to optimize the particle identification algorithm in the HL-LHC environment, estimating how the PID performance is affected by the occupancy increase and signal-to-noise ratio worsening [30, 31].
From these studies it resulted that RICH occupancy must be kept below 30% and the single photon angular resolution must be lower than 0.5 mrad [22]. Such a resolution takes into account uncertainties related to refractive index variation at different photons wavelength, pixel granularity, and optical system uncertainties

(on the optical emission point or on the particle track direction reconstruction). Photon detectors, optical system and tracker system upgrade are crucial to reach the required performance.

1.4.1 Main requirements on photon detectors

Currently, there are no photon detectors meeting all the requirements. Thus, a consistent R&D campaign is ongoing to develop devices able to reach the aimed characteristics and be suitable for Upgrade II RICH readout.
The most crucial features of such detectors must be:

1. peak occupancy reduction, achievable by increasing the granularity to pixel sizes smaller than $1 \times 1\,\mathrm{mm}^2$;
2. angular resolution improvement: depending on chromatic uncertainties, related to the optical system, and pixel spatial resolution;
3. timing resolution improvement: measuring single photon time-of-arrival with a resolution lower than 100 ps is required to associate Cherenkov photons to the corresponding tracks;
4. LHC will operate at a 40 MHz crossing rate, and to keep a good signal-to-noise ratio and a negligible dead time, the requirements are:
   (a) dark-count rate limited to below $100\,\mathrm{kHz/mm}^2$;
   (b) good radiation tolerance, allowing to sustain a fluence of around $2 \cdot 10^{13}\,1\,\mathrm{MeV\,neq/cm}^2$ for the expected integrated luminosity of $300\,\mathrm{fb}^{-1}$.

Angular resolution

The goal for the Upgrade II is reaching an angular resolution of 0.38 mrad on RICH1 and 0.22 mrad on RICH2. This improvement must be accompanied by an equivalent improvement of the tracking system.

Improving the angular resolution requires chromatic uncertainty reduction, improved pixel granularity and emission point error reduction.
In order to reduce the chromatic uncertainty the photon detection efficiency (PDE) spectrum must be moved from the blue region towards the green region keeping a comparable light yield.
The current RICH1 peak occupancy for a MaPMT ($2.8 \times 2.8\,\mathrm{mm}^2$) is about 35%, but the LHCb simulation showed that in the HL-LHC environment the occupancy is saturated. Conversely, pixels with a $1 \times 1\,\mathrm{mm}^2$ size would have an occupancy

of about 18%, proving that improvements on pixel granularity are crucial to keep the occupancy at a manageable level.

The optical geometry will be upgraded as well to reduce its contribution to the Cherenkov angle resolution; according to the simulations, aiming to reach resolution values of $\sim 0.20\,\text{mrad}$ for RICH1 and $\sim 0.10\,\text{mrad}$ for RICH2.

The possibility of replacing the current fluorocarbon gas radiators with eco-friendly gases is under studied, including CO_2 in RICH2; however, a possible drawback is the degradation of the angular resolution.

Timing resolution

The optics system ensures that the Cherenkov photons generated by a single particle reach the detection plane within an interval of $\sigma_{RICH1} = 5\,\text{ps}$ in RICH1 and $\sigma_{RICH2} = 50\,\text{ps}$ in RICH2. Exploiting the tracking system information it would be possible to determine photons time of arrival for a given track within 10 ps for both RICH systems [32].
Such excellent intrinsic timing resolution would allow to strongly improve PID by reducing the combinatorial background.

The timing distribution is dominated by the primary vertex distribution contribution, which is of order of $\sim 200\,\text{ps}$.
As already done for the Upgrade I detectors, a hardware time-gate can be used to exclude out-of-time background photons. It is foreseen to reduce the hardware time-gate from the current 6 ns to 2 ns thanks to a better timing resolution of the front-end electronics, and it will provide a timestamp for each photon with a resolution of $\mathcal{O}\,(10\,\text{ps})$ within the gate.

2

Single photon detectors

2.1 RICH Upgrade II photon detector candidates: SiPM and MCP

In high occupancy regions, the MaPMTs that are being used during Run3 and will be used in Run4 are not suitable, lacking the required pixel granularity and timing resolution.
Moreover, the current proposal for the RICH1 optics upgrade does not leave enough space for magnetic shielding, requiring detectors which are minimally affected by strong magnetic fields. Thus, new photodetectors are require to meet the requirements on the granularity, the timing resolution and the magnetic resistance.

Currently, the most promising candidates are SiPMs and MCPs.
Overviews on SiPM and MCP technologies are presented in Subsection 2.1.1 and 2.1.2, respectively, and a comparison of advantages and disadvantages of both technologies for the purpose of the LHCb RICH upgrade will be proposed in Subsection 2.1.3.

2.1.1 SiPM technology overview

Single-Photon Avalanche Diode operation

A Silicon Photomultiplier (SiPM) is an array of Single-Photon Avalanche Diodes (SPADs), solid-state detectors featuring a single photon counting capability with excellent timing resolution. These detectors are based on a divergent multiplication generated by an ionising interaction within a high-electric field region in a semi-conductor, typically silicon, and the following discharge quenching triggered by an external circuit [33].

A SPAD consists of an abrupt p/n junction, with a lowly doped layer either on the p or the n side [34, 35]. The junction can be either right below the SPAD surface or buried. Under reverse bias condition, the lowly doped side is fully depleted; a high-electric field is generated on the opposite side, forming the multiplication region, while the depleted part is the drift region, where the photo-electrons are drifted towards the multiplication region.
Since the operating principle is based on a divergent multiplication, the bias must be set above the breakdown voltage.
The external circuit features a quenching resistor, having the function to quench the discharges.
A simplified schematic of a SPAD featuring a p^+/n^- junction is presented in Figure 2.1.

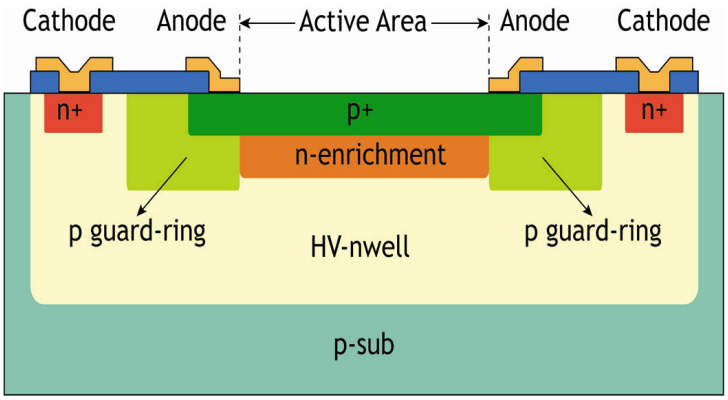


Figure 2.1: Schematic of a SPAD model featuring an abrupt p^+/n^- junction [36]. SPAD main elements, such as high-field (multiplication) region, drift region, guard structure and silicon substrate, are visible.

The model describing the SPAD operation comprises two probability parameters: the avalanche breakdown triggering probability is the percentage of photo-generated carriers which trigger a Geiger discharge; the quenching probability

is the probability that the number of carriers crossing the multiplication region fluctuates at zero to a certain time, and the avalanche is extinguished.

If the avalanche is quenched, the lateral diffusion is usually limited to a few micrometers from the discharge generation point. However, carriers created during the multiplication can generate another discharge, speeding up the current growth.
At a first approximation, the SPAD generates the same charge regardless the number of photons triggering the avalanche, so these detectors are not suitable to perform photon counting measurements with expected timing differences lower than the SPAD recharging time. However, the detector can be segmented into an array of independent SPADs, so that each photon may interact with a different SPAD, providing a count proportional to the number of photons. The response is linear, provided that the number of photons with a timing difference lower than the recharging time is low compared to the number of SPADs in the SiPM.

SiPM main parameters

An array of SPADs combined in parallel, each one with its own quenching resistor, is called an analog Silicon Photomultiplier (aSIPM); the SPAD signal may be locally digitised, composing a so called digital SiPM (dSiPM).

Except for the SPAD parts already described (abrupt junction, high-field region and drift region), a backside contact is provided by a highly doped silicon substrate.
At the SPAD edges two structures are present, as visible on Figure 2.2: the guard ring, providing a smooth and fast electric-field transition to low values, and an isolation structure which electrically separates different SPADs.

The main parameters describing a SiPM are:

- breakdown voltage;
- photo-detection efficiency (PDE);
- Primary and Correlated noise, measured by the Dark Count Rate (DCR) and the Excess Noise Factor (ENF), respectively;
- Single-Photon Timing Resolution (SPTR).

The breakdown voltage is the minimum bias above which the diode operates in Geiger mode. It increases proportionally to the depletion region thickness; analogously, it increases proportionally to the temperature.

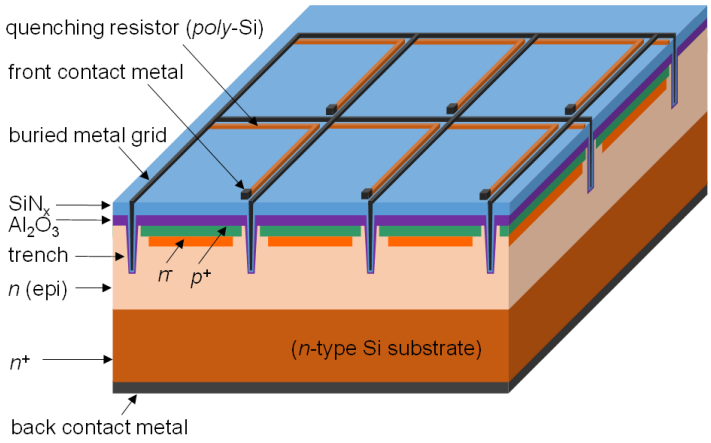


Figure 2.2: Schematic of a SiPM, an array of SPADs [37].

The PDE is strongly dependent on the light absorption coefficient, which for silicon varies by several orders of magnitude in the wavelength range of a typical application. Thus, depending on the application, the SiPM structure has to be optimised, taking into account the *quantum efficiency* (QE), namely the probability for a photon to create a primary electron-hole pair in the active volume, the avalanche breakdown triggering probability, and the *fill factor* (FF), namely the active-to-total area ratio of a SPAD.
The quantum efficiency depends on two factors: the probability of a photon to cross the anti-reflective coating which is typically formed on the detector surface, and the probability to create a carrier that can reach the multiplication region. The latter is dominant and depends on the absorption depth, which in silicon goes from about 10 µm for UV light (photons are absorbed close to the surface) to about 900 µm for near IR light. Designing properly the SPAD structure to measure long wavelength light is difficult, because thick drift regions cause electric field distortions due to border effect; these distortions lead to carriers flowing towards the guard ring instead of the multiplication region. On the other hand, some carriers may be generated in the undepleted subtrate, and some of them can reach the depletion region by diffusion, increasing the QE, but generating a delayed signal with respect to the prompt ones.
The fill factor term is related to the inactive region of a SPAD, which are the guard ring and the isolation structure which electrically and optically separates the SPADs. These elements have to be designed to simultaneously maximize their effectiveness and minimize their width.

There are two categories of noise related to a SPAD, primary noise and correlated noise. The former is due to a carrier generated by either thermal generation or tunneling which is collected in the depleted region and triggers a discharge in the high-field region. Differently, a correlated noise event is a discharge triggered by a previous discharge.
The number of primary noise events in a defined time interval follows a Poisson distribution, and it defines the Dark Count Rate. The main source of primary noise is thermal generation; in case of pure thermal generation, the DCR shows a proportionality to $e^{-1/T}$, but typically DCR is increased by the presence of high electric fields because the rate of electrons captured and emitted by traps is increased by tunneling. Thus, to reduce the DCR, generation centers such as material impurities must be minimised: this reduces the overall DCR, and it decreases more rapidly with cooling. This is particularly important after irradiation.
When considering SiPMs, another noise source is the optical cross-talk, a process where the avalanche is triggered by a carrier generated in a close region of an adjacent SPAD. The cross-talk may be prompt or delayed, when the carrier is generated in the active or un-depleted region of the close SPAD, respectively: in the former case, the drift is fast, and the difference between the discharge times in the two SPADs would be of order 10 ps, while in the latter the carrier diffusion takes longer, and the two signals can be distinguished. There are many solutions to reduce the cross-talk: reducing the un-depleted region; using substrate with short diffusion length; using a buried junction below the active area to prevent diffusion; using trenches with absorbing material to separate the cells.
Eventually, the last noise source is the afterpulse process, due to carriers generated in the high-field region which are trapped and emitted after a certain time, generating a second discharge. The emission probability is exponential in time, so the maximum number of carriers is emitted immediately after the main avalanche: thus, a hold-off time is enough to reduce this type of noise.

Another key feature of SiPMs is their excellent timing resolution, evaluated by measuring the Single Photon Timing Resolution (SPTR), which is the precision of the estimation of a visible photon arrival time [33].
The timing distribution typically shows a Gaussian distribution and an exponential tail towards longer arrival times. The former is due to several contributions: timing jitter of the avalanche build-up; electric field non-uniformity within a SPAD and among different SPADs; spread of the collection time (CTS) of charges from the absorption point to the high-field region; spread of the transient time (TTS), taking into account the photon absorption position within the active area; jitter caused by the front-end electronics. The exponential tail is due to carriers generated in the un-depleted region.

2.1.2 Micro Channel Plates

General description and main parameters

A microchannel plate (MCP) is an array of channels operating as electrons multipliers, exploiting the channel's walls as a continuous sequence of dynodes. Each channel, depending on the bias voltage applied between the two MCP sides, is able to amplify the electrons signal with a gain of $10^3 - 10^7$. The small transit time spread allows a timing resolution of $20 - 30\,\text{ps}$, and the spatial resolution is limited only by the channel diameter and pitch. A schematic of the operating principle of an MCP is shown in Figure 2.3.

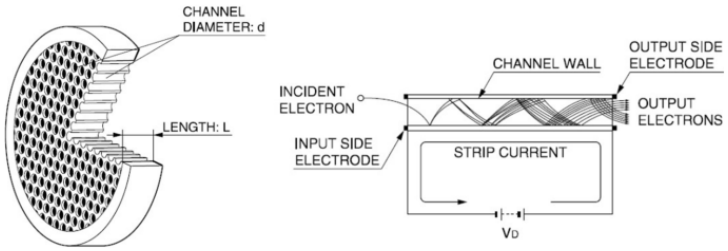


Figure 2.3: MCP operating principle schematic.

A fundamental parameter describing the MCP is the length-to-diameter ratio, on which depends most of the electrical parameters [38]. Moreover, an important parameter affecting the MCP efficiency is the open-area-ratio, namely the ratio between the integrated area of the pores and the total MCP area. These MCP geometrical parameters are typically:

- channel diameter: $\text{d} = 6 - 25\,\mu\text{m}$;
- channel length: $\text{L} = 0.4 - 1\,\text{mm}$;
- length-to-diameter ratio: $\alpha = \text{L/d} = 40 - 100$;
- open-area-ratio: $55 - 65\%$.

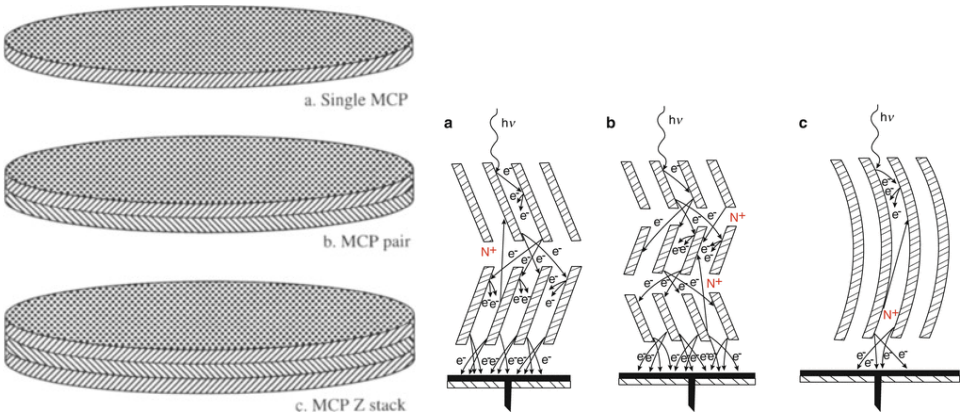
Combining MCPs to the photon conversion into an electron will allow to achieve single photon sensitivity over large areas with high resolutions and with a low dark count rate. Moreover, MCPs have the advantage to be minimally affected by magnetic fields [38].

Main downsides and solutions

The main downside of MCPs until few years ago was their limited lifetime, mostly caused by the ion feedback induced by the electrons hitting the MCP channels.

The ion feedback is a typical deteriorating effect present in a MCP: the high charge pulse reaching the MCP output may create residual gas ions, that would be accelerated backwards to the channel input, degrading the photocathode quality and reducing the QE. Here the ions may produce other electrons, which are multiplied generating smaller output pulses following the original one. This effect increases the channel dead-time and decreases the MCP lifetime. Such an effect becomes very important at high gains, of order of 10^5.

The ion-feedback effect may be mitigated by using curved channels, to prevent the ions from reaching the channel entrance, but fabricating MCPs with small curved channels is difficult.
A similar effect can be achieved by stacking two MCPs with straight and tilted channels with opposite bias angles, as shown in Figure 2.4b. This configuration is called "Chevron" configuration, and it allows to reach gains of $10^6 - 10^7$. The output charge resolution in this configuration can be increased be reducing the gap between the two MCPs [39].
Analogously, configurations with three MCP stacks are possible, and they are called "Z-stack" configuration. An example is shown in Figure 2.4.



(a) (b)

Figure 2.4: **(a)** Examples of different MCP stacks configuration: single MCP with straight channels, two MCP stacks in Chevron configuration and 3 MCP stacks in Z-stack configuration [40]. **(b)** Detail of MCP stacks in different configuration: single MCP with curved channels, Chevron configuration and Z-stack configuration, respectively [41].

Moreover, a possible solution to reduce ion-feedback effect has been proposed on a recent technique consisting of coating the MCP pores with an atomic layer deposition (ALD) [42], that could consist either of resistive or secondary emission layers: this solution increases the device's lifetime by almost two orders of mag-

nitude, since they are now able to operate up to larger integrated anode charge densities (more than 16 C/cm^2, with respect to integrated anode charge densities lower than 1 C/cm^2 for MCP without ALD). Figure 2.5 shows the photocathode relative quantum efficiency dependence on the integrated anode charge received using different MCP-PMT models; clearly visible is the lifetime improvement due to the introduction of the ALD technique.

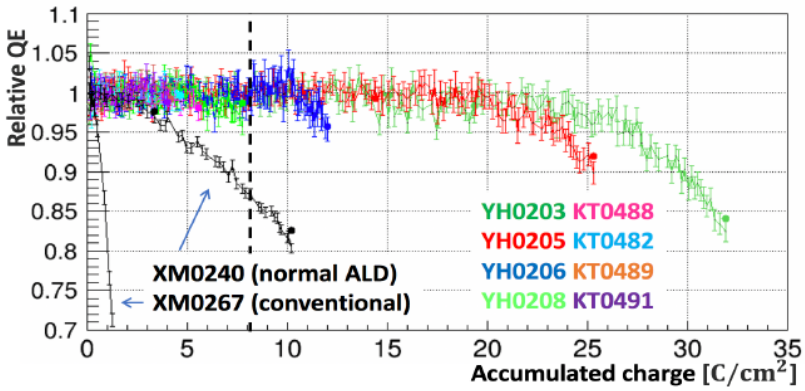


Figure 2.5: Photocathode quantum efficiency (relative to the QE measured immediately after the production) dependence on the integrated anode charge [43].

Another downside is given by a possible electrons back-scattering, which may happen at MCP input but also on the output anode. This effect can generate image halos, reducing the spatial resolution. A first solution to reduce this effect is decreasing the gap between the photocathode and the input face of the MCP, and the gap between the MCP output and the anode.
To mitigate it, an important technique has been introduced, consisting of the end-spoiling of the output channel electrodes. This technique consists of the evaporation of electrodes onto the input and output MCP surface: the material penetrates each channel by a depth d_{es} measured as a ratio of the channel diameter d. This end-spoiling removes the secondary emission from the end of the MCP channels, affecting the angular and energy distributions of the output electrons.
On one hand, the end-spoiling improves the spatial resolution, but on the other hand it reduces the gain: an optimal balance between the two is given by end-spoiling with a depth d_{es} of a few channel diameter d; typically, the end-spoiling used is referred to as 1d, 2d or 3d, depending on the ratio between the end-spoiling penetration and the channel diameter.

Main applications

Micro-channel plates originally have been developed for night vision application with high resolution, coupling them with image intensifiers to form the so called second-generation image intensifier tubes. With respect to standard image intensifiers, where photons are focused on the photocathode through optical elements, and photoelectrons are directly accelerated towards the anode, these tubes provide a gain higher by one order of magnitude, leading to higher resolution. Moreover, image distortion effects are solved.

Due to their characteristics, MCPs are suitable for timing applications requiring high performance.
They are perfect candidates for high timing resolution PMTs. The first MCP-PMT has been developed in 1970 [44], based on an MCP with 40 µm pore diameter, reaching a transit time spread (TTS) of 500 ps. Later developments, based on MCPs with pore diameter of $6 - 12$ µm, reached a TTS lower than 50 ps.
Due to their geometrical characteristics, including narrow channels and close gaps between the MCP-PMT elements, these photodetectors can be used in strong magnetic fields while preserving their performance.

Eventually, several time-of-flight (ToF) and particle identification (PID) detectors have been developed for HEP experiment, based on the detection of Cherenkov photons.
MCP-PMT satisfy all the requirements for these applications: robustness to magnetic fields, high gain, high efficiency, fast signal transmission and high rate capabilities. An example of a PID detector is the BaBar Detector of Internally Reflected Cherenkov (DIRC) [45] or the Time-of-Propagation (ToP) developed for the upgrade of Belle-II PID detector [46]. Similarly, the PANDA experiment PID system will be focussed on DIRC based on MCP-PMTs [47, 48].
For the low-momentum PID upgrade of LHCb a TORCH (Timing of internally Reflected Cherenkov photons) detector has been proposed [28, 29]. The reconstruction of Cherenkov photon directions needs high spatial and timing resolution, satisfied by MCP-PMTs with TTS lower than 50 ps and anodes segmented in pads of 0.4 mm $\times$ 6.4 mm.

2.1.3 Benefits and drawbacks of SiPMs and MCP

SiPMs are a very attractive candidate for the LHCb RICH Upgrade II for many reasons.
They are characterised by a high photon-detection efficiency that, in particular, peaks at longer wavelengths with respect to an MaPMT, satisfying the requirement to move the PDE towards green regions.

Moreover, these devices are insensitive to magnetic fields, requiring no magnetic shields, and they operate at low voltage.

SiPM's main drawback is their high dark-count rate, in particular after strong irradiation; therefore, cryogenic cooling, neutron shielding and annealing are required [49].
Studies to meet these requirements are ongoing: some possibilities to reduce the dark-count rate which have been taken into account are the use of micro-lensing, to reduce the effective pixel area, and the use of time gating on the front-end electronics [22, 23].

Conversely, MCPs have a low dark-count rate, and thanks to that and their excellent timing resolution, typically of $\mathcal{O}(30\,\text{ps})$, they are a very promising candidate for the LHCb RICH Upgrade II.
The main drawback of MCPs is their restricted lifetime and gain saturation at high rate, as discussed in Subsection 2.1.2, even though significant improvements have been obtained using ALD coating.

Development of detectors aiming to fully exploit MCP characteristics and to overcome its disadvantages are ongoing [22, 23].
Among these, the development of a MCP-PMT with a pixelated anode, consisting of a CMOS ASIC able to read out charge signals at very high rate, could allow to preserve the MCP timing and spatial resolution, while operating it at lower gain, increasing the lifetime.
Studies are being made on Large Area Picosecond Photo Detectors (LAPPDs) as well [50], which are single-photon detectors with dimensions of typically $20\times20\,\text{cm}^2$ composed of borosilicate glass MCPs, able to reach a timing resolution of about 50 ps. However, the spatial granularity requirements would not be met at their current state.

2.2 Pixelated ASIC coupled to MCPs

Pixelated ASICs are usually designed to be coupled to high-granularity pixel sensors, but they can also be exploited to read out Micro Channel Plates or Gas Electrons Multipliers [51, 52, 53, 54].

The first circuit designed to read out a GEM was the PIXIE, developed in 2004 by the INFN Pisa section to measure X-ray polarization in space [55]. The PIXIE-1 was the first gas pixel detector to be developed. After that, a following generation has been designed to be coupled to a CdTe sensor composed of hexagonal pixels.

Both Medipix2 and Timepix have been used to detect photons, electrons and

neutrons reading out MCPs [56]. Reading out MCPs with pixelated ASICs allows to reach a high spatial resolution limited only by the MCP channel diameter and pitch, and to reach good timing performance. Demonstrators of optical MCP image tubes have been built based on a single Medipix2 ASIC [52] and on an array of 2×2 Timepix [53].

2.2.1 State of the art

MCP-PMT with Medipix2

The first optical MCP image tube, shown in Figure 2.6, consists of an MCP sealed within a vacuum tube, with a photocathode coated on the input window, and a Medipix2 ASIC used as pixelated anode. A photon interacting with the photocathode generates an electron by means of the photoelectric effect. This free electron, called photoelectron, is accelerated towards the MCP by a suitable electric field. The MCP is biased with a voltage difference between $\sim 1600\,\mathrm{V}$ and $\sim 1800\,\mathrm{V}$ to produce a gain between $\sim 10^3$ and $\sim 2 \cdot 10^4$, producing an electron cloud. This electron cloud is directed to the Medipix2 pixel input pads by means of another electric field.
The voltage applied between the MCP output and the Medipix2 is $600\,\mathrm{V}$, across a distance of $300\,\mu\mathrm{m}$, resulting on an electric field of $2\,\mathrm{V}/\mu\mathrm{m}$. The Medipix2 allows to read a complete frame in $286\,\mu\mathrm{s}$ [52].

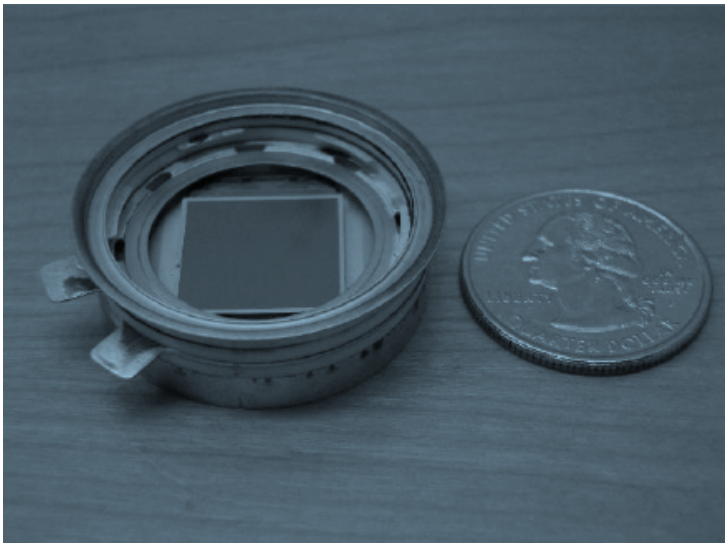


Figure 2.6: Image of the Medipix MCP-PMT tube assembly before the installation of the MCP stack and of the photocathode window, with the Medipix2 ASIC still visible [52].

An important requirement on the design comes from the need to seal the Medipix2 in vacuum: this in turn sets constraints on the mechanical and electrical connection to the ASIC. The substrate on which the Medipix2 is bonded must be able to withstand the temperature reached during the tube baking process needed to reduce the outgassing. This requirement led to the choice of an alumina-based ceramic substrate (Al_2O_3): a choice that also limits the available pin density, which is the density of electrical connections to the assembly. Moreover, the distance between the MCP and the ASIC has been minimised in order to preserve the MCP spatial resolution.
A stack of two Hamamatsu MCPs mounted in Chevron configuration has been used; these MCPs are characterised by channels with a diameter of 6 μm tilted by 13°, with a channel aspect ratio L/d = 80.

Gain and efficiency measurement have been performed with scattered light, in order to select the best voltage value for the MCP. Since an efficiency plateau appears above an MCP bias voltage of −1700 V, the voltage has been set below this value to increase the MCP lifetime.
The multi-alkali photocathode quantum efficiency has been measured, resulting on a peak lower than 4% at 410 nm.
Response uniformity measurements have been performed using a diffused light, resulting in a relative standard deviation of the pixel counting of 10%, as shown in Figure 2.7.
The dark count rate, dominated by the thermal noise of the photocathode, has been measured to be 0.004 counts/pixel/s.

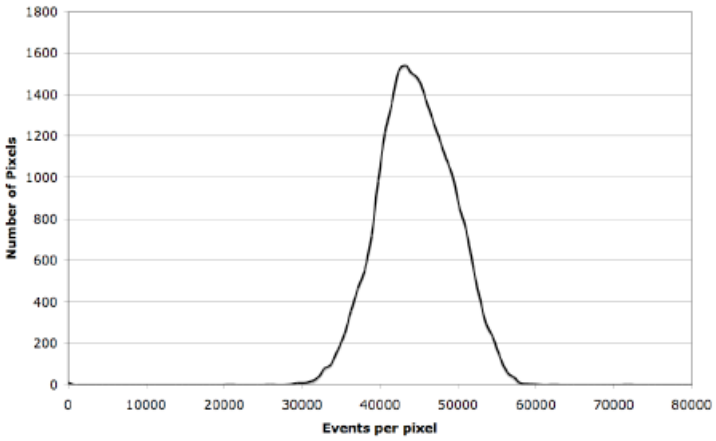


Figure 2.7: Photon counting distribution on a flat field measurement performed with the MCP-PMT assembly with Medipix2 as pixelated anode. The relative standard deviation is 10% [52].

The resolution has been estimated by illuminating a pinhole mask placed in front of the photocathode, with 50 µm wide pinholes, spaced 2 mm × 4 mm apart. The resulting clusters of pixels have a resolution of 74 µm FWHM, and their centroids have resolution of ∼ 5 µm.

MCP-PMT with array of Timepix ASICs

A larger version of an optical MCP-PMT with a pixelated anode, shown in Figure 2.8, has been developed in 2013, based on an array of four Timepix ASICs [53]. The MCP-PMT structure is analogous to that of the Medipix2 based MCP-PMT but using components optimised for the larger area and improved performance.
The tube is closed by a planar input window, with a semi-transparent bi-alkali photocathode coated on it. At a distance of 4.5 mm from the photocathode, two MCPs in Chevron configuration are placed. The array of Timepix is placed at 0.5 mm from the MCP output.
The voltage applied between the photocathode and the MCP is 600 V, while the voltage between the MCP and the anode is 800 V.

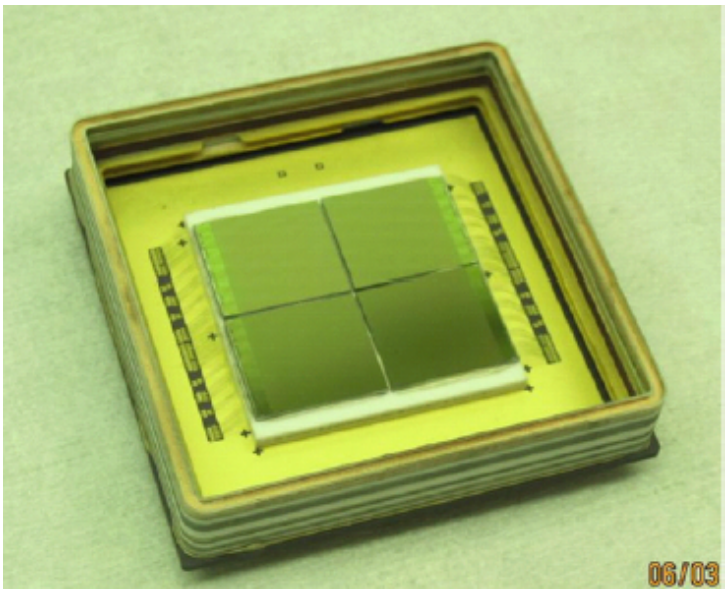


Figure 2.8: Picture of the Timepix based MCP-PMT tube assembly before the installation of the MCP stack and of the input window. A 2 × 2 array of Timepix ASICs is vistible [53].

The photocathode QE has been measured to be higher than 20% at ∼ 390 nm, and the MCP open-area-ratio is ∼ 60%. A measurement of the MCP-PMT efficiency, including the efficiency of the Timepix ASICs, is presented in Figure 2.9. Increasing the MCP bias the number of signals which rise above threshold initially

increases, to eventually reach a plateau, due to the fact that all the electrons emitted by the photocathode generate a signal above threshold.

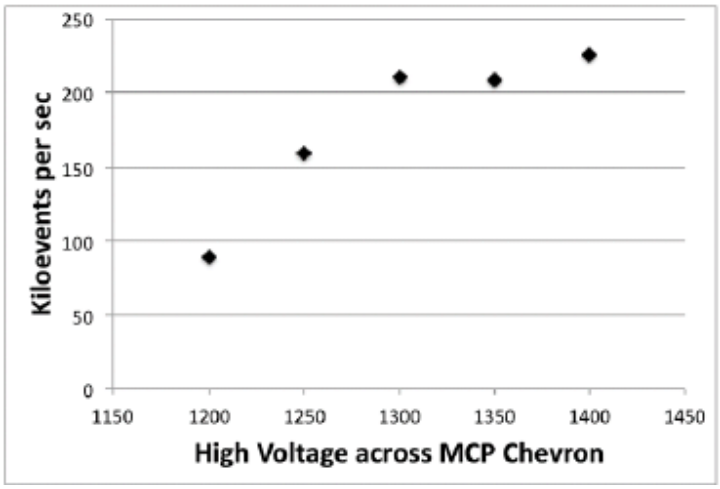


Figure 2.9: Rate of detected events depending on MCP voltage [53].

The spatial resolution is degraded by the large gap between photocathode and MCP: it has been measured placing a pinhole mask, with holes diameter of 50 µm, and the best images resulted in an FWHM of 165 µm.
However, as explained in Subsection 3.2.3, operating Timepix in Time-over-Threshold (ToT) mode, i.e., estimating the charge spread on a pixel by measuring the time the signals stays above threshold, and computing the cluster's centroid, the spatial resolution is highly improved, reaching sub-pixel resolution. Indeed, it has been possible to resolve the MCP channels spacing of 32 µm, measuring them with a resolution better than 5 µm. Figure 2.10 shows an example of a uniform flat field measured in ToT mode, highlighting the MCP pores resolution.
Light inputs cannot reach such a resolution due to the gap between the photocathode and the MCP. However, using tubes with optimised distances between its elements, and with proper MCP channels diameters and spacing, light measurements can reach in principle sub-pixel resolutions as well.

The timing performance of this detector, that is the resolution of the Time-of-Arrival (ToA) of the signal, is limited mainly by the time-walk effect, namely, the ToA dependence on the ToT: a lower signal induced in the same instant as a higher signal will rise above threshold later, resulting on a delay with respect to the true signal timestamp, as shown in Figure 2.11. Due to this effect, when an electron cloud is spread over a certain number of pixels, the smaller signals rise above the threshold later then higher signals.
Correcting this effect is possible, knowing both the timestamp and the charge

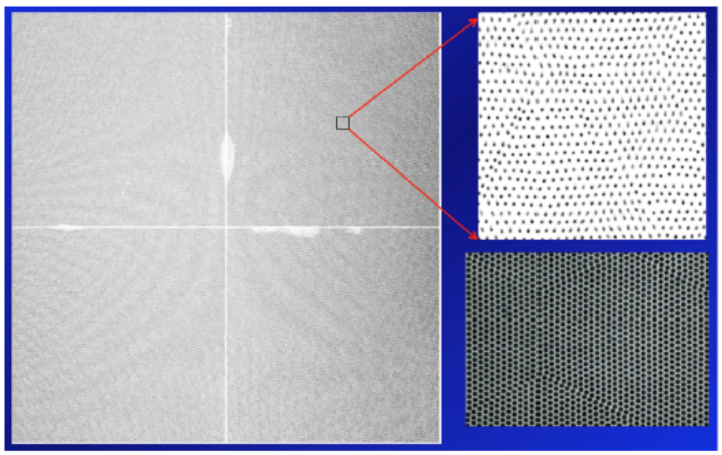


Figure 2.10: Flat field response operating the Timepix ASICs in ToT mode. Using the X, Y, and ToT information to compute the centroid of each cluster, the MCP pores are resolved, as shown on the upper right figure. The resulting pattern is coherent with the pattern of an MCP observed with an optical microscope, shown in the bottom right figure (in a different scale with respect to the upper right figure) [53].

information of a signal. However, Timepix does not allow to measure simultaneously ToT and ToA, making the correction infeasible.
The resulting timing resolution saturates then to $100 - 200$ ns.

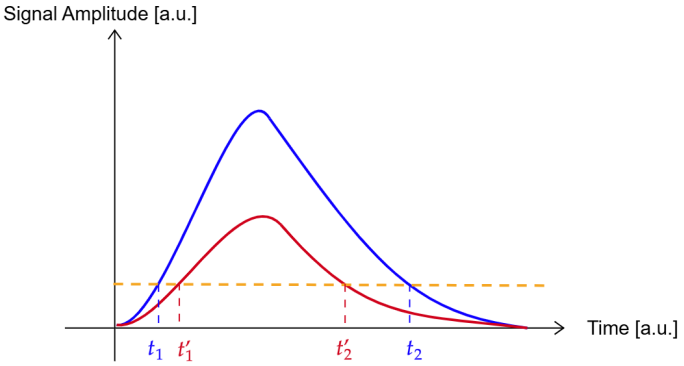


Figure 2.11: Representation of the time-walk effect: a lower signal induced simultaneously with a higher signal will rise above the threshold slightly later than the higher signal.

3

4DPHOTON project

The production of a new photodetector could enable significant advances in several fields, such as particle physics, life sciences or optical quantum physics experiments [57]. Such a detector must be able to measure single photons reaching simultaneously excellent timing and spatial resolution, and high rate capabilities.

The future HEP experiments will require an increase in timing and spatial resolution and rate capabilities with respect to the current available detectors, as explained in particular for LHCb experiment in Chapters 1 and 2. For example, the current photodetectors in the RICH detectors are not adequate in a high luminosity environment. In high multiplicity environments the Cherenkov rings overlap, and a global fitting algorithm does not allow to disentangle different rings unless precise Time of Arrival information is provided.

Regarding the life science field, a standard technique to measure fluorescence lifetime is the time-correlated single-photon counting (TCSPC), consisting of detecting with a timing resolution of O(ps) fluorescence photons emitted by samples excited by an ultra-fast laser [58].
There are also methods based on an entire field image recording. These measurements are usually performed using gated detectors, which grant good timing resolution, but lack efficiency, since photons are lost due to the gated frame-based acquisition.

A new detector combining excellent timing and spatial resolution with high rate capabilities and large active area would have a fundamental role improving current imaging techniques.
A four-dimension charged particle tracker has already been developed [59], but an analogous detector to detect photons providing timing and spatial information with high resolution is missing. Among the existing detectors, there is not one able to detect single-photons combining excellent timing ad position resolution, low noise level and high rates, and covering a large active area.

In the context of the 4DPHOTON project a detector that will meet these requirements is being developed [60, 61]. This detector consists of a hybrid detector, made of several components of different technologies, independently optimised.
The 4DPHOTON detector is based on a vacuum tube, with a photocathode, an embedded MicroChannel Plate (MCP) and a Timepix4 ASIC used as a pixelated anode.

3.1 4DPHOTON project introduction

4DPHOTON is a project funded by the European Research Council (ERC) under the European Union's Horizon 2020 research and innovation programme (Grant agreement No. 819627). It is hosted by the Italian National Institute for Nuclear Physics (INFN), and coordinated by the Principal Investigator (P.I.) prof. Massimiliano Fiorini. The European Center for Nuclear Research (CERN) and the University of Ferrara (UNIFE) are providing a fundamental contribution to the project.

The goal of the project is the development of a new photodetector with a large active area, able to measure single photons reaching simultaneously excellent spatial and timing resolution, keeping a low noise level even at room temperature [60]. These unprecedented performances could allow to remove the limitations of many light imaging applications, due to the lack of detectors able to reach simultaneously excellent resolutions both in space and time.

Moreover, the resulting detector will be able to sustain a high rate and it will be compact. Thus, this detector can bring great advantage to high energy physics experiments, providing an innovative possibility for new Ring Imaging Cherenkov detectors, able to efficiently identify particles in high luminosity environments.

3.2 Brief detector description and operating principle

The "hybrid" assembly, which cross section is presented in Figure 3.1, is based on a vacuum tube, containing the components of the MCP-PMT assembly under high vacuum ($\sim 10^{-10}$ mbar).
A silicate window, transparent in the IR, visible and UV range, is placed on the top part of the tube acting as the photon entrance window. A high quantum-efficiency photocathode is coated on the inner part of this window.
A MCP stack in Chevron or Z-stack configuration is placed after the photocathode, with the function of multiplying the single electrons emitted by the photocathode.
A bare Timepix4 ASIC CMOS is used as embedded pixelated anode, and it will be described in deeper detail in Chapter 4.

A ceramic carrier board, to which the Timepix4 is bonded, acts as the bottom cap of the tube assembly and it provides an interface between the vacuum and in air parts of the detector. Input and output signals together with the power lines feeding the ASIC are transmitted through pins granting high speed performance; a custom Pin Grid Array (PGA) allows to plug the detector into custom socket on a Printed Circuit Board (PCB).
In turn, the PCB allows to connect the detector to a custom FPGA-based data acquisition system, which controls the configuration of the detector and the data readout.

During usage the Timepix4 can reach a power consumption of up to 5 W, so an heat sink will be connected to a chiller system, providing an active cooling to extract the heat generated by the ASIC, and preventing the temperature to rise so high that it to affect the detector operations.

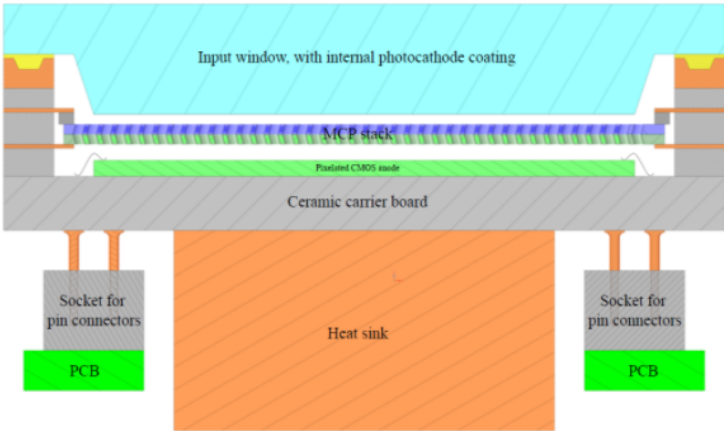


Figure 3.1: Simplified cross section of a of the detector assembly.

The operating principle of the detector, schematised in Figure 3.2, is the following:

- a photon entering the input window is converted in the high Quantum Effiency (QE) photocathode, producing a photo-electron;
- the photo-electron is transported by an electric drift field onto the MCP stack, where additional electrons are freed and accelerated, increasing the electric signal;
- the electrons cloud produced by the MCP is carried by a second drift field onto the input bump-bonding pads of a bare Timepix4 ASIC, where it is sensed by the readout electronics;
- the Timepix4 amplifies, discriminates and digitizes the MCP signal.

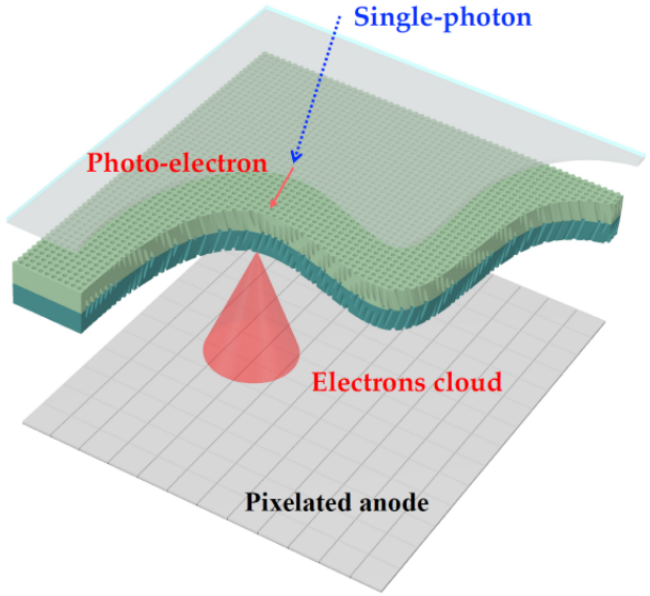


Figure 3.2: Visual representation of the hybrid detector operating principle.

3.2.1 Optical window and photocathode

The input window is suitably shaped to place the photocathode close to the MCP stack. This allows to achieve better spatial resolution. The electron will have an initial momentum component parallel to the photocathode [62]: this will make the electron drift parallel to the photocathode and orthogonally to the drift field. This transverse motion is stopped when the electron is channeled in one of the MCP channels. The entity effect of this motion is to shift the detected electron position in a random direction by an amount proportional to the initial momentum and

on the flight time of the electron from the photocathode to the MCP. This flight time can be minimised by increasing the electron drift speed, that is by increasing the voltage difference between the photocathode and MCP, and by minimizing the flight distance.

The baseline photocathode material will be either a bi-alkali variant, an alkali antimonide with a composition of K-Sb-Cs or Rb-Sb-Cs [63], or a multi-alkali variant, with a composition Na-K-Sb-Cs [64]. Both of them have excellent timing capabilities, a good quantum efficiency and negligible dark count rate. The multi-alkali spectral response is higher than the bi-alkali spectral response, covering from the ultraviolet to near infrared region. The photocathode is chosen to have a high Quantum Efficiency (of the order of $30 - 40\%$) in the Cherenkov photon region, namely the blue-green region, between $\sim 300\,\text{nm}$ and $\sim 450\,\text{nm}$.
Moreover, it grants a low dark count rate, of about $10^2 - 10^3\,\text{Hz/cm}^2$ at $300\,\text{K}$.
It must be noted that suitable photocathode materials are the one allowing for a uniform photocathode coat the photocathode over a large area to accommodate the large anode area set by the Timepix4 dimensions.
Using a photocathode to externally convert photons to electrons gives flexibility to the design, since it allows to modify the spectral sensitivity just by replacing the photocathode material. In this way, with different photocathodes it will be possible to detect photons from the near-IR to the near-UV.

3.2.2 Microchannel plate

The MCPs will be used in a Chevron or Z-stack configuration, in order to reduce the ion feedback, as explained in Subsection 2.1.2.
For the purpose described in this work, the MCPs will operate at gain of a few 10^4 instead of the standard applications gain of 10^6, increasing the lifetime by one order of magnitude. Studies are ongoing to perform the ALD with optimised materials, in order to further increase the detector lifetime. Further details on the characteristics of the mounted MCP will be provided in Section 3.4.

3.2.3 Pixelated anode: Timepix4

The pixelated anode is a bare Timepix4, which is a CMOS ASIC in a $65\,\text{nm}$ technology able to reach high resolutions and rate capability developed by the Medipix4 collaboration [51]. As already established by the works described in Section 2.2, this ASIC could work under high vacuum and it is suitable for using it inside a vacuum tube based assembly described in Section 3.2 [52, 53].

The Timepix4 is composed of 512×448 square pixel with a $55\,\mu\text{m}$ pitch, for a total active area of $\sim 6.94\,\text{cm}^2$. Therefore the spatial binary resolution is given

by the 55 µm bins, corresponding to $\sim 16\,\mu m$ r.m.s. resolution.

The bare ASIC will be mounted on the ceramic carrier board through wire-bonding connections: the MCP signals will be sensed by bump-bonding pads. Pixelated electronics will then amplify and discriminate the signals in each pixel, as shown in the simplified schematic in Figure 3.3.

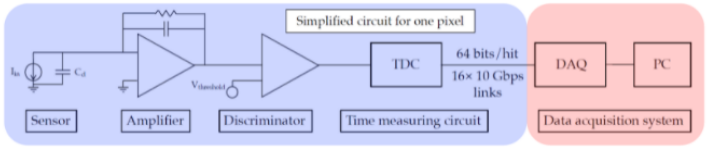


Figure 3.3: Simplified schematic of the electronic circuit for a single pixel on the and the data acquisition system on the right.

A Time to Digital Converter (TDC) tags each signal with a time-stamp having a 195 ps bin size, that corresponds to a 56 ps r.m.s. resolution. It allows to simultaneously obtain information on the event Time-of-Arrival (ToA) and Time-over-Threshold (ToT).
Timepix4 has high rate capabilities, reaching a maximum bandwidth of 163.84 Gb/s and a maximum hit rate of ~ 2.5 Ghit/s/chip. Such high rates require a fast output transmission, provided by 16 high speed links which can be operate up to 10.24 Gb/s. For each event a single pixel output is a 64 bits data word, encoded using the 64b/66b protocol.

Timepix4 ensures also a low equivalent noise charge ($\sim 80\,e^-$) per pixel, which allows to set a threshold close to $700\,e^-$ to the whole ASIC masking just few pixels.

Further details on Timepix4 will be given in Chapter 4.

Clustering improvements to the measurements' resolution

The ToA and ToT are simultaneously measured for each pixel. Single pixels spatial and timing resolutions are $\sim 16\,\mu m$ and ~ 56 ps, respectively, as mentioned in Subsection 3.2.3. The equivalent charge released in a pixel is estimated from the ToT information. Moreover, the ToT is used to correct the time-walk effect, as explained in Section 6.6.

An important advantage is given by the possibility to perform three-dimensional clustering (2 spatial dimensions and a timing dimension) exploiting the pixel coordinates and the time-stamp information. Multiple sampling obtained by measuring the time on several pixels within the clusters will allow to improve the timing resolution. Performing a weighted average of ToA values belonging to the same

cluster, using the corresponding ToT as weight, will improve the timing resolution on the cluster centroid to $O(10\,\text{ps})$. Similarly, the spatial resolution of the cluster centroid will be improved to $\sim 5 - 10\,\mu\text{m}$, approaching the MCP channel spacing [65].

As mentioned in Section 3.2, the electrons cloud generated in the MCP will spread over several pixels: by optimizing the distance between the MCP and the Timepix4 it will be possible to be close enough to preserve the precise spatial information granted by MCP channels with diameter of order of $O(10\,\mu\text{m})$, and to be far enough to cover a number of pixels needed to improve the resolution through the centroid algorithm.

3.2.4 Cooling system

The Timepix4 ASIC has a power dissipation of a few Watts when operating, generating heat dissipated inside the vacuum tube. To prevent the temperature to damage the electronics or affect the operational stability or the vacuum sealing, an active cooling is required.

The detector is cooled down with a liquid cooling system. A copper heat exchanger is coupled to the bottom side of the ceramic carrier, to extract the heat from the region closest to the ASIC. As shown in Figure 3.4, the contact area between the heat exchanger and the ceramic is a 20 mm side square, resulting in a $4\,\text{cm}^2$ contact area.
After preliminary tests on the first tube prototypes, it appeared that the heat extraction was not efficient enough, so an additional copper ring has been coupled to the input window, as shown in Figure 3.5, to cool down the tube from both sides. As shown in Figure 3.4, the ring is characterised by an inner radius of 20 mm and an outer radius of 31 mm, resulting in a contact area of $17.62\,\text{cm}^2$. Thus, the total contact area between the MCP-PMT and the cooling system is $21.62\,\text{cm}^2$. In particular, this improvement is meant to grant a sufficient cooling on the MCP and photocathode as well, which would otherwise exchange heat mostly through radiating processes.

3.2.5 Off-detector readout electronics

The architecture of the Timepix4 ASIC is data-driven: an output signal is produced in a pixel, encoded and transferred to the off-detector electronics just when the pixel is hit. As mentioned in Section 3.2.3 the ASIC can measure a maximum event rate of about 2.5 Ghits/s, corresponding to a maximum output bandwidth of about 160 Gb/s. An external DAQ system receives the data from the detector, processes them, and stores the processed data in the PC memory.

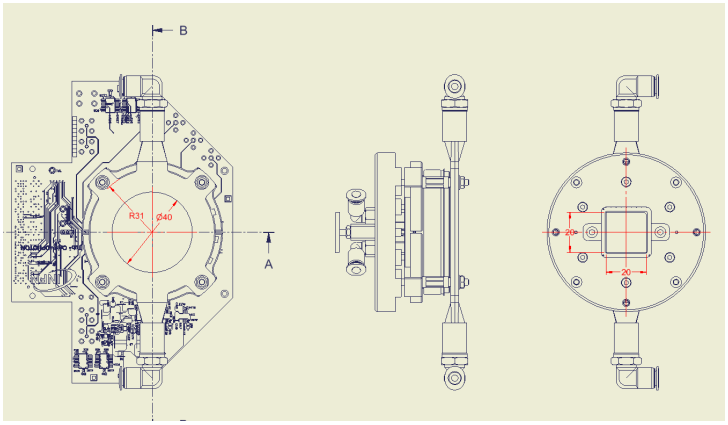


Figure 3.4: Mechanical schematic of the heat exchangers coupled to the MCP-PMT. From left to right: top view of the MCP-PMT, showing the cooling ring meant to cool down the photocathode and the MCP, with a contact area of 17.62 cm^2; side view of the MCP-PMT; bottom view of the MCP-PMT, showing the square heat exchanger in contact with the bottom side of the ceramic carrier, with a contact area of 4 cm^2.

The DAQ system will be connected to the detector using a custom mezzanine, namely the tube card, which hosts the MCP-PMT custom PGA socket, providing power and communication to the MCP-PMT itself. This mezzanine is connected to the main control board by using an FPGA Mezzanine Card (FMC) connector. The DAQ system routes the Timepix4 I/O signals to an FPGA implementing communication with a remote server for Timepix4 control. Moreover, the DAQ system is equipped with an optical transceiver, to allow for high-speed data transmission of the output data.

3.3 Vacuum tube

The vacuum tube, developed by Hamamatsu Photonics, has been designed following some constraints to reach the aimed performance of the project. Among these requirements, the main ones are: position resolution of order of 10 µm and timing resolution less than 100 ps on single photon measurements; quantum efficiency higher than 20% for a wavelength around 400 nm, and for visible light as well; MCP gain of $10^4 - 10^5$ without exceeding a bias voltage of 2000 V; high geometrical efficiency, including a high Open-Area-Ratio for the MCP; long-term reliability, requiring excellent vacuum tightness, no ion feedback, temperature stability.

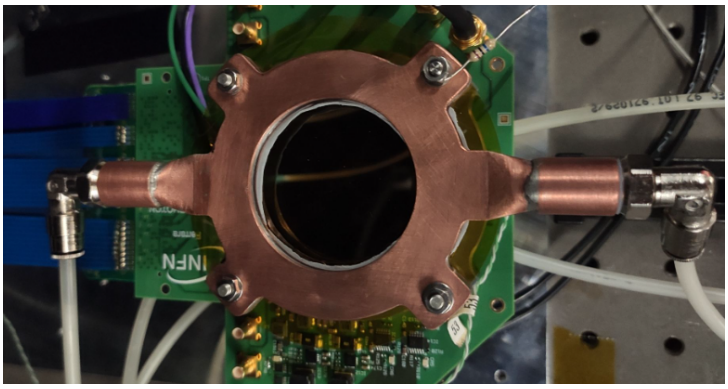


Figure 3.5: Cooling copper ring in contact with the external face of the MCP-PMT input window.

3.3.1 Geometrical characteristics

The target performance of the detectors firstly translate on some geometrical constraints both on the tube structure itself and on the elements disposition within it.

In particular, to achieve simultaneously excellent spatial and timing resolution, the detector geometry needs to feature:

- the smallest possible photocathode-to-MCP distance: as explained in Section 3.2, the photoelectrons are emitted by the photocathode with a transverse direction, thus the position they impinge on the MCP is slightly displaced with respect to the position they are emitted from by the photocathode; therefore, a small distance between photocathode and MCP is needed to avoid a large displacement and preserve high spatial resolution; in particular, a distance lower than 300 µm is required, as well as excellent planarity between the two surfaces;
- optimised MCP-to-anode distance: since the electrons clouds emitted by the MCP present a spread, increasing the distance between the MCP and the anode can increase the number of pixels where a cloud is detected, allowing to improve spatial and timing resolution through a centroiding algorithm. However, if a cloud is spread on too many pixels, each of them would receive a low amount of charge, increasing the signal jitter and timewalk and reducing the timing resolution; thus, the distance between these elements has to be optimised.

Studies are ongoing with several vacuum tube configurations to select the one reaching best combined spatial and timing performance.

The Timepix4 ASICs mounted in the tubes have been thinned down from their original thickness of $\sim 700\,\mu m$ to a thickness of $300\,\mu m$.
The Timepix4 is wire-bonded to the ceramic carrier, thus the wire-bond stand-off height above the ceramic carrier provides another constraint on the MCP-to-anode distance, which cannot be lower than $300\,\mu m$.
Considering that the dielectric strength of vacuum is $> 10\,V/\mu m$ and that the voltages applied between the lowest MCP face and the Timepix4 range from 100 V to 500 V, there is a safe margin to avoid electrical discharge between the MCP and the anode or the bonding wires.

A cylindrical shape has been selected for the vacuum detector development: the main drawback of this shape is the active area ratio of the device, that is not maximised considering the Timepix4 rectangular shape. However, it allows to obtain better vacuum stability and better mechanical stability of the internal components, due to the difference between internal and external pressure. Moreover, it allows to respect with higher accuracy the geometrical constraints on the distances between the elements, on their planarity and their co-planarity.

3.4 Micro Channel Plate requirements and description

The MCP used needs to satisfy the spatial and timing resolution requirements presented in Section 3.3; to reach those requirements, the microchannels are required to have a diameter of $6.0\,\mu m$ and a pitch of $7.5\,\mu m$.
Moreover, given the Timepix4 diagonal size of 38.83 mm, the MCP effective diameter has to be at least of 42 mm, corresponding to outer diameter of order of 50 mm.
The MCP open-to-area ratio must be at least 60% to maximize the detection efficiency.

3.4.1 Main characteristics of the mounted MCPs

A balance between the lateral electrons cloud spread and the MCP gain is needed, to inject enough charge on each pixel allowing the Timepix4 to fully exploit its timing performance, and simultaneously spreading the cloud over enough pixels to improve the resolution through clustering analysis.

The MCP has to be operated at a gain of $10^4 - 10^5$ to decrease the ion feedback and increase the detector lifetime. The Timepix4 is characterised by a low noise level, as it will be discussed in Section 4.4, allowing to operate the MCP at such low gains. This has many advantages, including MCP lifetime increased by more

than one order of magnitude with respect to standard applications, where the MCP are operated at gain of order 10^6, and increase rate capabilities due to a lower recharging time of the MCP channels and lower electronics dead-time due to lower time-over-threshold values of the received signals.

Mainly, two configurations have been considered to reach the required performance at this low gain: double stack MCP in Chevron configuration and three-stack MCP in Z configuration. Both of them allow to reach higher gains at low voltage and to reduce the ion feedback, as stated in Subsection 2.1.2.

The bias angle of the MCP channels is 5°, because this allows to reach a good compromise between gain and resolution [66].

End-spoiling is performed both on input and output channels: the effect of the end-spoling on the output MCP face, as said in Section 2.1.2, is to reduce the gain and collimate the electron cloud, improving the spatial resolution. Two configuration are under test:

- 1d end-spoiling, allowing a good balance between spatial resolution and gain;
- 3d end-spoiling, improving the spatial resolution, but reducing the gain.

Conversely, the end-spoling on the input face has been kept below 0.5d, to reduce the probability that the input electrons impact on the electrode instead of the channels emitting walls.

3.5 Ceramic carrier

Within the 4DPHOTON phototube, the Timepix4 ASIC is mounted on a ceramic carrier, using die-attach material and wire bonding connections, allowing to connect input/output signals outside the tube via PGA connectors.

The ceramic carrier has been developed by INFN, CERN and Kyocera, and produced by Kyocera.

This multilayer ceramic board provides vacuum feed through connections for the readout chip input/output signals. A PGA connection of the input/output signals is used on the back side, arranged around the Timepix4 perimeter to fit into a suitable socket on the external PCB. This configuration allows an opening in the middle, directly underneath the ASIC, to allow the attachment of a heat sink or a cooling element. The output pins are connected through a spring-loaded contact pins technology [67] to a custom socket on the electronics board that transfer the digital signals from the tube to the acquisition system via a combination of electrical/optical high-speed connections.

3.5.1 Ceramic requirements

A fundamental requirement for the ceramic was that the high-speed signals from the ASIC serial links must not be degraded by the wire-bonds, the pass-through traces and the output pins. A simulation has been performed by Kyocera, including both effects due to the ceramic carrier and the pins. This simulation reported a theoretical insertion loss of $-5\,\mathrm{dB}$ at $20\,\mathrm{GHz}$ estimated to be sufficient to transmit signals at $10\,\mathrm{Gb/s}$.

Moreover, the carrier must be compatible with its use in a vacuum tube, so it must not present outgassing, and it should be temperature resistant. At the same time, it should allow Timepix4 cooling by placing a cooling system on the bottom part. Eventually, alignment marks and symmetry breaking elements are needed to grant a precise alignment of Timepix4 on the top part and a correct connection of the carrier to the custom socket.

The Timepix4 ASIC power consumption is of $\sim 2.8\,\mathrm{W}$ during operation in normal conditions, when it is dominated by the analog power consumption. When operating in conditions of maximum rate, the digital power overcomes the analog one, as shown in Figure 3.6, and Timepix4 can reach a power consumption of $\sim 5\,\mathrm{W}$. The heat has to be removed by conduction from the top part of the carrier, where the Timepix4 is mounted, to the bottom part, coupled to a heat exchanger connected to a chiller. The contact area between the heat exchanger and the sensor is a square thermanl pad in the center of the bottom part of the ceramic. Simulations have been conducted to determine the minimum area of the thermal pad needed to cool the ASIC to $\sim 20\,^{\circ}C$ in environmental conditions, assuming the thermal pad is kept at $14\,^{\circ}C$.

It must also be noted that the Timepix4 power consumption is not constant during operation. The data-driven architecture will cause the power consumption to spike each time a new signal is digitised.
These power consumption spikes will happen on a timescale of the internal TDC clock ($\sim 1.56\,\mathrm{ns}$) and they will have the net effect of lowering the voltage fed to the Timepix4. Because of this, bypass capacitors are embedded in the ceramic design by alternating power and ground planes. Additional filtering capacitance is present on the bottom side of the ceramic and at the tube card level.

3.5.2 Ceramic carrier description

The ceramic carrier is composed of four parts:

- the top layer houses the Timepix4, glued and wire-bonded to a series of pads, and kept inside the ultra-high vacuum tube;

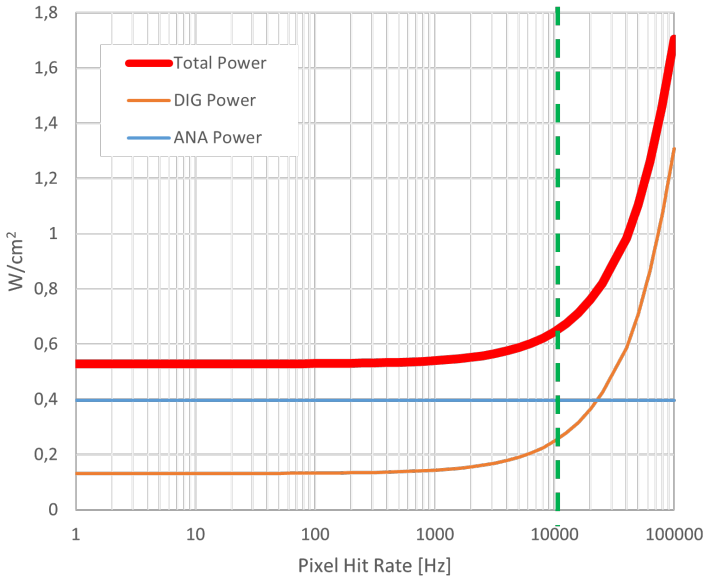


Figure 3.6: Timepix4 analog and digital power consumption per cm^2. Timepix4 area is $6.94\,cm^2$ [68].

- the internal layers contain the traces and the vias to transmit the Timepix4 signals to the bottom part;
- the bottom layer, not kept in vacuum, consists of a series of pins and a central thermal pad to connect the cooling system;
- a flange is brazed to the lateral part of the carrier, to connect to the corresponding flange of the tube.

In its final design, the ceramic has a circular shape, with a diameter of 43.2 mm and a thickness of 8.2 mm.

Top layer

The top layer includes the die bonding pads for the Timepix4 attachment, and the wire bonding pads for I/O signals and power supplies, as shown in Figure 3.7.

This side is treated with a metalization coating connected to ground, with exception of the connecting pads. A central area of dimensions $24.70 \times 29.96\,mm^2$ is dedicated to house the ASIC. Two wire bonding pad rows are placed along the short side of Timepix4, and they are treated to allow wire bonding with 99.9% Au wire with a diameter of $25 - 30\,\mu m$.

Four additional pads are placed along the Timepix4 long side, and they can be

used to monitor the charge received from the MCP per unit of area.

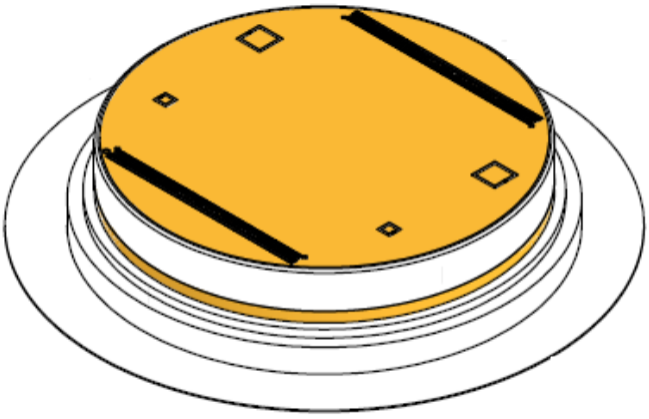


Figure 3.7: Profile layout of the ceramic carrier.

Internal layers

The 32 ceramic carrier internal layers are used both to route I/O signals to the external socket and to provide the power to the ASIC. The layers used for a single power net are filled with a conductor plane to maximize the capacitance between the net and the ground; dedicated layers are used to route I/O signals. The resulting overall bypass capacitance of the ceramic itself is limited by the number of layers and the presence of routing planes. The total capacitance per power net is $\sim 1.5 - 4.5\,\mathrm{nF}$. Direct vias from the top to the bottom layer are used to enhance the thermal conductivity of the ceramic carrier in the area dedicated to the connection with the bottom cooling plate.

Bottom layer

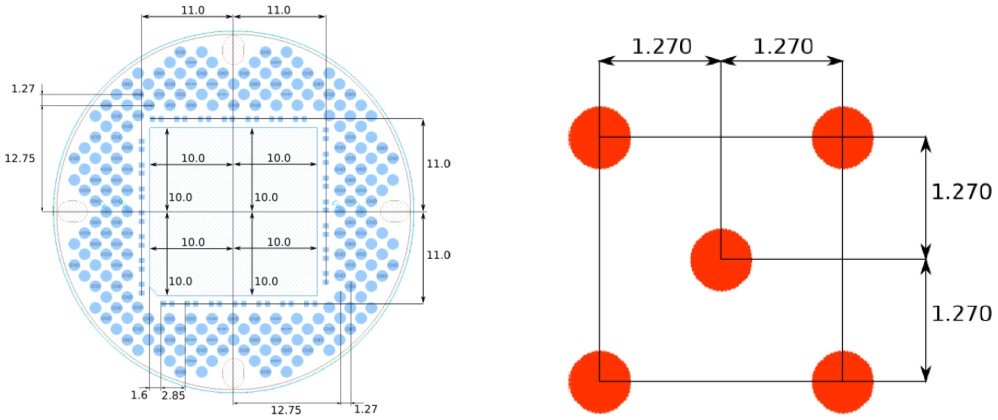
The bottom layer hosts both the pins used to connect the detector to the socket and the thermal pad to cool down the ASIC.

A central square of dimensions $20.0 \times 20.0\,\mathrm{mm}^2$ is dedicated to host the heat sink pad.

Around the thermal pad perimeter, a line of pads to solder decoupling capacitors is present. These capacitors decouple the ASIC power nets from the ground; in particular, the several capacitors decouple the VDDA, VDD, VDD GWT, VDD PST and VDD PLL nets.

Around the perimeter defined by the capacitors line, the pins used to route I/O

signals are placed, based on the footprint shown in Figure 3.8b, in a matrix of 31 rows and 31 columns, as shown in Figure 3.8a. The pin closest to the bottom right corner is missing, to break the symmetry and allow a correct connection to the socket. Pins have a length of 4.6 mm and a core diameter of 0.46 mm.



(a) (b)

Figure 3.8: **(a)** Carrier pin matrix. **(b)** Carrier pin footprint.

3.6 Applications

Several application fields will benefit from the development of this detector, such as high-energy physics, life sciences or material sciences. In general, this detector will provide great advantages to the applications and the technologies where the measurement of single photons on a large area with simultaneous excellent spatial and timing resolution is required.

Future HEP experiments will operate in environments with high particle intensities, and these environments call for new experimental challenges: the detectors will be required to have improved timing resolution, granularity and rate capabilities. Existing detectors cannot satisfy such requirements. Thus, the 4DPHOTON detector will bring a great advantage to these experiments.
For example, Ring Imaging CHerenkov (RICH) detectors will be empowered by this detector since they can exploit excellent timing measurements to perform a precise time association of the hits, that will allow to discriminate overlapping rings.

The gold-standard technique of the fluorescence lifetime, related to life sciences, is the time-correlated single-photon counting (TCSPC): this technique consists of recording with picosecond precision the single fluorescence photon emitted by

a sample, excited by an ultra-fast laser pulse [69]. Typically this measurement is done with non-imaging fast detectors, but the TCSPC technique, exploiting cameras to image the entire field, is already well established.
This 4d photon technique is faster, but requires single-photons recorded with a resolution of few picoseconds, and requires high rates capabilities. Current detectors have a good timing resolution, but the frame-based nature lead to single-photon losses. Such a problem would be overcome by the data-driven architecture of the 4DPHOTON phototube. Moreover, new imaging techniques can be explored thanks to the characteristics of the new hybrid detector: for example, combining super-resolution in wide field images (e.g. PALM, STORM, etc. [70]).

4

Timepix4 ASIC

4.1 Hybrid pixel detectors

One of the most important elements of High Energy Physics experiments are their particle trackers, aiming to reconstruct the particle trajectories. Developing detectors with this task is very complex, since they must be able to reconstruct trajectories of particles with a high spatial and timing density.
The need for fast detectors with high granularity triggered the initial development of hybrid pixel detector (HPD) and it is still pushing their growth.

Hybrid pixel detectors consist of arrays of μm-scale fully depleted semiconductor p-n junctions that are sensitive to radiation. The read-out electronic chip, which is bonded to the sensitive detector, is designed to align with the detector's structure. This configuration creates a read-out chain where each sensitive element is individually connected to its corresponding read-out electronics.

The connection between electronic and detector is performed through a bump-bonding technique, consisting of small spheres of solder, indium or gold establishing the electrical connection between detector and chip. This connection has the function of a mechanical connection as well. The number of channels is typically very high, thus it is complicated to have an output connection dedicated to a single channel. Therefore, the readout logic is usually gathered on a single region close to the electronic periphery, to allow an easier access.

Hybrid detectors are characterised by pixels with small dimensions. They typically have an active area $\lesssim 10^{-4}\,\mathrm{cm}^2$, reading a detector section with a thickness of hundreds of µm. Thus, the pixels present a very low capacitance, of order of $\lesssim 0.1\,\mathrm{pF}$, allowing fast signals shaping keeping a low noise level. A typical noise level on a single pixel is then of order of $200\,e^-$ for a common electronic working at 40 MHz. Setting a threshold at $\sim 7-10\sigma$ of the noise allows to operate removing almost completely spurious events without decreasing the detecting efficiency on energy regions covered by most common applications.

4.1.1 Main applications of Hybrid pixel detectors

High energy physics applications

Firstly, hybrid pixel detectors were developed in 1980s to track particles in collider experiments of high energy physics, in order to discriminate tracks left by different particles.

The first hybrid pixel detector was developed for the RD19 project [71].
It was followed by the development of DELPHI modules, where large sensors started to be bonded to multiple ASICs, since the integrated circuit cannot be too large due to the number of transistors and their dimensions, leading to complicate mash alignment if the ASIC is too large.

The four experiments along LHC are equipped with HPD, used in different configurations and with different scopes.
The improvement of the timing resolution reached by the ASIC coupled to the detectors lead to an improvement on the vertex reconstruction precision in high energy physics experiments.

Material science, biology and other applications

Due to their performance in terms of noise level, readout speed and efficiency, hybrid pixel detectors started to be applied also to fields not related to high energy physics, bringing great advantages to biology, medicine and material science as well [72, 73]. For example, technologies used on Free Electron Laser or synchrotron applications, as well as medical technologies like the spectral Computed Tomography, have been revolutionised thanks to pixel detectors intrinsic high spatial resolution, and the low intrinsic noise of hybrid detectors, granting a better Signal-to-Noise Ratio.
Several integrated circuits have been developed to match the requirements of these research fields.

In 1998 the PILATUS circuit has been developed by the Swiss Light Source synchrotron detector group [74]. This ASIC was dedicated to X-rays experiments.

In 1998, the DELPHI pixel group released the XPD1 circuit, characterised by pixels of size 130 µm [75]. Based on the following generation of XPAD circuits, XPAD2, the first large area HPD was developed, exploiting it for material sciences by performing diffraction experiments.

Medical imaging

Several circuits have been developed to exploit their advantages on medical imaging techniques, improving imaging resolution with respect to standard X-ray cameras and CT scanners.

The MARS micro-CT scanner is based on Medipix chips [76]. Different versions exist, consisting of assemblies of different Medipix ASICs and different coupled sensors.
The image quality of these detectors is outstanding.

4.2 Medipix Collaboration

The Medipix collaboration has been founded in 1998 aiming to develop ASICs for hybrid pixel detectors for particle detection, imaging and tracking, applying these technologies into several fields, including high energy physics experiments, nuclear physics, medical and biology applications, and material science applications.

Within this context, in May 2016 the Medipix4 Collaboration has been set to provide a next generation of Medipix family application-specific integrated circuit (ASIC), and currently the collaboration is composed of 19 members.

The two chips developed by this collaboration are the Timepix4 [77, 51], developed in 2019, that will be described in more detail in the following sections, and the Medipix4 [78], developed in 2022. The Medipix4 is built in a 130 nm technology, and consists of a pixel matrix of 320 × 320 pixels with a square pitch of 75 µm. A Charge Summing architecture is implemented in the ASIC to correct the charge sharing effect among adjacent pixels.

Both of the ASICs developed have a 4-side buttable architecture, with an integrated periphery compatible with the use of Through-Silicon-Via. This architecture allows two improvements: firstly, it is possible to develop larger chips, since the power supply can be better distributed across the matrix. Moreover, more chips can be mounted side by side in order to cover a larger detector.

These aspects will be presented in more detail in the following sections.

4.3 Timepix and Medipix ASIC generations

4.3.1 Medipix family

The first chips developed by the Medipix collaboration are photon counting devices, part of the Medipix ASIC family.

Medipix1

The Medipix1 is the first CMOS ASIC able to detect single photons on a large area, performing photon counting measurements through frame based readout [79].
Developed in 1997, it consists of a matrix of 64×64 pixel with $170\,\mu m$ pitch. Each pixel contains a 15-bit depth counter, measuring the number of hits above threshold while the frame is read.
It has been used in application bump bonded both to silicon and GaAs detectors.

Medipix2

The Medipix2 ASIC [80] has been developed in 250 nm CMOS technology in 2007, and it is formed by a matrix of 256×256 pixels, each with a size of $55\,\mu m \times 55\,\mu m$. It allows to measure both positive and negative signal, making it suitable for coupling with different kinds of detectors. The readout is frame based on 14-bit counters for each pixel: for each frame time the pixel counts the number of hits above a set threshold, and this photon counting information is forwarded to the readout at the end of each frame.
The intrinsic noise has been estimated to be $100\,e^-$; two threshold levels can be set to perform a window discrimination. The minimum operating threshold is $\sim 700\,e^-$.

Medipix3

The Medipix3 chip [81, 82] is an evolution of Medipix2, allowing to perform color imaging and to remove dead-time.
Developed in a 130 nm CMOS technology, it is composed by 256×256 square pixels of $55\,\mu m$ side. However, it allows to be coupled to pixel detectors with $110\,\mu m$ pitch, using four ASIC pixels to read out a single sensor pixel.
Each pixel contains 2 counters, active alternately, in order to read one out while the second is counting, and remove the dead time. Each of these counters have a

programmable depth of 1, 2, 12 bits. Alternatively, a single 24-bit counter can be used, performing a sequential readout instead of the continuous readout granted by the two counters alternation. Clearly, when a 110 µm pitch sensor is coupled to the chip, 8 counters are used to read out a single sensor pixel.
Similarly to the Medipix2 ASIC, two threshold can be set per pixel, allowing to perform window gating and to perform spectral imaging. When operating in spectroscopic mode, namely gathering 4 pixels and reading them out together, 8 threshold levels can be set to perform finer window gating.
An important innovation is the introduction in Medipix chips of a Charge Summing architecture, allowing a reduction of the charge loss due to charge sharing effect.

The noise level has been measured to be 80 e^- in Single Pixel Mode (SPM), and 175 e^- in Charge Summing Mode (CSM). The minimum operating threshold is $\sim$ 700 e^-.

Medipix4

The Medipix4 ASIC is the latest generation ASIC of the Medipix family [78].
Developed in 130 nm CMOS technology, it is the first chip of the Medipix family to be 4-side buttable, allowing for large area tiling using Through-Silicon-Vias.
It is composed of a 320 × 320 pixel matrix with 75 µm pitch. Similarly to its predecessor, it can be coupled also to sensors with a pixel pitch of 150 µm. The former operation mode is called Fine Pitch Mode (FPM, consisting of an matrix of 320 × 320 pixel with 75 µm pitch), and the latter is called Spectroscopic Mode (SM, consisting of an effective matrix of 160 × 160 pixel with 150 µm pitch).
Analogously to Medipix3, single pixel and charge summing acquisition are possible, as well as sequential and continuous readout. Each 75 µm side pixel has 2 counters that can be programmed to have 2 or 12 bits depth in continuous readout mode (alternating the readout of the two counters), or depths of 1, 2, 12 and 24 bits in sequential readout mode.

Differently from Medipix3, this ASIC can measure only negative signals. The Equivalent Noise Charge is $\sim$ 100e^-, corresponding to a minimum operating threshold of $\sim$ 560e^- in SPM and $\sim$ 930e^- in CSM.

4.3.2 Timepix family

The Timepix family was born in 2006 as a development of the Medipix family, driven by the need of measuring single-photons-related quantities, as their Time of Arrival on the detector and the deposited energy. The Timepix family is based on the concept of assigning also a time-stamp to the measured hits by instantiat-

ing on-pixel clocks, improving the information received with respect to a photon counting chip.

Timepix

Timepix [83], designed in 250 nm CMOS technology, consists of a matrix of 256 × 256 pixels with a 55 µm pitch. The readout is frame based, as the first Medipix chips, but Timepix can be operated in three different modes: Time-of-Arrival mode, energy mode (through the measurement of the Time-over-Threshold) and photon counting mode. Both ToA and ToT can be measured, but not simultaneously. Timepix is characterised by a timing resolution of 10 ns, and the pixel dead time is of the order of 300 µs, corresponding to the readout time of one frame.
The main specifications of Timepix are presented in Table 4.1.

Table 4.1: Main specification of the Timepix ASIC [83].

General specification	
CMOS technology	250 nm
Pixel size	55 µm × 55 µm
Pixel matrix	256 × 256
Analog front end	
Polarity	Positive and negative
Noise	100 e^- rms
Threshold variation	35 e^- rms
Minimum operating threshold	700 e^-
Digital front end and readout	
Acquisition modes	1. Charge (ToT) 2. Time (ToA) 3. Photon Counting
Readout type	Frame based
Zero suppressed readout	No
Counters per pixel	1 counter of 14 bits
Readout dead time	≥ 300 µs
Timestamp binning	10 ns
DACs to set voltages	13 of 8 bits

Timepix3

In 2014 the Timepix family has grown with the development of Timepix3, designed in 130 nm CMOS technology [84].
As for Timepix, the pixels are arranged in a matrix of 256 × 256 pixels with a

pitch of 55 µm.
Simultaneous ToA and ToT information are provided, differently from Timepix.
An important introduction made in Timepix3 is the possibility to perform a data-driven readout, with a maximum rate of 40 Mhits/s/cm^2: it consists of an event-by-event zero suppressed readout, where a pixel starts the process to send off-chip the data right after the hit, and only in the case of a hit. This kind of readout allows to reduce the pixel dead time, reaching a dead time of the order of 475 ns. More details on this readout will be provided in Subsection 4.9.2.
The timing resolution improved as well with respect to Timepix, reaching a time bin size of 1.562 ns.
A comparison between the main characteristics of Timepix and Timepix3 is shown in Table 4.2.

Table 4.2: Comparison between main features of Timepix and Timepix3 [85].

	Timepix	**Timepix3**
General specification		
CMOS technology	250 nm	130 nm
Pixel size	55 µm × 55 µm	
Pixel matrix	256 × 256	
Analog front end		
Polarity	Positive and negative	
Noise	100 e^- rms	62 e^- rms
Threshold variation	35 e^- rms	30 e^- rms
Minimum operating threshold	700 e^-	500 e^-
Digital front end and readout		
Acquisition modes	1. Charge (ToT) 2. Time (ToA) 3. Photon Counting	1. Time (ToA) and Charge (ToT) 2. Time (ToA) 3. Photon Counting (PC) and integral charge (iToT)
Readout type	Frame based	1. Data Driven (DD) 2. Frame based
Zero suppressed readout	No	Yes
Readout dead time	> 300 µs	> 475 ns
Timestamp binning	10 ns	1.562 ns

Timepix2

Based on the Timepix3 architecture, two others ASICs have been produced with different goals and improvements: Timepix2 (2018), and Timepix4 (2020).

Timepix2 is an ASIC in 130 nm CMOS technology, with a matrix of pixels analogous to Timepix and Timepix3 [86]. In this chip, shutter functionalities have been improved, preventing it from truncating hits acquired straddling the shutter falling edge, and ignoring hits which started before the shutter rising edge.
The ToT linearity range has been extended, reaching in adaptive gain mode a saturation at 950 ke^-, corresponding to 3.42 MeV in Si detectors [87, 88].
The possibility to power off specific pixels which are not used has been introduced, to reduce power consumption.
In Table 4.3 the main Timepix2 specification are shown.

Table 4.3: Main specifications of Timepix2 [89].

General specification	
CMOS technology	130 nm
Pixel size	55 µm × 55 µm
Pixel matrix	256 × 256
Sensitive area	1.98 cm^2
Analog front end	
Polarity	Positive and negative
Noise	61 e^- rms
Threshold variation	40 e^- rms
Minimum operating threshold	600 e^-
Digital front end and readout	
Single frame	ToT and ToA
Continuos Read-Write (CRW)	1. ToT and PC 2. 2 counters for ToT 3. 2 counters for ToA 4. 2 counters for PC
Timestamp binning	> 10 ns
Maximum readout bandwidth	3.2 Gb/s

4.3.3 Other ASICs based on Medipix and Timepix families

Other ASICs have been designed, based on the technologies and the knowledge reached developing the chips of the Medipix and Timepix families.

The CLICpix1, produced in 2013, and the CLICpix2, produced in 2016, are de-

signed in 65 nm CMOS technology [90, 91].
They are characterised by matrices of 64×64 and 128×128 pixels, respectively, with a 25 µm pitch, and they can measure both ToA and ToT.

The VeloPix, built in 130 nm CMOS technology, has been designed in 2016 for a trigger-less upgrade of LHCb VELO detector.
It consists of a matrix of 256×256 pixels with 55 µm pitch, analogous to Timepix, Timepix2 and Timepix3.
It has a data-driven architecture and provides timing information on the hits arrival, with a maximum reachable hit rate of 900 Mhits/s/ASIC, thanks to an increased output bandwdith of 20 Gb/s.

4.4 Timepix4 general description

Timepix4 is the latest generation application-specific integrated circuit (ASIC) of the Timepix family [77, 51], mainly targeted for single particle detection in hybrid pixel detectors [77]. It is a CMOS ASIC in 65 nm developed by the Medipix4 Collaboration for the readout of hybrid pixel detectors, which is able to reach high spatial and timing resolutions together with high rate capabilities.

With respect to the previous ASIC of this family, Timepix3, Timepix4 has several improvements, such as the 4-side buttable architecture. Its sides measure $24.7\,\text{mm} \times 29.96\,\text{mm}$, thus it has an active area almost 4 times larger than Timepix3 ($\sim 2\,\text{cm}^2$ to $\sim 7\,\text{cm}^2$). The output packets are composed by 64 bits instead of 48 bits, but thanks to a significantly larger output data bandwidth (from $\sim 5\,\text{Gb/s}$ to $\sim 160\,\text{Gb/s}$) the maximum output rate is higher too, reaching $3.58 \times 10^6\,\text{hits/mm}^2\text{/s}$. As in the case of Timepix3, the front end can be configured to read out signals of both polarities, so Timepix4 can be operated both to collect holes (positive polarity) or electrons (negative polarity). Furthermore, the energy resolution has been improved from $< 2\,\text{keV}$ to $< 1\,\text{keV}$. Finally, the timing resolution has been improved, moving from a timing bin size of 1.56 ns to 195 ps.

Other comparisons are presented in Table 4.4.

The Timepix4 ASIC has been released in 4 submissions since 2019:

- **Timepix4v0:** released in 2019; the chip is operational, but an excessive noise is observed in some of the pixels. The source of the noise was found to be cross-talk (electromagnetic coupling) between transmission lines in the ASIC peripheries and front end. Furthermore, the 640 MHz clock used in the edge peripheries and the Voltage Controlled Oscillators (VCO), see Section

Table 4.4: Comparison between main features of Timepix3 and Timepix4 [92].

		Timepix3	Timepix4
General specification			
CMOS technology		130 nm	65 nm
Pixel size		55 µm × 55 µm	
Pixel matrix		• 256 × 256 • 3-side buttable	• 448 × 512 • 4-side buttable
Sensitive area		1.98 cm^2	6.94 cm^2
Analog front end			
Polarity		Positive and negative	
Noise		62 e^- rms	80 e^- rms
Threshold variation		30 e^- rms	40 e^- rms
Minimum operating threshold		500 e^-	500 e^-
Digital front end and readout			
Data driven	Mode	ToA and ToT	
	Event packet dimension	48-bit	64-bit
	Maximum rate	$0.43 \cdot 10^6 \frac{hits}{mm^2 s}$	$3.58 \cdot 10^6 \frac{hits}{mm^2 s}$
	Maximum pixel rate	1.3 kHz	10.8 kHz
Frame based	Mode	PC and iToT	Continuous Read-Write: PC (8 or 16 bits)
	Frame	Zero suppressed	Full frame
	Maximum rate	$0.82 \cdot 10^9 \frac{hits}{mm^2 s}$	$\sim 5 \cdot 10^9 \frac{hits}{mm^2 s}$
Timestamp binning		1.562 ns	195 ps
Energy resolution		< 2 keV	< 1 keV
Maximum readout bandwidth		5.12 Gb/s	163.84 Gb/s

4.7, are not to specification;

- **Timepix4v1:** released in 2020; it introduced an improved shielding in the peripheries, and 640 MHz clock in the peripheries was recovered; VCOs still do not oscillate at the nominal frequency of 640 MHz;
- **Timepix4v2:** released in 2021; VCOs are improved, thus allowing Time-to-Digital Converter (TDC) to work correctly; further shielding improvements were introduced.
- **Timepix4v3:** released in 2022; it introduces larger Input/Output wire-

bonding pads to ease the wire-bonding.

4.5 ASIC layout

4.5.1 Pixel arrangement

Timepix4 consists of a 512×448 square pixel array with 55 µm pitch, for a total active area of $\sim 6.94\,\mathrm{cm}^2$.
The top surface of the ASIC consists of a uniform matrix of bump bonding pads: each pad opening has an octagonal shape with a side-by-side distance of 16 µm and an octagonal passivation with side-by-side distance of 12 µm, as shown in Figure 4.1.

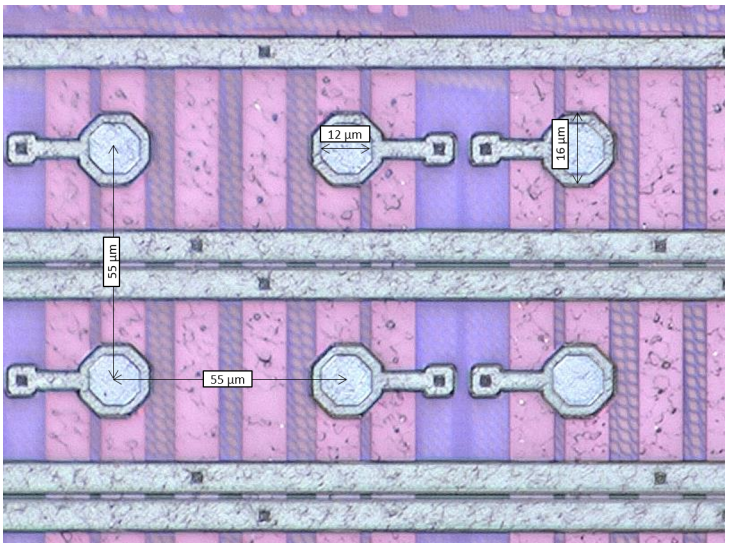


Figure 4.1: Timepix4 bump bonding pads opening [93].

A basic matrix layout is presented in Figure 4.2.
The pixels are organised in two matrices of 256×448 pixels each, that will be referred to as TOP and BOTTOM matrices. These two sub-matrices share the same design, including that of the readout architecture. While significantly easing the design this means that the two matrices will have independent readout channels: data coming from the TOP matrix will use different physical links with respect to data coming from the BOTTOM matrix. As shown, three peripheries are present:

- **edge peripheries**: mostly used for data readout, both of them contain 8 serializers that can be configured to operate up to 10.24 Gb/s each, and 8×8 router; they contain also a PLL, configuration logic, 224 End-of-Columns

(EOC) blocks, and I/O pads (both Through-Silicon-Via and Wire Bonding); they will be referred to as TOP and BOTTOM periphery;

- **CENTER periphery**: it hosts analog blocks, like global Digital-to-Analog-Converters (DAC) and Analog-to-Digital-Converters (ADC), that are going to be described in more detail in Section 4.6; it also contains temperature and power supply sensors; as in the edge peripheries, this contains also EOC blocks (2×224), configuration logic, and I/O pads (only TSV).

Pixels are gathered in groups of 2×4 pixels, called SuperPixels, as shown in Figure 4.2. In turn, 4 adjacent SuperPixels of the same double column form a SuperPixelGroup (SPG), and finally 16 SPGs form a full double column.

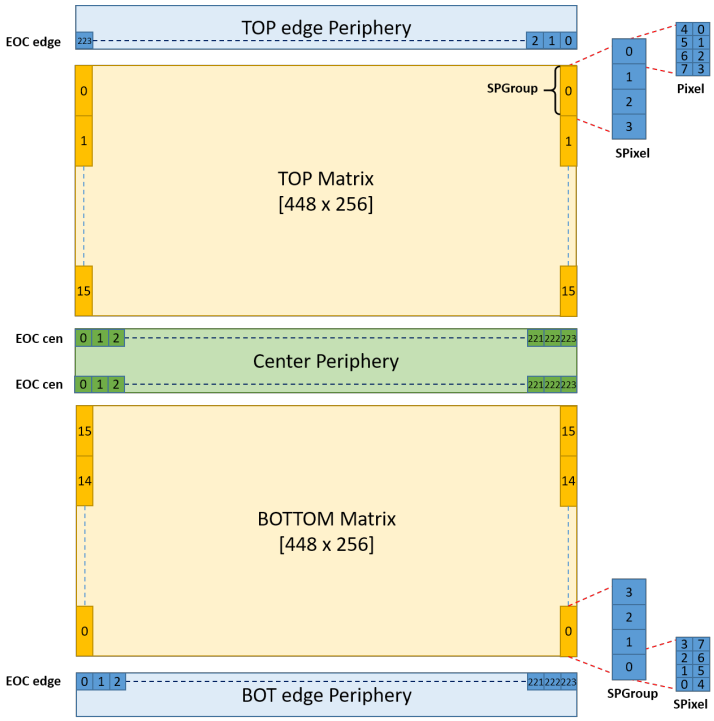


Figure 4.2: Timepix4 pixel matrix organization [68]. EoC (End-of-Column) indicates the end of a double readout column. Spixel (Super Pixel) indicated a set of 8 pixels sharing the same local VCO. SPgroup (Super Pixel Group) indicates a set of 4 Super Pixels sharing a common set readout resources. The Top and Bottom Matrix are two independent sub-matrices of pixel sharing the same design. Peripheries indicate the configuration and readout resources. It must be noted that in the real design the resources of the central periphery share the same physical space of the two matrices, so that no gap is present in the active area.

4.5.2 Wire-Bonds and Through-Silicon-Via

Two WireBond extenders are placed at the edge of the TOP and BOTTOM peripheries, to provide connection for I/O signals through wire bonds.
As described in Subsection 4.3.1, the Timepix4 architecture, as the Medipix4 architecture, is compatible to be used as well with Through-Silicon-Via. The advantages of this technique are:

- possibility to have a 4-side buttable architecture needed to place several chips adjacent to cover larger detectors;
- better power supply distribution;
- increased active area thanks to the different dicing options (removing the wire-bond extenders the active area would increase from 93.7% to 99.5% of the total chip area).

4.6 Analog periphery

The analog periphery, located as a center hidden periphery between the TOP and BOTTOM matrices. The most relevant blocks comprised in this periphery are:

- slow control;
- center PLL;
- EOC (center End-of-Column, digital and analog);
- BandGap and Biasing Digital-to-Analog Converters (DACs);
- 12-bits Analog-to-Digital Converter (ADC).

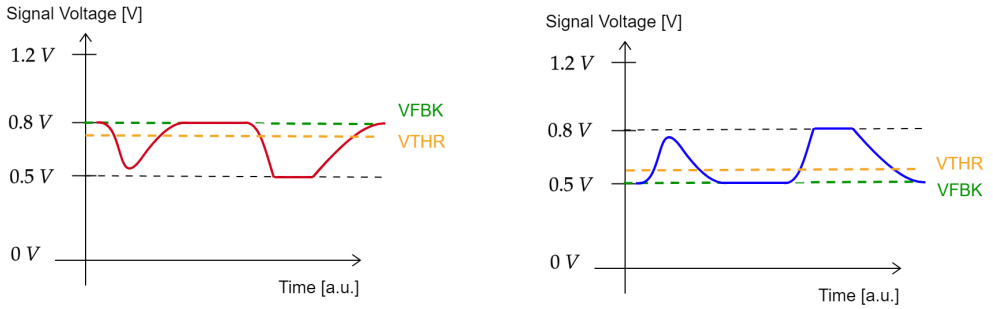
The BandGap circuitry generates a stable voltage to be used as reference for the biasing DACs.
There are 13 DACs different analog biasing circuits in the center periphery: 5 DACs bias the preamplifier circuit, 5 of them are used for the discriminator circuit, 2 DACs generate the voltages to set the test-pulse charge, and the latter bias the DAC circuitry to tune the threshold at pixel level.
The DACs are either voltage DACs (type V), providing a voltage output linearly dependent on the DAC value set, or current DAC (type I), providing a current output linearly dependent on the DAC value set. The current DACs feature either NMOS or PMOS transistors, generating currents adapted to the levels in the analog EOC to match the target transistors in the pixels. Table 4.5 reports the main characteristics of each DAC, such as the block circuit biased by it, the DAC type, its range (in bits) and the output voltage or output current range.

Table 4.5: Main parameters of the biasing DACs, including the block circuit biased, the DAC name and its type (voltage output or current output), the length of the register setting the DAC and the output range.

Block biased	DAC name	DAC type	Range [# bits]	Output range
Discriminator	VBiasDiscTailNMOS	I	8	3.1 µA
Discriminator	VBiasDiscPMOS	I	8	2.6 µA
Discriminator	VBiasDiscTRAFF	I	8	4 µA
Discriminator	VCascDisc	V	8	1.2 V
Discriminator	VThreshold	V	14	1.2 V
DAC	VBiasDAC	I	8	160 nA
Preamplifier	VBiasPreamp	I	8	1.45 µA
Preamplifier	VCascPreamp	V	8	1.2 V
Preamplifier	VBiasLevelShift	I	8	1.45 µA
Preamplifier	VBiasIkrum	I	8	100 nA
Preamplifier	VFBK	V	8	1.2 V
Test pulse	VTpulseCoarse	V	8	1.2 V
Test pulse	VTpulseFine	V	14	1.2 V

The linear output dynamic range of the Timepix4 analog front-end is between $\sim 500\,\mathrm{mV}$ and $\sim 800\,\mathrm{mV}$, which corresponds to a range of $\sim 8.5\,\mathrm{ke}^-$ in high gain configuration ($\sim 35\,\mathrm{mV/ke}^-$), and to a range of $\sim 15\,\mathrm{ke}^-$ in low gain configuration ($\sim 20\,\mathrm{mV/ke}^-$). The threshold is set based on the difference between the output voltages of the VThreshold and the VFBK DACs, as shown in Figure 4.3. The latter sets the baseline of the preamplifier output, and its nominal value is selected depending on the signal's polarity (500 mV for negative polarity, 800 mV for positive polarity). Thus, the VThreshold output is set higher than the VFBK voltage for negative signals, and lower for positive signals. The maximum settable threshold, depending on the gain configuration, can be either $\sim 8.5\,\mathrm{ke}^-$ or $\sim 15\,\mathrm{ke}^-$. The least significant bit current of the threshold equalization DACs located in each pixel are set by the VBiasDAC.

The VBiasPreamp DAC determines the slope of the rising edge of the preamplifier output. At higher output DAC voltages the slope increases, decreasing the analog front-end contribution to the timing resolution, thus improving the resolution at low voltages.
The VBiasLevelShift DAC generates a voltage reference, used in the analog EOC to derive two other voltages, in turn used to bias the VBiasLevelShiftN and the VBiasLevelShiftP lines. Based on the polarity selected, only one of the two lines is enabled.
The VBiasIkrum DAC defines the time in which the preamplifier output signal



(a) (b)

Figure 4.3: Schematic representation of the baseline and threshold setting through VFBK and VThreshold DACs, configuring the Timepix4 in **(a)** hole collecting mode (positive polarity) and **(b)** electron collecting mode (negative polarity).

returns to zero for a fixed charge. Increasing the DAC voltage would reduce this time, making the signal returning faster to zero: this would reduce the probability of analog pile-up, namely the probability of a second hit reaching the pixel before it is read-out, and it would increase the rate sustainable without analog pile-up, but it will degrade the ToT resolution. Conversely, reducing the DAC voltage would lead to the signal returning to zero slower, reducing the affordable rate but increasing the charge measurement resolution. The setting of this DAC must be a customised trade-off depenending on the application.
Two DACs are used to inject test pulses on selectable pixels, the VTpulseCoarse and the VTPulseFine. As shown in Figure 4.4, the voltage on the testpulse input capacitor is a differential voltage obtained by the difference of the VTPulseCoarse DAC voltage and the VTPulseFine DAC. The voltages of both the DACs, as well as those of the other DACs, are affected by resistive drops along the double columns due to the pixel load; using a differential voltage to generate the test pulse allows to apply the same voltage to each input capacitors, regardless of their location along the double column.

4.7 Analog and Digital Front-end

The Timepix4 front-end can be configured to be sensitive either to electrons or holes. The analog and digital front-end can be divided into three levels: pixel level, SP level, and SPG level.
The analog front-end components are all contained at the pixel level. A switch is used to power enable the pixel or not. If the pixel is powered, the signals received by the input pads are amplified by a charge sensitive amplifier, shown

in Figure 4.4, including a programmable feedback capacitance, which allows to choose among several pixel gains:

- in high-gain mode, only a metal-to-metal capacitance of 3 fF is used, resulting in a gain of $\sim 35.8\,\mathrm{mV/ke^-}$ when the Timepix4 is operating in electron collecting mode, and $\sim 34.5\,\mathrm{mV/ke^-}$ in hole collecting mode;
- in low-gain mode, a capacitance of 3 fF is added in parallel, resulting in a gain of $\sim 20.5\,\mathrm{mV/ke^-}$ both in electron and hole collecting mode.

Additionally, if the Timepix4 is configured to measure positive signals, an adaptive gain mode can be programmed by enabling a MOS capacitance, to extend the ToT dynamic range up to $\sim 800\,\mathrm{ke^-}$ instead of $\sim 200\,\mathrm{ke^-}$ [94].
The feedback loop has the function to reset the front-end and to compensate for leakage current; it is based on the Krummenacher circuit [95] and is optimised for electron collecting mode; it can compensate up to 10 nA per pixel.
A global threshold is set through DACs in the central periphery, as explained in Section 4.6. Moreover, at pixel level, it is possible to locally tune the threshold by shifting the global one through a 5-bit DAC.

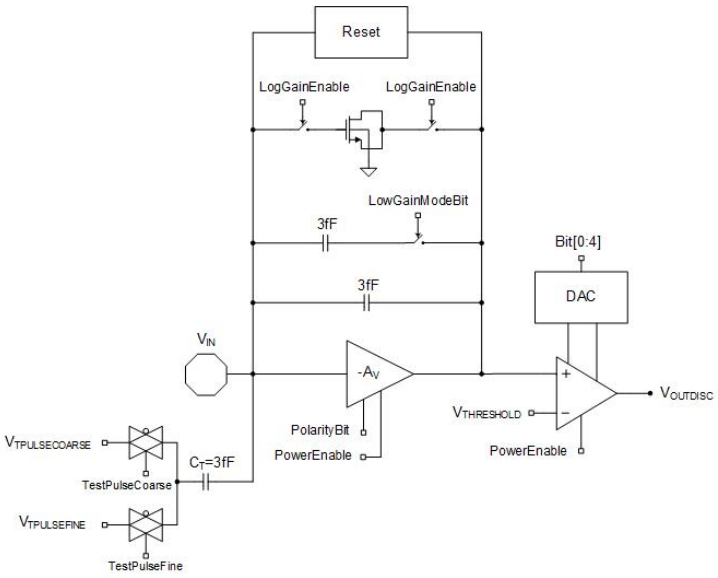


Figure 4.4: Block diagram of the pixel analog front-end [77].

Signals exceeding the threshold are processed by the digital front-end, generating output data words and starting the read-out data transmission process, as shown in Figure 4.5. The pixel can be digitally masked in order to avoid the digitised signal to produce an output packet.

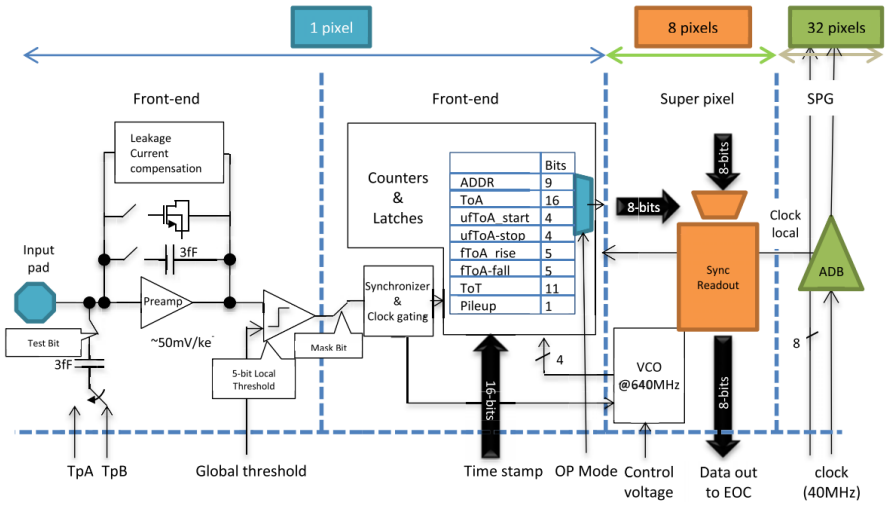
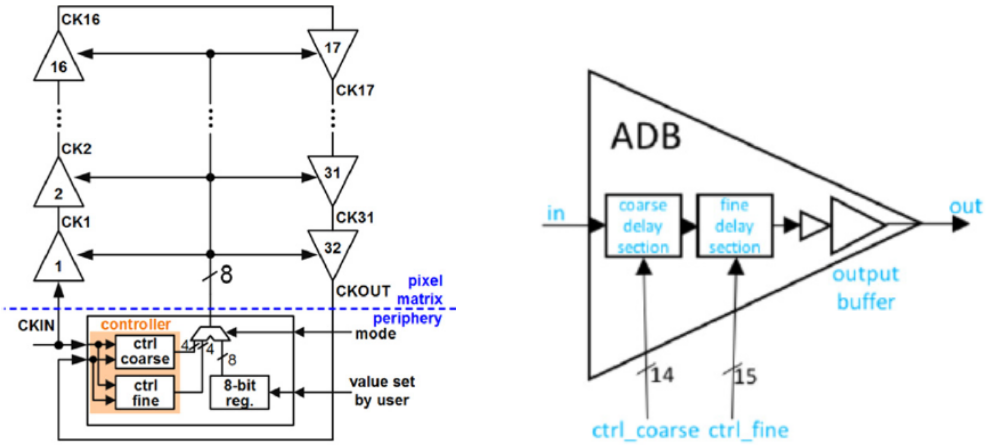


Figure 4.5: Simplified block diagram of the pixel front-end electronics and the pixel, SP and SPG structure [77].

A time stamp is provided by a Time to Digital Converter (TDC), which measures the Time-of-Arrival (ToA) and the Time-over-Threshold (ToT) exploiting a local Voltage-Controlled Oscillator (VCO), shared by the eight pixels of the SP. The TDC nominal bin size is 195 ps that corresponds to ~ 56 ps r.m.s. resolution.
To reach the desired timing performance, the timestamp clock must be stably distributed across the matrix. To do that, each SPG block uses two phases of the DLL clock obtained from two of the Adjustable Delay Buffers (ADBs) in the DLL loop: one of them propagates the clock up the double column, while the other propagates it back to the edge periphery. Thus, the two clocks on each Super Pixel Group will have the same frequency and a fixed phase relationship. At the end of the double column a controller, that is the DLL control logic, maintains the delay between the output clock and the input master clocks at 25 ns, by adjusting the ADB's delay with fine steps of 4 ps. A schematic of the DLL clock distribution architecture is shown in Figure 4.6.

At the SP level, besides the VCO shared by the pixels, a readout synchronizer block is present: this has the function to ask permission for transmitting pixel data, in order to correctly determine the data transmission priority. More details on the packets generation and transmission will be provided in Section 4.8.



(a) (b)

Figure 4.6: (a) Schematic representation of digital DLL in a Timepix4 double column, comprising the coarse and fine controller, the distribution tree and two Adjustable Delay Buffers per SPG, represented as triangles. (b) Detail of an Adjustable Delay Buffer [77].

4.8 Data readout

The Timepix4 data readout is highly configurable: data can be read out either through slow control or high-speed links, and the output bandwidth can be set from a minimum of 40 Mb/s to a maximum of 163.84 Gb/s; moreover, two acquisition modes are available, namely frame-based acquisition and data-driven acquisition, described in Section 4.9. The output data words[1] generated are 64-bit long, regardless of the acquisition mode. In the case of frame-based acquisitions the information of a Super Pixel are contained either in one (8 b per pixel) or two packets (16 b per pixel). Conversely, in the case of data-driven acquisitions a 64 b data word contains the information of a single pixel. A detailed description of acquisition modes and on the structure of the data-stream will be given in Section 4.9.

[1]In the context of the Timepix4 data acquisition we will refer to "64b data-word" to indicate the output of a pixel (data-driven mode) or of a SP (frame based). "Control word" will indicate the 64b Timepix control words. "64b/66b encoded word" will indicate the scrambled and extended data word transmitted on the Timepix4 differential outputs, regardless if it is a 64b data-word or a control word. "Data packet" will indicate the data belonging to a single frame in frame based acquisition mode. Lastly, "data segment" will indicate the internal structure of a data packet in frame based acquisition mode.

4.8.1 Edge periphery data path

Once a data word is produced, either in frame-based or data-driven mode, the permission to transmit the data word down the double column is requested. In data-driven mode, a priority encoder determines the pixel read-out order, while in frame-based mode data words are transmitted in order based on the source SP position (reading before the Super Pixels closer to the edge periphery).

Once transmitted down the double column, data words or data packets are processed and transmitted off-chip by the edge peripheries data paths, which architecture is shown in Figure 4.7.
The data path of both the edge peripheries is composed of a data fabric, a packet processor, 8×8 routers, Physical Coding Sublayer Transmitter (PCS TX) and a Gigabit Wireline Transmitter with a Clock Cleaner (GWT-CC). Routers, PCS TX and GWT-CC are used only if the read-out is done through high-speed links, and will be discussed in Subsection 4.8.2.

The data fabric of an edge periphery is split in two halves, Left and Right, and it contains 224 EOC in total. It propagates the words or packets received by the EOCs to the packet processor, placed between the two halves.
Each half is split in 4 data segment, called L0-L3 and R0-R3, respectively, each one collecting the data of 1 double column out of 4, for a total of 28 double columns read by each segment.

The packet processor allows to filter out data words received with a too high latency (only when the ToA_ToT readout mode, described in Subsection 4.9.2, is used), and to add to the data flow control words providing information external to the pixels data packets, but needed to correctly decode them as, for example, shutter related information, global clock timestamps sent periodically (heart beat), or information on the frame structures. More details on these control words will be provided in Section 5.2.1.

4.8.2 High speed readout

As said, the high-speed readout is based on a Physical Coding Sublayer Transmitter (PCS TX) and a Gigabit Wireline Transmitter with a Clock Cleaner (GWT-CC), which serializes the words stream and transmits them to an off-chip receiver. A basic schematic of the high-speed readout block, comprising router, PCS TX and GWT-CC, is reported in Figure 4.8. The high speed readout has a high configurability. Each link can be configured to operate at different speed, from 40 Mb/s to 10.24 Gb/s, and it is possible to use from 1 to 8 links per half matrix. This results in a maximum bandwidth of 163.84 Gb/s obtained if 16 links are

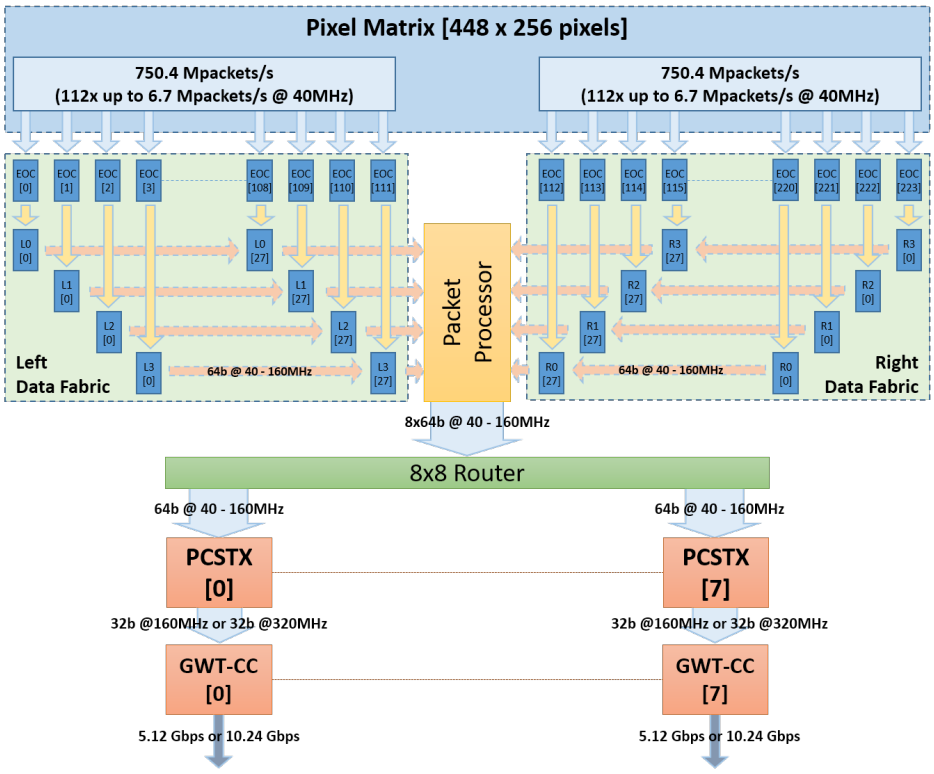


Figure 4.7: Edge periphery data path architecture [77].

active at the maximum speed of 10.24 Gb/s.

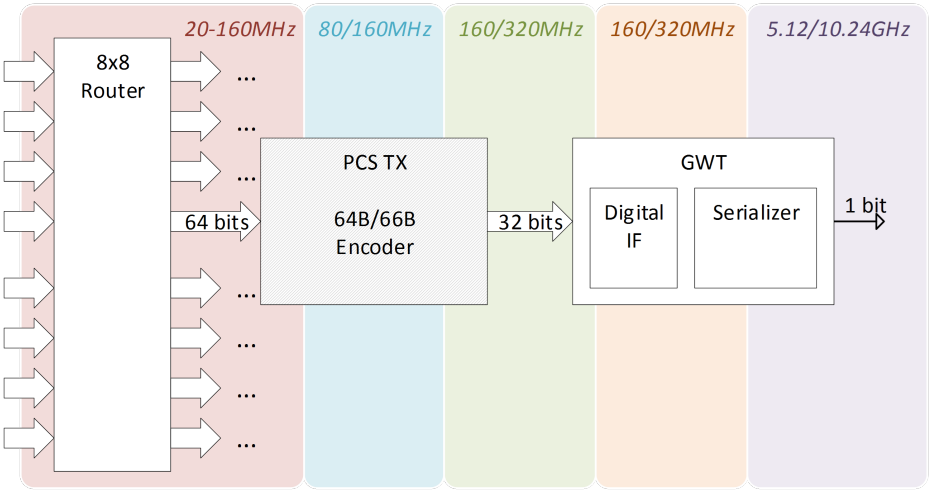


Figure 4.8: Basic schematic of high-speed readout architecture, including 8×8 router, Physical Coding Sublayer Transmitter (PCS TX) and a Gigabit Wireline Transmitter with a Clock Cleaner (GWT-CC) [96, 97].

A programmable 8×8 router maps data segments of the data fabric to one of the PCS TX encoder, depending on the output channels enabled. When Timepix4 is configured in frame-based mode, the router is not programmable and data are automatically routed to PCS TX encoder depending just on the number of high-speed links enabled in each periphery.

The PCS TX works as an interface between the router and the GWT-CC, transmitting words out of chip. Its tasks are encoding data based on the 64b/66b standard encoding communication protocol [98], and alignment. In addition, it includes modules to allow bypass the PCS TX, to enable test-patterns to test link alignment and to control the transceivers speed.
PCS TX is composed by the following main blocks:

- *aFIFO*: asynchronous FIFO providing clock domain crossing and backpressure compensation;
- *Scrambler*: scrambles the input data into pseudo-random output data using a self-synchronous scrambler;
- *Pseudo-Random Test-Pattern control*: Pseudo-Random Pattern Controller (PRCP) to generate the test patterns (PRTP);
- *Gearbox*: add synchronization headers to the input data to be transmitted and aligns them to the output bus;

- *Bit splitter*: controls the transceiver speed.

The scrambler and the gearbox are fundamental to encode the data before its transmission. The 64B/66B encoding, defined in the IEEE 802.3 Standard [98], transforms 64-bit data words into 66-bit encoded words, scrambling them in order to ensure that enough bit transitions are present to allow a stable clock recovery and alignment on the receiver side.
Firstly, words are scrambled following a polynomial function ($\mathrm{G}(x) = 1 + x^{39} + x^{58}$), without changing their length.
After the scramble, a synchronization header of 2 bits is added for every 64 bits of payload: the header is equal to '01' for data blocks and to '10' for control blocks, so that every 66-bits block starts with a transition, regardless of whether they are control or data blocks. Since the payload is pseudo-randomly scrambled, this is the only position within a block which always contains a transition, allowing to synchronize the encoded words once received.

The link speed can be decreased by sending each bit in output multiple times, increasing its duration without modifying the clock frequency. The reference clock used can run either at 320 MHz or 640 MHz: thus, links speed can be configured from 40 Mb/s to 5.12 Gb/s when the 320 MHz clock is used, and from 80 Mb/s to 10.24 Gb/s using the 640 MHz clock.
The bit splitter controlling the link speed has also the function to reduce the data word length from 64 bits to 32 bits.

The test-pattern generator can generate square waves, as well as PRTP patterns and Pseudo Random Bit Stream (PRBS-31, PRBS-23, PRBS-15, PRBS-7).
This module has been used to test the correct operation of the high-speed links, currently up to 5.12 Gb/s, both with wire bonds and TSV.

Words of 32-bits are sent to the GWT-CC serializer circuit, which converts them into a single-bit serial stream, transmitted off-chip.
A PLL, represented in Figure 4.9 by the PLL-CC block, cleans the external clock to use it as reference in the DLL circuit, to ensure a low jitter clock. The data, which are initially in a clock domain which may have a jitter higher than the clock cleaned by the PLL, are written in a dual port FIFO, as shown in Figure 4.9, which is then read using the cleaned clock, transmitting the data from a "dirty" to a "clean" clock domain. Multiplexers controlled by DLL select bit-by-bit the data and send them to differential line drivers.

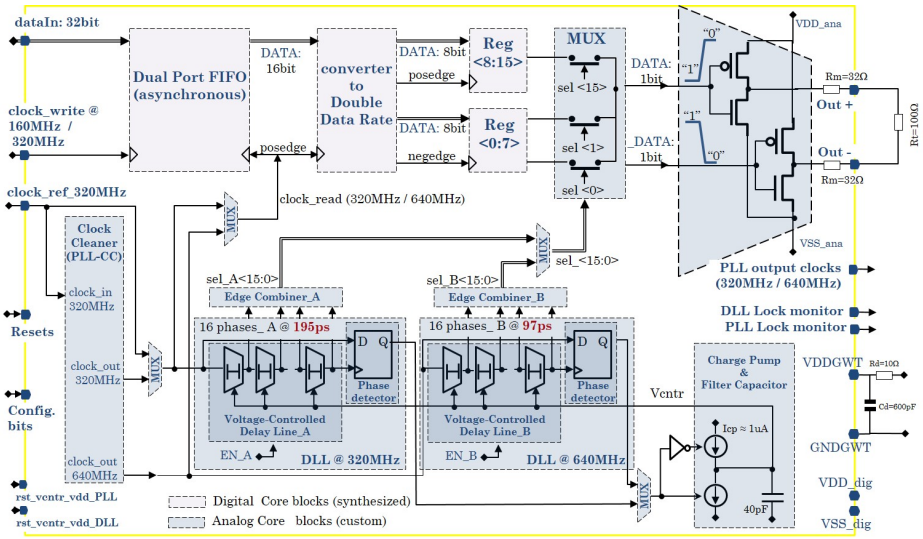


Figure 4.9: Schematic of the Gigabit Wireline Transmitter with a Clock Cleaner (GWT-CC) [96, 97].

4.9 Acquisition modes

Timepix4 can be configured in order to work in two different acquisitions: the frame-based acquisition, in which the whole matrix is read-out synchronously with the 40 MHz core clock, and the data-driven acquisition, in which pixel hits initiate the data transmission process only and right after the hit.

4.9.1 Frame-based acquisition

The frame-based acquisition is a non zero-suppressed readout of the entire matrix providing photon counting of the hits detected in a fixed time interval, called frame.
Providing only photon counting information, it is suitable for high rate environments, reaching maximum hit rates of $\sim 5 \times 10^9$ hits/mm^2/s.
Each pixel contains two counters, leading to continuous read/write (CRW) operation, since one counter is read while the other is counting. These counters have programmable depths, of 8 or 16 bits.

Each data word produced by a SP is 64-bits long, hence the data of 8 pixels can be contained in a single 64 b data word when using the 8-bit counter mode, otherwise two 64 b data word are needed if the 16-bits mode is used.
Frame and segment starting and ending packets are sent as well, providing information on the frame number and the pixel address, respectively. Information on the pixel address is not encoded in the output data, rather it is deduced by the

position of the data word in the data packet. This can be done since all pixels will output a fixed length word at the end of a frame. These data will be contained between two control words marking the begin and end of a frame thus forming a data packet.
The frame structure is given by the packet sequence presented in Table 4.6. After the frame start packet, 8 segments have to be read out (L0, L1, L2, L3, R0, R1, R2 and R3); each segment reads 1/8 of the 28 double columns, and each double column contains 64 SP (a single half matrix is considered, since the readout of the two halves are independent), so a total of 1792 data packets is read out for each segment. When the 16-bits counter mode is used, double the number of packets is generated.

Table 4.6: Format and packet order of a frame-based readout.

64b/66b data-word	**Timepix4 data-word identifier**	**Description**
10, 0x1E, C0:C7	Idle	Idle data word before frame 1 start
01, D0:D7	Frame_start	Frame 1 starts
01, D0:D7	Segment_start	First segment of frame 1 starts
01, D0:D7	Data	First data word of frame 1
...	N x Data	Rest of first segment data words
01, D0:D7	Segment_end	First segment of frame 1 ends
...	N_2 x Segments	Remaining segments of frame 1
01, D0:D7	Frame_end	Frame 1 ends
10, 0x1E, C0:C7	Idle	Idle data word before frame 2 starts
01, D0:D7	Frame_start	Frame 2 starts
...	N_3 x Frames	Remaining frames until readout disabled

The frame can be read out both through the slow control or through the 16 high speed links. The frame duration is automatically tuned in order to maximize the frame rate, depending on the available bandwidth. As an example, for most of the acquisitions presented in this thesis, a single link per half matrix has been used, operated at 2.56 Gb/s. The frame rate automatically set for this output bandwidth is 2790.1 FPS (Frame Per Second) when using the 8-bits mode, 1395.1 FPS with the 16-bits mode.

The frame rate can be arbitrarily decreased by adding a waiting time between the end of a frame read out and the beginning of the following frame.

4.9.2 Data-driven acquisition

The second kind of acquisition is the data-driven acquisition: this is an event-based, zero-suppressed readout, where a pixel generates a 64 b data word and starts the process to transmit it off-chip once it has been hit.
There are two data-driven acquisition modes:

- photon counting: provides only spatial information on the pixel coordinates;
- TOA_TOT_MODE: provides spatial, timing and charge information.

Data-driven photon counting

This acquisition mode is an event-based mode which provides the coordinates of the hit pixels and a photon count for each pixel, with a counter depth of 24 bits. Table 4.7 presents the structure of the data word generated by this acquisition mode, expressing for each of the data field the number of bits used, as well as its position within the data word, between the Most Significant Bit (MSB) and the Least Significant Bit (LSB).

A threshold can be set to tune the minimum number of hits that a pixel must receive before generating a data word.
It must be noted that the actual data word may not be sent out as soon as the threshold is reached since the priority encoder present in the Timepix4 readout architecture may hold the generation of the output data word.
In these cases the counter will be incremented during the additional wait time, thus generating words with a value above the threshold.

Table 4.7: Description of the 24-bit photon counting mode 64 b data word format.

Quantity name	Width [# bits]	MSB	LSB	Description
Top	1	63	63	Top: 1, Bottom: 0
EoC	8	62	55	EoC edge address
SPGroup	4	54	51	SPGroup address
SPixel	2	50	49	SPixel address
Pixel	3	48	46	Pixel address
UNUSED	22	45	24	-
Event Count	24	23	0	Binary counter for PC counter

ToA-ToT acquisition mode

The TOA_TOT_MODE provides the pixel coordinates of a hit, a timestamp (ToA) and the length of the signal (ToT), that can be converted to charge. Table 4.8 presents the structure of the output 64 b data word generated by the ToA-ToT acquisition mode.

Table 4.8: Description of the ToA_ToT mode 64 b data word format and of the information provided by it.

Quantity name	Width [# bits]	MSB	LSB	Description
Top	1	63	63	Top: 1, Bottom: 0
EoC	8	62	55	EoC edge address
SPGroup	4	54	51	SPGroup address
SPixel	2	50	49	SPixel address
Pixel	3	48	46	Pixel address
ToA	16	45	30	ToA coarse value @40 MHz
ufToA_start	4	29	26	UltraFine ToA start code
ufToA_stop	4	25	22	UltraFine ToA stop code
fToA_rise	5	21	17	Fine ToA rise @640 MHz
fToA_fall	5	16	12	Fine ToA fall @640 MHz
ToT	11	11	1	ToT coarse value @40 MHz
Pileup	1	0	0	No Pile-up:0, Pile-up:1

4.10 Time-of-Arrival and Time-over-Threshold measurements

The time-to-digital conversion in the Timepix4 ASIC occurs in three stages [99]. The first stage involves determining the 40 MHz clock cycle in which the preamplifier's output signal crosses the threshold. Once this event is detected, a clock generated by the SuperPixel VCO is activated. This clock operates at a nominal frequency of 640 MHz, providing the fine-Time-of-Arrival (fToA), as illustrated in Figure 4.10a. The clock remains active until the next rising edge of the 40 MHz clock, allowing the number of 640 MHz cycles to provide a more precise ToA measurement, refining the timing resolution from 25 ns to 1.56 ns.
If another signal crosses the threshold in a pixel within the same SuperPixel while the VCO is already active, its fToA is measured using the currently running 640 MHz clock. Furthermore, when the VCO is running, four internal phases of the oscillator are latched by the next rising edge of the 40 MHz clock to subdivide the 1.56 ns bins into eight smaller intervals, each with a nominal width of 195 ps,

delivering the Ultra-fine-Time-of-Arrival (UfToA), as depicted in Figure 4.10b.

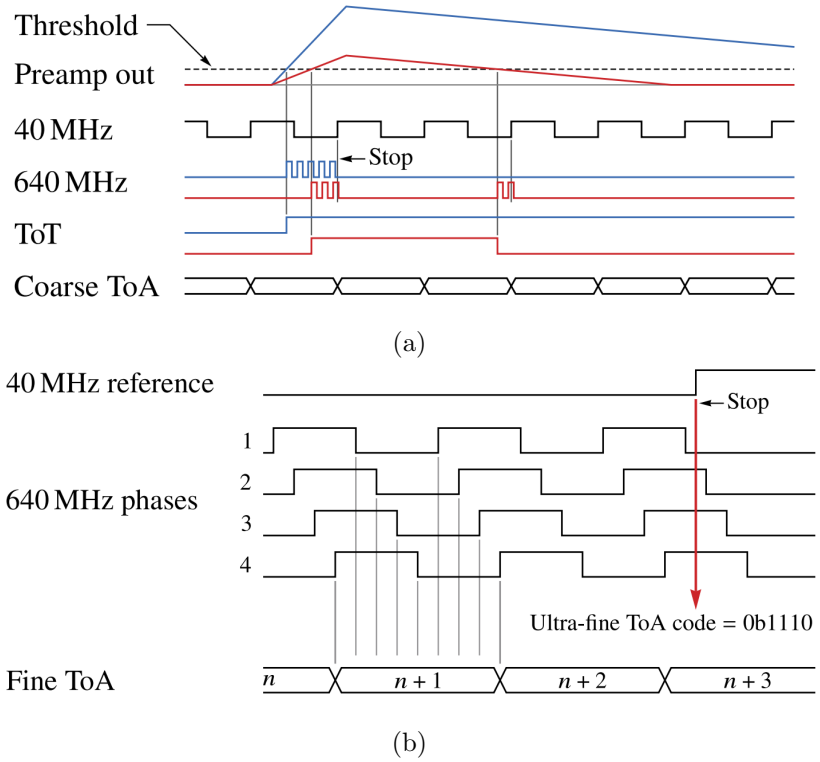


Figure 4.10: **(a)** Operation of the ToA and fToA measurement. **(b)** Copies of 640 MHz clock shifted providing the UfToA measurement [99].

5

Data Acquisition and data analysis softwares

The development of a software to control Timepix4 and read out the data is included in the project, as well as the development of a data analysis framework, where the data packets are decoded and processed, and the analysis is performed.

5.1 DAQ software architecture

The software is required to be very fast and to grant a high-speed readout, in order to match the Timepix4 output bandwidth. Moreover, it must be user-friendly, and allow the possibility to modify tasks and acquisition setup with simple variations of some parameters.
To satisfy the speed requirement, the C++ language has been chosen, being fast and low-level enough to allow complete control of the setup and the output data. The flexibility requirement is satisfied by the choice of an object-oriented paradigm, pursued when developing this software. For each hardware component an independent class has been developed, creating a flexible structure that can be easily adapted to hardware variations. Different setups could be based on different DAQ systems. Using an object-oriented software allows to develop classes for each DAQ system and several communication protocols, preserving the possibility to exploit the Timepix4 and this software for several applications, simply by adapting the

DAQ class to the DAQ system used.
The last requirements for the software is to be user-friendly enough. This is not trivial, since the Timepix4 architecture has hundreds of different registers, which can lead to a large number of possible configurations, but makes more complex its use. It is then necessary to find a compromise between the simplicity of operation and the details that can be reached. Therefore, it has been chosen to grant a very simple use of the Timepix4 for basic operation, without, however, depriving the possibility to perform detailed bit-by-bit changes.

The software structure, presented in Figure 5.1, is divided in two main sections: the slow control and configuration section, linked also to the slow readout, on one hand, and the high-speed readout on the other hand. Both sections are connected to a Command Line Interface, where the user can control the configuration and the readout operations.
The slow control communications are based on the protocol of the DAQ system being used, exploiting a client-server paradigm based on a server running on the board which accepts user's requests.
The fast readout is based on the User Datagram Protocol (UDP), making it independent on the DAQ system type and the DAQ chosen, since the UDP packets are sent directly to the computer.

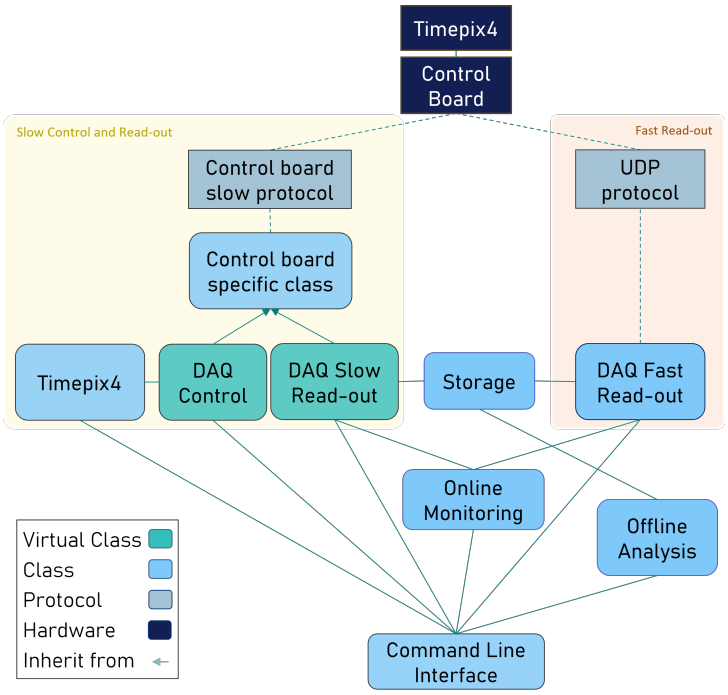


Figure 5.1: Data Acquisition software structure.

The software will allow to adapt to several DAQ systems: a specific custom DAQ system class will inherit the virtual class *DAQControl*.
This class must contain four fundamental methods needed to communicate with the Timepix4: two methods to read a DAQ system and a Timepix4 register, and two methods to write to them, respectively.
What can be done through slow control is based entirely on this *write* and *read* methods.
In addition to the classes meant to configure the Timepix4, the *SlowControlReadout* class is responsible for the data readout through slow control, performing a polling of the 256-bit long TOP and BOTTOM readout registers.
The configuration classes will be described in more detail in Subsection 5.1.1, while the *SlowControlReadout* class is described in more detail in Subsection 5.1.2.

A different protocol is used to read out the 16 high speed serial links. The register polling would be too slow to keep up with the links speed, so a faster "push" architecture is used instead: the DAQ system pushes directly the UDP packets to the PC, without any requests by the client.
That is the reason why this class is not dependent on the specific DAQ system used, and it could be used on different DAQ systems without modifications.
This class contains methods to read out and store data on disk, to allow both online and offline data processing and analysis.
The acquisition class used for the high-speed readout will be described in more detail in Subsection 5.1.2.

5.1.1 Timepix4 and DAQ system configuration classes

This part of the software includes all the classes needed to configure the Timepix4 and the DAQ system.

The *DAQControl* class contains several *Application Program Interfaces (API)* to configure the Timepix4, which are based on the fundamental reading and writing methods; some of them are low-level, managing for example single registers functions, or writing on a single column of pixels, while others are high-level methods such as, for example, the function performing a complete configuration of the Timepix4.

The information needed by the methods of the *DAQControl* class are found in the *Timepix4* and *Typedef* classes, containing structures, enumerations and static methods meant to simplify the APIs and the user applications.
In particular, the *Timepix4* class contains information on the Timepix4 registers and the methods to get information, such as the registers addresses or lengths. Furthermore, it manages dedicated structures to perform a complete configuration

of the Timepix4.
On the other hand, the *Typedef* class contains all default parameters of the Timepix4 registers, and defines the structures where the registers information are memorised.

DAQ control class

The four fundamental methods to communicate with the Timepix4 and the DAQ system are *readTpx4()*, *writeTpx4()*, *read32()* and *write32()*, respectively. Their functioning is dependent on the DAQ system communication protocol, so these functions must be re-implemented in the specific DAQ system class if the DAQ system changes. The only connection between the hardware and the software is represented by this class, so it is sufficient to modify this object to adapt the software to a different DAQ system.

The Timepix4 read function returns a *DAQReplyType* object, which contains the method to convert the reply into *string*, $uint16\_t$, $uint32\_t$, $uint64\_t$ or $vector < uint64\_t >$. The methods are fundamental to convert the bytes received into a more manageable type. This must be chosen accordingly to the length (16, 32 or 64 bits) of the Timepix4 register. The $vector < uint64\_t >$ type is useful for the data readout registers, that are 256-bits long and contains up to four 64-bits data packets.

It is necessary to create an object of the used DAQ system specific class, in order to communicate with it and the Timepix4. Since a board may control more than one Timepix4, any Timepix4 related function requires an ID to send the request to the correct ASIC.

The DAQ class contains also a set of APIs, accessible from any DAQ system class. The low-level classes perform simple operations, for example, the configuration or read out of single registers. The methods used to configure the matrix are part of this group of APIs, allowing the managing of the configuration at a single pixel level.
The mid-level methods configure different registers related to the same specific settings, for example, the methods to configure the clock settings, the DACs output, the acquisition mode or the high-speed links.

Eventually, the high level APIs consist of just two functions, namely *confTimepix4()* and *confThreshold()*.
The first method performs a basic but complete configuration of the Timepix4, including the clock settings, the shutter configuration, the DACs setting, the read-out mode configuration, and if needed the test-pulse configuration.

The DACs setting is managed by the *confTimepix4()*, but the DAC_THR and the DAC_FBK configuration is performed by the second method as well, in order to set the global threshold.

After a complete configuration of the Timepix4, it is still possible to configure specific blocks of the ASIC, using lower-level APIs to fine tune the configuration according to the need.

Timepix4 class

The *Timepix4* class contains helper methods to be used in the configuration and the readout.
For example, its functions can be used to check the writability of a register or to decode a value read from a register.

These methods are static, so they do not need an instantiation, and they can be accessed by any object. This class does not communicate with the DAQ system, and consequently cannot communicate with the Timepix4. As said before, the communication with the hardware is left to the *DAQControl* class only, to keep the software easier for the user.

5.1.2 Data acquisition classes

Once the Timepix4 is configured and the acquisition is running, the data can be read out and saved either through slow control or high speed links.
In each case, a dedicated thread is allocated, allowing to perform other operations with the Timepix4 while reading the data.

Slow control readout

The slow control readout, as said, consists of the polling of the Timepix4 registers dedicated to store the output data, the TOP and BOTTOM PacketRead registers. These registers are 256-bit long, and can contain up to four packets of 64 bits. Thus, using in a loop the basic read function, that is the *readTpx4()* function, could result on time losses and a software slowdown due to a too large number of calls. Therefore, the function *readTpx4Repeat()* has been implemented, reading N times a given register. This method can improve the readout time, reducing the function call overhead and optimizing the data conversion and storage.

The data are not processed and are saved in a raw format, as a stream of 64-bits packets.

The slow control class is dependent on the DAQ system, since it is based on a

register polling. To adapt the readout to a different DAQ system it is sufficient to re-define the basic *readTpx4()* method and, potentially, the *readTpx4Repeat()* one.

Fast readout

A dedicated class has been implemented to perform fast readout, exploiting the 16 high speed links.

Conversely from the slow control readout, this class needs to keep up with much higher data rates. Thus, two dedicated threads are allocated, one to read the data from Timepix4 and the other to store them.
The two threads operate following a reader-writer paradigm on a shared circular array, shown in Figure 5.2. One thread listens to the UDP port, catches the data and writes them in the array; the second thread reads data from the array and stores them in a file.

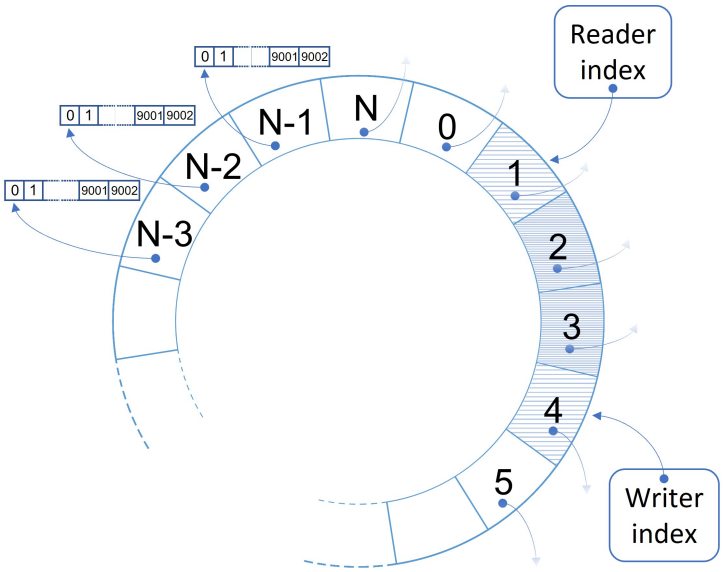


Figure 5.2: Scheme of the circular buffer array used in the fast readout.

The circular array is a small array of char pointers, pointing independently to heap memory areas.
Jumbo frames, which are Ethernet frames with a payload higher than the standard Ethernet frames, are enabled on the DAQ PC, to reduce the overhead and to allow keeping up with the Timepix4 output rate. The maximum dimension of a jumbo

frame is 9000 bytes, so the arrays of char pointers are 9002 long, since 2 bytes are acquired to store the number of bytes actually received.

To ensure the thread safety of the entire structure, there are two mutexes:

- the first mutex keeps track of the element currently read, and avoid that the writer performs operations on the elements currently accessed by the reader;
- the second mutex keep track of the element that is being written, and protects the array accessed by the writer.

The threads interacts just with single elements, without altering the main buffer, so other mutexes are not needed to protect it.

The *fastReadout()* object automatically connects to a UDP port and keeps listening, so it is not dependent on the specific DAQ system used, and there is no need to modify it when a hardware variation occurs.

Online monitoring

Both slow and fast readout allow for an online monitoring of the received data.

This online monitoring is performed by an additional thread which communicates with the readout threads through a shared memory. The readout threads store the data in the shared memory, a part from the store file, and the online monitor thread reads the data from the shared memory and allows for a simple data decoding and analysis.

Online monitor is typically used to quickly extract information on the hits position, their ToT and their ToA.

5.2 Data analysis architecture

A custom data analysis framework has been developed to process the data acquired with the Timepix4, and to exploit them for several applications.
Having a direct control on raw data or on data after a simple decoding has a fundamental role for the debugging, so it is required that the analysis framework has low-level access to the data. At the same time, it also should be user-friendly enough to allow complex analyses and operations to be performed with simple commands. Furthermore, it is required to be built in a modular way, to make it easier to implement and add other classes and objects to extend the analysis to different applications.

Starting from these requirements, the software as been built object-oriented, using C++ language, following the architecture shown in Figure 5.3.

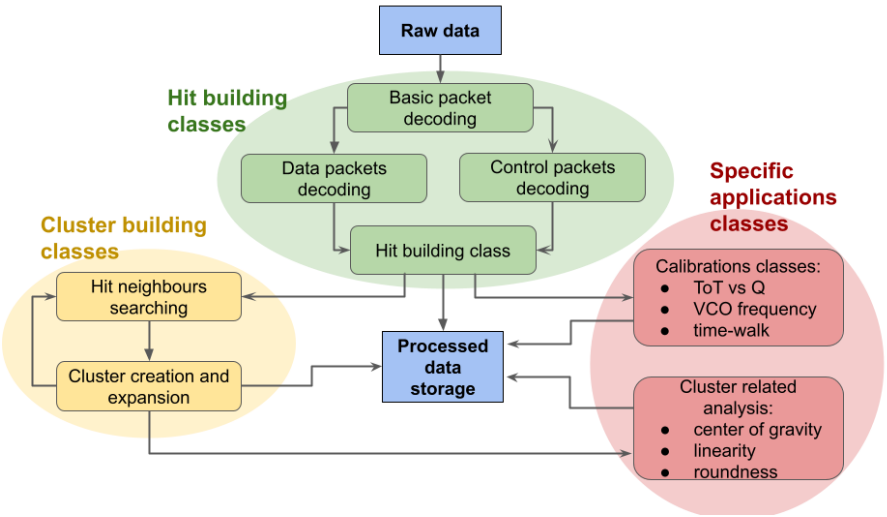


Figure 5.3: Simplified structure of the analysis software classes.

The software consists mainly on three sections:

- data decoding and event building: the bit stream is read from the storage file; a basic decoding is performed, transforming the bit stream into a set of basic information like pixel address, coarse ToA, fine and ultra-fine ToA, and ToT; the hit event is built, decoding the ToA starting from the coarse and fine information and taking into account information external to the data packet, for example the last heartbeat timing;
- data clustering: a density based clustering is performed starting from the hit built in the previous steps, gathering several hits on a single cluster object; various quantities and information related to the clusters, such as the cluster centroid, charge, dimension and a weighted ToA, can be extracted from the cluster object built;
- specific application interface: the methods implemented on the other sections can be used to perform given operations and to store specific quantities on processed file, depending on the particular application chosen by the user.

5.2.1 Data decoding and event building

The packets are decoded differently depending on two main criteria:

- the packet type: the data word format differs from control word format;

- acquisition mode: as explained in Section 4.9, the frame based readout logic and the data-driven readout are very different, leading to a different organization of the packets and data-words. Moreover data words acquired using the TOA_TOT_MODE are different from data obtained in data driven 24-bit photon counting mode, as shown in Subsection 4.9.2.

Packets formats: data and control packets

Timepix4 can be configured to send out different types of control packets, to provide information external to the data and not dependent on the specific source of signal that is being measured, but fundamental to check the correct operation of the Timepix4.
The generic format of a control packet and the information provided are represented in Table 5.1. The control packets can be distinguished looking at the header, that corresponds to the EoC address in the case of data packets. Data packets, describing data coming from the pixel matrix, have an EoC included between 0x00 and 0xDF, while control packets have a header greater than 0xE0.

Table 5.1: Description of the control word format.

Information name	Width [# bits]	MSB	LSB	Description
Top	1	63	63	Top: 1, Bottom: 0
Header ($\geq$ 0xE0)	8	62	55	Ctrl/status header
Segment	3	54	52	Segment address
Data	52	51	0	Ctrl/status data

There are several types of control word that can be sent, summarised in Table 5.2.

In particular, the T0_SYNC is a packet sent when the T0_SYNC command is received, providing a starting time for the acquisition, that can be associated also to a global ToA clock reset. Analogously the SHUTTER_RISE and SHUTTER_FALL are sent when receiving the SHUTTER_RISE or SHUTTER_FALL commands. The HEARTBEAT packet is a packet that can be sent at a tunable frequency to extend the dynamic range of the ToA measurement.

The data packets received in frame-based acquisition are simply counters of 8 or 16 bits for each pixel; more details will be given in Subsection 5.2.1.

The data packets received in data-driven acquisition, regardless from the readout mode used, contain the pixel coordinates in the first 18 most significant bits (MSB), as already explained in Section 4.9.

The TOA_TOT_MODE and the 24-bit PC packets differ on the information provided on the 55 least significant bits (LSB).

Table 5.2: List of possible control packets.

Header (EoC address)	Packet name	Description
0xE0	Heartbeat	Packet with a time stamp sent periodically
0xE1	Shutter_rise	Time stamp of shutter rise
0xE2	Shutter_fall	Time stamp of shutter fall
0xE3	T0_sync	Time stamp of T0_sync
0xE4	Signal_rise	Configurable trigger
0xE5	Signal_fall	Configurable trigger
0xEA	Ctrl_data_test	Continuous stream of packets
0xF0	Frame_start	Data frame start (FB mode)
0xF1	Frame_end	Data frame stop (FB mode)
0xF2	Segment_start	Readout segment start (FB mode)
0xF3	Segment_end	Readout segment stop (FB mode)

Looking again at the structure of the 24-bit PC packets, presented in Table 4.7, among these 55 bits only the lowest 24 are considered, used as a counter of hits in the pixel described by the address.

The information provided by these bits in the TOA_TOT_MODE packets are much more instead, as visible in Table 4.8, and consists of:

- ToA: coarse ToA measurement, expressed in 40 MHz clock cycles (units of 25 ns);
- fToA_rise: fine measurement of the time passed since the signal rised above threshold until the rising edge of the following 40 MHz clock cycle, expressed in 640 MHz (units of 1.56 ns);
- fToA_fall: analogous to fToA_rise, express the time passed since the signal felt below threshold to the next 40 MHz clock cycle rising edge;
- UfToA_start: returns the code related to the fraction of the 640 MHz clock where the signal raised above threshold, as explained in Section 4.10;
- UfToA_stop: similarly to UfToA_start, it returns the 640 MHz fraction where the 40 MHz clock rising edge following the signal rising edge happens, and it is the second component of the ultra-fine ToA measurement;
- ToT: coarse ToT measurement, expressed in 40 MHz clock cycles (units of 25 ns);
- pileup: provides information on pileup events, and has to be considered a

warning for rate exceeding the actual DAQ bandwidth; the pileup bit is '1' when a second event happens on a pixel while the pixel readout is still ongoing.

Data-driven acquisition decoding

The 24-bit PC packet decoding is trivial, since decoding the pixel address and the photon counter is enough.

However, decoding the described quantities of the TOA_TOT_MODE packets is not enough, since it only provides with semi-raw information such as, for example, the UfToA codes. In order to build the hit event, a limited ToA, namely a ToA value which has not been corrected for the ToA clock roll-ove, has to be built as:

$$\begin{aligned} \mathrm{ToA}_{\mathrm{dec,lim}} = (\mathrm{ToA} - (\mathrm{fToA}_{\mathrm{rise}} - (\mathrm{ufToA}_{\mathrm{start}} - \mathrm{ufToA}_{\mathrm{stop}})/8)) \\ /(\mathrm{ratio\_VCO\_CLKDLL} \cdot 640/\nu_{\mathrm{VCO}}) - \mathrm{toa\_clkdll\_c} \end{aligned} \tag{5.1}$$

where ratio_VCO_CLKDLL $= 640\,\mathrm{MHz}/40\,\mathrm{MHz} = 16$ is the ratio between the nominal VCO frequency and the DLL clock frequency, ν_{VCO} is the real VCO frequency, specific for each Super Pixel, and toa_clkdll_c is a correction dependent on the pixel position, related to the delay of the DLL clock provided by the ADB introduced in Section 4.7.

The dynamic range of this quantity is approximately given by the highest number reachable by the 16 bits measuring the coarse ToA with 25 ns clock cycles, thus it is $\sim (2^{16} - 1) \cdot 25\,\mathrm{ns} \sim 1.638\,\mathrm{ms}$, that is sensibly lower than typical acquisition durations. For this reason, the dynamic range has to be extended by taking into account the last heartbeat signal.

It has to be noticed that the dynamic range of the ToT is 51175 ns, setting a maximum limit to the signal amplitude measurable. As it will be shown in Section 6.4, this corresponds to about $300\,\mathrm{ke}^-$.
However, the ToT dependence on charge is not linear on the whole ToT dynamic range. Beside the non-linearity at very low charge, the ToT dependence on the charge remains linear up to about $200\,\mathrm{ke}^-$, while for higher charges it starts to saturate and decrease, defining the so called Volcano effect [100].

Frame-based acquisition decoding

As explained in Section 4.9.1, in the frame-based acquisition the packets are sent out sequentially, describing a complete frame, and therefore they have to be decoded sequentially. They cannot be decoded independently, as happening in the

data-driven acquisitions, because in this kind of acquisition the packet order is fundamental.

The frame and segment information are provided by control packets with the structure presented in Table 5.3.

Table 5.3: Frame and segment control packets structure.

Field	MSB	LSB	Description
Top	63	63	Top: 1, Bottom: 0
Header	62	55	Packet type [frame/segment start/end]
Segment address	54	52	Source segment of the packet
Readout mode	51	50	Counters depth [0b10: 8b; 0b11: 16b]
Unused	49	0	

As explained in Subsection 4.8.1, there are 8 segments on each periphery datapath, 4 on the left side and 4 on the right. Each of these segments manages the packets of 28 double columns, as shown in Table 5.4.
For each segment, the double columns are read out sequentially following the order on each line in Table 5.4.

Table 5.4: Mapping of double columns on different segments.

Segment	Segment address	Double column
L0	0x0	0,4,8,...,108
L1	0x1	1,5,9,...,109
L2	0x2	2,6,10,...,110
L3	0x3	3,7,11,...,112
R0	0x4	112,116,...,220
R1	0x5	113,117,...,221
R2	0x6	114,118,...,222
R3	0x7	115,119,...,223

Between a Segment_start and a Segment_end packets, a data packet per SuperPixel is read out, as explained in Subsection 4.9.1. These packets don't provide information on the pixel address. Instead, this information can be obtained from the packet position, since the pixels within the 28 double column read by the same segment are read out sequentially.

5.2.2 Data clustering

Most of the particles interact with the detector by depositing energy in several neighbouring pixels, leaving traces with characteristic shapes depending on the interaction mechanism between the particle and the material. Therefore, it is

mandatory to implement a clustering algorithm to give an adequate interpretation of the events observed and to correctly extract physics information.

The choice of the clustering algorithm must be taken by considering the kind of events expected, their rate and the way particles interact with the detector. As said, the analysis framework is initially meant to be useful in the debugging phase, where assemblies bonded to Si detectors have been used.
A simple spatial and timing cut could not be precise enough, since close clusters may be cut or gathered together erroneously. The cluster shape cannot be a useful information either, since there are too many possible cluster shapes among photons, β particles, α particles or muons interacting in the sensor.
A characteristic common to the different clusters is the timing distance between adjacent pixels belonging to a common cluster, depending only on the intrinsic charge collection time of the detector used and on the intrinsic time walk of the pixel. In a $100 - 500\,\mu m$ Silicon detector thick this quantity is of order of tens of nanoseconds. Conversely, different timing ranges are covered by clusters generated by different detected particles: in a $100 - 500\,\mu m$ silicon detector thick this quantity is of order of tens of nanoseconds for minimum ionizing particles, or hundreds of nanoseconds for highly ionizing particles [101, 102]. Such a dynamic range is much lower of the highest rate reachable by a pixel. This lead to choose a density based algorithm for the clustering, in particular the so called Density Based SCAN (DBSCAN) algorithm.

Density Based Scan (DBSCAN) algorithm

The DBSCAN algorithm [103] is an algorithm used to partition data points and gather them into clusters based on the distance between them. It consists of looking for neighbors of a given hit based on a distance set in the interested phase space, and to build the cluster by looking for neighbors of the hits already labeled as part of the cluster.

The algorithm depends on two main parameters:

- a radius ϵ, defining the distance between two points to consider them neighbors;
- the minimum number of neighbors points m that a point must have to be considered a *core point*, namely, a point from which a cluster construction is began or extended.

Once these two parameters have been defined, accordingly to the application's requirements, the core point can be recognised.
Among them, one is randomly selected to start the first cluster. All the neighbors

of this first core points are included in the cluster; if among these points there are other core points, their neighbors are added to the cluster as well, until no more core point can be added to the cluster.
After the first cluster has been completed, another core point is randomly selected, and a new cluster is started.

Repeating this process allows to cluster the data according to their density in an arbitrary space. However, due to the sequential structure of the algorithm, it has to be noted that non-core points are assigned to the first cluster meeting the distance requirements, not necessarily to only one.

This algorithm is very adaptable to different applications, since any phase space can be used to perform the clustering, provided a suitable distance definition for that space.
Thus, correctly tuning its parameters is fundamental to optimize the clustering results.

In particular, it has been adapted to the Timepix4 output data by defining a maximum spatial distance and a maximum timing distance to decouple the two quantities. Hits belonging to the space within the maximum spatial and timing distances, centered on a given hit, are considered its neighbors.
A particle can deposit energy along a diagonal direction, so at least a distance $d_{sp} = \sqrt{2}$ pixels has to be considered as maximum spatial distance. To take into account the possible presence of masked pixels, this distance is increased to $d_{sp} = 2 \cdot \sqrt{2}$.
Regarding the timing distance, it has been chosen to be large enough to surely include all the hits related to a cluster, but low enough to avoid the possibility of multiple clusters uniting. At the same time, it should not be too low with respect to the acquisition duration, to avoid a too great increase of the number of timing slices defined to search for neighbors. Thus, a good compromise for the setup used to characterize the Timepix4 is hundreds of ns or a few µs.

Moreover, this algorithm grants an high flexibility, which allows to adapt it to different applications by simply changing the spatial and timing maximum distance parameters. For example, if a reference signal is provided on a corner of the matrix, it can be associated to a cluster simply by increasing the spatial parameter in order to cover the entire matrix when looking for neighbors of an hit, including then the reference signal too.

6

Timepix4 characterization

A detailed characterization of the Timepix4 ASIC, especially in terms of timing resolution, is necessary to correctly assess the performance of the MCP-based hybrid photon detector. In this chapter the steps needed to characterise a Timepix4 assembly are presented, including basic ASIC diagnostic, equalization and calibration procedures, and timing and energy resolution estimation.

The work presented in Sections 6.3, 6.4, 6.5, 6.6 and 6.7 has been published recently [104], except for Subsection 6.5.1, which is part of a previous work [99]. Besides, the measurements and analysis presented in Section 6.8 are part of a different work, recently published as well [105, 106].

6.1 Basic Timepix4 diagnostic

At first, a diagnostic of the basic operation of the Timepix4 has been implemented, in order to test the correct digital operations of the pixels, the correct propagation of the DLL reference clock across the double columns, the operation of the global voltage and current DACs, and the stability of the power supply and DACs outputs in different columns. The presented diagnostic measurements have been performed on a Timepix4_v2 assembly.

6.1.1 Digital test

The objective of this test is to check that the Timepix4 registers are working properly, and that the values assigned to them are correctly written.
To do that, the idea is to write a certain value on the pixel configuration register, and to read it back.
Each pixel has a 8-bit long configuration register, as shown in Table 6.1.

Table 6.1: Bits structure of a single pixel configuration; each pixel is configured through a single byte, allowing to set the local threshold shift, the pixel powering and its masking, as well as the transmission of testpulse generated in the center periphery and transported along the double column.

Bits position	Name	Reset value	Description
[0:4]	dac_bits	5'b00000	Pixel level threshold trim
5	power_enable	1	0: pixel power disabled; 1: pixel power enabled
6	tp_enable	0	0: test pulse disabled; 1: test pulse enabled
7	mask_bit	0	0: pixel un-masked; 1: pixel masked

The maximum value writable on a register of 8 bits is 255, so for each pixel a random integer between 0 and 255 has been selected, obtaining an array of 448×512 integers. This random configuration is written on the pixel matrix, then it is read two times and compared bit-a-bit with the original random configuration, obtaining a map of the pixels not working properly, as shown in Figure 6.1.

A deeper test of the correct reading/writing operation is done by repeating an analogous procedure on each register of the Timepix4.

6.1.2 DLL clock configuration and ADB bypass

The reference clock is distributed to the pixels of a double column exploiting a DLL mechanism: the clock entering the double column from the central periphery and the clock coming out from the double column must always differ by 25 ns, as explained in Section 4.7. The double column comprises 32 ADBs; in each SPG there is an ADB which propagates the clock from the edge periphery to the center, and one propagating it backwards. These ADBs tune the delay added to the clock in order to correctly propagate it.

When the DLL locks, the DLL lock codes are fixed at a certain number depending on the difference between the IN and OUT clock. Higher is the delay added across

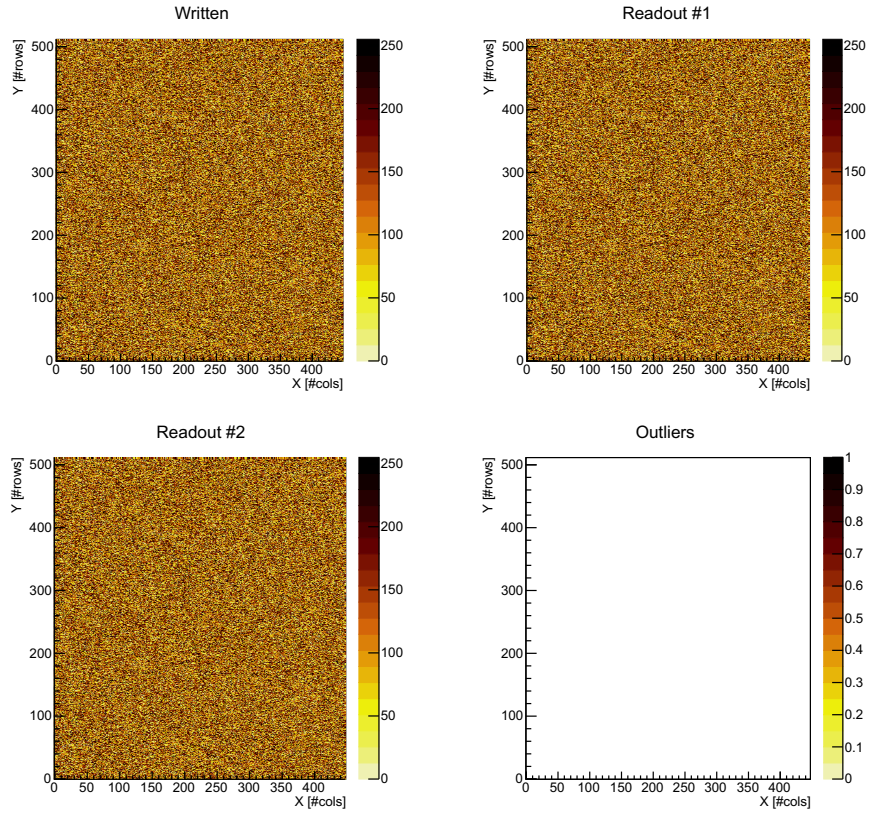


Figure 6.1: Comparison between a random bit configuration written on each pixel and the configuration read out two times to test the correct digital operation of the pixel registers.

the double column, and lower is the DLL lock code. A first diagnostic test consists of scanning these codes for all the double columns. The resulting distribution, shown in Figure 6.2, can be representative of the power supply distribution as well. A higher power supply would cause the ADBs to add a lower delay, increasing the DLL lock code.

In order to achieve excellent timing performances, it is required that the phases of the reference clock across the column are well distributed. If an ADB is not working properly, it could cause the phase after it to be corrupted. To keep this effect under control, the same scan described right above is repeated 32 times, bypassing each time a different ADB. A lock code too different from the average lock code of that double column, when bypassing other ADBs, indicates that the interested ADB is corrupting the phase and it is not working properly.

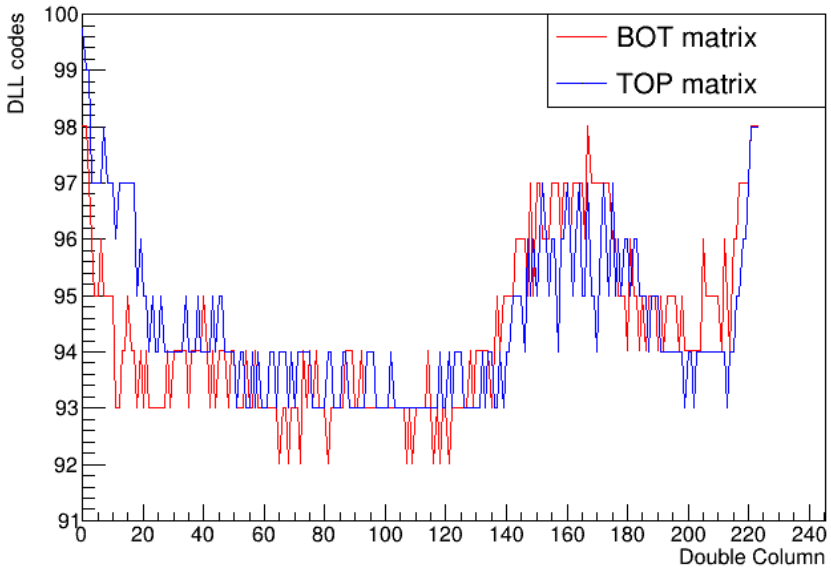


Figure 6.2: Double column DLL (dDLL) locking codes distribution for both the half matrices.

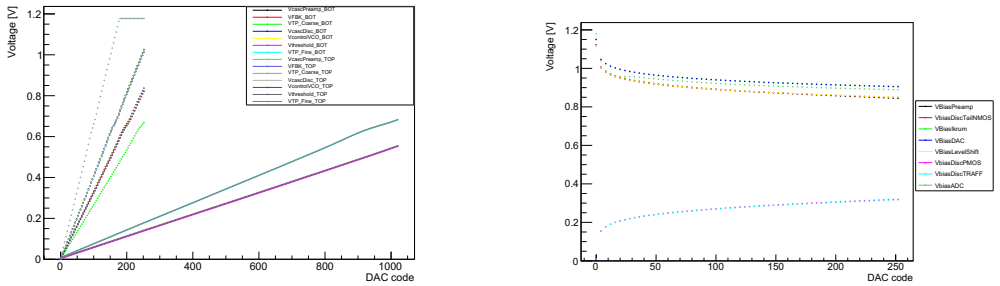
6.1.3 DACs scans

The current and voltage DACs in the central periphery are fundamental for the correct operation of Timepix4, as shown in Section 4.6. In order to test their correct functioning, for each of them a scan is done covering the complete range of possible values, and reading the set voltage through an internal or external ADC.

While doing this operation, the pixels are kept without power, in order to avoid a resistive drop of the voltage in the output of the DACs.
The voltage is measured right after the DACs output, before the pixel load.

The voltage DACs trends are shown in Figure 6.3a. The voltage can be tuned through two different registers, one selecting the DAC value, and the other defining the DAC gain. Flat or not-linear trends indicate some defects on the DAC under test.

The measured voltage trend for the current DACs, shown in Figure 6.3b, is not expected to be linear, differently from the voltage DACs ones. Indeed, in this case it is the current trend to be linear, while the voltage one depends on the response of either the NMOS or PMOS transistor, depending on the DAC, where the current enters.



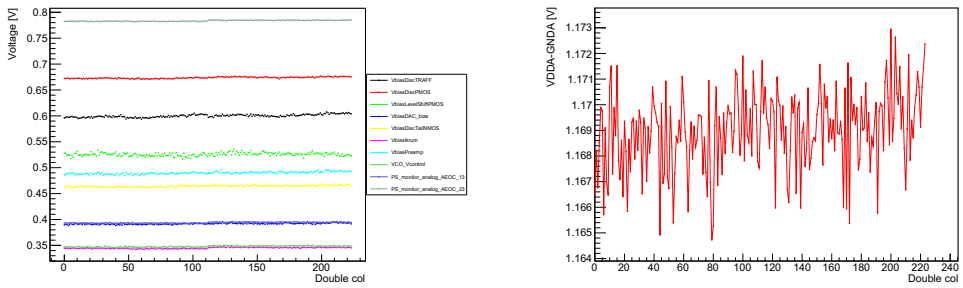
(a) (b)

Figure 6.3: Output voltage dependence on the DAC code set on **(a)** voltage DAC scan and **(b)** current DAC scan. The output voltage is measured right at the DAC output with the pixels not powered, to avoid voltage drops.

To test the stability of the voltage produced by the DACs on different double columns, a fixed value is selected for each DAC, and the pixels are powered. Measuring the voltage after the pixel load, near the edge periphery, gives an indication on possible broken pixels across the matrix which generate drops or peaks on some voltages generated by the DACs.
On the contrary, flat trends like the one shown in Figure 6.4a shows that the voltages are uniform and there are no anomalies in the double column.
The measurement of the voltage measured by the power supply monitor analog EoC can provide an estimation of the analog power supply, called VDDA, as shown in Figure 6.4b.

6.2 Threshold equalization

Different pixels are expected to have different front end responses, e.g., different gain, different noise or different signal baseline. The threshold equalization is mandatory to avoid excess of noise in some pixels, due to a threshold set to low. The Timepix4 achieves a low equivalent noise charge ($\sim 80\,e^-$) per pixel. This, combined with minimal threshold dispersion after equalization, enables the setting of a low threshold across nearly the entire ASIC, with only a few noisy pixels requiring masking [77]. The idea of the equalization is to use a 5-bit DAC on each pixel to shift the global threshold set by the DAC_THR in the central periphery, defining a local threshold.
There are several different methods to equalize the matrix; in particular, two methods among them appeared to be particularly stable and precise: the first method is a data-driven equalization based on the minimum noise level, while the latter is a frame-based equalization based on the maximum noise level.



(a) (b)

Figure 6.4: **(a)** Current DAC output voltage distribution on each analog EoC of both matrices. The voltage is measured on the analog EoC after the resistive drop due to the current drain by the powered pixels, to test the correct voltage distribution across each double column. **(b)** Analog power supply VDDA estimated from the measurement of the voltage of the Power supply monitors measured on each analog EoC.

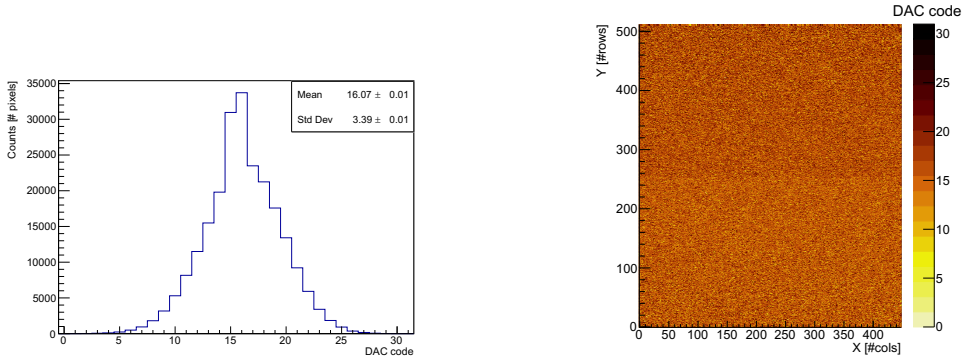
6.2.1 Data driven equalization

The method based on the minimum noise level is applied by operating the Timepix4 in data-driven mode, performing acquisitions with the 24-bit photon counting mode.
The idea is to measure, for each pixel and each local threshold shift set with the 5-bit DAC, the global threshold values at which the pixel starts to count signals, measuring for each shift DAC value the global threshold level at which the noise is reached. Afterwards, for each pixel, the local threshold shift which allows to set the global threshold closest to zero before reaching the noise level is selected. This idea is applied by selecting a certain local DAC shift value and a global threshold value; a short measurement is performed (typically 200 µs), and if a pixel has detected a certain number of hits, the data are registered, the global threshold set is register as noise level for that pixel when using the particular threshold shift set in the DAC, and the pixel is masked for the following scan. Then this scan is repeated varying the global threshold on a predefined range and keeping the local DAC shift value. Once this procedure has been repeated for each local DAC shift value, the local shift with the noise level closest to zero is selected for each pixel.

6.2.2 Frame based equalization

The second method consists of setting the global threshold in the maximum noise condition, and looking for the local DAC shift code corresponding to the max-

imum noise for each pixel. The voltage of the DAC_THR and the one of the DAC_FBK are kept equal, equivalent to set the threshold to an effective value of $0\,e^-$, in order to generate the maximum noise. To avoid rate issues related to the high noise, the measurements are performed using the frame based readout and keeping the shutter open for just 200 µs.
For each local DAC shift value the photon counting is registered for each pixel. When all the DAC shift values have been scanned, on each pixel the shift corresponding to the minimum number of photon counted is selected.
Such a method is much faster than the one based on the data-driven acquisition, and much more stable. The distribution of the DAC codes is shown in Figure 6.5.



(a) (b)

Figure 6.5: Mono-dimensional **(a)** and bi-dimensional distributions of the dac codes set to shift the threshold at a pixel level, resulting from the frame based equalization.

6.3 Voltage-Controlled Oscillator frequencies calibration

It has been observed that the different VCOs were oscillating at different frequencies. This effect can be quantified by studying the following quantity:

$$\mathrm{ufToA_{cycle}} = \mathrm{fToA_{rise}} \cdot 8 + \mathrm{ufToA_{stop}} - \mathrm{ufToA_{start}} \tag{6.1}$$

where $\mathrm{fToA_{rise}}$, $\mathrm{ufToA_{start}}$ and $\mathrm{ufToA_{stop}}$ are the fine and ultra-fine corrections of the ToA described in Section 4.10. Figure 6.6 represents a simplified schematic of the $\mathrm{fToA_{rise}}$ and ufToA codes measurements. The $\mathrm{fToA_{rise}}$ is the number of 640 MHz clock cycles between the discriminator output rising edge and the following 40 MHz clock cycle rising edge. The $\mathrm{ufToA_{start}}$ and $\mathrm{ufToA_{stop}}$ codes are obtained as shown in Figure 4.10b, from the discriminator output rising edge and

the following 40 MHz clock cycle rising edge, respectively. Since the the 640 MHz clock generated by the SuperPixel is activated only when a signal is detected in one of the pixels composing the SuperPixel, as said in Section 4.10, the $\text{ufToA}_{\text{start}}$ value is always equal to 0 for the first hit measured in a SuperPixel, and it can be different from 0 only if a second hit is detected on the same SuperPixel before the following 40 MHz clock cycle.

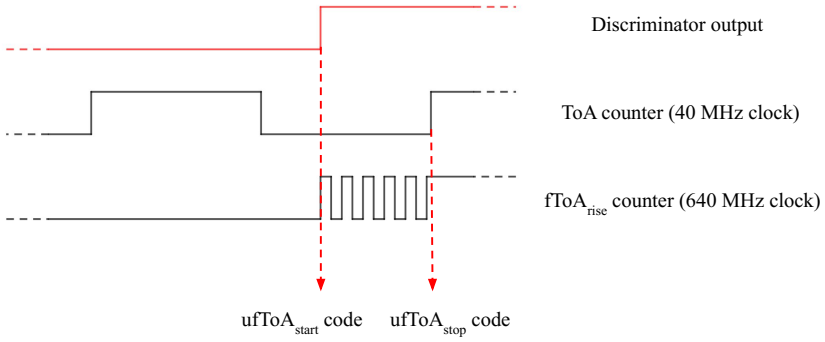


Figure 6.6: Simplified clock schematic of the $\text{fToA}_{\text{rise}}$ and ufToA measurements [104].

The quantity defined in Equation (6.1) represents the number of ultra-fine bins that would fit between the discriminator output rising edge and the rising edge of the next 40 MHz TDC clock cycle.
The corresponding histogram allows to estimate the range of $\text{ufToA}_{\text{cycle}}$ correlated to each TDC, as shown in Figure 6.7.

This range covers a period of 25 ns, depending only on the stability of the 40 MHz clock.
Thus, in nominal conditions, i.e., the VCO oscillating at $\nu_{\text{VCO}} = 640\,\text{MHz}$, this range would be

$$\text{range}(\text{ufToA}_{\text{cycle}}) = 8 \cdot \text{nbins}(\text{fToA}) = 8 \cdot \frac{\nu_{\text{VCO}}}{\nu_{\text{refclk}}} = 8 \cdot \frac{640\,\text{MHz}}{40\,\text{MHz}} = 128 \qquad (6.2)$$

Measuring this range on different pixels proves that different VCOs oscillate at different frequencies.
If the frequency is not properly accounted for, both the ufToA and fToA bin widths will be inaccurately estimated. This can lead to significant errors, especially when

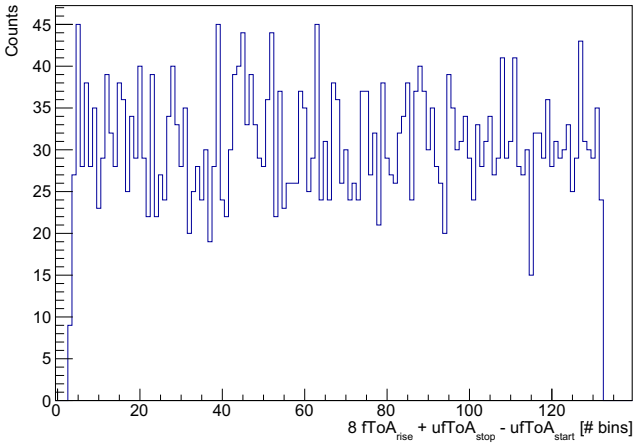


Figure 6.7: $\text{ufToA}_{\text{cycle}}$ distribution obtained measuring laser pulses on a single pixel [104].

the signal's rising edge occurs far from the next reference clock rising edge (when the VCO stops). In such cases, a large number of fToA and ufToA bins contribute to the measurement, and the bin width error must be considered for each one of them.
For instance, if the range of $\text{ufToA}_{\text{cycle}}$ is 131 instead of 128, inverting Equation (6.2), yields a VCO frequency of 655 MHz, resulting in a ufToA bin width of 191 ps instead of 195 ps. A signal measured on the $\text{ufToA}_{\text{cycle}}$ bin number 3 would be measured with a decoded ToA error of just $\epsilon_3 = \text{ToA}_3 - \text{ToA}_3^* = 3 \cdot 4\,ps = 12\,\text{ps}$, but the error on a signal measured on the bin 131 would be $\epsilon_{131} = \text{ToA}_{131} - \text{ToA}_{131}^* = 524\,\text{ps}$.

Therefore, it is essential to measure and calibrate the frequency for the TDCs across the entire matrix. To carry out this calibration, internal digital test pulses have been transmitted to one pixel for each TDC to measure the VCO frequency.

The internal test pulse is synchronised with the 40 MHz reference clock, allowing to set its phase ϕ with respect to this clock. By fixing the phase in relation to the clock, the populated $\text{ufToA}_{\text{cycle}}$ bin does not vary. On the other hand, by varying the phase, different bins are populated, defining pairs $(\phi, \text{ufToA}_{\text{cycle}})$.
The 16 pairs $(\phi, \text{ufToA}_{\text{cycle}})$ have been fitted with a linear function $\text{ufToA}_{\text{cycle}} = \text{p}_0 + \text{p}_1 \cdot \phi$, as shown in Figure 6.8. The slope p_1 [Hz] is associated to the VCO frequency through the relation

$$\nu_{\text{VCO}} = \frac{\text{p}_1}{8} \tag{6.3}$$

where the coefficient 8 represents the ratio between the width of the fToA bins and that of the ufToA bins.

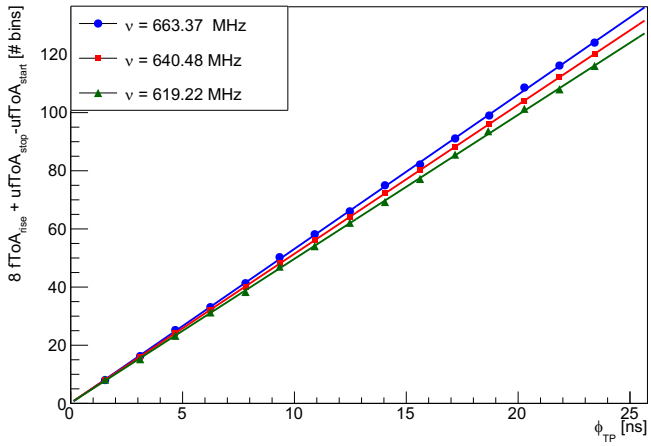
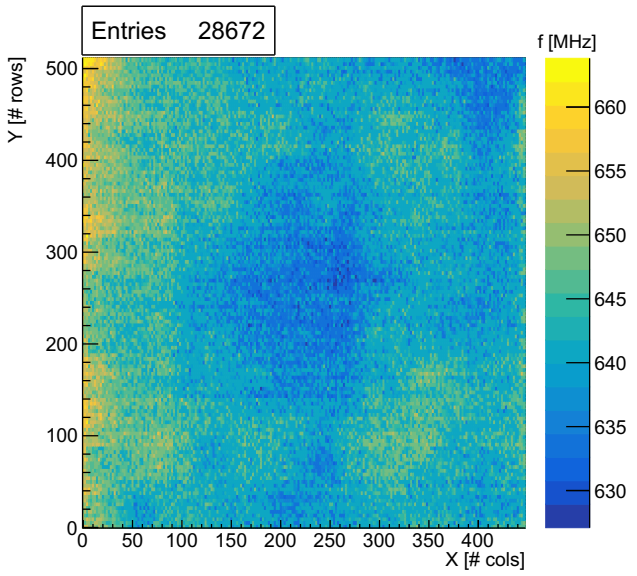


Figure 6.8: $\text{ufToA}_{\text{cycle}}$ dependence on VCO for different pixels [104].

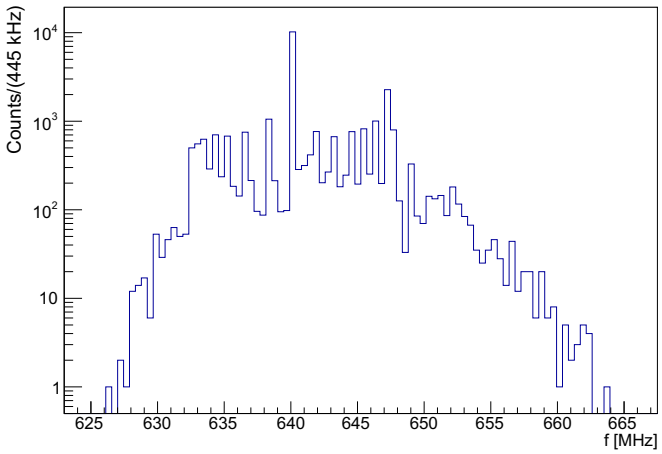
By measuring this frequency for each TDC a map of the VCO frequencies has been produced, as shown in Figure 6.9a.

In Figure 6.9b it can be observed that the frequency distribution peaks at the nominal frequency of 640 MHz, but spans a range of approximately $\sim$ 40 MHz. The circuit allows for adjusting the VCO frequency within a range of about $\sim$ 20 MHz, so it would not be possible to perform measurements adjusting all the VCOs in order to make them run at the same frequency. However, this discrepancy will not pose a significant issue, as correcting their contributions during offline analysis will maintain the timing resolution, as outlined in Subsection 6.5.4.
The Timepix4 on-pixel TDC's VCO frequency is locked by a PLL running with the same VCO placed at the center of the chip. The distributed control voltage suffers from local GND reference mismatch due to internal power supply drops. In Figure 6.9 is reported an indirect measurement of the internal digital power supply which corresponds approximately to $\sim 1\,\text{mV/MHz}$.

A second calibration method has been recently developed.
It consists of noise based measurements aimed at populating the $\text{ufToA}_{\text{cycle}}$ histogram for each pixel, in order to compute the $\text{ufToA}_{\text{cycle}}$ range with a direct measurement.
This method has the advantage of including the complete front-end chain, taking into account all the contribution given by the analog front-end, which are bypassed when digital test-pulses are injected. Moreover, it allows to avoid possible con-



(a)



(b)

Figure 6.9: VCO frequency bi-dimensional **(a)** and mono-dimensional **(b)** distribution over the whole matrix [104].

tributions due to the synchronization between the TDC clock and the test-pulse clock.
The results indeed seem to be more stable and precise than the ones obtained with the test-pulse based method, but further studies are ongoing to select the best method.

6.4 Charge calibration against Time-over-Threshold

A per-pixel calibration of the Time-over-Threshold (ToT) measured against the deposited charge has been conducted across the entire matrix using the Timepix4's internal analog test pulse [107, 108, 109]. This test pulse is a signal with a known and selectable amplitude injected into a capacitor located at the input of the front-end chain. This setup allows the injection of several pulses carrying different charges on each pixel. While the capacitances can vary by approximately 1 % across different pixels, they have been assumed to be equal for calibration purposes, which may slightly affect the calibration performance. The ToT exhibits a non-linear dependence on the deposited charge [107, 108, 109], so for each pixel, the pairs $(\mathrm{ToT}, \mathrm{Q})$ have been fitted using the function:

$$\mathrm{Q}(\mathrm{ToT}) = \mathrm{p}_0 + \mathrm{p}_1 \cdot \mathrm{ToT} - \frac{\mathrm{p}_2}{\mathrm{ToT} - \mathrm{p}_3} \tag{6.4}$$

where Q is in ke^- and ToT is in ns. Figure 6.10 displays the measured ToT calibration for a pixel, along with the overlaid fitting function. The maximum injected charge corresponds to approximately $14\,\mathrm{ke}^-$ due to test pulse saturation with the specific DAC parameters used in this measurement, presented in Table 6.3.

By repeating this procedure across all Timepix4 pixels($\sim$ 230 thousands) a bi-dimensional distribution of the fit parameters has been obtained, enabling a per-pixel calibration that spans the entire matrix. For instance, Figure 6.11 illustrates the distribution of the p_1 parameter across the matrix. A distinct structure arising from the gain differences between the top and bottom halves of the matrix is clearly visible, along with vertical patterns indicative of varying behaviours among the different double columns.

A validation of the resulting calibration has been obtained by measuring the X-rays spectrum produced by ^{241}Am and ^{137}Cs sources, which were used simultaneously irradiating the entire detector matrix from a few cm distance. The measurements have been carried out using a Timepix4_v2 assembly bonded to a 100 µm thick n-on-p planar silicon detector, described in more detail in Subsection 6.5.2, biased at $-150\,\mathrm{V}$. All pixels, except for the noisy ones, have been enabled

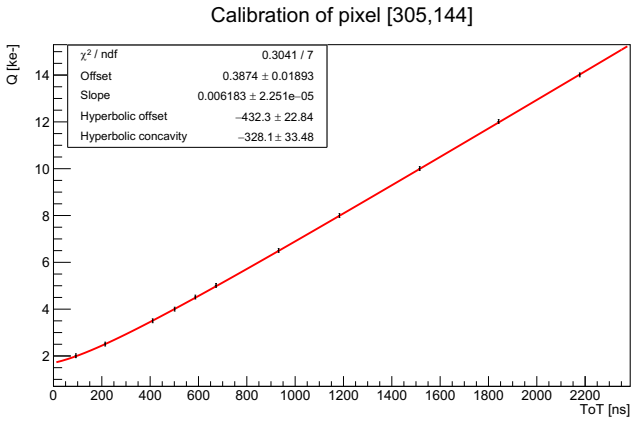


Figure 6.10: Example of the charge non-linear calibration against ToT of a single pixel [104].

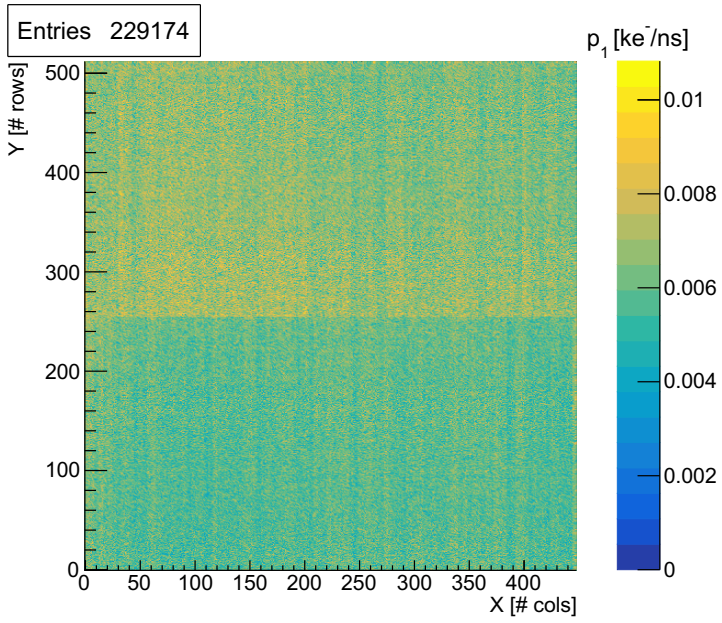


Figure 6.11: Example of the fit parameter p_1 distribution over the matrix [104].

and irradiated, as shown in Figure 6.12e. The injected charge expressed in ke^- is converted in keV when using the sources by multiplying by a factor $3.6\,eV/e^-$, which is the average energy required to produce $e-h$ pairs in Si. The enhancement in resolving power provided by the per-pixel calibration is clearly evident in the difference between the uncalibrated cluster ToT spectrum (Figure 6.12a) and the energy calibrated one (Figure 6.12b). The peaks of ^{241}Am at 13.9 keV, 17.8 keV, 20.8 keV, 26.35 keV and 59.5 keV are well resolved and their energy is accurately estimated, as well as the ^{137}Cs peak at 32.0 keV. Figures 6.12c and 6.12d show a spectrum comparison based on the cluster size considered, for the entire spectrum up to 70 keV and specifically for the peak at 59.54 keV, respectively. An offset is observed between the peaks corresponding to single-pixel clusters and those associated with two-pixel clusters, attributable to a small calibration error introduced by the uncertainty in the capacitors used to convert the test pulse DAC voltage into charge for each pixel.

Table 6.2 summarizes the energy values corresponding to the measurements from the radioactive sources: it presents the expected energies of the measured peaks, along with the measured values and the full-width-half-maximum (FWHM) values derived from the Gaussian fit used to extract these measurements.

Table 6.2: Measured energy of ^{137}Cs and ^{241}Am main emissions compared with expected energies, considering all clusters [104].

Nuclide	$\mathbf{E_{expected}}$[keV]	$\mathbf{E_{measured}}$[keV]	$\mathbf{FWHM_{measured}}$[keV]
Np Lα	13.9	14.3	1.6
Np Lβ_1 + Np Lβ_2	17.7	17.8	2.0
Np Lγ_1	20.7	21.3	2.4
^{241}Am	26.3	26.5	2.6
Ba Kα_1 + Kα_2	32.0	32.0	2.7
^{241}Am	59.5	59.4	4.7

6.5 Timing resolution measurement

6.5.1 Previous timing resolution measurements

Measurements prior to this thesis work have been performed to asses the Timepix4 timing resolution, in particular, to estimate the contribution due to the digital front-end and the contribution due to the analog front-end jitter. To estimate the digital front-end contribution, the TDC bins sizes have been measured by sending external test pulses through the digital pixels [99]. The principle of the measurement is to send pulses with a frequency of 100 Hz, synchronised and delayed

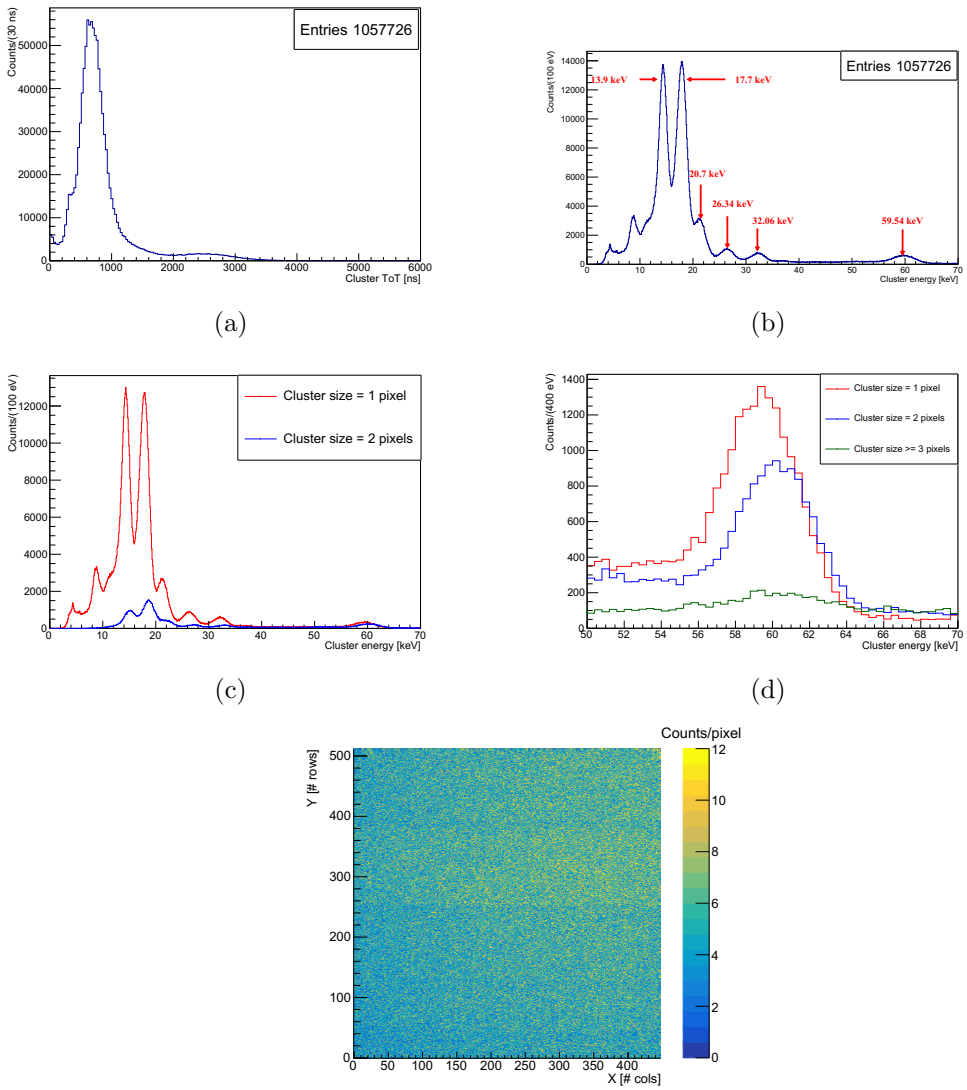


Figure 6.12: **(a)** ^{241}Am and ^{137}Cs ToT spectrum measured on the entire matrix, considering all clusters [104]. **(b)** ^{241}Am and ^{137}Cs energy spectrum measured on the whole matrix after the per-pixel calibration, considering all clusters [104]. **(c)** Comparison of the calibrated spectrum due to 1-pixel clusters and 2-pixels clusters [104]. **(d)** Comparison of the peak at 59.54 keV resulting from clusters with size 1, 2 or greater [104]. **(e)** Hitmap of the events measured irradiating the matrix with ^{137}Cs and ^{241}Am [104].

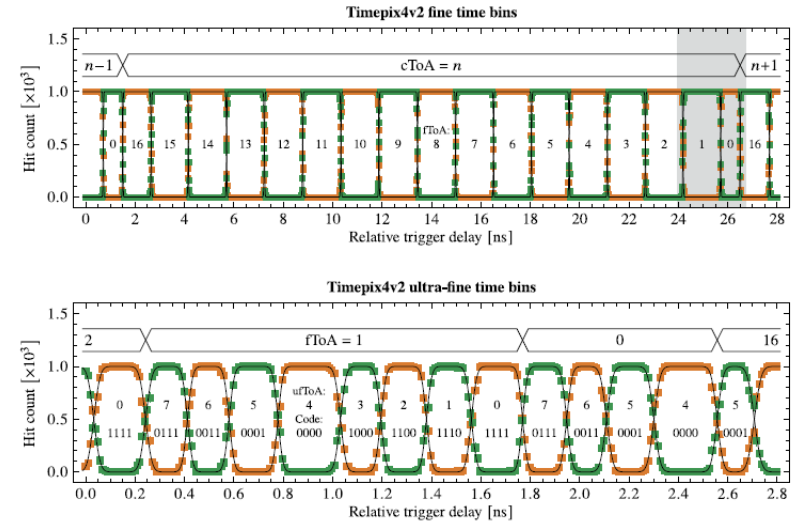
with respect to the external reference clock of 10 kHz. The external pulses delay is settable with a precision of 10 ps, so it is possible to populate the complete ToA clock cycle of 25 ns with a step of 10 ps, being able to discriminate among the fToA bins and the ufToA bins as well. For example, considering the fToA bins, for each delay set on the test-pulse the number of events measured on an even fToA bin and the number of events measured on an odd fToA bin have been extracted, resulting in the plot in Figure 6.13a. Fitting these plots with error functions the width of each bin has been obtained. As presented in Figure 6.13b, the average fToA bin dimension is $w_{fToA,TOP} = 1.583$ ns for the TOP matrix and $w_{fToA,BOTTOM} = 1.547$ ns for the BOTTOM one, while the ufToA width is about $w_{ufToA} \sim 195$ ps. Both of these results are compatible with the nominal values.
A similar measurement has been performed sending internal digital test pulses. These are synchronised with the reference clock entering the DLL columns, so the ADBs on the DLL column have been exploited to precisely shift the reference clock at the end of the column. Only the first 4 ADBs have not been bypassed, and this made possible to generate a shift between the testpulse and the reference clock with a precision of 1 ps, making possible to measure the ufToA bin sizes with higher precision [99].

On the other hand, a measurement of the analog front-end jitter has been performed using the analog internal test pulse tool [99]. This measurement consists of sending pulses corresponding to different charge values, considering the ToA clock rising edge as the reference timing, since the test pulse is synchronised with it. Sending the pulses at different charge values allows to extract the jitter trend dependence on the ToT.
This measurement has been performed both on bare and bonded assemblies, configuring them both in electron-collecting mode or hole-collecting mode.

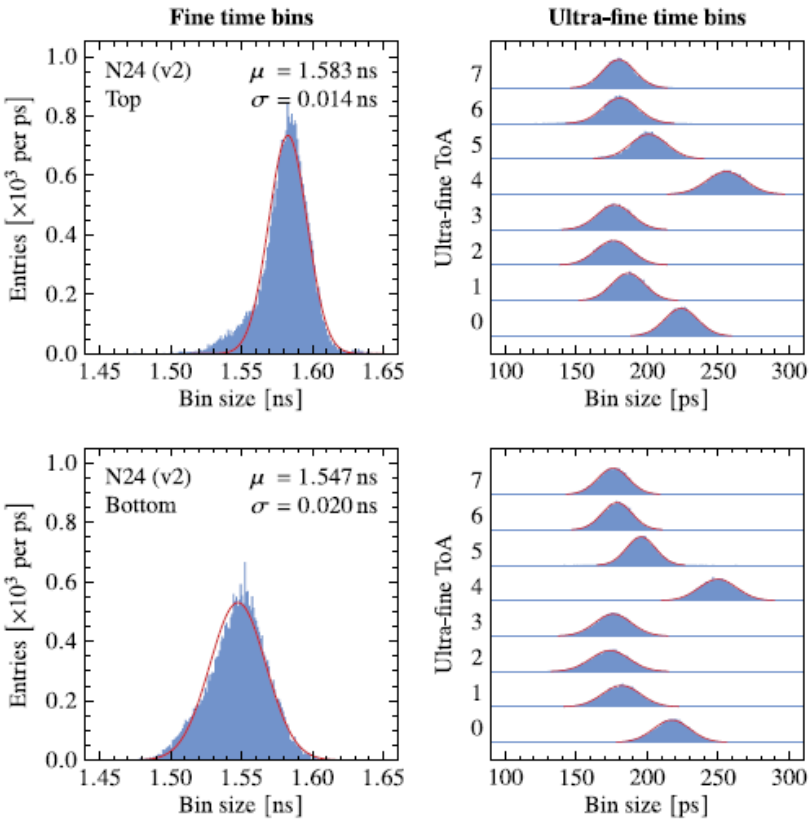
Configuring the chip in hole-collecting mode the jitter presents an asymptotic trend at about $\sim$ 100 ps, both on bare ASICs and bonded ones, as shown in Figures 6.14. Bonded sensors present a worst resolution at low charges.

On the other hand, configuring the ASIC in electron-collecting mode, no asymptotic trend appears, and the resolution can reach below 50 ps both with bare and bonded assemblies.

Indeed, when a pulse is received from a positive polarity sensor, the PMOS input transistor M_0 shown in Figure 6.15 is closed during the input signal first edge; hence, the decoupling capacitor M_0 discharges through the current source, as shown in Figure 6.15b, causing the slope of the voltage signal to be limited to $\frac{dV}{dt} = \frac{KI_{bias}}{C_0}$, which lead to a plateau in the jitter.
Conversely, when a pulse is received from a negative polarity sensor, the M_0 is



(a)



(b)

Figure 6.13: **(a)** Hits received by each fToA and ufToA bin as a function of the external test pulse delay [99]. **(b)** Distributions of fToA and ufToA bins sizes [99].

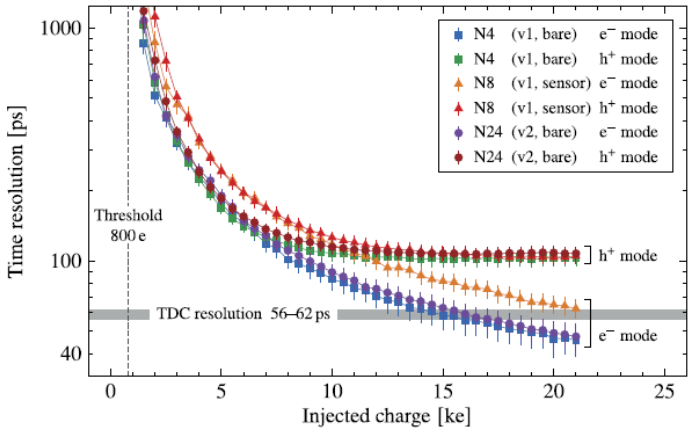


Figure 6.14: Timing resolution of the analog front-end as a function of the charge injected with the analog test pulse tool provided in Timepix4 [99].

open during the input signal first edge, and the C_0 capacitor is charged with a charging time depending on M_0 bias voltage, as shown in Figure 6.15a, which in turn depends on the signal amplitude; thus, since the charging time is not constant, there is no slew rate limitation.

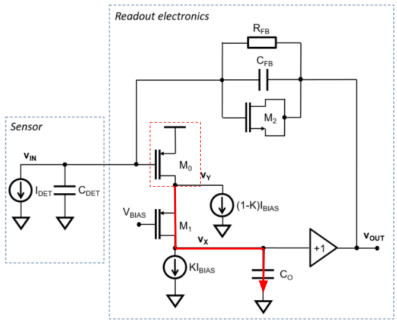
6.5.2 Experimental setup

The measurements presented in the thesis consist of sending simultaneous signals to different pixels and measuring the time-difference between them to estimate the timing resolution. To achieve this, a pulse generator (Active Technologies PG-1072) with a measured interchannel jitter of 7 ps r.m.s. has been used to produce two synchronised pulses with a period of 5 ms. The two pulses are not synchronous to the Timepix4 reference clock.

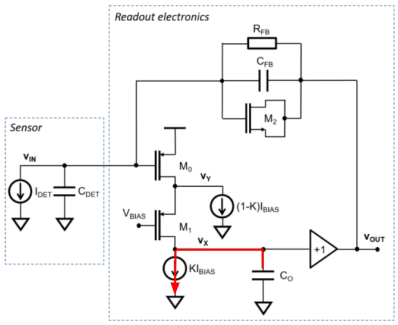
The first pulse is sent directly to one of the Timepix4 digital pixels. The second pulse is used to trigger a pulsed diode laser (PicoQuant PDL-800 B driver with LDH-P-1060 laser head), which emits an infrared ($\lambda = 1060$ nm) laser pulse, This pulse is then attenuated and directed to the Timepix4 via an optical fiber patch cord, which leads to a microcollimator. The microcollimator is positioned with micrometric precision using linear translation stages. The complete setup is illustrated in Figure 6.16.

DAQ system: Timepix4 assembly and SPIDR4 DAQ system

The Timepix4 ASIC used in this measurements is bump-bonded to a 100 µm-thick n-on-p silicon detector, and glued and wire-bonded onto a carrier board developed



(a)



(b)

Figure 6.15: Schematic of the Charge Sensitive Amplifier, part of the pixel analog front-end. The current path followed with **(a)** negative polarity sensors avoids slew rate limitation, while in case of **(b)** positive polarity detectors the C_0 capacitor discharge through the current source limits the slew rate.

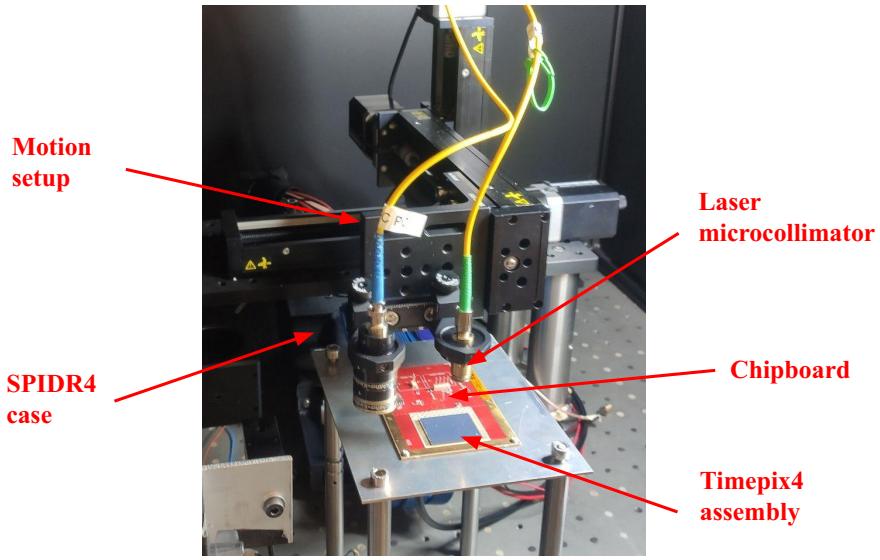
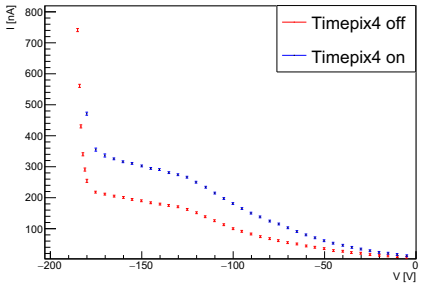
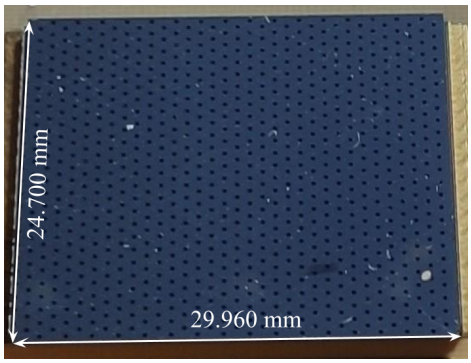


Figure 6.16: Laser setup used on the described measurements [104].

by Nikhef. The silicon sensor has a breakdown voltage of $-180\,\mathrm{V}$, as shown in Figure 6.17a, and it is biased at $-150\,\mathrm{V}$ for the measurements presented here. When the Timepix4 is powered on, the current flowing through the sensor increases due to higher temperatures, but the breakdown voltage remains unaffected. The sensor features a back-side metallization with a pattern of circular openings with 300 micron diameter (visible in Figure 6.17b) which allow the laser light to enter the silicon bulk. With an attenuation coefficient of around 900 microns for the 1060 nm wavelength, the silicon ensures an almost uniform generation of electron-hole pairs throughout its thickness.



(a)



(b)

Figure 6.17: **a** I-V dependence of the Si sensor bonded to the Timepix4 [104]. **b** Holes pattern in the metallization coated on the Si sensor [104].

In the measurements described in this thesis, the Timepix4 operates in electron-collecting mode with a threshold set to 1000 e^- after pixel equalization. Since these measurements do not require sensitivity to very low energies, an higher threshold helps to avoid noisy events. The DACs configuration set used in the measurements described in Sections 6.3, 6.4, 6.6 and 6.7, reported in Table 6.3, results in a pixel current of 7.67 µA. Increasing the power per pixel would improve the timing resolution at low input charges, where the resolution is primarily limited by the front-end contribution [99].

Table 6.3: DAC settings of the Timepix4 used in the measurements presented in Sections 6.3, 6.4, 6.6 and 6.7 [104]. **(a)** Bias voltage DACs. **(b)** Bias current DACs.

DAC name	DAC value set	DAC gain set
VcascPreamp	170	5
VFBK	128	2
VCascDisc	130	5
VControlVCO	0	2
VThreshold	8192	5
VTPCoarse	128	2
VTPFine	512	5

DAC name	DAC value set
VBiasPreamp	100
VbiasDiscTailNMOS	60
VBiasIkrum	5
VBiasLevelShift	90
VbiasDiscPMOS	40
VBiasDiscTRAFF	50
VBiasADC	128
VBiasDAC	50

The Timepix4 carrier board is connected via a flat cable to a SPIDR4 DAQ system, developed by Nikhef, which is used both to configure the ASIC and to transfer the output data to a data acquisition PC. During the measurements, two high-speed links were employed (one link per half matrix), each operating at 2.56 Gb/s.

Laser setup and configuration

The infrared laser pulse has a full-width-half-maximum (FWHM) duration of approximately 36 ps, with a jitter relative to the laser trigger and synch-output signals of less than 20 ps r.m.s., as specified in the datasheet. The intensity of the light per pulse is adjusted using a variable fiber optics attenuator (VOA Electronics V1000F). After attenuation, the light is collimated and focused to illuminate the smallest possible region on the sensor's back-side. Precise positioning and focusing of the laser spot in the center of the metallization openings are achieved using three remotely controlled linear translation stages with micrometric precision, mounted in a 3D configuration.

Once focused, the laser spot has a gaussian shape, with a standard deviation measured to be about 1.4 pixels, as shown in Figure 6.18, effectively covering

a wide Time-over-Threshold range. The laser was focused on a pixel near the center of the bottom half matrix, ensuring consistent illumination of the same pixel region throughout the entire measurement.

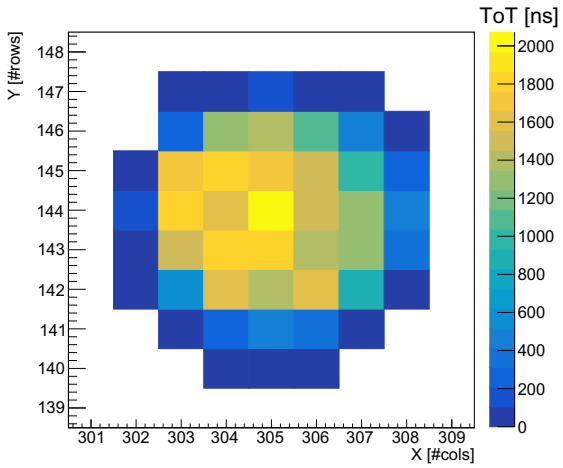


Figure 6.18: ToT distribution among the pixel on a laser pulse event [104].

To estimate the timing resolution contribution from the laser setup and the pulse generator alone, the jitter of the laser pulse, triggered by one output of the pulse generator, was measured using an oscilloscope (Tektronix MSO 70804C, 8 GHz, 25 GS/s). The measurement was performed relative to the second output of the pulse generator, which is typically sent to a Timepix4 digital pixel in the other measurements presented in this work. The laser pulse has been detected using an Ultrafast Photodiode (ALPHALAS InGaAs Photodetector UPD-35-UVIR-P). The measured jitter amounts to (10.9 ± 0.1) ps r.m.s. which is negligible compared to the other contributions to the detector timing resolution, as described in Section 6.5.4.

6.5.3 Measurements and analysis description

The typical measurement consists of illuminating the Timepix4 assembly in a fixed position with a variable amount of light per pulse at a constant repetition rate of 200 Hz.

Once each cluster has been created during the clustering process, the ToA of each pixel in the cluster is compared with the ToA of the reference signal ($\mathrm{ToA_{ref}}$), which is the one sent to the digital pixel input.

A priori each pixel in the cluster is expected to have different time walk contributions, and different ToT vs charge (Q) calibration.

For this reason, the analysis was first conducted on individual pixels. However, several corrections and calibrations still need to be applied to optimize performance, as outlined in the subsequent sections. Once all corrections and calibrations have been implemented, cluster-related quantities, such as cluster time and cluster charge, will be introduced.

6.5.4 Timing resolution contribution

The achievable timing resolution is influenced by several factors, which are detailed in this section. Some of these factors, such as the TDC resolution, are intrinsic and cannot be eliminated, while others, like the time walk effect and variations in VCO frequency, can be corrected.

The impact of effects such as time walk and jitter can be minimised by maximizing the charge collected in a single pixel. The measurements presented in this section are conducted with this assumption in mind, focusing on the central (most illuminated) pixel within the cluster. The laser attenuation was adjusted to ensure that the central pixel received more than $50\,\mathrm{ke}^-$, thereby reducing the influence of time walk and jitter.
Further measurements performed with a variable attenuation will be described in Sections 6.6 and 6.7, along with an explanation of the time walk correction.

Measured variation of the Voltage Controlled Oscillator frequency

Precise timing measurements necessitate accounting for and correcting the different VCO frequencies, either through the Timepix4 configuration or during offline analysis, as demonstrated in Section 6.3.

Without accounting for VCO frequency variation, the measured timing resolution is approximately 200 ps r.m.s.. However, after correcting the timing measurements using the proper VCO oscillation frequency, the standard deviation of the ToA difference between the central pixel and the reference pixel shows significant improvement, reaching a standard deviation

$$\sigma_{VCO} = 126 \pm 1\,\mathrm{ps\,r.m.s.} \tag{6.5}$$

as shown in Figure 6.19.

The measurement above is based on a VCO frequency correction applied at the analysis level after data acquisition, during which the VCOs were operating at different frequencies.

A second measurement was performed by equalizing the VCO frequencies at the

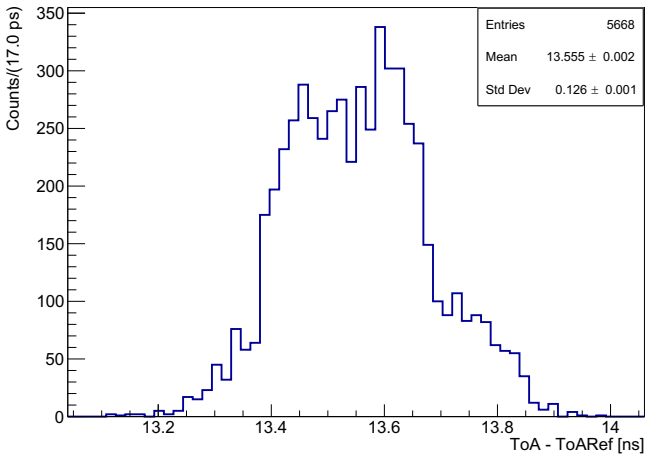


Figure 6.19: Distribution of ToA − ToA_{ref} after the VCO frequency correction [104].

Timepix4 configuration level before the measurement, setting the VCO frequencies of the two pixels to the nominal 640 MHz value. The results is $\sigma_{\text{adj-VCO}} = 132 \pm 1$ ps r.m.s., which is slightly worse than the previous measurement.

All measurements presented in the following sections are corrected for the VCO frequency variation at the analysis level, after data acquisition.

Reference signal resolution

The resolution of the reference signal has been assessed using externally generated test pulses. A periodic pulse has been generated and transmitted to the reference pixel via the digital pixels, and the difference between the ToA of each pulse with the previous one has been computed. These external pulses are not synchronous with the Timepix4 reference clock at 40 MHz, and their period (T = 1165 ns) is not multiple of 25 ns. As a result, they effectively span the entire range of fToA and ufToA bins, ensuring that the resulting resolution inherently accounts for variations in bin widths.

The standard deviation of the ($\text{ToA}_{n+1} - \text{ToA}_n$) distribution is measured to be $\sigma(\text{ToA}_{n+1} - \text{ToA}_n) = 102 \pm 1$ ps r.m.s., as shown in Figure 6.20. Since this outcome is related to the difference between two signals recorded by the same TDC, the resolution of the reference signal can be approximated as follows:

$$\sigma_{\text{REF}} = \sigma(\text{ToA}_{n+1} - \text{ToA}_n)/\sqrt{2} = 72 \pm 1 \text{ ps r.m.s.} \tag{6.6}$$

The above result is slightly higher than the resolution expected from a 195 ps time bin ($195\,\text{ps}/\sqrt{12} = 56\,\text{ps}$). This discrepancy may be due to factors associated with the generation and distribution of the external test pulse itself.

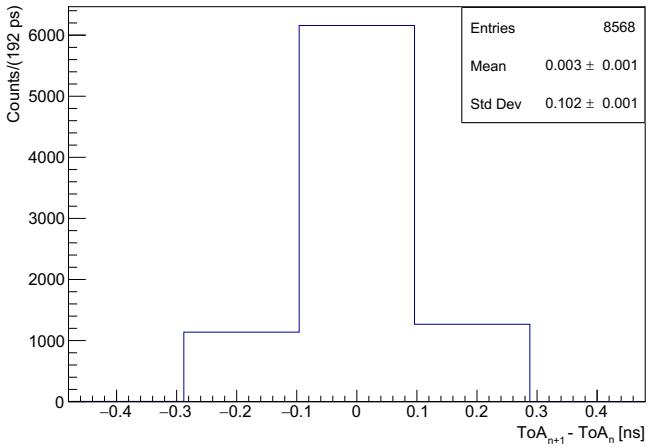


Figure 6.20: Distribution of the period $\text{ToA}_{n+1} - \text{ToA}_n$ of external periodic test pulses sent to a single pixel through digital pixels [104].

Residual contribution to the timing resolution

The timing resolution obtained so far, denoted as σ_{VCO}, represents the error associated to the difference $\text{ToA} - \text{ToA}_{\text{ref}}$. Consequently, the timing resolution for a single Timepix4 pixel for a charge greater than $50\,\text{ke}^-$ can therefore be calculated subtracting in quadrature the contribution due to the reference signal (σ_{REF}):

$$\sigma(\text{ToA})_{\text{final}} = \sqrt{\sigma^2_{\text{VCO}} - \sigma^2_{\text{REF}}} = 103 \pm 1\,\text{ps r.m.s.} \tag{6.7}$$

The value above includes, to a first approximation,contributions from signal generation within the silicon sensor, front-end jitter, and the TDC bin width.

6.6 Time walk correction and single pixel timing resolution charge dependence

To achieve precise timing measurements, it is crucial to correct for the time walk effect in individual pixels [110, 111, 107, 101]. To estimate this effect, a series of measurements was conducted by varying the laser attenuation in fine increments. This variation in intensity allowed the charge values to span the range of approximately [$\sim 10\,\text{ke}^- - 200\,\text{ke}^-$] with a nearly continuous distribution. The resulting

time walk spectrum is shown in Figure 6.21. As shown, the distribution has been fitted using the following function:

$$\mathrm{TW(ToT)} = \mathrm{ToADiff(ToT)} = \mathrm{ToA} - \mathrm{ToA_{ref}} = \frac{\mathrm{p_0}}{\mathrm{Q^{p_1}} + \mathrm{p_2}} + \mathrm{p_3} \tag{6.8}$$

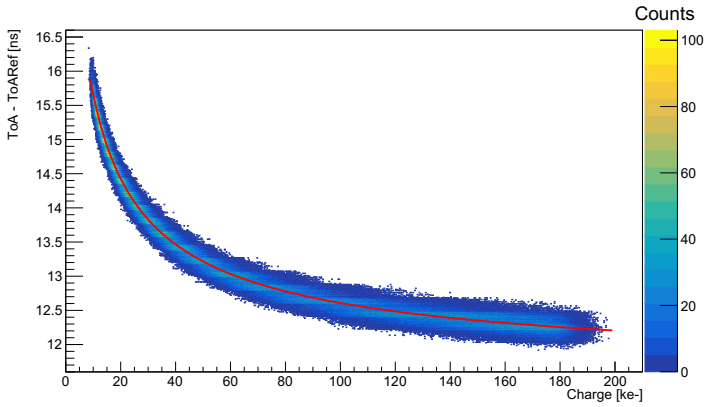


Figure 6.21: Single pixel time walk distribution superimposed with the fitting function [104].

Afterwards, the time walk effect has been corrected for each measured ToA value, by subtracting the charge-dependent correction given by Equation (6.8). The resulting time walk corrected plot is shown in Figure 6.22.

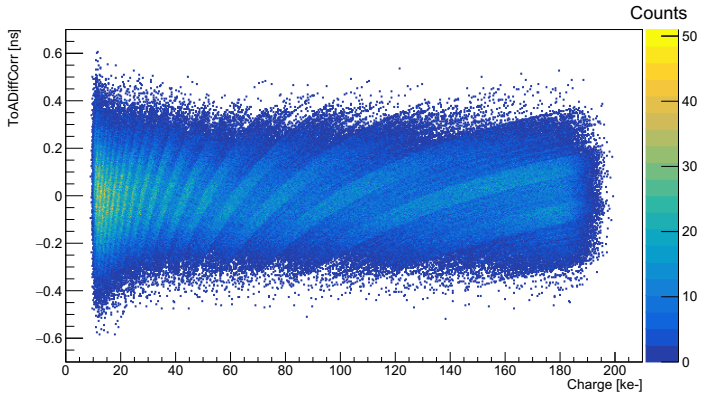


Figure 6.22: Single pixel $(\mathrm{Q}, \mathrm{ToA} - \mathrm{ToA_{ref}})$ distribution after time walk correction [104].

The distribution in Figure 6.22 was further analyzed by dividing it into several "vertical slices," each corresponding to a narrow charge range of approximately $4\,\mathrm{ke^-}$. For each of these charge slices, the timing resolution was estimated by

calculating the standard deviation of the slice's projection onto the ToADiffCorr axis. The resulting resolutions are plotted in Figure 6.23.

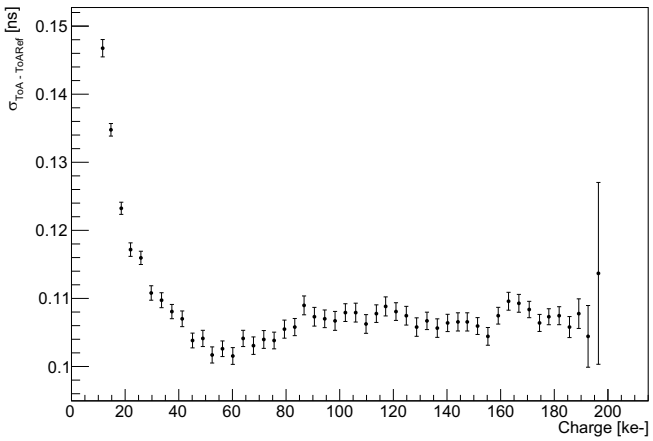


Figure 6.23: Timing resolution dependence with respect to the calibrated charge for a single pixel, after the reference signal contribution has been subtracted [104].

Starting from low input charges, the timing resolution improves progressively, reaching a minimum value of $\sigma_{\mathrm{ToA-ToARef}} = 124.4 \pm 0.8\,\mathrm{ps}$ r.m.s. for charge values from $52\,\mathrm{ke}^-$ to $60\,\mathrm{ke}^-$ before subtracting the contribution of the reference signal. However, at higher input charges, the timing resolution begins to degrade again, eventually saturating at $\sigma_{\mathrm{ToA-ToARef}} = 129 \pm 2\,\mathrm{ps}$ r.m.s. for charges exceeding $80\,\mathrm{ke}^-$.
To estimate the single pixel timing resolution at an input charge of $80\,\mathrm{ke}^-$, the contribution of the reference signal is subtracted in quadrature from the total measured timing difference. This results in a single pixel timing resolution of $\sigma_{\mathrm{ToA}} = 103 \pm 3\,\mathrm{ps}$ r.m.s., as shown in Figure 6.23, which represents the intrinsic performance of a Timepix4 pixel under these conditions. After subtracting the reference signal contribution the resolution plateau reached for charges exceeding $80\,\mathrm{ke}^-$ results to be at $\sigma_{\mathrm{ToA}} = 109 \pm 3\,\mathrm{ps}$ r.m.s., as shown in Figure 6.23.

When measuring the charge distribution (ToT) using a laser with fixed intensity, the result typically follows a Gaussian-like pattern. This spread is caused by two factors: the electronic noise from the Timepix4 front-end and the intrinsic variations in charge collection in the silicon detector. At a constant laser intensity, the timing distribution should also exhibit a Gaussian shape.
However, since the arrival time measurement is quantised into bins of 195 ps, one might expect the hits to be spread across several 195 ps bins, particularly if the

oscillation frequencies of the reference VCO and the laser-excited pixel's VCO were identical. In reality, there are slight frequency mismatches between these VCOs, leading to finer quantization effects but still producing discrete peaks, as seen in Figure 6.19. This timing quantisation generates the horizontal structures visible in Figure 6.21. Once the time walk correction is applied, these horizontal bands transform into tilted structures, as shown in Figure 6.22.

As higher injected charges are used, the broader spread of the measured charge values causes an overlap in the distributions at different laser intensities. This charge overlap becomes more pronounced, potentially complicating the resolution of timing and charge measurements across the full range of laser intensities.

Similarly, the ToA − ToARef distributions at different laser intensities may as well overlap and produce a wider distribution: in particular, due to the time-walk effect, the timing distributions of measurements performed at similar laser intensity may be peaked on values corresponding to adjacent integer multiples of the timing bins. Thus, gathering the measurements would result on an overlap of one distribution tail with another distribution peak, generating a wider distribution, as shown in Figure 6.24.

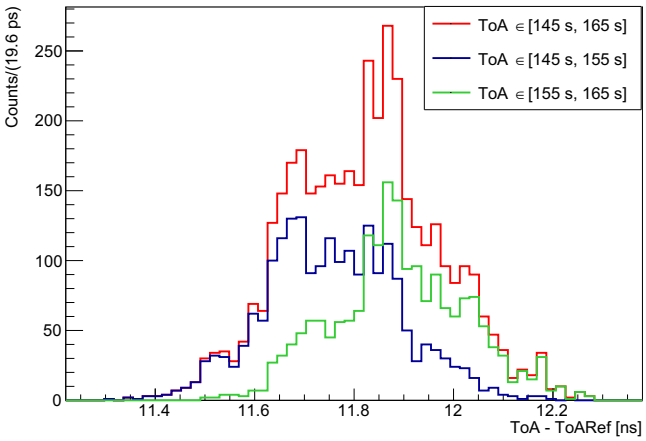


Figure 6.24: Overlap of the timing distribution of measurements performed at close injected charge values, explaining the worsening on the timing resolution at high charge. The green and the blue distributions where obtained with two separate measurements at fixed laser intensity, while the red one is the sum of both measurements.

Due to these effects, the ToA − ToARef distributions related to different laser intensities will overlap when selecting the events using the "vertical slice" method described above. This overlap and the distribution quantisation will result on

a spread larger than the one that would be obtained performing a single measurement at a fixed charge corresponding to the considered slice charge. This explains the degradation of the resolution observed in Figure 6.23 at high charges ($Q \gtrsim 70\,ke^-$).

6.7 Cluster timing resolution

When dealing with clusters of multiple pixels, combining data from different pixels allows for more precise timing information, as long as the time walk effect at the individual pixel level is properly corrected.

The ToA for each pixel in a cluster is corrected for the time walk effect using Equation (6.8). Afterwards, the "cluster ToA" ($ToA_{cluster}$) is calculated as the weighted-average of the ToA of individual pixels within the cluster, with the weights being the respective charge values of each pixel. Instead, the "cluster charge" is simply the sum of the individual pixels' charge.

The cluster ToA as a function of the cluster charge is shown in Figure 6.25.

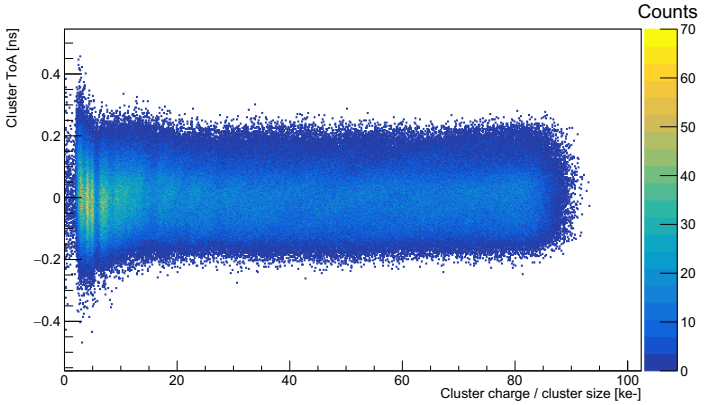


Figure 6.25: Cluster ToA distribution as a function of the cluster charge [104].

The slice analysis described in Section 6.6 was repeated over the complete cluster charge range. The distribution shown in Figure 6.26, where the "cluster ToA" resolution ($\sigma_{\mathrm{ClusterToA}}$), evaluated as the standard deviation of the $ToA_{cluster} - ToA_{ref}$ distribution, is plotted as a function of the cluster charge.

The timing resolution distribution reaches its minimum for a cluster charge in the range $Q \in [\sim 900\,ke^-; \sim 1300\,ke^-]$, with the minimum value being:

$$\sigma_{\mathrm{ClusterToA}} = 79 \pm 1\,\mathrm{ps\,r.m.s.} \tag{6.9}$$

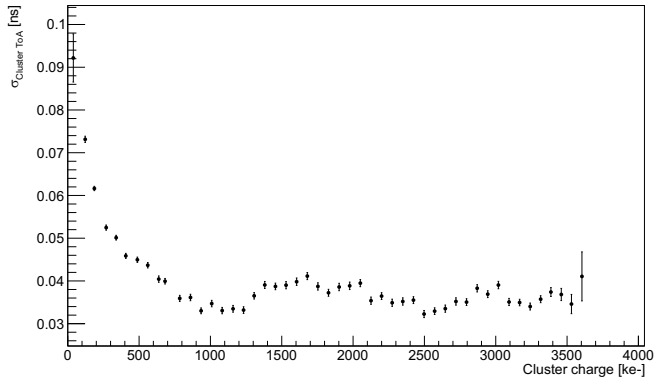


Figure 6.26: Cluster timing resolution ($\sigma_{\mathrm{ClusterToA}} = \sigma(\mathrm{ToA_{cluster}} - \mathrm{ToA_{ref}})$) as a function of the calibrated cluster charge [104].

After subtracting the contribution from the reference signal ($\sigma(\mathrm{ToA_{ref}})$) in quadrature, the true minimum cluster timing resolution is:

$$\sigma_{\mathrm{True\,ClusterToA}} = 33 \pm 3\,\mathrm{ps\,r.m.s.} \tag{6.10}$$

Measurement fluctuations of the order of a few ps in Figure 6.26 attributed to the intrinsic overlap between ToA distributions centered around different timing bins, as discussed in Section 6.6.

6.7.1 Timing resolution dependence on the cluster size

In all the measurements presented, the laser spot on the silicon sensor remained fixed, as shown in Figure 6.18. Surrounding the central pixel, which receives the highest illumination and thus the largest charge, several pixels detect signals due to the optical spread of the laser beam or charge-sharing effects.

It is important to estimate the minimum cluster size needed to reach the best resolution results obtained in Section 6.7. To do this, the analysis was repeated using "artificial" clusters of different sizes, created by removing selected pixels from the original physical cluster through software as shown in Figure 6.27.

For each artificial cluster, the timing resolution distribution has been computed as a function of the cluster charge, as shown in Figure 6.28. To facilitate comparison, the cluster charge has been rescaled by dividing it by the cluster size. The distribution for a single-pixel cluster is consistent with the results of Section 6.6. Figure 6.28 shows two major contributions to the cluster timing resolution. The first is the dependence on cluster charge: initially, increasing charge improves

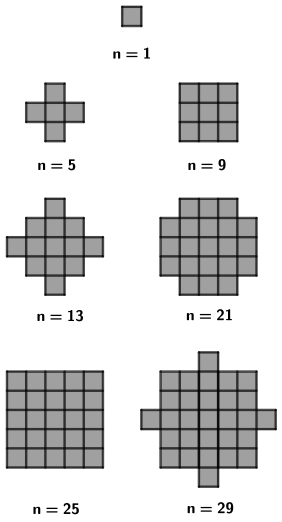


Figure 6.27: Sketch showing clusters of different size (n) artificially created via software [104].

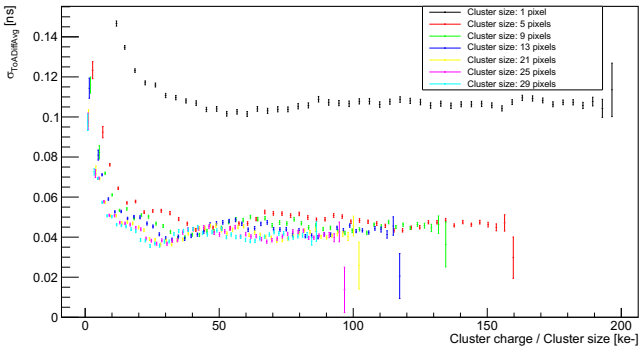


Figure 6.28: Cluster timing resolution as a function of the cluster charge, divided by the cluster size. Different cluster sizes are presented as different colors. Timing resolution of the reference pixel has not been subtracted [104].

resolution due to reduced front-end jitter, but at high charge values, the resolution degrades, as explained in Section 6.6. The second is cluster size: a notable improvement in resolution occurs when increasing from a single-pixel to a 5-pixel cluster, with only marginal gains beyond this. This confirms that high-resolution results can be achieved with smaller clusters.

In order to decouple the cluster charge and the cluster size contributions, clusters with different sizes but "fixed" charge have been analysed. Figure 6.29, for instance, shows only clusters with charge in the range $[360\,\mathrm{ke}^-, 380\,\mathrm{ke}^-]$. This is equivalent to selecting a fixed total amount of charge spread over a different number of pixels. Increasing the cluster size introduces two competing effects: the charge per pixel decreases, worsening timing resolution due to increased front-end jitter, while the statistical averaging of pixels improves overall resolution. For larger clusters, the charge spread dominates, reducing the resolution, whereas for smaller clusters, the averaging effect prevails, improving the resolution.

In Figure 6.29 the first factor is dominant for larger cluster sizes, because the charge would spread more, and the average factor would not be able to compensate for the loss of resolution in each pixel due to the increased jitter. On the contrary, the improvement due to the average is dominant for low cluster sizes, because each pixel collects more charge and therefore the jitter contribution is much reduced.

Figure 6.29 has been obtained from a "vertical" slice of Figure 6.28 for a given cluster charge range. Therefore, depending on the actual sensor coupled to the Timepix4 ASIC and its geometry, it will be possible to find the optimal cluster size in order to have the best timing resolution, depending on the expected total amount of charge that will be spread onto the Timepix4 matrix.

The same analysis was conducted for artificially shaped asymmetric clusters, as shown in Figure 6.30, where the darkest pixel represents the one which received the highest amount of charge.

After subtracting the reference resolution, the timing distributions presented in Figure 6.31, again show a clear improvement over single-pixel resolution, with limited further gains at higher multiplicities. Notably, "compact" 3-pixel clusters (e.g., featuring shapes A and C, where the highest-charge pixel is central) achieve resolution comparable to 4, 5, or 6-pixel clusters.

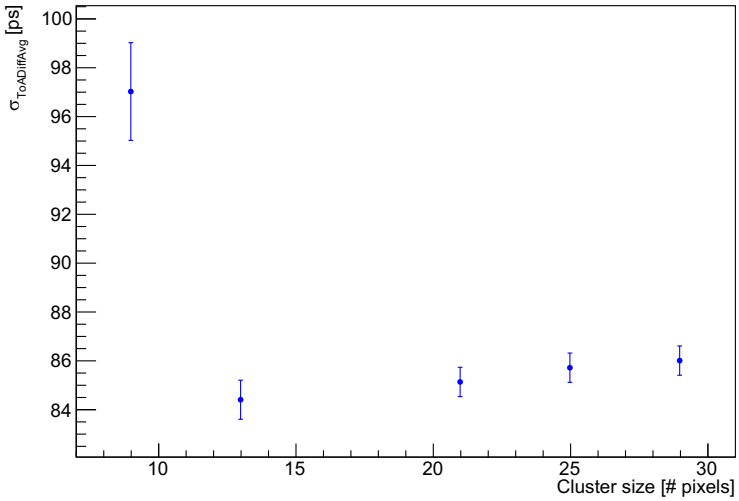


Figure 6.29: Example of the cluster timing resolution dependence on the cluster size for a fixed range of cluster charge. A cut between 360 ke^- and 380 ke^- on the cluster charge has been placed. Timing resolution of the reference pixel has not been subtracted [104].

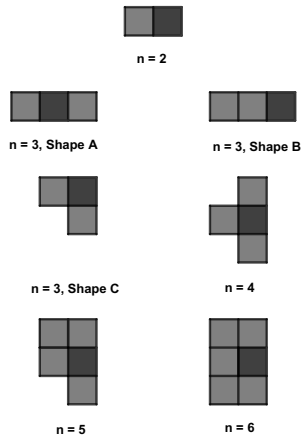


Figure 6.30: Sketch showing clusters of different size (n) with asymmetric shapes artificially created via software. The darkest pixel on each cluster represents the one receiving the highest amount of charge within the cluster [104].

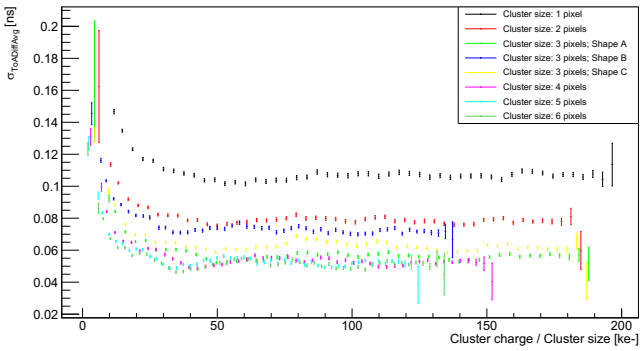


Figure 6.31: Cluster timing resolution of clusters with asymmetric shapes as a function of the cluster charge, divided by the cluster size. Different cluster sizes are presented as different colors. Timing resolution of the reference pixel has been subtracted [104].

6.8 Characterization of an assembly bonded to a Si detector with an X-rays beam

Further characterization of a Timepix4 assembly bonded to a 300 µm Si detector has been performed by measuring monochromatic X-rays at the SYRMEP (SYnchrotron Radiation for Medical Physics) beamline of the ELETTRA synchrotron facility [105, 106].
The aim of these measurement is an energy calibration of the pixels ToT response performed with X-rays, to compare it with the one obtained using the internal testpulse and improving the calibration methods. Moreover, an estimation of the energy resolution has been obtained, as well as an estimation of the pixels dead time.

6.8.1 Test-beam setup

The SYRMEP line allows to select monochromatic radiation through two Si crystals in Bragg diffraction geometry [112]. The photon energy can be selected in a range between 8.5 keV and 40 keV.
The beam intensity can be tuned by inserting aluminum filters or by defocusing one of the Si crystals. It is monitored by an ionization chamber placed forward to the setup.
The beam shape is tuned through slits: the beam horizontal width is 28.6 mm, while its high is 3 mm, with a gaussian vertical profile, as shown in Figure 6.32.

The p-on-n Si detector bonded to the tested assembly has been powered with a

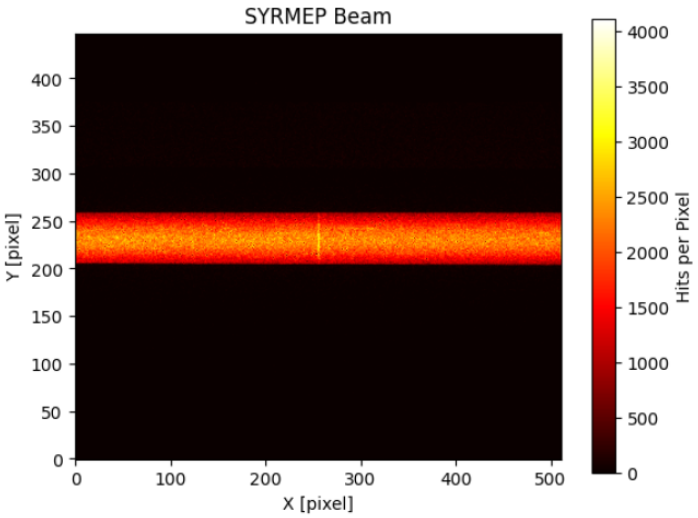


Figure 6.32: Beam cross section of the detector, defining a rectangular shape which covers entirely the detector along the X direction, and 3 mm along the Y direction [105].

bias of 100 V. The Timepix4 is connected through a flat FMC cable to a SPIDR4 system, to be configured and read out.
The assembly is cooled down using a liquid cooling system, setting the liquid temperature at 15 $°C$.
Both the SPIDR4 and the assembly are mounted on hexapod motion stages, used to grant a uniform photon distribution across the matrix. A picture of the setup is shown in Figure 6.33.

6.8.2 Testpulse calibration correction using X-rays beam

To perform a calibration to convert ToT in charge and energy, a sufficiently high number of hits per pixel are required. For this reason, radioactive sources are more suitable to validate a calibration instead of performing one; to have enough statistic, it is necessary to use either internal testpulses or X-ray beams.

A series of flat field acquisitions has been performed by generating several monochromatic X-rays. The detector was scanned to obtain a uniform irradiation, reaching about 4000 hits/pixel.

Considering only single pixel clusters, each pixel presents a gaussian ToT distribution at fixed photon energy, generating a pair (Q_i, ToT_i) for each photon energy set.
As explained in Section 6.4, these pairs' distribution on a pixel is then fitted using

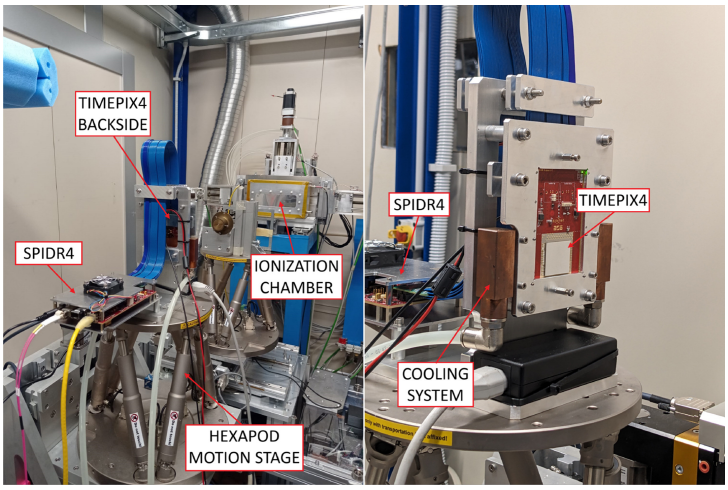


Figure 6.33: Experimental setup used in the beamtime campaign at the SYRMEP line in ELETTRA synchrotron facility [105].

a function:

$$Q_{\text{X-ray}} = p_{1,\text{Xray}} \cdot \text{ToT}_{\text{X-ray}} + p_{2,\text{Xray}} - \frac{p_2}{\text{ToT}_{\text{X-ray}} - p_3} \tag{6.11}$$

The lower energy reachable by the X-ray beam without losing in intensity and resolution is not low enough to finely populate the non-linear region of the ToT calibration. This affects a lot the low energy calibration, in particular the one of clusters with more pixels, as shown in Figure 6.36a, where the 2-pixels clusters presents a shifted and less resolute peak with respect to the 1-pixel clusters. To improve the calibration on that region as well a testpulse calibration has been performed, scanning energies in the range from 4.7 keV to 50.7 keV.

On each pixel, this calibration shows discrepancies with respect to the X-ray calibration, as shown in Figure 6.34.
To compensate for this effect, a linear correction is applied to the testpulse calibration $Q_{\text{TP}}(\text{ToT}_{\text{TP}})$ in order to match the linear regions of each calibration:

$$Q_{\text{TP}}(\text{ToT}_{\text{TP}}) = p_{1,\text{Xray}} \cdot \text{ToT}_{\text{TP}} \cdot g + p_{2,\text{Xray}} + h \tag{6.12}$$

where g is a correction factor of the calibration slope, and h is a correction factor on the charge offset.

One of the factors affecting the slope discrepancies is the uncertainty on the value of the test-pulse input capacitors, discussed in Section 4.6 and shown in Figure 4.4. However, the g coefficient spatial distribution presents structures, visible in

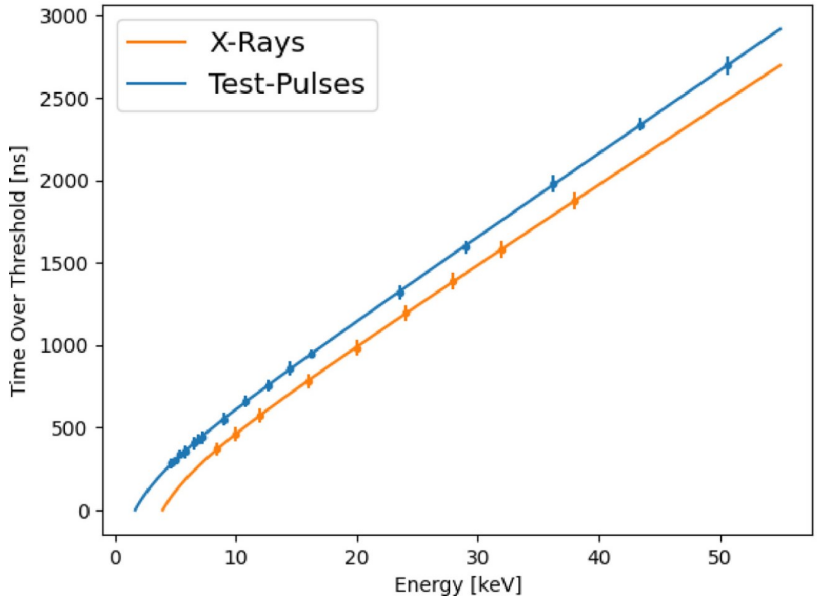


Figure 6.34: Comparison of testpulse based and X-rays based ToT calibrations for a single pixel [105].

Figure 6.35, resembling the power supply distribution, which has a dispersion due to the chip large area and the wire-bond connections.
Such measurements can be used to calibrate the test-pulse input capacitors values, since an hardware correction is not feasible due to the complexity required to reduce the plates alignment during the chip production.

Once the testpulse calibration has been corrected and merged to the X-ray one, the shift of the peaks of more pixels clusters is reduced, and their resolution improved, as visible in Figure 6.36b.
The resolution improvement is higher in the low energy region, where the X-ray calibration was poorer, as shown in Figure 6.36c.

6.8.3 Pixel dead time estimation

To estimate the pixel dead time the beam intensity has been sequentially increased, and monitored through the ionization chamber.
Just a few pixels have been unmasked to avoid saturating the readout bandwidth.
The linearity has been measured at two different energies:

- at 11 keV, with the flux of absorbed photons on the ionization chamber in the range of $\left[2.74 \cdot 10^4 - 1.73 \cdot 10^8\right]$ hits $\cdot$ mm$^{-2} \cdot$ s^{-1};
- at 20 keV, with the flux of absorbed photons on the ionization chamber in

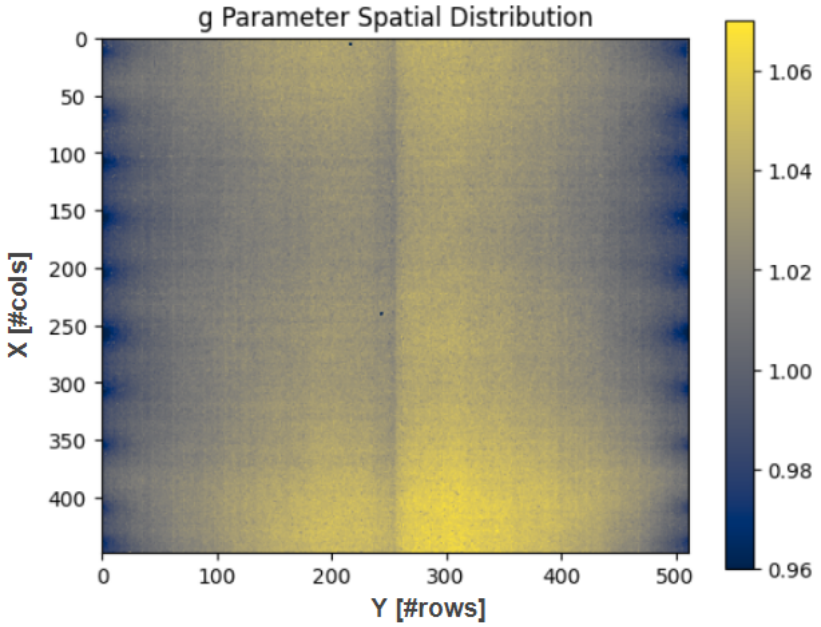


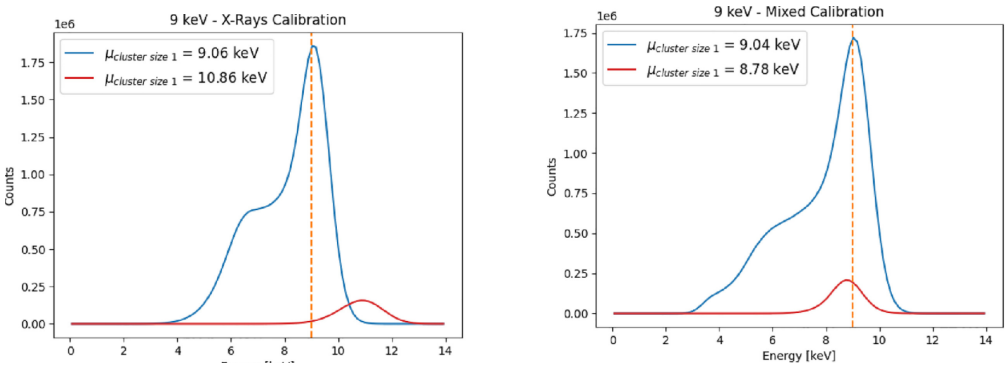
Figure 6.35: Spatial distribution of the parameter correcting the slope of the test-pulse based calibration to make it match with the X-rays based calibration [106].

the range of $\left[1.88 \cdot 10^6 - 3.24 \cdot 10^7\right]$ hits $\cdot$ mm$^{-2} \cdot$ s^{-1}.

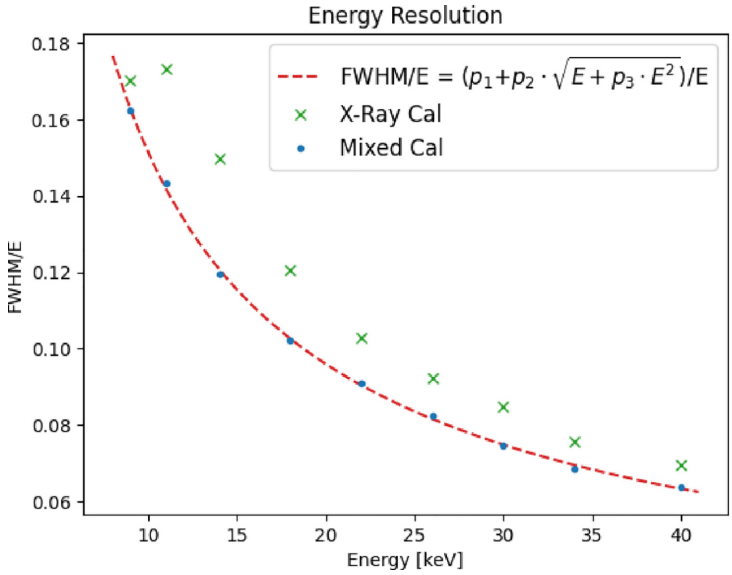
Comparing the rate of photon counting measured on the Timepix4 with the expected rate assessed using the ionization chamber, a linear behaviour is followed up to $4 \cdot 10^7$ hits $\cdot$ mm^{-2}s^{-1} at 11 keV, and up to $3 \cdot 10^7$ hits $\cdot$ mm^{-2}s^{-1} at 20 keV, as shown in Figure 6.37.

Fitting these distribution both with paralyzable electronic and non-paralyzable electronic models [113, 114], the dead time can be obtained. In a non-paralyzable model, the hits received during the dead-time are lost, but they do not add delays to the readout, so the saturation rate is the opposite of the dead-time. On the contrary, in a circuit which can be modeled with a paralyzable model, an event received during the dead-time is lost, and it restarts the dead-time; hence, when the saturation rate is reached, the circuit would not be able to record data anymore. In semi-paralyzable models once an event arrives during the dead-time, it extends the dead-time, but not adding the full dead time as in the paralyzable model circuits.

At 11 keV, a dead-time $\tau_{\text{par}} = (544 \pm 15)$ ns has been computed using the paralyzable model, while a $\tau_{\text{non\_par}} = (745 \pm 54)$ ns has been obtained with the non paralyzable model. At 20 keV, the dead-time estimations for the paralyzable and



(a) (b)



(c)

Figure 6.36: (a) Spectrum of 9 keV X-rays photopeak measured on the whole matrix applying the X-rays based calibration, considering 1-pixel size (blue) and 2-pixels size (red) clusters. (b) Spectrum of 9 keV X-rays photopeak measured on the whole matrix applying the mixed (X-rays and testpulse) based calibration, considering 1-pixel size (blue) and 2-pixels size (red) clusters. (c) Energy resolution improvement given by the mixed calibration with respect to the X-rays calibration [105].

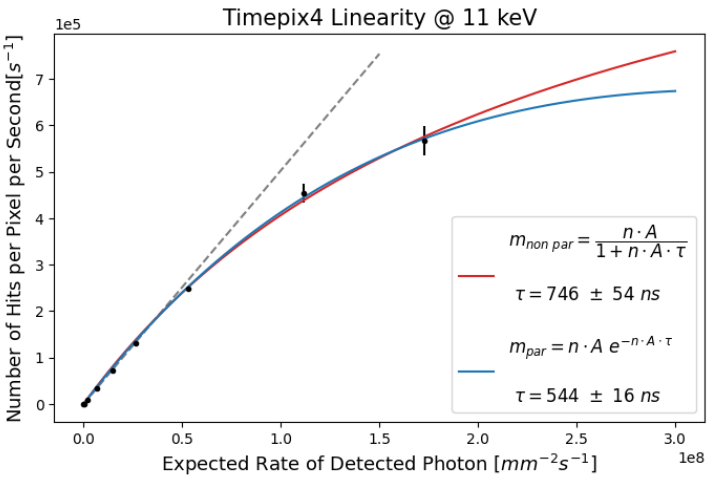


Figure 6.37: Event rate per pixel as a function of the expected rate based on the ionization chamber rate of detected photons [106].

non-paralyzable models are $\tau_{\text{par}} = (760 \pm 56)$ ns and $\tau_{\text{non\_par}} = (817 \pm 67)$ ns, respectively.

These results are affected also by the compensation current set: an higher compensation current reduces the ToT of a signal, reducing the dead time but also worsening the energy resolution; conversely, a lower compensation current improves the energy resolution but increases the dead time.
The DAC values set during these measurements are equivalent to the ones set for the timing measurements with the laser setup, shown in Tables 6.3; the $\text{DAC}_{\text{Ikrum}}$ value generates a compensation current of ~ 2 nA/pixel, which is a good balance between high rates capabilities and good energy resolution.

7

4DPHOTON phototube characterization

7.1 Off-detector electronics: tubecard and FMC adaptor

A modular FPGA-based readout system has been developed to configure the Timepix4 through the slow control and read out data either through the slow control or the high speed links.

The ceramic carriers holding the Timepix4 are housed on custom PCBs, called "tube-cards", shown in Figure 7.1: the tube-card provides the power supply to the ASIC and allows to communicate with Timepix4 and read out the data.
A custom socket, visible within the blue square in Figure 7.1, developed by INFN Ferrara and CERN to allow the connections with the ceramic carrier, are mechanically mounted on the tube-card. The socket contains spring-loaded contact pins [67] to provide electrical connection between the tube-card and the ceramic carrier pins, as anticipated in Section 3.5. Analogously to the ceramic, the socket and the tube-card are missing a pin connection close to one of the corners of the central grounded square, highlighted by the red square in Figure 7.1, to break the symmetries and grant an unambiguous alignment.
The tube-card PCB also allows to monitor signals from the analog pads placed on

the ceramic carrier top side, described in Subsection 3.5.2, and it includes components to monitor the Timepix4 power supplies and ADCs to read back the values of Timepix4 internal reference voltages.

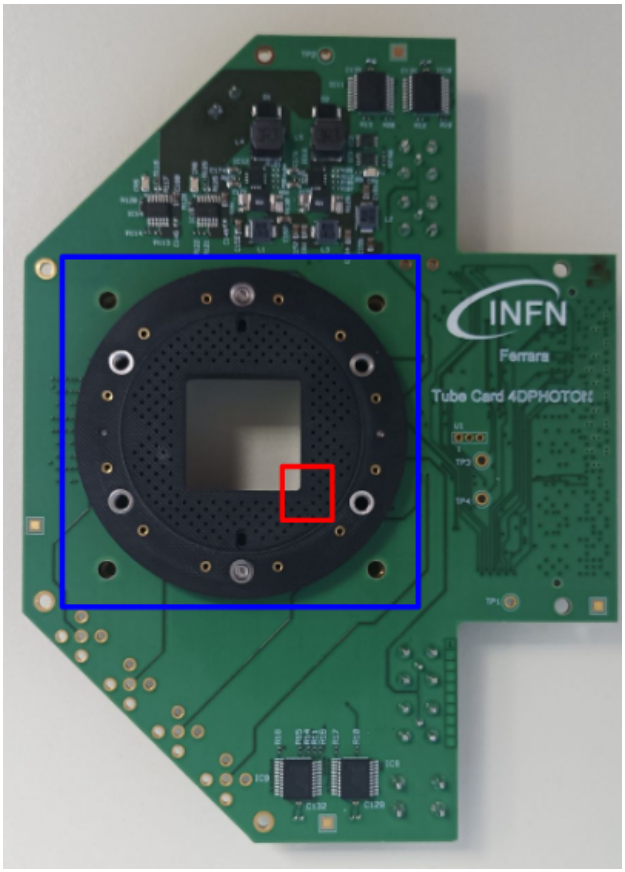


Figure 7.1: Custom PCB developed to house the ceramic carrier. A socket mounted on the PCB, highlighted by the blue square, allows for electrical connections with the ceramic carrier pins. The socket and the tube-card, as the ceramic carrier bottom layer, miss a pin connection in the region within the red square, to break the symmetries and provide an unambiguous alignment.

This PCB is connected through an FMC VITA57.1 HPC style connector to a main DAQ board, based on a commercial AMD/Xilinx KCU105 Development Kit.
Data received from the Timepix4 ASIC are routed to the FPGA present on the board (Xilinx Kintex Ultrascale XCKU040-2FFVA1156E). This architecture allows to exploit the FPGA to read out the eight Timepix4 Multi-Gigabit Transmitters (MGT). Data transmitted are then pre-processed and transmitted to a DAQ server through two 10G UDP ethernet connections.
Conversely, configuration and monitoring data from both the Timepix4 and exter-

nal sensors are instead controlled using a 1G Ethernet connection from the DAQ server.

The tube-card FMC connector pins have been routed in order to be compatible with the FMC pins routing of the SPIDR4 DAQ system; this routing differs from the default one of a commercial FMC, thus an FMC adaptor card has been developed to allow connections between the tube-card and the Xilinx KCU105 Development Kit.
Figure 7.2 shows the basic DAQ system, composed of the control board (1), the FMC adaptor (2) and the tube-card (3).

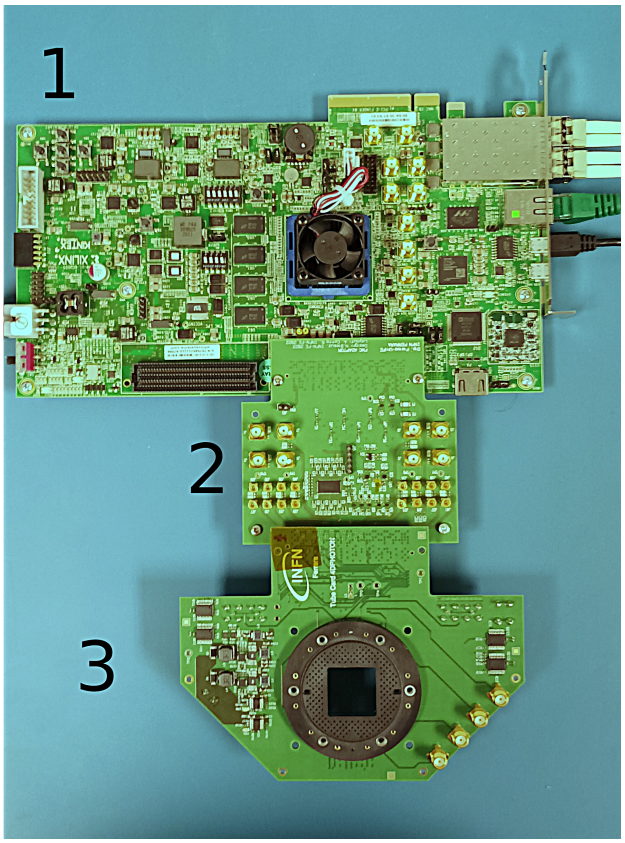


Figure 7.2: Picture of the basic DAQ system.

Custom firmware and software to program the DAQ system and configure the system have been developed by the INFN Ferrara Electronic Service.

7.2 Ceramic carrier boards quality test

After the production, the ceramic carriers must undergo a quality test procedure, to verify their electrical, mechanical and thermal properties.

A preliminary optical inspection is made to verify that no visible defects are present.

One sample has been used to perform a mechanical characterization at CERN metrology service. The goal of this characterization was the verification of the planarity, the carrier dimension, carrier's thickness and its uniformity, the lateral flange position, and the connection pins length.
Such a measurement is crucial for more aspects:

- non-planarity on the ceramic carrier top face or on the Timepix4 would lead to inhomogeneity on the drift electric field generated between the MCP output and the Timepix4, heavily affecting the spatial resolution;
- pins too short would prevent the carrier to reach a good electrical connection, impeding the communication with Timepix4;
- the section dimensions are crucial to allow a correct assembling of the carrier within the vacuum tube, as well as avoiding contacts between the flanges and metallic elements used in the cooling system, that would cause discharges.

The Timepix4 glued to the ceramic carrier presents an overall planarity in accordance with technical specifications. However, local deviations are present due to stresses and strains applied by the glue which cannot be predicted in advance.

In parallel to the mechanical characterization, a thermal one has been performed to verify the proper cooling provided by the heat sink in the bottom part connected to a chiller, while having a thermal load on the top. The thermal conductivity is consistent with the specifications; however, an additional cooling ring has been introduced, as described in Subsection 3.2.4, to improve the tube performance.

7.2.1 Electrical tests

Basic electrical tests are needed to verify the correct connection between the carrier's connectivity map and the design net-list, measure the resistance of each connection and ground. This can be dome by exploiting the bypass capacitor pads included on the bottom of the ceramic carrier.

Then, the impedance profile of signal lines is evaluated using a Time Domain Reflectometer. The resulting differential impedance on the serial output nets is measured to be within a window of 10% around the target impedance of $(100 \pm 10)\ \Omega$.

Eventually, Timepix4 is used to perform more complex tests to evaluate the correct transmission of I/O signals and the goodness of the ASIC operations after its connection to the ceramic.

The first step of the electrical quality tests based on Timepix4 consists of the Timepix4 diagnostic described in Section 6.1. These diagnostic allows to:

- verify the quality of the digital operation;
- verify that the DACs work correctly;
- verify that the DLL can lock correctly, and check if some ADBs may be bypassed;
- verify that the power is correctly supplied.

After these basic diagnostic, a test pulse is sent to an arbitrary pixel pattern, as shown in Figure 7.3, to check the correct transmission of output signals.

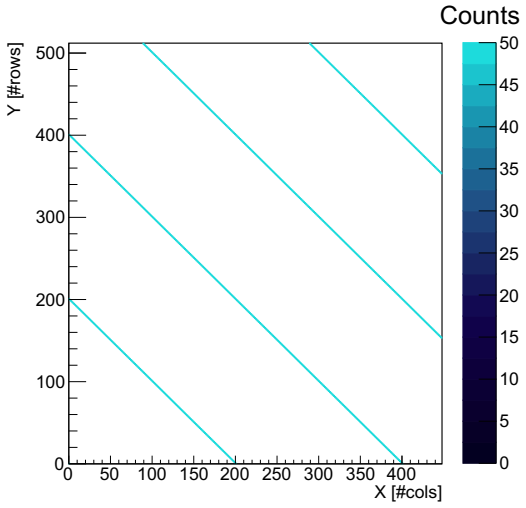
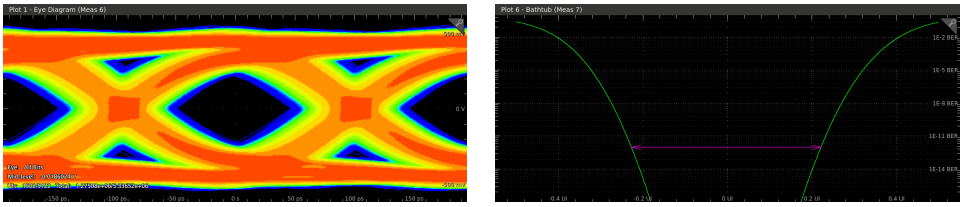


Figure 7.3: Test pulse pattern used to perform a joint quality test on the test pulses and the readout (either through slow control or high speed links).

Eventually, the quality of the high-speed links has been tested. The Timepix4 gives the possibility to send a command to take a "snapshot" of the lock status of the DLL and the PLL blocks of each link, visible in Figure 4.9.
A first test is performed by configuring all the 16 links, and then by monitoring the returned snapshots. If at least one is not correct, all the links are reset and configured again. This procedure is repeated up to 10 times, registering in the end the optimal or the last result.
After checking the links together, each one of them is tested singularly. After the

configuration of a single link, a Timepix4 tool allows to send a PRBS 31 signal through it, as explained in Subsection 4.8.2; the output signal can be monitored from the FMC-adaptor using an oscilloscope. Connecting the SMA connectors pair related to the configured link to the oscilloscope, it is possible to perform a basic serial data analysis, producing an eye diagram and a bath-tub diagram to estimate the bit-error rate of the link, as shown in Figure 7.4. The links have been tested up to 5.12 Gb/s. This bit rate is currently limited by the bandwidth oscilloscope used to analyze the output signal. A eye diagram horizontal opening of $\sim$ 95 ps is measured, corresponding to a bath-tub opening of $\sim \pm 0.2\,UI$ at a Bit Error Rate (BER) of 10^{-12}, considered to be acceptable in the current setup. The total measured signal jitter is $\sigma \approx 100$ ps. The eye-diagram highlights little to no inter symbol interference is present confirming the small impact of impedance discontinuities on the transmission line.



(a) (b)

Figure 7.4: **(a)** Eye diagram and **(b)** bath-tub diagram obtained testing a high speed link at 5.12 Gb/s sending a PRBS-31.

The set-up used to perform these test has been reproduced in Ferrara, CERN and Hamamatsu. The three identical setups allow to perform ceramic quality tests in parallel. The setups in Ferrara and at CERN are used to test that the ceramic carrier batches are produced to specification. Instead, the setup present in Hamamatsu is used to test the ceramic carrier and Timepix4 assemblies during the manufacturing process of the tube assembly.

7.3 Phototube quality tests

7.3.1 Quality test setup and DAQ system

Replicas of the quality test setups used to verify the correct behaviour of the hybrid detector have been built in Ferrara and Hamamatsu.
The phototube is kept within a dark box to reduce the photon hit rate on the photocathode and to decrease the noise and the output rate. A cooling system connected to a chiller is used to cool down the photodetector up to $\sim 0\,°C$. The cooling system of the tube is composed by two parts, as explained in Subsection

3.2.4: a hollow copper plate with coolant flowing inside is placed in contact with the central region of the ceramic carrier bottom layer; a copper hollow ring is in contact with the quartz window, in order to better cool the photocathode and remove heat from the MCP from both sides. To prevent the temperature from falling below the dew point temperature, dry air is fluxed within the dark box, reaching a relative humidity of about 5%, that grants a dew point temperature of $-20\,°C$.

A HiVolta DT1415ET power supply from CAEN is used to provide high-voltage power supply to the MCP sides and the photocathode.

The tube card carrying the tube is connected through a 1 m long flat cable to the FMC-adaptor and the AMD/Xilinx KCU105 Development Kit control board, both placed outside the dark box.

The power supplies and the DAQ system are connected to a programmable Power Unit Distribution, to automatically power up the Timepix4.

The Timepix4 configuration is equivalent to the one described in Section 6.5.2.

7.3.2 Electronics tests

The first quality tests of the detector consists again on the basic Timepix4 diagnostic, to verify that it is still working properly after the tube baking.

After this first test, the MCP-PMT is powered, applying high voltages to the different MCP-PMT elements:

- between the voltage between the Timepix4 and the MCP lower side (the closest one to the Timepix4), that will be referred to as $V_{Tpx4-MCP}$, is set to order of $100 - 300\,\mathrm{V}$;
- the voltage between the MCP lower and upper side, that will be referred to as V_{MCP}, is set to order of $1600 - 2000\,\mathrm{V}$ in the case of MCP-PMT with Chevron configuration, or order of $2100 - 2500\,\mathrm{V}$ in case of Z-stack configuration; this value will be used to tune the MCP gain;
- the voltage between the MCP upper side and the photocathode, that will be referred to as $V_{MCP-PHC}$, is set to order of $100 - 200\,\mathrm{V}$.

When the detector is powered, the basic diagnostic is repeated again. If the Timepix4 is responding correctly, after the threshold is equalised a proper characterization is performed measuring physics quantities as dark count rate (DCR), gain, spatial and timing resolution.

Prototypes features

Five prototypes have been received from Hamamatsu, with different features, namely the number of MCP stages mounted within the tubes, and the end-spoiling depth.

The prototypes identification numbers that will be referred to in the next subsections are summarised in Table 7.1, as well as their main features.

Table 7.1: Available MCP-PMTs prototypes number of MCP stacks and end-spoiling depths.

Ceramic ID	Tube version	MCP stacks	End-spoiling
TP_0007	v1	2	1d
TP_0012	v2	2	2d
TP_0019	v3	2	3d
TP_0024	v4	3	1d
TP_0017	v5	3	2d
TP_0005	v6	3	3d

In the following subsection the measurements performed to characterise the MCP-PMT v4, with 3 MCP stages and 1d end-spoiling depth.
Its photocathode quantum efficiency peaks at 380 nm, reaching an efficiency of 33.32%.
The MCP stack resistance, considering all the three stages, has been measured to be 39.7 MΩ, and the average distance between the Timepix4 and the MCP outer faceplate is 372 µm.

Further studies will be performed to fully characterise and compare the other prototypes.

7.3.3 Dark count rate and gain

The dark count rate and the gain are estimated performing data-driven acquisition in dark conditions. Measurement have been performed at several conditions, varying the voltage between the tube elements, namely between the Timepix4 and the MCP, between the MCP stacks sides and between the MCP and the photocathode.

The electron clouds generated by a photon typically spread over number of pixels, generating clusters with a size dependent both on the MCP gain and the voltage applied between the MCP bottom face and the Timepix4. Thus, the dark count rate is estimated as the number of reconstructed clusters.

An example of the resulting photon counting distribution is shown in Figure 7.5a, obtained biasing the MCP at $V_{MCP} = 2100\,\mathrm{V}$, and applying voltage differences $V_{MCP-PHC} = 75\,\mathrm{V}$ and $V_{Tpx4-MCP} = 150\,\mathrm{V}$, respectively.
The reason of the dark count rate structure is under investigation, and many possible effects are being considered and tested. Field distortions have been ruled out by illuminating specific regions of pixels by precisely moving the micro-focused laser over the MCP-PMT, biasing the MCP with low voltage in order to stay in low gain condition, where the investigated structure is more evident: the distances between the illuminated clusters centroids are comparable with the distances set on the motion setup, with an error lower than the Timepix4 pixel size over distances of $\mathcal{O}(10\,\mu\mathrm{m})$, proving that field distortions are negligible. Increasing the MCP gain the effect is less visible, but still present, as shown in Figure 7.5b: in particular, it can be noticed that the clusters are smaller in the regions where they were missing at low gain, suggesting gain inhomogeneities across the matrix, visible also in the cluster charge distributions presented in Figure 7.5c and 7.5d, obtained at MCP bias 2100 V and 2200 V, respectively. Currently, the possibility of a mixed effect is under investigation: on one hand, the cluster sizes and charges suggest a not-uniform gain, due to MCP stacks co-planarity defects; on the other, the cushion-shaped structure suggests that an effect related to the Timepix4 rectangular shape is present as well, possibly due to a non perfect planarity of the ASIC glued to the carrier.

Figure 7.6 shows the dependence of dark count rate on the MCP bias voltage measured in the MCP-PMT v4 with ID TP_0024. As expected, increasing the gain, an higher number of electrons reaching the MCP may generate a cloud arising above threshold, increasing the dark count rate observed. However, at higher gain a plateau is expected to be reached, as shown in Figure 2.9 [53].
The dark count rate is dependent on the threshold set as well, since an higher number of lower charge events is cut off when a higher threshold is set.
For this reason the characterization has been performed keeping a threshold at $1000\,\mathrm{e}^-$, to minimize the number of cut-off events.

The gain estimation is given by the reconstructed cluster charge. The cluster charge spectra obtained varying the high voltages conditions are presented in Figure 7.8. As expected, the gain ranges from $\mathcal{O}\left(10^3\right)$ to $\mathcal{O}\left(10^4\right)$.
At low gain values the cluster charge spectra are expected to have an exponential distribution, while a more resolved peak would appear at higher cluster charges when increasing the MCP gain to $\mathcal{O}\left(10^5 - 10^6\right)$, as shown in Figure 7.7.

Hence, the gain for each voltage condition tested is estimated as the distribution average, corresponding to $\mathrm{E}[Q] = \frac{1}{\lambda}$, where λ is the parameter describing the

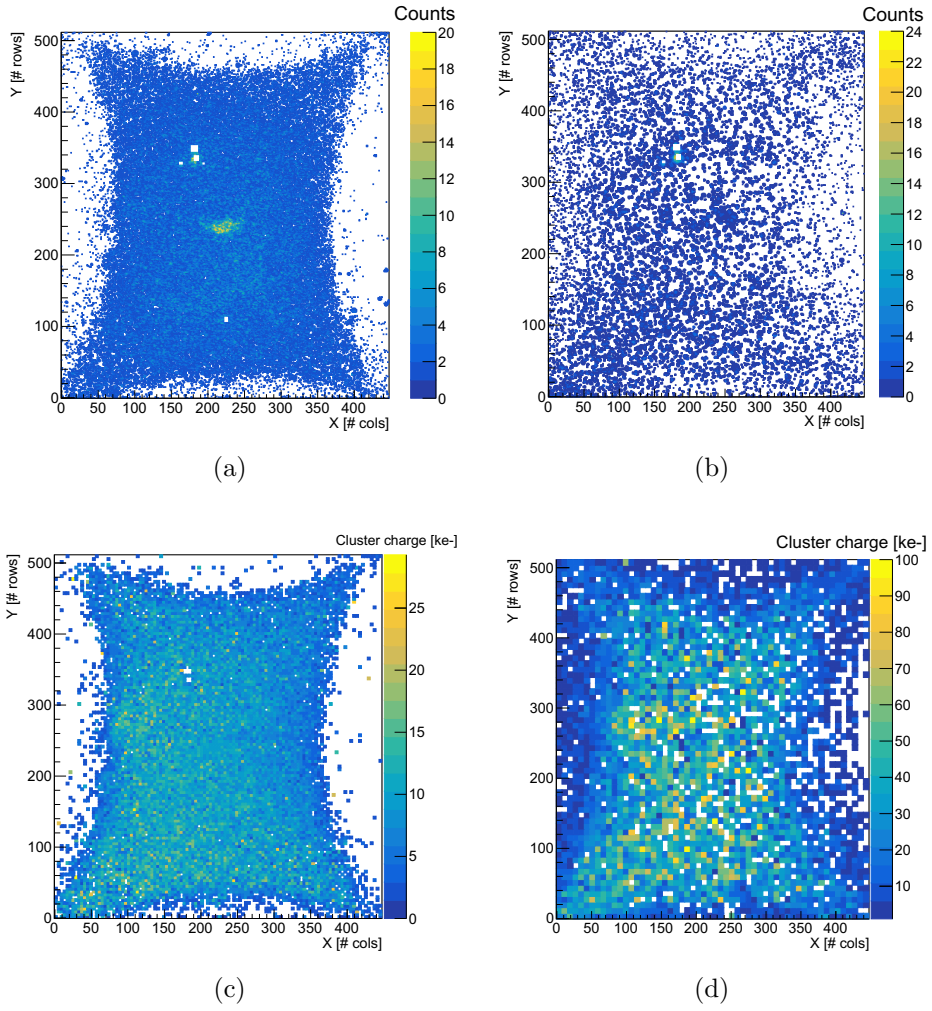


Figure 7.5: **(a)-(c)** Dark count and cluster charge spatial distribution, respectively, obtained with a 10 minutes long acquisition biasing the MCP at $V_{MCP} = 2100\,\mathrm{V}$, and applying a voltage difference of $V_{MCP-PHC} = 75\,\mathrm{V}$ and $VTpx4 - MCP = 150\,\mathrm{V}$, respectively. **(b)-(d)** Dark count and cluster charge spatial distribution, respectively, obtained with a 1 minute long acquisition biasing the MCP at $V_{MCP} = 2200\,\mathrm{V}$, and applying a voltage difference of $V_{MCP-PHC} = 75\,\mathrm{V}$ and $VTpx4 - MCP = 150\,\mathrm{V}$, respectively.

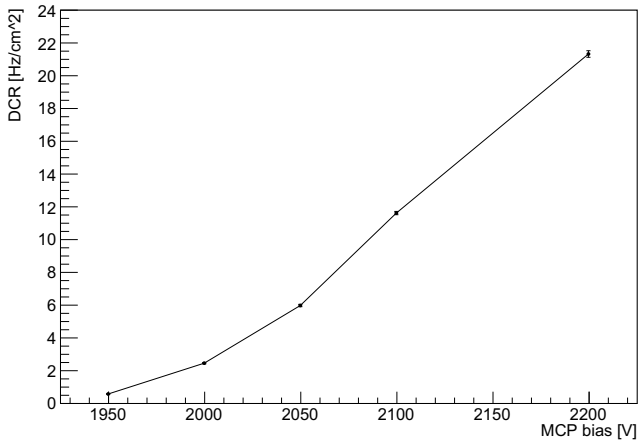


Figure 7.6: Dark count rate dependence on the MCP bias.

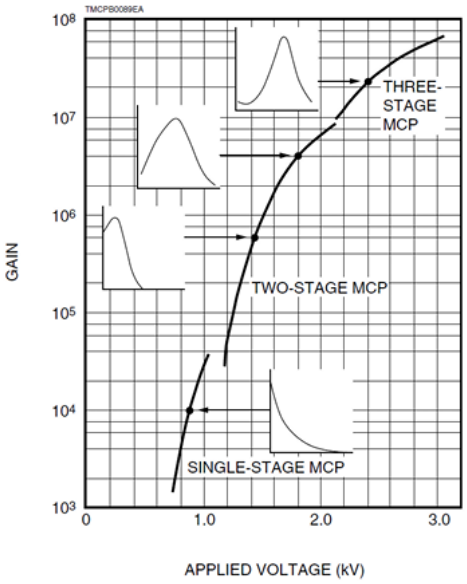


Figure 7.7: Expected gain dependence on the applied voltage for a single stack, a Chevron configuration and a Z-stack configuration MCPs [115]. The original image originates from Hamamatsu Photonics K.K. technical document on MCP assemblies [116].

exponential distribution slope. Being an exponential distribution, the error associated to each gain estimation will be $\sigma = \frac{1}{\lambda} = \mathrm{E}[Q]$ as well.
Figure 7.9 shows the gain trend at several MCP bias voltages.

Similarly to the dark count, the gain presented a strong dependence on threshold

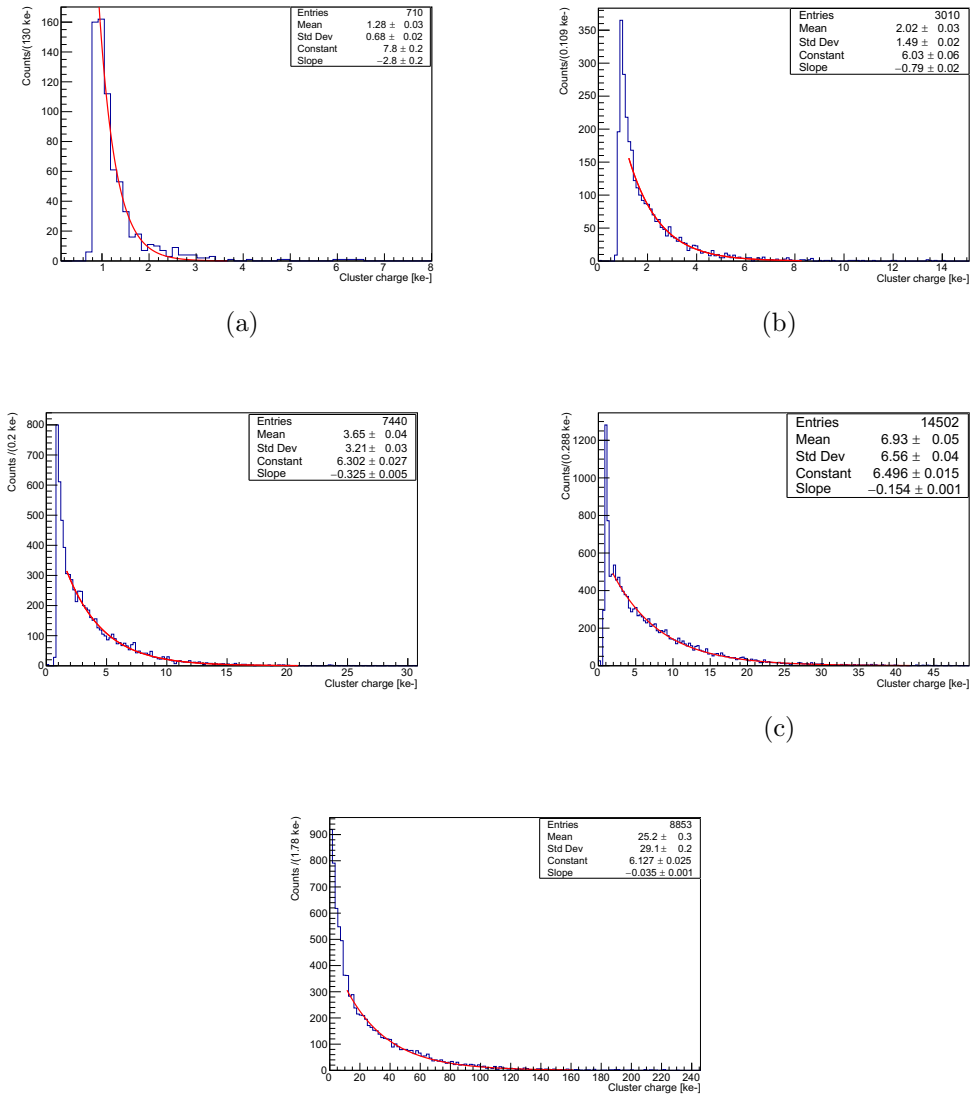


Figure 7.8: Cluster charge spectra measured applying a voltage difference of $VTpx4 - MCP = 150\,\text{V}$ and $V_{MCP-PHC} = 75\,\text{V}$, at different MCP bias: **(a)** 1950 V (3 minutes acquisition), **(b)** 2000 V (3 minutes acquisition), **(c)** 2050 V (3 minutes acquisition), **(d)** 2100 V (3 minutes acquisition), **(e)** 2200 V (1 minute acquisition).

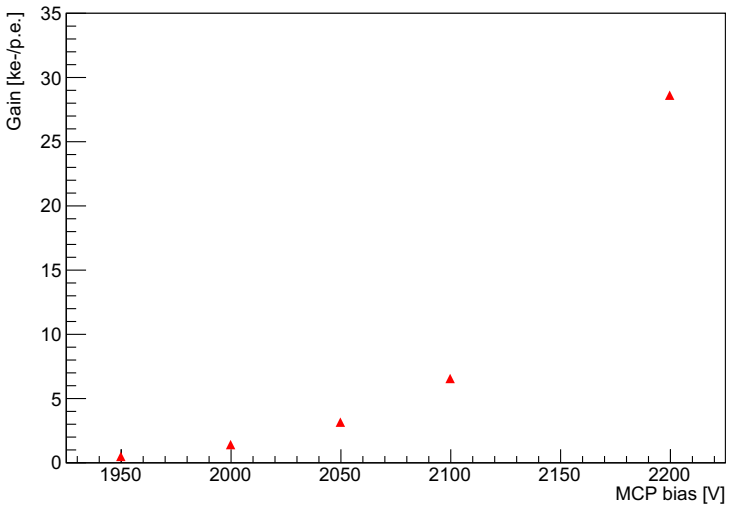


Figure 7.9: Gain dependence on the MCP bias computed on the entire Timepix4 matrix.

as well, especially at higher MCP gain, due to the fact that an higher number of pixels in the clusters halos receives a low charge and does not rise above threshold, reducing the reconstructed cluster charge.

The cluster charge spectra presented in Figure 7.8 are related to the whole matrix; however, the gain estimated from those spectra are affected by the non-uniformity of the gain spatial distribution, observed in Figures 7.5c and 7.5d. Thus, the gain estimation has been repeated with an analogous analysis, focusing on the matrix center region alone. The obtained gain values at low MCP bias are slightly higher, but compatible with the ones obtained considering the total matrix, as reported in Figure 7.10, since the gain is not high enough to populate the lower gain regions; increasing the MCP bias the gain difference becomes evident, since the low gain region are more populated, and this decreases the estimated gain when considering the overall matrix.

When the MCP bias is set to $\sim 2300\,\mathrm{V}$, the distribution deviates from the exponential one, and a peak appears at higher cluster charge. Measurements have been performed at $V_{MCP} = 2300\,\mathrm{V}$ and $V_{MCP} = 2400\,\mathrm{V}$ selecting a central Timepix4 region, to prevent low gain region events to affect the cluster charge distribution; the respective cluster charge distribution are shown in Figure 7.11.
The gain obtained in these distributions is estimated as the mean of the peak. Thus, the central region gain trend measured is extended to these MCP bias values, as shown in Figure 7.12.

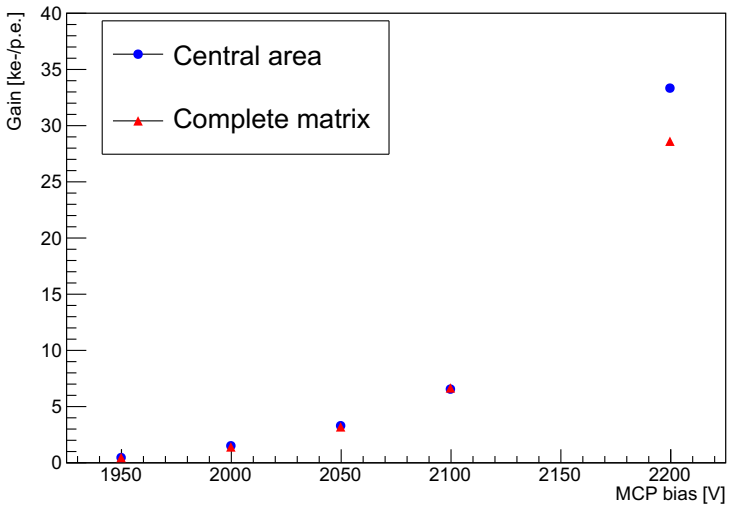


Figure 7.10: Comparison between the gain estimations obtained considering the complete matrix (red triangles) and the central region alone (blue circles).

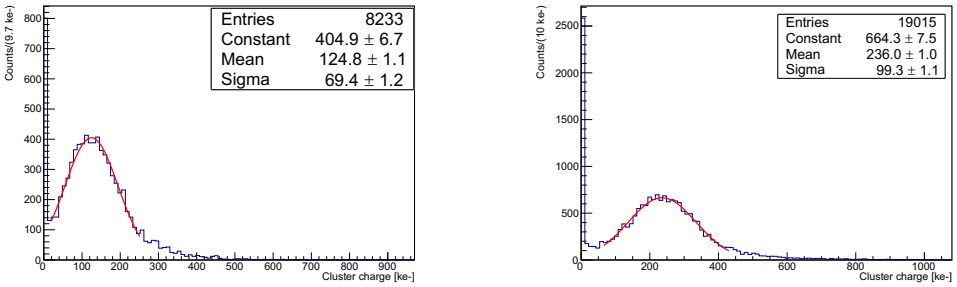
7.3.4 Timing and spatial resolution measurements using laser setup

Measurements analogous to the ones described in Section 6.5 have been performed to estimate spatial and timing resolution of the hybrid photodetector. The concept of the measurement is equal to the one performed on the assembly bonded to a Si sensor: two simultaneous signals, not synchronous to the Timepix4 clock, are generated to be used as trigger for a pulsed diode laser and as a reference signal directly sent in input to Timepix4 digital pixels, respectively; the timing resolution is estimated from the distribution of the ToA difference of the laser and the reference events on the target.

Laser setup and configuration

The first photodetector prototypes tested have a photocathode with a high quantum efficiency in the blue and UV region. For this reason, the pulsed diode laser (PicoQuant PDL-800 B driver) is connected to a PicoQuant LDH-P-C-405 laser head emitting laser pulses with a wavelength $\lambda = 405\,\text{nm}$. The laser pulses are driven onto the Timepix4, where it is focused through a microfocus, moved through translation stages with micrometer precision.

The 405 nm laser pulse is emitted with a time distribution with FWHM of 56 ps, and a jitter with respect to the laser trigger lower than 20 ps r.m.s. from datasheet.



(a) (b)

Figure 7.11: Cluster charge spectra measured applying a voltage difference of $VTpx4 - MCP = 150\,\mathrm{V}$ and $V_{MCP-PHC} = 75\,\mathrm{V}$, at different MCP bias: **(a)** 5 minutes measurement with MCP bias at 2300 V, **(b)** 10 minutes measurement with MCP bias at 2400 V.

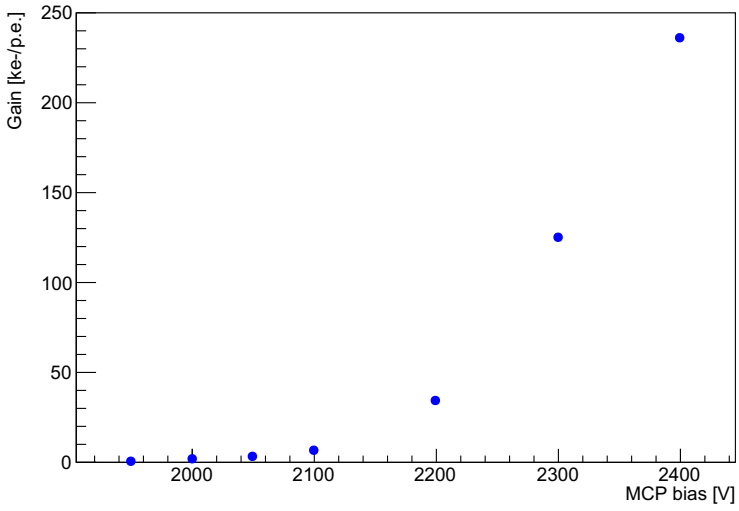


Figure 7.12: Gain dependence on the MCP bias estimated on a central region of the Timepix4.

The pulse intensity is tuned using a variable fiber optics attenuator (OZ Optics DA-100 Digital Variable Attenuator). The microfocus has been placed in order to focus the laser on a central region of the photocathode, generating a circular spot of few pixels on the Timepix4 after the MCP amplification. The standard deviation of the laser spot at the minimum intensity set was measured to about 1.2 pixels r.m.s..

Measurement and analysis description

Analogously to the measurements performed with the assembly bonded to a Si sensor described in 6.5.2, the photocathode has been illuminated on a fixed position with a variable amount of light, sending pulses with a fixed repetition rate of 10 Hz.
The voltage difference $V_{Tpx4-MCP}$ was set to 150 V, the MCP bias to 2400 V and the voltage difference $V_{MCP-PHC}$ to 75 V.
The laser attenuator has been tuned in order to detect an average of 1 laser event each 10 digital pixels signal, to test the detector timing resolution in single photon regime. Indeed, when a few photons are detected by the MCP-PMT, the photon detection is a rare event which can be described with a zero-truncated Poisson distribution. The sample average can be estimated based on the average of the underlying Poisson distribution as:

$$x = \frac{\lambda}{1 - e^{-\lambda}} \tag{7.1}$$

and it can be seen that a Poisson distribution with $\lambda = 0.1$ is needed to have an average number of ~ 1 photon per sample. Considering the non-zero suppressed Poisson distribution underlying, it's characterised by a probability distribution:

$$P_\lambda(n) = \frac{\lambda^n}{n!} e^{-\lambda} \tag{7.2}$$

so its average λ can be estimated from the probability to measure 0 photons, as:

$$\lambda = -ln(P_\lambda(0)) \tag{7.3}$$

Thus, setting the attenuation in order to observe events 1 time each 10 triggers, the Poisson distribution average results to be $\lambda = 0.1$, corresponding to a sample average on the zero-suppressed Poisson distribution $x = 1$.

The analysis is analogous to the one performed in Section 6.5.
At first, the difference between each laser event ToA and the associated digital pixel ToA_{ref} is computed for each pixel illuminated by the laser. The time-walk spectrum resulting for the most illuminated pixel is reported in Figure 7.13.

The time-walk spectra have been fitted using the function 6.8, and each measured ToA value has been corrected with the correction given by the interpolation. The resulting time-walk corrected plot related to the most illuminated pixel is reported in Figure 7.14.

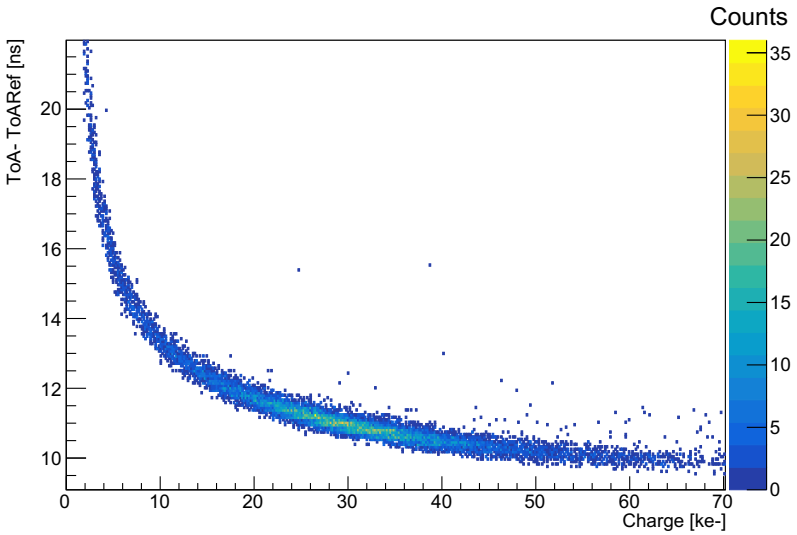


Figure 7.13: Single pixel time walk distribution.

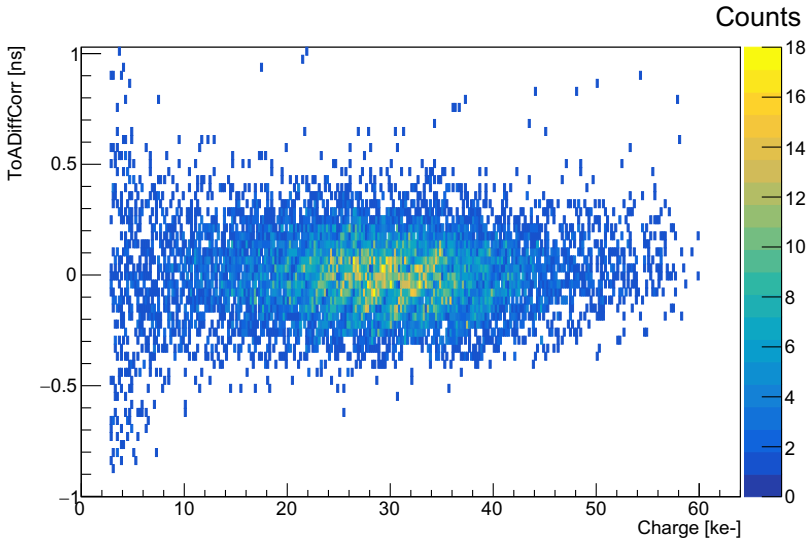


Figure 7.14: Single pixel $(Q, ToA - ToA_{ref})$ distribution after time-walk correction.

Analogously to the analysis performed in Subsection 6.6, the timing resolution distribution of each pixel has been estimated by calculating the standard deviation of vertical slices of the corrected $(Q, ToA - ToA_{ref})$ spectra. Afterwards, the contribution given by the reference signal resolution has been subtracted.
The resulting distribution, shown in Figure 7.15, is consistent with the results ob-

tained on the measurements performed on the assembly bonded to a Si detector, shown in Figure 6.23. A best resolution $\sigma_{\mathrm{ToA-ToARef}} = (107 \pm 6)$ ps is reached for $\mathrm{Q} \sim 40\,\mathrm{ke}^-$.
The expected contributions due to the MCP and the photocathode are lower than 50 ps; the digital front-end contribution is of ~ 55 ps; the contribution due to the pulse generator and the laser trigger is of $\mathcal{O}\,(10\,\mathrm{ps})$, as shown in Subsection 7.3.4. Hence, the resulting resolution is dominated by the analog front-end contribution. It can be improved by optimizing the DAC settings, for example by increasing the preamplifier output signal slope to reduce its jitter.

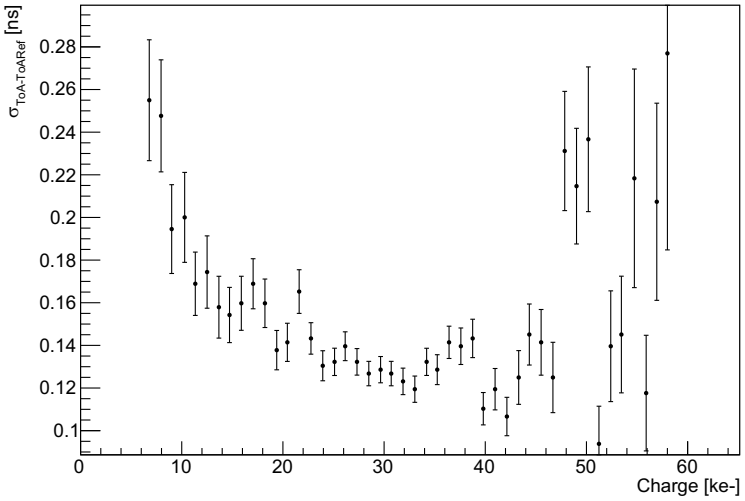


Figure 7.15: Timing resolution dependence with respect to the charge received by the pixel. The reference signal contribution has already been subtracted.

As done for the assembly bonded to the Si sensor, the analysis has been extended to the laser cluster.
A cluster ToA ($\mathrm{ToA_{cluster}}$) is calculated as weighted-average of the pixel ToA after the time-walk effect has been corrected, using the hits charges as values. A cluster charge ($\mathrm{Q_{cluster}}$) is computed as the sum of each pixel cluster.
The $(\mathrm{ToA_{cluster}}, \mathrm{Q_{cluster}})$ spectrum is shown in Figure 7.16.
A slice analysis analogous to the one applied at the pixel level is used to obtain the timing resolution distribution. A slight improvement is obtained, as shown in Figure 7.17, reaching a resolution plateau at $\sigma_{\mathrm{ClusterToA}} = (88 \pm 9)$ ps.
The clusters generated by the electrons clouds emitted by the MCP have most of the charge read out by a single pixel; the 8 neighboring pixels still receive enough charge to avoid a resolution degradation due to an increased jitter on the analog front-end, while a larger halo of pixels receive a much lower amount of charge.

Hence, the improvement obtained on the cluster analysis in Subsection 6.7 is not evident as in the case clusters with many pixels receiving an high amount of charge.

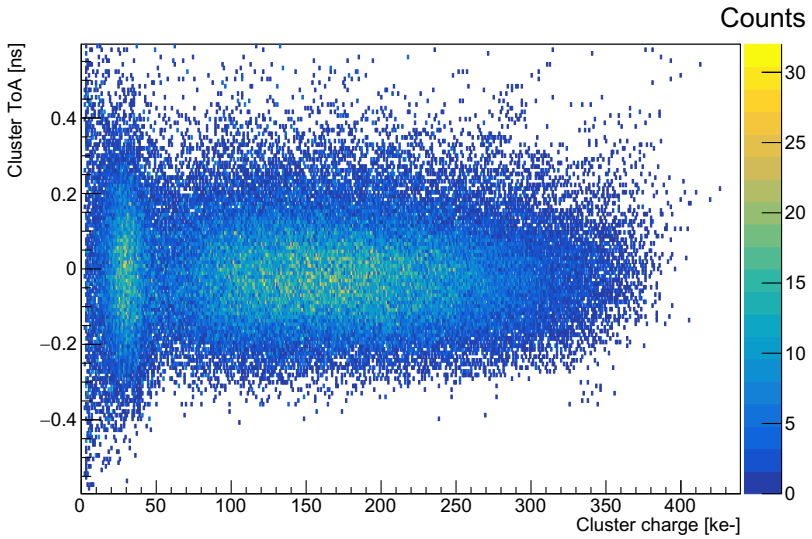


Figure 7.16: Cluster ToA distribution as a function of the cluster charge.

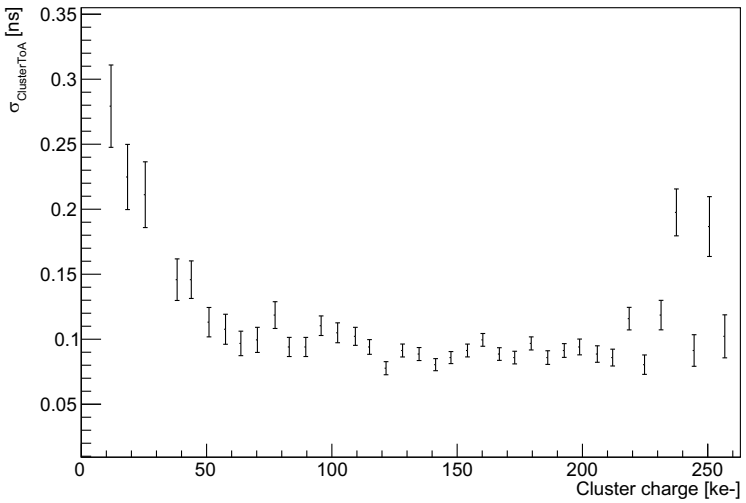


Figure 7.17: Cluster timing resolution as a function of the cluster charge. The reference signal contribution has already been subtracted.

7.3.5 MCP-PMT characterization overview

A set of characterization measurements has been carried out to verify the correct operation of the first MCP-PMT prototype. These measurements include the dark count rate and gain assessments performed under dark noise conditions, as well as timing resolution measurements conducted using a $405\,\mathrm{nm}$ picosecond laser setup.
The average gain and dark count rate values across the matrix are consistent with the reference values provided by Hamamatsu Photonics Japan (HPK) and meet the target values required by the project. However, further investigations are necessary to better understand the source of the gain variations observed across the matrix.
The timing resolution results are currently higher than expected. Ongoing efforts aim to reduce the dominant contributions to these results, including improvements in VCO calibration, tests at higher MCP bias to increase the charge received by each pixel and reduce signal jitter, and optimizing electron cloud focusing to distribute the charge across more pixels, thereby enhancing the multi-sampling effect in cluster timing resolution estimation. A precise estimation of the spatial resolution is still in progress. Nevertheless, preliminary analysis of the laser measurements has already demonstrated sub-pixel resolution.

In summary, the preliminary characterization measurements confirm that the first prototype is functioning correctly. The results are very promising, showing that all targeted detector specifications have been met or are within reach in the near future.

8

Testbeam with Cherenkov setup

A test-beam has been organised at the CERN SPS North Area, aiming to characterize the performance of the first detector prototypes using a Ring-Imaging Cherenkov configuration. The setup consists of a tracking telescope made of two Timepix4 bump-bonded pixel detectors, a solid radiator for the production of Cherenkov photons, followed by an optical section that allows to image the emitted Cherenkov photons into a ring on a set of photodetectors under study.

A GEANT4 simulation is needed, to study the experimental setup response and provide precise previsions on the photons timing and spatial distributions. Such a simulation needs to take into account elements as the photocathode quantum efficiency, the available protons energy, the angular and energetic distribution of the particles, and the background contribution due to nuclear interactions.

The analysis of the simulated data, in particular the performance in terms of tracking resolution, Cherenkov angle resolution and the photon timing resolution, which is expected to be of the order of 10 ps per single track, is fundamental to correctly define the experimental setup of the test-beam.

8.1 Experimental setup

The test beam has been performed at CERN SPS, in the H8 beamline. This line provided an hadron secondary beam, composed by $\sim 80\%$ of protons, $\sim 20\%$ of pions, $\sim 1\%$ of muons and a negligible fraction of electrons. The particles energy has been assessed to $E = (140 \pm 1.8)\frac{\text{GeV}}{c}$.
The maximum intensity of the beam is about 100k particles in each spill of 4.8 s. The beam section is gaussian on both the directions perpendicular to the beamline, with $\sigma \sim 5\,\text{cm}$ and divergence with $\sigma \sim 1\,\text{mrad}$.

The experimental setup comprises a tracking system, a RICH system and a system measuring events timing. A schematic representation of the setup is shown in Figure 8.1.
The single systems are described in the following subsections.

8.1.1 Tracking system

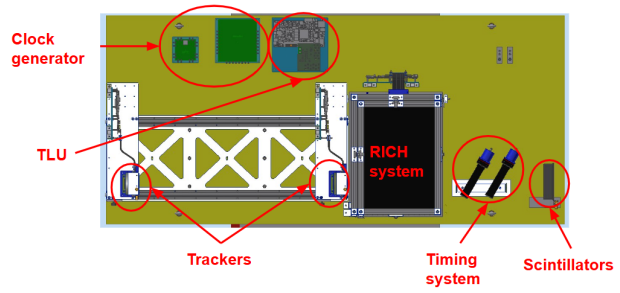
The tracking section is composed of two Timepix4 v2 assemblies bonded to 300 µm thick p-on-n planar silicon sensors, and it is placed upstream with respect to the full setup. During the test beam campaign several bias values have been applied to the silicon sensors, ranging from 100 V to 150 V. The two Timepix4 assemblies are 100 cm apart, to grant a high resolution on the reconstruction of particle direction.

The expected resolution on the single tracker is of about 16 µm r.m.s., thus, being 1 m apart, the expected track angular resolution is $\sim 23\,\mu\text{rad}$, without considering the Coulomb scattering. This provides an important information on the incident position and direction of a proton on the Cherenkov radiator, allowing to correctly compare the position reconstructed from the Cherenkov rings with the real ones.

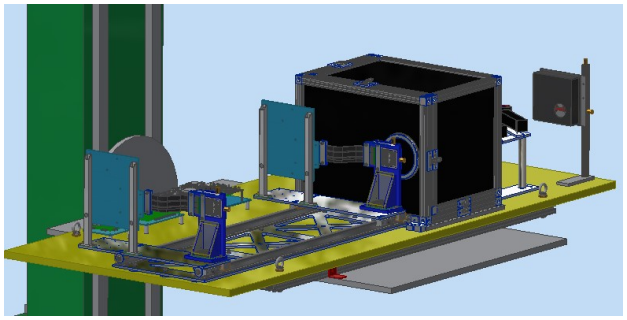
8.1.2 RICH system

The RICH system is located within a dark box downstream with respect to the tracking system. It includes a Cherenkov radiator, the optics system used to drive the Cherenkov photons to the detector, and a single prototype of hybrid MCP-PMT used as photodetector.

Let's consider a reference system $(\hat{x}, \hat{z})$, where $\hat{z}$ is directed along the beam axis with the same verse, and $\hat{x}$ is horizontal and perpendicular to $\hat{z}$, and it points in such a verse as to form a right-handed system with a vertical $\hat{y}$ axis directed upwards. The system origin is placed in the vertex of the spherical lens used as radiator.
The optics system is divided in two sections by a tilted mirror, as shown in Figure



(a)



(b)

Figure 8.1: **(a)** Schematic of the test-beam setup seen from above: it comprises a tracking station composed of two Timepix4 assemblies bonded to Si sensors, a RICH system enclosed within a dark-box, a timing system consisting of two Cherenkov detector, and two scintillators to align the setup to the beam. An external clock generator and a Trigger Logic Unit (TLU) are used to provide an external reference clock and external T0_sync and shutter signal to the three Timepix4. **(b)** Lateral view of the testbeam setup.

8.2, which moves the optical axis from the $\hat{z}$ axis to the $\hat{x}$.
The optical elements used are commercially available, produced either from Edmund Optics, as the mirror, or Thorlabs Inc., as the lenses.

All the optical elements used are in fused silica, having a refractive index ranging from 1.45 to 1.5 in the wavelength range of Cherenkov photons.
The Cherenkov radiator is a LA4545 plano convex lens [117], characterised by a diameter of 50.8 mm, a maximum thickness of 10.6 mm, the radius of the spherical surface of 45.0 mm and a focal length of 93.0 mm. The planar surface is downstream with respect to the spherical one. The beam particles energies are high enough for the Cherenkov angle to saturate: hence, the photons are produced with an almost constant angle of 48.53°, regardless of the particle generating them. The limit angle to obtain complete internal reflection ranges from 41.7° to 43.6°, depending on the refractive index of the material, thus the Cherenkov photons produced are internally reflected on the planar surface. An aluminium coating has been placed on the spherical surface to reflect back the photons towards the following optics elements.
The radiator vertex is in position (0.0 mm, 0.0 mm) in the reference system described before.

Afterwards, a LA4078 plano convex lens [118] is placed with the vertex in the position (0.0 mm, 25.0 mm), with the planar surface upstream. This lens features a diameter of 50.8 mm, as the previous one, while the maximum thickness is 14.2 mm, and the spherical surface radius is 34.5 mm. The focal length is 75.0 mm.

Following the first doublet, an Edmund Optics mirror 84-425 [119], with a cylindrical shape with diameter 75.0 mm and a thickness of 7.5 mm. The downstream surface features a metal coating, and its center is in the position (2.0 mm, 52.0 mm). The mirror is tilted by 45°, moving the optical axis from the $\hat{z}$ axis to the $\hat{x}$ one.

The first element seen by the optical axis is a LA4795 plano convex lens [120], placed in the direction shown in Figure 8.2. The lens has a diameter of 75.0 mm, a maximum thickness of 11.0 mm, and the spherical surface radius is 92.0 mm. The focal length is 200.7 mm, while the back focal length is 193.2 mm. The lens vertex is placed in (70.0 mm, 50.0 mm).
Afterwards, two more LA4795 lenses, with vertexes in (98.0 mm, 50.0 mm) and (120.2 mm, 50.0 mm) positions, respectively, form a doublet.

Eventually, a LA4384 plano convex lens [121] is placed, with vertex in (121.0 mm, 50.0 mm) position. This lens has a diameter of 75.0 mm, a maximum thickness of 26.9 mm, and a spherical surface radius of 41.4 mm. The focal length is 71.9 mm.

Placing the detector so that the entrance window is perpendicular to the optical

axis, and its center is in the (180.0 mm, 50.0 mm) position, this optical system focuses the Cherenkov photons on the detector plane on a ring having diameter of 18.0 mm with a dispersion of 0.9 mm.

The main characteristics of the optical elements used in the optics system are summarised in Table 8.1.

Table 8.1: Main characteristics of the optical elements used in the optics system. The thickness referred to the lenses has to be intended as the maximum thickness of the lens. The spherical surface radius and the focal length are referred to the lenses only.

Code	**Element description**	**Diameter [mm]**	**Thickness [mm]**	**Spherical surface radius [mm]**	**Focal length [mm]**
LA4545	Plano convex lens	50.8	10.6	45.0	93.0
LA4078	Plano convex lens	50.8	14.2	34.5	75.0
LA4795	Plano convex lens	75.0	11.0	92.0	200.7
LA4384	Plano convex lens	75.0	26.9	41.4	71.9
84-425	Cylindrical mirror	75.0	7.5	/	/

8.1.3 Timing system

Along the beam direction, downstream with respect to the RICH system, a couple of Cherenkov detector provides a precise timing measurement to be used as timing reference to measure the MCP-PMT timing resolution.

These detectors consist of borosilicate glass (BK7) thin plates, with dimensions 12.5 mm × 11.0 mm × 100.0 mm, kept within dark box with optimised dimensions welded on them. One of the smallest faces is coupled through a custom light guide to commercial MCP-PMTs (H15547-07 [122] and R3809U [123]). The plates are tilted by 60° with respect to the beam direction, to allow Cherenkov photons to be internally reflected by the surfaces on the long plate side and to reach the MCP-PMT to be read out. The photons emitted towards the surface opposite to the light guide are not totally reflected, and they are diffused by the black box walls to prevent their read out, either they exit from the face opposite to the light guide or from other surfaces.

A resolution on the reference timing of 30 ps is expected.

8.2 GEANT4 simulation

8.2.1 GEANT4

GEANT4 [124, 125, 126] is a software package which allows to simulate the interactions of particles with a material and their passage through it. It has been firstly developed in 1998 in the context of the RD44 project, a collaboration of CERN and KEK [127]. The reference documentation allows to develop specific applications to simulate customised detectors and experimental setups [128]. Several elements of a simulation process can be directly controlled, such as, for example geometry, materials, particles included and their interactions, generation of primary events, tracking of particles, response of detector components, storage and visualization of events and tracks.

GEANT4 is based on a set of physics models, to correctly manage particle interactions at different energies.

8.2.2 Simulation description and physics settings

The application developed using GEANT4 comprises the overall setup, including the tracking system, the RICH system and the timing system. Hence, it is comprehensive of the beam simulation, its interaction with the Timepix4 assemblies bonded to the silicon sensors, the beam interaction with the Cherenkov radiator and the following photons production, the transport of the photons through the optics system, and the beam interaction with the Cherenkov detectors used to provide timing references.

The application has been written in order to be general enough to allow changes, in order to easily adapt it to hardware variations. For example, it allows to change very easily the beam composition, as well as the material composition of the radiator.
Moreover, the geometry definition allows to easily add optical elements, as well as varying the number of 4DPHOTON detector used, and to optimize the setup elements placing in the space.

The simulation has been used to: estimate the expected Cherenkov ring resolution; estimate the timing distribution of the photons within a Cherenkov ring; define the best disposition of the detectors, to select the best setup option among the proposed ones.

Beam simulation

Several variations of the test-beam application have been built using different particle sources configuration, in order to study different effects.

A first particle source configuration consists of a pointy source of protons generated with an energy $E_p = 180\,\text{GeV}$, and directed along the $\hat{z}$ direction, orthogonally to the Cherenkov radiator surface.
To study the effect of a source having finite dimension, the configuration has been changed generating protons distributed uniformly within a circle of radius $r = 2\,\text{cm}$ center on the previous source point. The circle lies on the $\hat{x} - \hat{y}$ plane.

Similarly, another configuration consists of the generation of bunches of protons generated with a gaussian smearing in the $\hat{x}$ and $\hat{y}$ directions, with $\sigma = \sigma_x = \sigma_y = 1\,\text{cm}$.

Eventually, a mixed beam has been implemented, composed of 80% of protons, 20% of pions and 1% of kaons, to simulate a beam more similar to the SPS one.

Geometry settings

The Timepix4 assemblies composing the tracking station have not been simulated on the electronic aspects, but they have been taken into account to consider the correct material budget on-beam: each of them is simulated as a parallelepiped of $24.7\,\text{mm} \times 29.96\,\text{mm} \times 300\,\mu\text{m}$, connected to a second parallelepiped of $24.7\,\text{mm} \times 29.96\,\text{mm} \times 700\,\mu\text{m}$. On their back, the PCB in FR4 has a thickness of 1.6 mm.

The RICH optics system described in Subsection 8.1.2 has been implemented defining the optical elements and their optical properties, as refractive index or surfaces reflecting and transmitting indexes, based on the specifications provided by the producers [118, 121, 117, 120, 119]. The optics system Geant4 simulation is shown in Figure 8.2.

The photons are redirected onto the 4DPHOTON detector: only the input quartz window, which is 6 mm thick, has been simulated, to take into account its effect in the optical path. The photons positions are then registered in the window face where the photocathode is coated.

8.2.3 GEANT4 simulation results

The main information provided by the simulation to be compared with the measurements data is the spatial and temporal distribution of the photons reaching the photocathode, as well as the timing distribution of the Cherenkov photons detected by the timing system MCP-PMT.

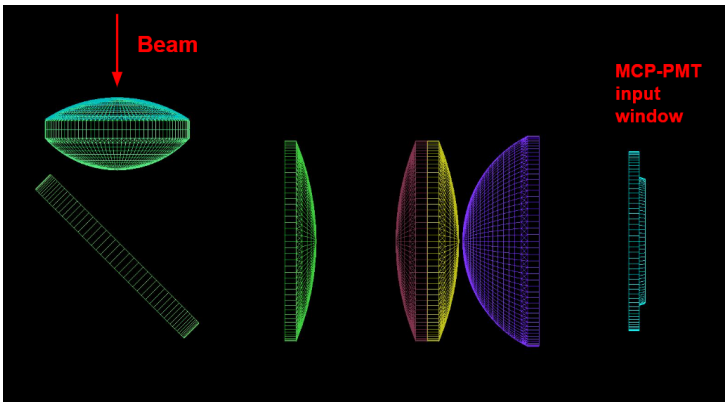


Figure 8.2: Geant4 simulation of the optics system designed for the RICH system of the test-beam.

The Cherenkov photons reaching the photocathode generate Cherenkov rings, whose integrated distribution results to have a radius of (9.0 ± 0.5) mm.
Photons are expected to be detected even within the circle defined by the Cherenkov ring, and around that circle, due to photons generated by particles produced by nuclear interactions of the primary beam particle.

The timing distribution of the photons detected in a single event results to have a standard deviation of $\mathcal{O}(80\,\text{ps})$.

8.3 DAQ and data storage setup

The DAQ and storage net is organised into 4 subnets, as shown in the schematic presented in Figure 8.3: the four subnets will be referred from now on as the *Slow control* subnet, the *Fast links* subnet, the *Storage* subnet and the *Remote* one.

The *Slow control* subnet is the one responsible of the configuration of all the instruments.
It includes the SPIDR4 DAQ systems controlling the 3 Timepix4 assemblies, which are the two bonded to the silicon detectors composing the tracking station, and the one mounted within the MCP-PMT prototype under test.
Two low voltage power supplies are used to power the three Timepix4, and two high voltage power HiVolta DT1415ET provides power to the silicon detectors, the MCP-PMT elements (photocathode, MCP input face, MCP output face), and the standard MCP-PMTs reading the Cherenkov detectors used for timing.

A custom Trigger Logic Unit (TLU) receives the Extraction Warning signals from SPS and generates T0_sync and shutter signals based on the SPS signals. The

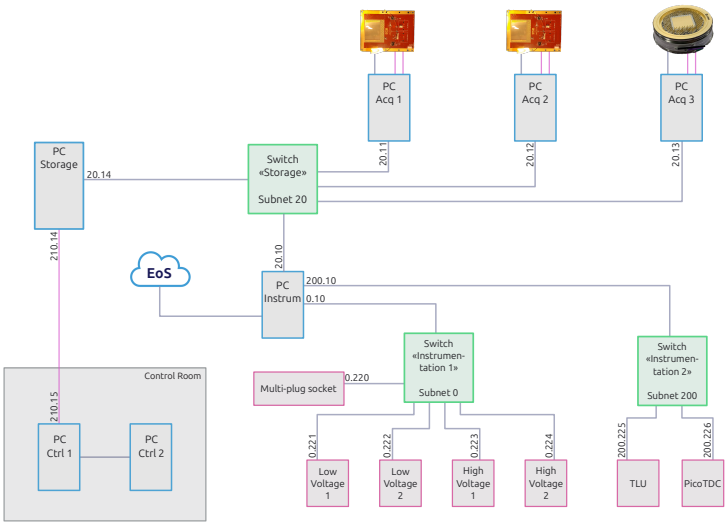


Figure 8.3: Schematic of the test-beam DAQ and data storage setup.

T0_sync and the shutter signals are simultaneously sent to the 3 SPIDR4 boards. A clock generator is used to provide an external reference clock to the SPIDR4 boards to synchronize the 3 of them and the 3 Timepix4.
A PicoTDC is used to precisely measure the timing reference signals and the TLU output signals to precisely correlate the Timepix4 measurements with the ones of the standard MCP-PMTs.

All the instrumentation is powered by a set of programmable Power Distribution Units (PDU).

Each Timepix4 is connected to a different PC, to separate their configuration and acquisition to better organize and manage the high rate expected.
As shown in Figure 8.3, all the other elements are connected through 1GbE cables to a switch 1Gbit, in turn connected to the control PC.

The data are read out through high-speed links, connected to PCIe boards mounted on the PCs connected to the SPIDR4 DAQ systems, forming the *Fast links* subnet.

The three acquisition PCs are linked through 10GbE connections to a 10Gbit switch, in turn connected to the storage PC, as shown in the *Storage* subnet section in Figure 8.3.

Eventually, the control PC and the storage PC are connected to remote PCs, which are the ones placed in the control room.

8.4 DAQ software configuration

The software used is the one described in Section 8.4. In particular, a specific application has been built to be adapted to the test-beam structure, allowing to synchronize the acquisition runs to the beam spills injection.

In particular, the configuration executable has been separated from the acquisition one, allowing to configure the Timepix4 only once within an arbitrary number of spills, while performing different acquisitions, one per spill injected.

The Timepix4 is configured in order to use external T0_sync and external shutter signals. The Extraction Warning signals are sent in input to the TLU, where they are used to generate the external T0_sync signal, and a 5 s long external shutter. Using such a configuration, the acquisition are started right before the spill injection, and stopped at the end of the spill.
The data are stored right after each spill acquisition.

8.5 Preliminary result

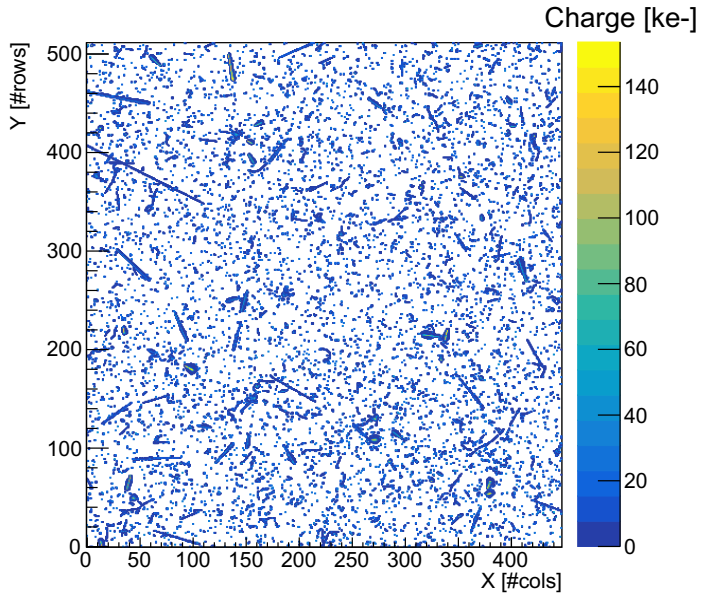
Preliminary results have been obtained promptly during the testbeam campaign, to monitor the quality of the acquired data.

In particular, it has been verified that particles were correctly detected in the two tracking stations, as shown in Figure 8.4a, and that Cherenkov rings were visible in the MCP-PMT device under test, as shown in Figure 8.4b. The integration of the Cherenkov rings above the background photons is evident, and it result to have a radius $R = (8.7 \pm 0.8)$ mm, consistent with the Geant4 simulation performed.

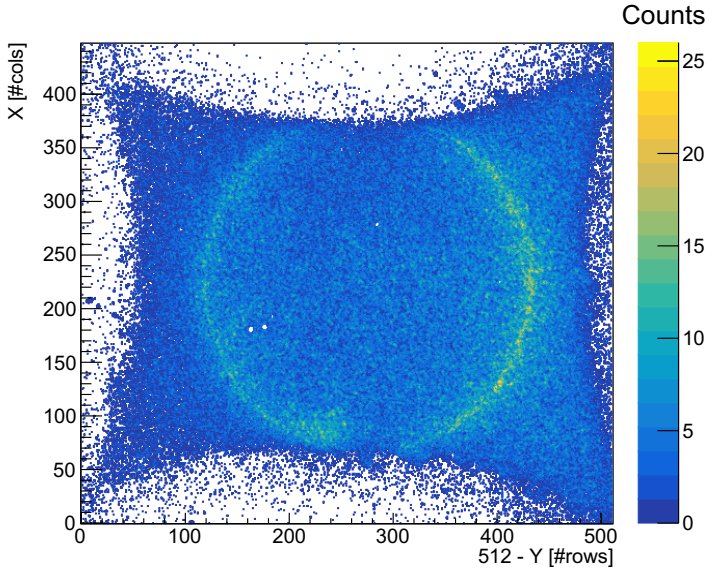
The MCP-PMT used is the v4 prototype, characterised by a Z-stack configuration with 1d end-spoiling, and different high voltage configurations have been tested.

The first tracks have been generated by correlating Cherenkov rings visible on the MCP-PMT to events detected on the tracking system, as shown in Figure 8.5.
A Cherenkov ring is selected among the data of the MCP-PMT, and an average ToA $\mathrm{ToA}_{\mathrm{ring}}$ of the ring photons is computed taking into account just the pixels with a highest charge, to minimize the time-walk effect. Afterwards, events with a ToA included in a window of 500 ns around $\mathrm{ToA}_{\mathrm{ring}}$ are searched to find a candidate track.

More detailed analysis are ongoing to better characterize the tracks timing resolution at different high voltage conditions, exploiting the PicoTDC measurements as well.



(a)



(b)

Figure 8.4: **(a)** Acquisition of a proton spill of 4.8 s on the first tracker, biasing the Si detector at 100 V. **(b)** Acquisition of the photons reaching the MCP-PMT during a proton spill. During the represented run the voltage differences between the MCP-PMT elements have been set to $V_{Tpx4-MCP} = 150\,\mathrm{V}$, $V_{MCP-PHC} = 75\,\mathrm{V}$, and $V_{MCP} = 2100\,\mathrm{V}$, respectively.

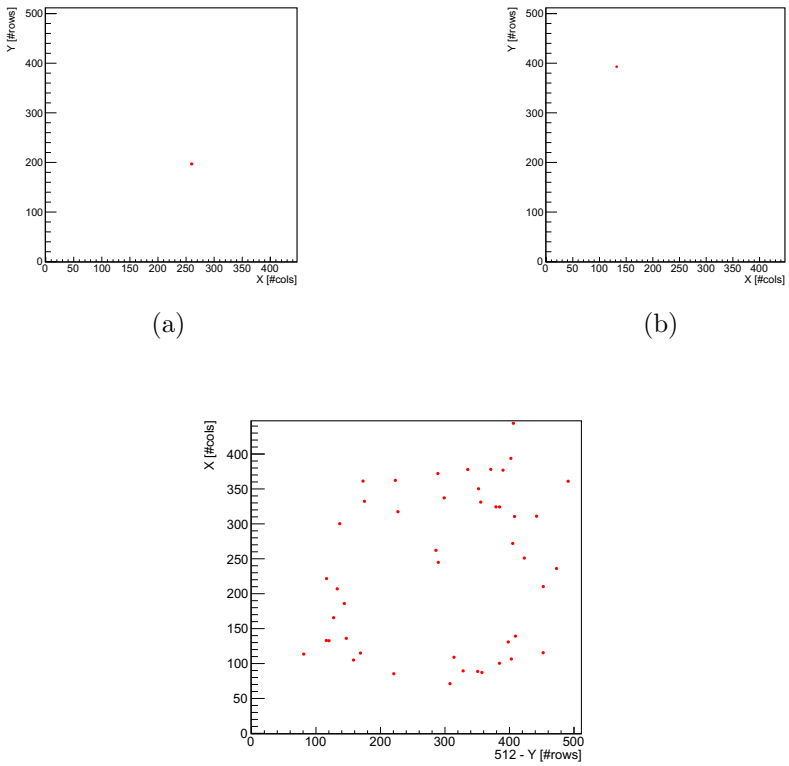


Figure 8.5: Candidate of a complete track observed in the test-beam setup, including **(a)** the beam particle passage in through the first tracker, **(b)** the beam particle passage in through the second tracker, and **(b)** the Cherenkov ring observed detecting the photons produced by the particle.

9

Conclusions

The necessity to develop new single-photon detectors with improved performance has became crucial for the upgrade of high energy physics experiments.
In particular, LHCb RICH Upgrade II will require an improvement on the angular resolution of tracks reconstructions, as well as a timing resolution improvement, aiming to measure single photons with a resolution lower than 100 ps to reduce combinatorial background. The RICH readout must sustain the LHC crossing rate of 40 MHz, requiring fast front-end electronics, a dark count rate lower than 100 kHz/mm^2 and good radiation tolerance.
These new single-photon detectors are required to reach excellent timing performance, to have a high granularity, and to grant a high rate capability.
Currently, the most promising candidates given such requirements are SiPM and MCP based detectors, both granting high granularity and excellent timing resolution. Nonetheless, no existing detectors can fully satisfy the requirements for the Upgrade II of LHCb RICH; thus, an R&D campaign is ongoing to develop new technologies able to cope with those requirements.

Within this framework, the 4DPHOTON project, funded by the ERC, hosted by INFN and supported by CERN and University of Ferrara, is developing a detector able to measure single photons with high spatial and timing resolution on a large active area, keeping a low noise even at room temperature.
Such detectors can also bring great advantages to light imaging applications in medical, biology and material science, or any field where single-photons are re-

quired to be efficiently identified, even with high photon fluxes.
The detector under development is a "hybrid" assembly, based on a vacuum tube housing a photocathode, a Micro Channel Plate, and a Timepix4 ASIC used as pixelated anode with integrated readout. The photons converted into photo-electrons in the photocathode are carried onto the MCP, where they are multiplied; the electron clouds produced by the MCP are spread over the Timepix4 pixels, where the electric signal induced is discriminated, digitised and read out.
The Timepix4 is housed in a ceramic carrier board, connected through a socket to a PCB to communicate with the ASIC.

The project includes the development of a custom DAQ system and a custom DAQ software, including the implementation of procedures to characterize Timepix4 assemblies, ceramic carriers and "hybrid" MCP-PMTs.
A DAQ software has been developed in order to be compatible both with the SPIDR readout system developed by NIKHEF and the custom DAQ system developed by INFN, Ferrara.
Automatic procedures to perform basic diagnostic of the Timepix4 operations have been implemented, such as tests of proper writing/reading operations, DACs scans, thresholds equalization.
The DAQ software and the analysis are currently used by several groups within the Medipix4 collaboration, and INFN groups which took part in the MEDIPIX4 project funded by INFN CSN5.

Firstly, Timepix4 assemblies bonded to silicon sensors were characterised.
A picosecond laser setup has been used to estimate the timing resolution of an assembly bonded to a 100 µm thick n-on-p planar Si detector, resulting on a resolution of 103 ps for a single pixel, which improves up to 33 ps when a weighted average is performed between the ToA of the entire laser cluster.
This study demonstrated that the Timepix4 ASIC allows to read out a detector maintaining a resolution below $\lesssim 100$ ps, and it is a proof of concept of the timing resolution improvement brought by the estimation of clusters' centroid ToA with respect to the single pixel ToA. Furthermore, the developed laser setup and timing resolution estimation procedure are suitable for following studies on the MCP-PMT prototypes or other assemblies bonded to semi-conductor detectors.

An automatic procedure based on the internal analog test-pulse tool has been implemented to perform a ToT calibration against the charge, resulting in a charge resolution going from FWHM/E $= (11.5 \pm 0.7)\,\%$ at E $= 13.9$ keV, to FWHM/E $= (8.4 \pm 0.3)\,\%$ at E $= 32.0$ keV and FWHM/E $= (7.9 \pm 0.2)\,\%$ at E $= 59.5$ keV.
Further characterization studies have been performed on an assembly bonded to

a 500 µm thick p-on-n planar Si detector during a test-beam campaign performed in the ELETTRA facility (Trieste). The aim of this test-beam was to improve of the ToT calibration and to estimate the pixel readout dead-time. Performing a calibration correction based on the X-rays, the charge resolution improved up to FWHM/E = (7.4 ± 0.3) % at E = 30.0 keV, and lower than FWHM/E $\sim$ 6.4% above E $\sim$ 40.0 keV; the pixel readout dead-time resulted to be of the order of $\mathcal{O}(500 - 800\,\text{ns})$, depending on the signal ToT measured.
The characterization of the Timepix4 assemblies bonded to Si detectors allowed to develop a set of procedures to correctly operate the Timepix4 exploiting its features in order to reach optimal performance on timing, spatial and charge measurements. These procedures set the basis for further characterization and analysis that have been carried out by other INFN groups pertaining to the MEDIPIX4 project, other groups included in the Medipix4 collaboration using the DAQ software described. Moreover, it allowed to better understand some Timepix4 features that can be improved in future generations of the Timepix ASIC family.

Three quality test setups have been commissioned in Ferrara, at CERN and in Hamamatsu, to characterize the ceramic carriers produced, and select the ones operating properly, in order to use them on the MCP-PMTs production. The setups comprise a ceramic carrier housing a Timepix4 ASIC, mounted on a custom PCB through a socket, and controlled through a custom DAQ system based on a commercial AMD/Xilinx KCU105 Development Kit control board.
The ceramic carriers quality tests includes mechanical tests, electrical continuity tests, and a diagnostic of the basic operations of the Timepix4 mounted on it, such as the correct operation of clocks, DACs, pixels and readout.

Furthermore, quality test setups have been commissioned in Hamamatsu and Ferrara to test and characterize the MCP-PMTs produced. The photo-tubes are kept within a dark-box, and connected to a DAQ system placed outside the box.
Baseline characterization includes dark count rate (DCR) measurements and gain measurements.
The setup commissioned in Ferrara includes also the laser setup used for the Timepix4 characterization, allowing to measure timing and spatial resolution as well.
Several prototypes have been produced, with different number of MCP stacks and different end-spoiling depth.
A detailed characterization has been performed on one of them, characterized by a Z-stack configuration and a 1d end-spoiling.
The gain is estimated as the average cluster charge measured at fixed high voltage condition. The trend measured is consistent with the expected one, ranging from a gain of $\sim 10^3$ to $\sim 2 \cdot 10^5$, varying the MCP bias from 1950 V to to 2400 V.

The dark count rate is estimated as the number of clusters detected in a 1 s interval. The dark count rate trend is consistent with the expected one as well, ranging from $\sim 1\,\mathrm{Hz/cm^2}$ to $\sim 25\,\mathrm{Hz/cm^2}$ varying the MCP bias from 1950 V to to 2200 V.
The timing resolution measurements performed with the laser setup are analogous to the ones performed with the assembly bonded to the Si detector. A resolution of $\sigma_{ToA-ToARef} = (107 \pm 6)$ ps has been obtained at the single pixel level, improving to $\sigma_{ClusterToA} = (78 \pm 5)$ ps when the entire electron cloud cluster is considered.
The characterization of the first prototype demonstrated that the "hybrid" assembly is working correctly, reaching the expected performance in terms of gain and dark count rate. It has been proved that timing resolution lower than 100 ps are reachable. A better resolution is expected to be obtained optimizing the Timepix4 analog front-end configuration.
The characterization procedure will be repeated on the other prototype versions, to compare the performance and select the best one to be produced.

Eventually, a testbeam has been organised to characterize the tubes with a Cherenkov setup. The testbeam setup includes a tracking system, based on two Timepix4 assemblies bonded to a 300 µm thick Si sensors, a RICH system, with a Cherenkov radiator and an optics system to drive the Cherenkov photons onto the device under test, and a timing system, based on Cherenkov detectors providing precise timing references.
The testbeam campaign has been performed at the CERN SPS North Area facility in October 2024; the beam reaching the experimental setup is composed by $\sim 80\%$ of protons, $\sim 20\%$ of pions, $\sim 1\%$ of muons.
Preliminary results have been obtained, as the measurement of Cherenkov rings and their correlation to the tracking stations events to generate the first tracks, proving that this innovative detector is suitable for use in a RICH detector. Further analysis are ongoing to study the tracks timing resolution using different high voltage configuration on the MCP-PMT tested.

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