Assessing GaN FET Performance Degradation in Power Amplifiers for Pulsed Radar Systems

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***Abstract*— GaN FETs have achieved superior performance in the design of microwave power circuits. Nevertheless, the amount of dispersion related to this technology poses severe issues for the correct modelling and characterization of these devices. In this paper, the effects of GaN FET dispersion on the design of power amplifiers with dynamic power supply, largely adopted in state-of-the-art high-efficiency pulsed radar transmitters, are discussed. In particular, we propose a technique for evaluating GaN device performance degradation in new-generation power amplifiers that represents an effective alternative to pulsed-RF multi-harmonic source/load-pull microwave setups.**

***Index Terms*— GaN FETs, measurement techniques, microwave transmitters, power amplifiers, pulsed radars.**

I. Introduction

GALLIUM Nitride has confirmed its supremacy on other compound semiconductors in all those applications requiring both high-power and high-frequency operation. Nevertheless, with respect to its major competitors at micro- and millimeter-wave frequencies, i.e., Gallium Arsenide and Silicon, more severe dispersive effects are present, which limit its complete exploitation. It is worth noticing that the amount of dispersion in GaN FETs is only partly related to fabrication process maturity while also partly ascribable to the physics behind their operation.

Nowadays, one of the most important application fields of GaN FETs is the design of radar transmitters [1],[2], where power amplifiers (PAs) can benefit efficiently from the advantages related to this technology. Nevertheless, the aforementioned dispersive effects strongly impact the circuit and system performances as extensively documented in literature (e.g., [3]). In particular, when pulsed radar operation is investigated, one of the most promising techniques for increasing the transmitter efficiency is to design PAs operating with dynamic power supplies (DPS) [1],[4]. The idea of DPS consists of varying the device bias condition according to the RF signal amplitude to continuously guarantee high-efficiency transistor operation. Due to the required pulse shape, with typically pulse width of tens of microseconds and duty cycle less than 10%, both in-pulse and pulse-to-pulse [5] transistor operations depend not only on the instantaneous voltages applied at the device ports but also on the thermal and trap-occupation states that introduce long-lasting time constants [6],[7]. As a matter of fact, carrier emission mechanisms are characterized by time-constants in the order of milliseconds, much slower than the time-constants associated with the capture mechanisms. As far as pulsed operation is concerned, carriers can remain trapped for several pulses, thus strongly affecting the device behavior over time. Therefore, transistor characterization carried out under traditional CW operation is not adequate when DPS operation is involved.

Clearly, the most appropriate solution is to measure the transistor behavior directly under actual pulsed operation with DPS and modulated RF signals [3]; examples of setups that could achieve such operating conditions at transistor level are reported in [8],[9]. Nevertheless, this solution, besides requiring a special purpose setup, experiences the inherent limitations related to nonlinear measurements at microwave frequencies in terms of costs, frequency, and power. Even using pulsed-bias S-parameters [10] cannot provide adequate results, since one cannot properly set the trap state induced by the DPS instantaneous drain-gate voltage peak [3]. On the other hand, pulsed S-parameter measurements based on newly introduced pulsed-I/V setups that enforce the trap state by very fast pre-pulses [11] could provide more consistent results, although such a characterization is still under development.

As an alternative, we propose to infer the actual performance of GaN transistors in pulsed radar operation by performing new, ad hoc experiments based on a recent measurement technique [12] and analyzing the results. Such a technique allows one to fix the thermal and trap-occupation states by means of a suitable load line synthesized at few megahertz and then to measure the S-parameters at microwave frequencies along all the *dynamic-bias* points belonging to the selected load line. In fact, due to the instantaneous modulation of the trap state forced by the dynamic drain-gate voltage peak [6],[7], the transistor small-signal behavior at each dynamic-bias point does not correspond to that measured under CW operation. As a matter of fact, the low-frequency (LF) load line mimics the PA DPS operation where, due to the slow de-trapping mechanisms, in-pulse and pulse-to-pulse regimes are set by the modulation of the trap state induced by the instantaneous drain-gate voltage peak [3].

Manuscript received July 23, 2018; accepted August 22, 2018. *(Corresponding author: Antonio Raffo.)*

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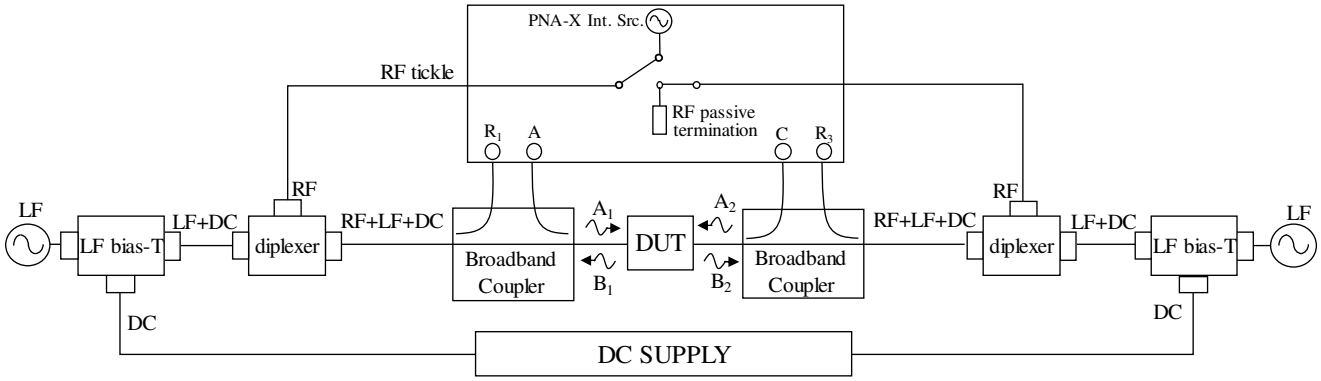


Fig. 1. Schematic of the setup adopted to measure dynamic-bias S-parameters. It consists of: a 10 MHz – 67 GHz Keysight PNA-X, a two-channel Tektronix arbitrary function generator to generate the LF signals, broadband bi-directional couplers with high-pass frequency response, broadband diplexers to combine DC, LF and RF paths, and bias-tees to separate DC and LF paths.

II. MEASUREMENT SYSTEM

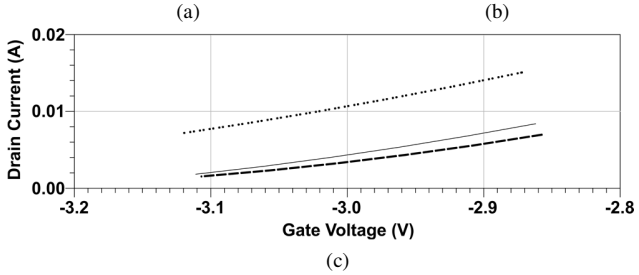
The measurement setup used for the characterization is shown in Fig. 1 and it consists of a 10 MHz – 67 GHz Keysight PNA-X. Under dynamic-bias operation, the device-under-test (DUT) is excited at its input and output ports simultaneously by an LF (i.e., in the range of megahertz) large signal and a high-frequency small signal, as illustratively shown in Fig. 1.

The LF signals are applied with an arbitrary function generator, and, combined with the DC bias voltages, set the large-signal operating point (LSOP) of the DUT. As the frequency of the LSOP is in the megahertz range, it actually allows synthesizing a specific load line at the transistor current source [7]. On top of the LF LSOP, an RF tickle is applied with the internal RF source of the PNA-X. This tickle, whose power is much lower than the LSOP power, is switched between the input and output ports in the frequency range of interest, with the other port terminated with a passive load, to allow the extraction of S-parameters under dynamic-bias operation at each RF frequency [12]. Intuitively, this measurement can be compared with the classical S-parameter measurement, where the LSOP is set by the DC bias voltages and the RF-tickle is the small-signal excitation used to get small-signal parameters. When, instead, the LSOP is not a constant and it is a slowly varying bias point, the parameters gathered by means of this measurement are named “dynamic-bias S-parameters”. The theoretical background for the calculation of dynamic-bias S-parameters is described in detail in [12].

To perform the measurements that we report in this paper, we used external couplers in front of the PNA-X receivers as the power levels of the LF signals exceeded the instrument test-ports maximum ratings. Moreover, the couplers that we used show a high-pass coupling characteristic, and this helped us to equalize the LF and HF signals to improve receiver sensitivity. The DC bias voltages, the LF, and the RF tickle signals are combined by means of LF bias-tees and broadband diplexers.

III. EXPERIMENTAL RESULTS

We performed dynamic-bias S-parameter measurements on a 0.25-µm GaN on SiC transistor with 200-µm periphery at the fixed bias V_{d0} = 20 V, V_{g0} = -2.75 V, I_{d0} = 15 mA, which corresponds to class-AB bias. Fig. 2 shows the synthesized LSOP load lines and the related drain-gate voltage loci. In these experiments the LF was set at 15 MHz, the amplitude of the input LF signal was kept constant, whereas the amplitude of the output LF signal was swept maintaining constant their relative phase. The power of the tickle was set equal to -30 dBm and f_{RF} was swept from 1 GHz to 30 GHz. For each LSOP, the dynamic-bias S-parameters were gathered for all the dynamic voltage values (v_g, v_d) dynamically reached along the LSOP. In this experiment, we focused on the dynamic-bias point at v_g^* = -3 V, v_d^* = 22.5 V, which is dynamically touched by all the LSOPs that we synthesized, as shown in Fig. 2 (filled circle). This dynamic-bias point corresponds to deep class-AB operation, and it is very sensitive to device dispersion, as demonstrated in Fig.2 (c) reporting the dynamic drain current as a function of the gate voltage around v_g^*. As expected [6], due to fast trapping effects, the current lowers as the drain-gate voltage peak increases.



(c)

Fig. 2. Measured LSOPs at V_{d0} = 20 V, I_{d0} = 15 mA and f_{LF} is 15 MHz. (a) Load lines and (b) drain-gate voltage loci, and (c) drain current as function of gate voltage around v_g^*. The filled circle in (b) marks the dynamic-bias point touched dynamically by each LSOPs.

As previously discussed, device dispersion causes important deviations between CW and actual device operation that

inevitably increase PA distortion under DPS operation [3],[5]. It is worth noticing that each LSOP corresponds to different trap and thermal states. Consequently, we can expect that at (v_g^*, v_d^*) the dynamic-bias S-parameters S_{21} and S_{22}, which are the most sensitive to dispersive phenomena, differ from the S-parameters measured with a VNA at the same bias-point applied statically. On the other hand, we do not expect to observe any significant difference between the dynamic-bias and the static-bias S_{11}. The S_{11} parameter is strongly linked to the transistor input capacitance, which is typically not affected by dispersion, as empirically shown in many works [6],[7]. Fig. 3 shows the dynamic-bias S_{21}-parameters measured at the dynamic-bias point (v_g^*, v_d^*) shown in Fig. 2. For the same device we measured also conventional S-parameters with a VNA at $V_{g0} = v_g^*$, $V_{d0} = v_d^*$. As can be seen in Fig. 3, the magnitude of the dynamic-bias S_{21} parameter differs from the static-bias S_{21} and decreases as the peak of the drain-gate voltage increases on the different synthesized LSOPs due to fast charge trapping induced by the maximum electric field in the channel [6],[7]. More importantly, the transistor gain slump shown in Fig. 3 is the origin of the effects documented at circuit [3] and system [5] levels for transmitters based on GaN PAs with DPS. These results represent a worst-case scenario assuming the trapped charges in the device do not have time to recover to any degree.

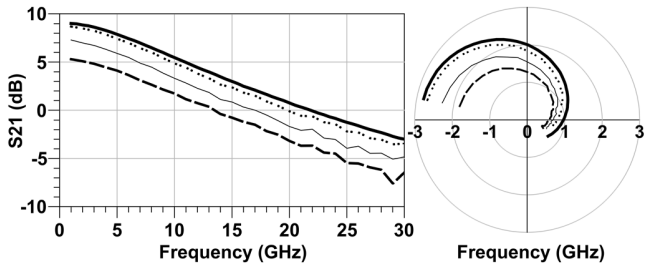


Fig. 3. Measured dynamic-bias S_{21}-parameters from 1 GHz to 30 GHz at the dynamic-bias point v_g^* = -3 V, v_d^* = 22.5 V, marked on the LSOP trajectories in Fig. 2, corresponding to a different instantaneous drain-gate peak (see Fig. 2b). Measured classical S-parameters (thick continuous line) at DC bias V_{g0} = -3 V, V_{d0} = 22.5 V.

Fig. 4 shows the S_{11} and S_{22} parameters measured by a VNA and by the setup in Fig. 1. As expected, we do not observe any significant difference in the S_{11} parameter, whereas small differences can be appreciated in the S_{22} parameter. As for the dynamic S_{21} parameter, this difference is due to the different trap and thermal states between the VNA measurement, where the trap and thermal states are determined only by the DC bias voltages, and the dynamic-bias operation, where the trap and thermal states depend on the dynamic LSOP.

As a matter of fact, Figs. 3-4 give a clear insight on the maximum degradation of transistor performance under DPS operation compared to standard CW operation. This could represent a valuable information for PA designers, posing an additional constraint on the load-line selection.

IV. Conclusion

High-efficiency radar systems require the design of advanced PAs under new operating modes. When GaN FETs are used for the design of such systems, dispersion mechanisms can significantly reduce the system performance. In this paper we report experimental data that, by mimicking the transistor behavior under actual operation, represent a valuable insight for evaluating the impact of dispersion effects and designing circuits that reduce the gap between estimated and actual system performance.

(a) (b)

Fig. 4. Measured dynamic-bias (a) S_{11}- and (b) S_{22}-parameters from 1 GHz to 30 GHz around the dynamic-bias point v_g^* = -3 V, v_d^* = 22.5 V, marked on the LSOP trajectory in Fig. 2. Measured classical S-parameters (thick continuous line) at DC bias V_{g0} = -3 V, V_{d0} = 22.5 V.

References

[1] E. McCune, "Nonlinear applications at the transmitter system level," in *Microwave Wireless Communications: From Transistor to System Level*. Oxford, U.K.: Academic, 2016, ch. 7.

[2] M. Rodriguez, *et al.*, "Resonant pulse-shaping power supply for radar transmitters," *IEEE Trans. Power Electron.*, vol. 29, no. 2, pp. 707–718, Feb. 2014.

[3] C. Florian, *et al.*, "A prepulsing technique for the characterization of GaN power amplifiers with dynamic supply under controlled thermal and trapping states," *IEEE Trans. Microw. Theory Techn.*, vol. 65, no. 12, pp. 5046–5062, Dec. 2017.

[4] A. Zai, *et al.*, "Supply-modulated radar transmitters with amplitude-modulated pulses," *IEEE Trans. Microw. Theory Techn.*, vol. 63, no. 9, pp. 2953–2964, Sep. 2015.

[5] J. Delprato, *et al.*, "Measured and simulated impact of irregular radar pulse trains on the pulse-to-pulse stability of microwave power amplifiers," *IEEE Trans. Microw. Theory Techn.*, vol. 62, no. 12, pp. 3538–3548, Dec. 2014.

[6] O. Jardel, *et al.*, "An electrothermal model for AlGaN/GaN power HEMTs including trapping effects to improve large-signal simulation results on high VSWR," *IEEE Trans. Microw. Theory Techn.*, vol. 55, no. 12, pp. 2660–2669, Dec. 2007.

[7] A. Raffo, *et al.*, "Behavioral modeling of GaN FETs: A load-line approach," *IEEE Trans. Microw. Theory Techn.*, vol. 62, no. 1, pp. 73-82, Jan. 2014.

[8] Jad Faraj, *et al.*, "Pulse profiling for AlGaN/GaN HEMTs large signal characterizations," in *Proc. 38th Eur. Microw. Conf.,* Oct. 2008, pp. 757–760.

[9] M.A. Casbon, *et al.,* "Waveform engineering beyond the safe operating region: fully active harmonic load pull measurements under pulsed conditions," in *IEEE Compound Semiconductor Integrated Circuit Symposium (CSICS)*, Oct. 2011, pp. 1-4.

[10] J.-P. Teyssier, *et al.*, "40-GHz/150-ns versatile pulsed measurement system for microwave transistor isothermal characterization," *IEEE Trans. Microw. Theory Techn.*, vol. 46, no. 12, pp. 2043–2052, Dec. 1998.

[11] A. Santarelli, *et al.*, "A double-pulse technique for the dynamic I/V characterization of GaN FETs," *IEEE Microw. Wireless Compon. Lett.*, vol. 24, no. 2, pp. 132–134, Feb. 2014.

[12] G. Avolio, *et al.*, "Dynamic-bias S-parameters: a new measurement technique for microwave transistors," *IEEE Trans. Microw. Theory Techn.*, vol. 464 no. 11, pp. 3946–3955, Nov. 2016.