Phase Change and Magnetic Memories for Solid State Drives Applications

Cristian Zambelli, *Member, IEEE,* Gabriele Navarro, Véronique Sousa, *Member, IEEE,* Ioan Lucian Prejbeanu, *Member, IEEE,* and Luca Perniola, *Member, IEEE*

***Abstract*—The state-of-the-art Solid State Drives now heterogeneously integrate NAND Flash and DRAM memories to partially hide the limitation of the non-volatile memory technology. However, due to the increased request for storage density coupled with performance that positions the storage tier closer to the latency of the processing elements, NAND Flash are becoming a serious bottleneck. DRAM as well are a limitation in the SSD reliability due to their vulnerability to the power loss events. Several emerging memory technologies are candidate to replace them, namely the Storage Class Memories. Phase Change Memories and Magnetic Memories fall into this category. In this work, we review both technologies from the perspective of their possible application in future disk drives, opening up new computation paradigms as well as improving the storage characteristics in terms of latency and reliability.**

***Index Terms*—Solid State Drives, Phase Change Memories, Magnetic Memories, PCM, MRAM, SSD, Applications**

I. INTRODUCTION

A. *Solid State Drives: the limitations of NAND Flash*

Solid State Drives (SSDs) are a consolidated storage platform in many applications ranging from consumer to enterprise scenario. The increased production of data, especially in the latter case, is pushing for denser, faster, and more reliable memory architectures in the storage tiers. The core medium in state-of-the-art SSDs is the NAND Flash memory technology, therefore the figures of merit of a drive are largely dictated by those of the Flash. Their continuous technology scaling to provide larger storage densities is however exposing a struggle for achieving an inherent level of reliability and performance suitable for SSDs.

The research activities for NAND Flash products development are in the direction of coping specific physical and architectural issues appearing at a nanoscale level that severely hinder their reliability [1]–[3]. However, new applications based on SSDs may find these attempts barely acceptable. To this extent, sophisticated memory controllers need to be embedded in the drive to hide the weaknesses of NAND Flash by reducing their failure rate especially for multi-level technologies. The lifetime of the storage blocks in the Flash, also known as the endurance (measured in sustainable Program and Erase cycles without producing uncorrectable errors), reduces by one or two orders of magnitude stepping from a Single Level Cell (SLC) to a Multi Level Cell (MLC) architecture [4]. Therefore, additional erase operations triggered by specific NAND Flash medium management (i.e., garbage collection) need to be carefully avoided to minimize the time to failure. Non-volatility of the data is hampered as well since the data retention on aged blocks is drastically reduced in MLC NAND Flash, therefore requesting frequent refresh (i.e., scrubbing) of the data with consequent power consumption and performance burdening [5]. Wear Leveling algorithms to spread the wear-out over the entire memory needs to be implemented to avoid block failures after few seconds as well as powerful Error Correction Codes (ECC) for transient failures [6].

Performance drawbacks of NAND Flash are also a concern. Their read and write speed are becoming inadequate in all the situations where the data responsiveness is critical. The programming of a single page of data (i.e., from 4 kB to 16 kB) and the erase of a block (i.e., few MB) may take up to several milliseconds in ultra-scaled multi-level products [7], whereas the data read is often in the range of hundreds of microseconds. To this latter time we must add the latency of the ECC to correct the corrupted data due to the poor reliability, forcing mostly a trade-off between achievable performance and lifetime enhancement [8], [9]. A solution for performance improvement is in the heterogeneous integration in the SSD of Dynamic Random Access Memories (DRAMs) to be used as cache buffers. However, DRAM cost and power requirements are limiting their amount in the range of few gigabytes for corresponding multi-terabyte NAND Flash SSDs.

The advent of three-dimensionally integrated NAND Flash (i.e., 3D NAND) [10] seemed to alleviate such a trade-off, but not the need for the DRAM to cope with the performance disparity between the host system and the SSD. Reliability is however still a concern [11].

B. *The need for a Storage Class Memory*

Next-generation SSDs should base on non-volatile memories (NVMs) that are able to provide at the same time higher performance and better lifetime figures than NAND Flash. Ideally, the performance should be that of DRAMs, but with the non-volatility, robustness, and low-cost features competitive with conventional magnetic storages (HDDs). Such a memory technology should also devise an easier scaling path to reach higher storage density, but keeping the offered reliability relatively unaltered. The term that was introduced

This work has been partially supported by the Università degli Studi di Ferrara through the initiative Bando per il finanziamento della ricerca scientifica "Fondo per l'Incentivazione alla Ricerca" (FIR) - 2016.

C. Zambelli is with Dip. di Ingegneria, Università degli Studi di Ferrara, Via Saragat 1, Ferrara (Italy), 44122. (e-mail: cristian.zambelli@unife.it)

V. Sousa, G. Navarro, and L. Perniola are with CEA, LETI, Minatec CAMPUS, 17 rue des Martyrs, 38054 Grenoble Cedex (France)

I.L. Prejbeanu is with University Grenoble Alpes CEA - CNRS, SPINTEC, F-38000 Grenoble (France)

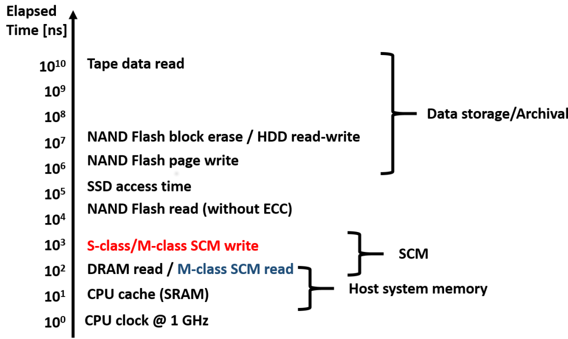


Fig. 1. Typical access times of different storage systems and memories. SCM performance is highlighted for comparison. Data from [13].

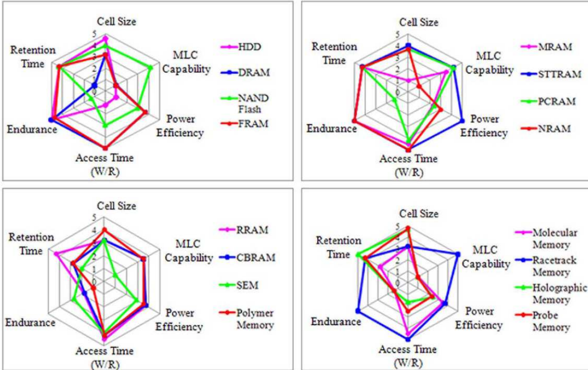


Fig. 2. Features assessment of several SCMs candidates along with NAND Flash and HDDs (reproduced with permission from [14]).

in literature for these memories is Storage Class Memories (SCMs) [12].

SCMs would bridge the gap between the access time of a storage system like an SSD and that of the memories like Static RAM (SRAM) or DRAM closer to the processing elements in the host system (Fig. 1). The target density of an SCM has to exceed the terabits capacity achievable by multi-level NAND Flash to be at least cost-competitive, while at the same time guaranteeing the attractive scaling features introduced by the 3D technology.

Given the mentioned features, the SCM integration in an SSD can be then broken into two different segments [12]: a total replacement of the Flash storage backbone or a coupling/replacement of the DRAM cache. For both solutions the idea is to have a hybrid SSD (i.e., traditional memories and SCMs) that gets performance metrics closer to that of the host system producing the data to store. The NAND Flash replacement could be possible with the slower variant of the SCM called S-class (i.e., Storage-class) [12]. These memories will have the same interface and access modes of NAND Flash except for the highest endurance and lower access times (acceptable access times are in the range of few microseconds), therefore requiring a dedicated memory controller whose functionalities are most legacy. High density is their utmost sought feature. The DRAM cache replacement could be achievable on the other hand by the fastest SCM variant called M-class (i.e., Memory-class) [12]. This memory class would require

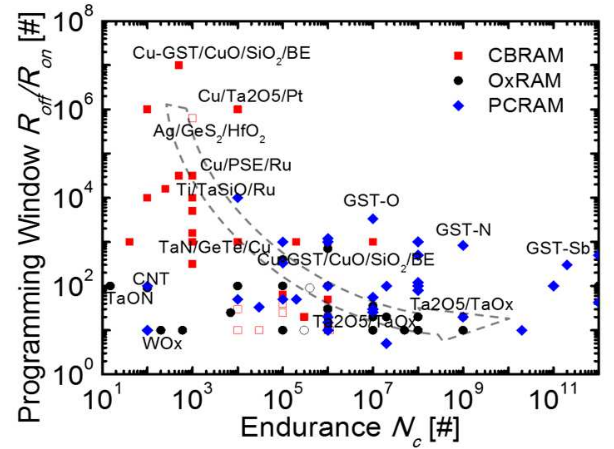


Fig. 3. Universal plot of the programming window versus the endurance capabilities of different SCMs (reproduced with permission from [15]).

access times in terms of hundreds of nanoseconds or less to be synchronous with the normal memory operations of the host system, but with specific power consumption considerations to take into account. Since M-class SCMs would never be faster than a DRAM cache they will not fully replace those memories in SSDs, but rather, their non-volatility feature will allow the total DRAM amount reduction with consequence on system cost and power consumption [13].

C. Phase Change and Magnetic Random Access Memories: an opportunity as SCM for SSDs

Several emerging non-volatile memory technologies have been studied by researchers and industries in the last decades (see Fig. 2). The most accredited are Resistive Memories (RRAM) using either native oxides or the conductive bridge paradigm, Phase Change Memories (PCM), and Magnetic Memories in the Spin-Transfer Torque realization (STT-MRAM) [15], [16]. Each of these technologies features peculiar advantages and drawbacks compared to DRAM and NAND Flash memories, although they target in common the SCM concept. The researchers observed that by looking into more detail on the single emerging memories there is an universal signature on their usage models and characteristics, despite from the very different physical principles ruling them. Their write speed, power consumption, and reliability metrics like endurance and data retention are related to each other following a global metric [15]. As an example, let us consider the case of PCMs. A trade-off seems to link the programming time for a write operation with the device data retention performances: the longer the time needed to operate a fine data write, the better the data retention will result [15], [17]. At the same time, we can appreciate the relationship between the programming window (i.e., metric for understanding how easy is to discriminate between stored logical bits in a memory cell) and the endurance capabilities of different phase change materials: larger programming window is typically associated to poor endurance capabilities [18] (see Fig. 3). Additionally, the better are the performances in endurance, the poorer is the data retention capability due to the low programming

window [15]. This means that before using these memories as an SCM or prior to design SSDs by integrating them into the system we must understand the trade-offs to be leveraged on. Requirements for M-class memories (i.e. high endurance and fast speed) are completely different from requirements for S-class memories (i.e., long data retention and acceptable endurance).

In this work we will review PCM and STT-MRAM technologies to understand their possible usage in SSD applications by considering these implications. This paper is organized in four sections spanning from physical considerations on each memory technology up to architectural constraints and design of SSDs. Section II describes the PCM technology. The considerations on materials exploited for the memory integration will expose a trade-off between using the PCM as an S-class or an M-class SCM. An insight in the reliability features of PCM in terms of endurance, data retention, and specific issues like disturb is presented an compared to the typical figures of merit of state-of-the-art Flash technology. Architectural and scaling constraints will follow by showing the main limiting factors in large densities achievement. Section III is dedicated to STT-MRAM. A review of the operation principles of this technology will be given as well as their integration capabilities. Reliability metrics will show the memory affinity to a specific SCM application. In Section IV, a set of possible applications of PCM and STT-MRAM in an SSD will be described ranging from hybrid storage with fully replaced NAND Flash up to DRAM backed-up caches for power-loss resilience improvement. Finally, in Section V we will draw some conclusions.

II. Phase Change Memories

Phase change memories (PCMs) are among the most promising technologies for future generations of Non-Volatile Memories (NVMs). The principal advantages of this technology are the low programming voltages, the very short reading and programming times, the good shrinking prospects and the low manufacturing cost due to the reduced number of required masks levels. To-date, the performances of several products have been published: Numonyx [19] and Hynix [20] presented a 1Gb memory while Samsung [21], [22] reported the results obtained with an 8Gb memory. Technology developments have also reached a high maturity level, thus enabling the first PCM product introduction as memory chips in cell phones [23].

The operating fundamentals of a PCM device rely on the amorphous to crystalline phase transformation of a small volume of phase change material. PCMs owe their success to the unique combination of properties of the phase change materials, among which the large electrical contrast between the amorphous and the crystalline phase, the high crystallization speed of the amorphous phase and the stability of the two programmed states at the user time scale. The PCMs concept was originally proposed in the 60's [24] referring to the alloy $Ge_{10}Si_{12}As_{30}Te_{48}$ as a switching material. Later, in the 80's, research works highlighted the ternary system GeSbTe with different compositions located on the pseudo-binary-line $GeTe/Sb_2Te_3$ and allowing crystallization times as

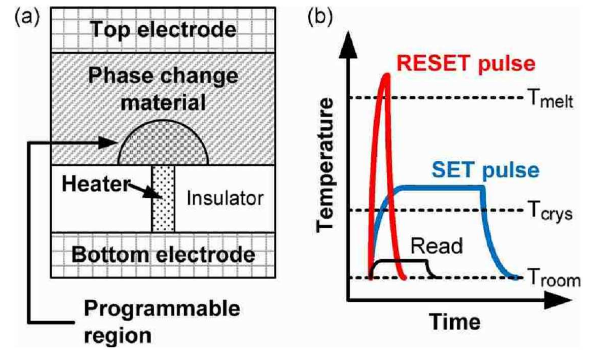


Fig. 4. (a) The simplified scheme of a PCM cell. The voltage applied between the top and the bottom electrode enables the current flow in the phase-change material. The active volume considered by the phase change transition is at the interface between the phase-change material and the heating element (i.e., heater). (b) Joule heating in the PCM cell makes possible the different programming/reading operations. The temperature is kept low during Read, the crystallization temperature of the phase-change material is achieved during SET operation and the melting temperature is reached during RESET operation (reproduced with permission from [27]).

short as a few tens of nanoseconds [25]. The stoichiometric compound $Ge_2Sb_2Te_5$ (i.e., GST) was initially developed for optical disks, taking advantage of the wide optical contrast between the ordered and disordered phases, before being used in the late 90's for PCM memory devices exploiting its large electrical contrast. On that date, this material had demonstrated an excellent endurance (over 10^{13} write/erase cycles) as well as the ability to store multiple levels of information in a memory [26]. However, PCM devices based on GST are not able to achieve the thermal stability required for high operating and storage temperature applications (e.g., automotive and industrial). Besides, high performance applications such SSDs and servers require high speed (i.e., high programming speed and low access time) and low programming current. In recent years, phase change material engineering focused in the GST system has enabled the optimization of the device performance in various directions, allowing to achieve either a reduction of the programming current, an increase of the programming speed or an enhancement of the thermal stability of the programmed states.

A. *Materials and operation principles*

A PCM is an array of memory dots in which each node of the array corresponds to a storage element placed in series with a selector element. The storage element is a variable resistor made of a small volume of phase change material sandwiched between two electrodes (see Fig. 4). The binary information is encoded through the phase of the material, the latter being either amorphous or crystalline. The reading operation is based on the difference in the electrical resistivity presented by the two states, the crystalline phase typically being 10^3 times more conductive than the amorphous phase. As for the writing operation, a programming pulse is applied to the storage element through a so-called *heater*, so that a portion of the phase change material is heated up by Joule effect. The adjustment of the magnitude and the duration of

this pulse allows switching between amorphous and crystalline states as follow:

- for the high resistance amorphous state known as the *RESET* state, the application of a programming pulse of short duration and high intensity heats up the phase change material above its melting temperature T_m. The geometry of the device and the thermal properties of the materials surrounding the active area are optimized in such a manner that the molten zone is rapidly quenched at a rate of more than 10^{10} K/s after the write pulse, thus resulting in the amorphous state at the end of the write operation;
- to obtain the low resistance crystalline state, known as the *SET* state, a programming pulse of longer duration but lower intensity is applied, thus heating up the phase change material in a temperature range between the glass transition temperature T_g and T_m. This allows the material to transform into a thermodynamically stable or metastable state, which is the crystalline phase.

The duration of the programming pulses required for the amorphization and for the crystallization are in the order of a few tens of nanoseconds, these durations being respectively governed by the thermal inertia of the cell which controls the time necessary to reach the melting of the phase change material and by the time required for the atomic rearrangements required for crystallization. These two transformations occur independently of the initial state of the material, thus allowing a direct programming operation, without any initialization step that would be time consuming.

The first property of the phase change materials required for the storage of a binary information in a PCM memory is the difference in electrical resistivity between the amorphous phase and the crystalline phase. Fig. 5 shows the variation of the electrical resistivity versus temperature for two typical phase change materials based on stoichiometric compounds: GST and GeTe. The sharp drops in resistivity observed respectively at $150°C$ and $180°C$ correspond to the crystallization of the materials. In both cases, the resistivity difference between the amorphous and crystalline phases exceeds several orders of magnitude.

Another fundamental characteristic of a phase change material is the electronic switching of the amorphous phase. As already mentioned, in the PCM memory devices, the transition between the amorphous and the crystalline phase is induced by the Joule effect resulting from the application of a programming pulse to the storage element. The Joule heating of the amorphous phase is only possible thanks to the electronic switching behavior observed when the amorphous material is submitted to a sufficiently high electric field [29]. In fact, the high resistivity of the amorphous material observed at low currents is explained by a Poole-Frenkel conduction mechanism in deep traps, while the threshold switching to the low resistivity observed at high electric fields is explained by a non-equilibrium population of shallow traps, and a substantial non-uniformity of the electric field in the amorphous layer. To illustrate this phenomenon, the schematic current-voltage characteristic presented in Fig. 6 tracks the evolution of a

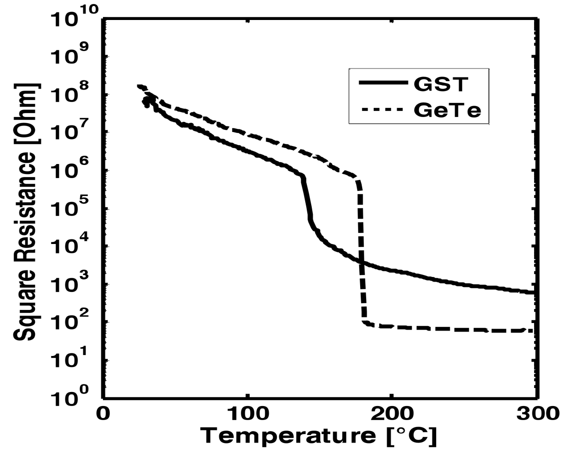


Fig. 5. Electrical resistivity variation as a function of the temperature for initially amorphous thin films of GST and GeTe (reproduced with permission from [28]).

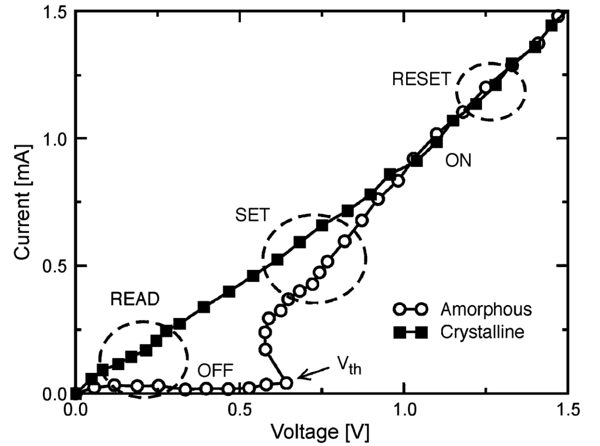


Fig. 6. Typical current-voltage characteristics of SET and RESET switching in PCM with the threshold switching voltage (V_{TH}) highlighted (reproduced with permission from [30]).

device initially in the RESET state: at low voltage, the current does not pass through the high resistance amorphous phase, so that Joule heating is negligible. However, there is a steep change at the voltage V_{TH} beyond which the amorphous material becomes conductive [30], [31]. For writing, electric pulses are applied at a higher voltage than the threshold voltage V_{TH} with a limitation of the current intensity. The pulse duration and the value of the current compliance govern the thermal stress applied to the storage element, thus resulting in the crystallization or amorphization of the phase change material.

B. Performance and reliability

1) Read/Write speed: in a PCM device, the speed of the writing process is primarily controlled by the crystallization kinetics of the material that affects the speed of the SET operation [32], [33]. At the same time, the crystallization kinetics has a strong impact on the thermal stability of amorphous phase. This relationship represents a conflict that is partly

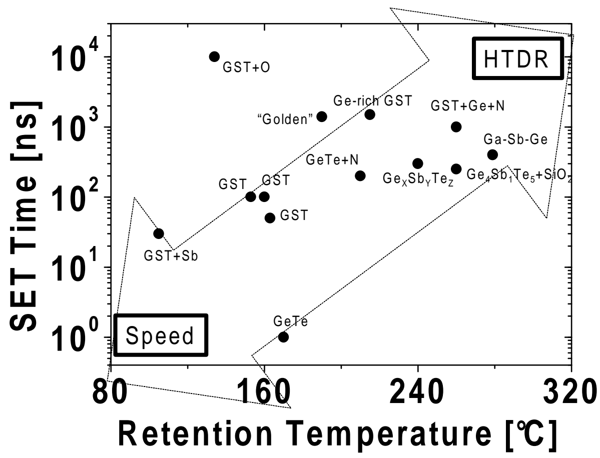


Fig. 7. Correlation between SET time and high temperature data retention (HTDR) of the RESET state in PCM devices based on different phase-change materials (reproduced with permission from [15]).

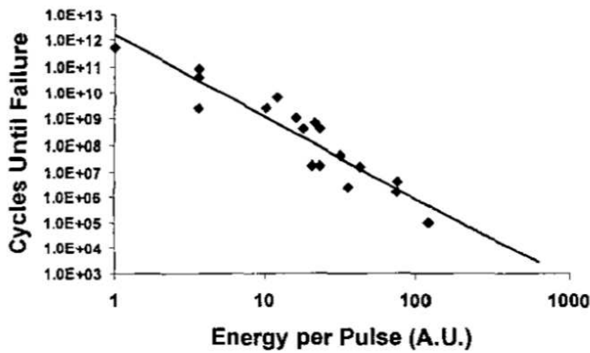


Fig. 8. Cycling endurance as a function of pulse energy, showing the strong correlation between the device failure and the cumulative energy delivered to the device during all the programming operations (reproduced with permission from [34]).

solved by the dependence in temperature of the crystallization speed which, on the one hand, helps to ensure the stability of the amorphous phase at the low temperatures used for memory retention, and, on the other hand, a high crystallization speed at the high temperatures used for memory programming. So far, dedicated materials have been engineered to ensure either a high writing speed targeting for example SSD applications, or a high thermal stability of the programmed states as required in embedded applications. This trade-off between speed and high temperature data retention (HTDR) is represented in Fig. 7 where the SET speed and the retention temperature are reported for PCM devices found in the literature based on different phase change materials.

The RESET operation is almost never taken in account in the programming speed analysis, since the solid to melted transition of the active volume of the device is considerably faster than the crystallization process and it often reaches the limits of the experimental equipments.

Crystallization times as small as a few nanoseconds have been demonstrated in GeTe [35]. Several interpretations have been proposed to account for these very short crystallization times [36], [37]. Note first that the phase change materials such GST or GeTe are stoichiometric compounds for which crystallization proceeds without any change in composition. In this case, the crystallization does not require long-distance diffusion of chemical species, which is a priori favorable to rapid crystallization process. Furthermore, the microstructure of the amorphous and crystalline phases plays a major role in the rate of crystallization. Thus, rapid crystallization phenomenon appears to stem from the similarities between the short range order (SRO) of the crystalline phase and the amorphous phase. Lencer et al. [38] concluded, from both atomistic calculations and experimental characterizations, that the amorphous and crystalline phases have a similar energy and short range order, while having a very different density of states, thus explaining the electrical contrast between the two phases.

2) Endurance: in NAND Flash the cycling of the memory cell relies on the charging and discharging of a storage layer, made possible by the electron tunneling through a thin oxyde layer. The endurance of NAND Flash is then impacted by the gradual oxide degradation induced by this charge flow during programming operations. For those memories this degradation occurs already after 10^3-10^5 cycles. On the contrary, PCM technology is well known for its capability of high cycling endurance up to more than 10^8 cycles [39]. The scaling of the PCM device must preserve the endurance performance, and it can be achieved only with the engineering of the interfaces/materials and of the optimization of the deposition quality of the materials, as the dimension of the active volume of the PCM device decreases. During programming operations the phase change material reaches the melting temperature and, even if the pulse is applied for few nanoseconds, the cumulative effect can lead to mechanical failures such as: delamination, cracks, local material stoichiometry or density changes (e.g., phases segregation), atomic diffusion, and materials inter-diffusion [40]–[45]. If stoichiometric compositions are known to maintain their composition even in the melted phase (e.g., GeTe, GST), non-stoichiometric compounds can more likely undergo phase segregation phenomena.

Loss of the phase-change mechanism can be attributed to:

- the high temperature gradient generated in the material during the RESET operation, that gives rise to strong volumetric variations. It causes a mechanical stress that in the long run can be detrimental, causing voids (responsible of a stuck at high resistance) or local material stoichiometry changes;
- the interaction with materials of the interfaces, generating unwanted compounds (e.g., diffusion of the metals of the electrodes in the phase change material);
- phase change material contamination (e.g., presence of oxygen) that even in small atomic percentage in the long run can cause the cell failure;
- phase separation generating stable compounds, but with physical and chemical properties different from the starting material (often responsible of a stuck low resistance).

In Fig. 8 the endurance of a PCM device is put in correlation with the total energy delivered to the material during all the programming operations. The higher is the pulse duration, the faster is the reaching of the cell failure state. This is in particular valid for the RESET operation that requires a

higher power consumption, with respect to SET operation, to completely melt the active volume of the cell.

Another phenomenon that can contribute to the cell failure is the phase elemental separation due to the different electronegativity of the atoms [46]. It is induced by the electric field applied on the active volume during the programming operation, that can provide an atomic displacement along the material thickness, inducing the loss of the phase-change properties.

3) Data retention: the retention of the charge accumulated in the storage layer of a NAND Flash memory depends on the quality of the oxide layer. The higher is its degradation along the cell life, the higher is the charge loss. As reported in [47], life time of NAND Flash is reduced by cycling and high temperature conditions. The specification of 10 years of data retention can be ensured at 95°C only in fresh SLC cells, while this temperature decreases at 55°C after 10^4 cycles. In MLC cells these specifications are even more relaxed [7].

Improving the stability of the written SET and RESET states (and then their retention) has been one major challenge in the development of PCM devices. Indeed, the thermal stability of the SET and RESET states can be compromised at high temperature by two physical phenomena:

- the ordering of the disordered phase material, meaning the crystallization of the amorphous material [48]. This crystallization is accompanied by a decay of the resistance of the device and can lead to the loss of the high resistance or RESET state;
- the structural relaxation in the disordered phase change material, which is accompanied by an increase of the resistance referred to as *resistance drift* [49]. As expected, this phenomenon is observed on the devices programmed in the RESET state in which the active material is amorphous, and thus it is highly disordered. But it is also observed on the devices in the SET state in which the material is polycrystalline. In this case, the drift of the resistance is interpreted as the result of the structural relaxation of some amorphous residues, and attributed to the presence of grain boundaries [50]. Since it corresponds to a gradual increase in the resistance of the devices, this can lead to the loss of the SET state, which will gradually get closer to the RESET state resistance level.

These two failure mechanisms unfortunately appear as competing phenomena: so far, experimental results have shown that materials allowing a higher stability of the RESET state also exhibit a higher drift of the SET state [17].

Regarding the size reduction of the volume of the PCM at nanometer scale, as reported in [51], it should lead to an improved retention. These material studies do not provide evidence of the impact of scaling on final device speed, however they provide a demonstration of the high potential scalability of this technology.

As already reported, retention of the RESET state is correlated with the crystallization kinetics of the phase change material. The higher the stability of the amorphous phase, the slower the SET operation (i.e., lower programming speed). It means that material engineering toward retention improvement

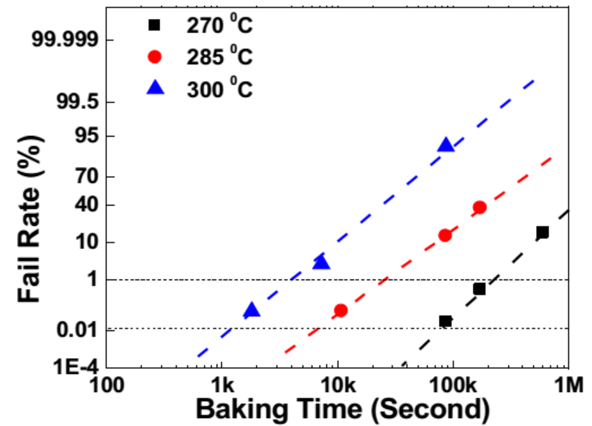


Fig. 9. Failure rate of GaSbGe-based PCM in a 128 Mb test chip. Only 1% of devices fails after one hour bake at 300°C (reproduced with permission from [52]).

is detrimental for device programming time ($> 1\mu$s). Even if it is the main trend, recent works [52] demonstrated that PCM integrating innovative ternary materials based on GaSbGe alloys can provide high temperature data retention (10 years of retention at 220°C) still featuring SET time below 100 ns. As reported in Fig. 9, a low device failure rate is granted even at operating temperatures of 300 °C. This result confirms the importance of material engineering in PCM technology, demonstrating that this technology is capable of retention performance achievable in NAND Flash only thanks to specific algorithms for errors correction.

4) Specific reliability issues and multilevel operation: the resistance drift induced by structural relaxation of the amorphous phase in PCM was highlighted as main responsible of the resistance window closing. In SLC PCM this problem can be solved thanks to improved pulse programming techniques able to optimize SET operations [53], [54]. Multilevel capability of PCM technology is an asset for SSD applications, however, the resistance drift represents a limiting factor. In the last decade, phase change materials engineering and development of innovative reading metrics and reading circuitries made possible the achievement of fast and reliable MLC PCM, up to more than 4 bits-per-cell [53], [55]–[60]. Other solutions showed how even the cell architecture can be improved in order to make the PCM drift-tolerant. In particular, the resistances of the PCM cell in the different programmed levels were stabilized thanks to the introduction of a surfactant layer in parallel with the phase change material [61]. All these developments, made possible to enable different innovative applications that are facing DRAM and/or NAND Flash limits. As an example, genetic-based optimization algorithm for chip multiprocessor equipped with PCM memory in green cloud environments was successfully demonstrated providing a MLC PCM configuration that balances the PCM memory performance as well as the efficiency [62].

In PCM technology, thermal crosstalk refers to the potential failure that a programmed cell can induce in neighbor cells due to the temperature rise induced during the programming operation itself. This problem was demonstrated to be irrel-

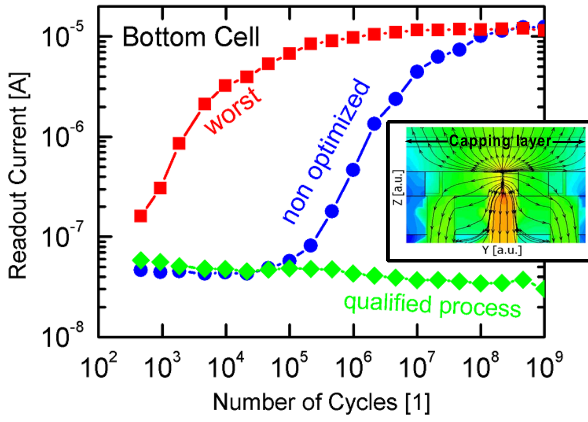


Fig. 10. Readout current of RESET PCM cell along the cycling of a neighbor cell, using different capping layers. Optimized layer (C) enables higher heat flux toward the top electrode and crosstalk immunity (reproduced with permission from [64]).

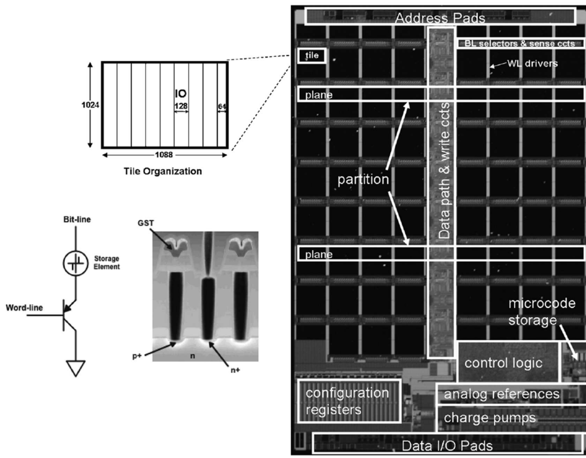


Fig. 11. Die microphotograph showing the array organization of a 256 Mb PCM demostrator with a detail of the storage element integration with the selection device (BJT) (reproduced with permission from [58]).

evant for PCM at least out to the 65 nm node [63]. With the scaling of the device, other studies have been conducted showing the possible impact of the thermal crosstalk in 45 nm technology node [64]. The main result of these analysis is that the closer the cells, the lower the number of programming cycles required to enable the disturb onset. In order to optimize the PCM cell and improve the crosstalk tolerance, different capping layers of the phase change material integrated were proposed with the main goal to tune the heat flux behavior toward the top electrode of the cell (see Fig. 10). Another possible solution to thermal crosstalk in highly scaled PCM arrays is represented by integration of materials capable of high thermal resistance. Indeed, the poor thermal conductivity of these materials makes the active volume surroundings of the PCM (and not involved in the phase-change transition) a perfect thermal barrier to heat loss in neighbour cells during programming [65].

C. Integration of a PCM

1) Cells selector - An integration constraint: the PCM cells integrated in array structures need a mechanism for addressing them during the read and the write operation. PCM cell is a passive element, therefore needs a selector that is able to guarantee a sufficient current for the SET and RESET operations in selected cells (the latter is the most power-hungry) whereas ensuring an adequate immunity from the read and the write disturb on the unselected ones [66]. An ideal selector should have a high ON/OFF resistance ratio to limit leakage paths in the array and a small footprint. Moreover, since the PCM element integration is performed at the Back-End-Of-Line (BEOL) of a CMOS process, the challenge is to manufacture a high quality selecting device on top of the pre-existing CMOS array decoding/sensing circuitry [27].

The storage density of PCM is mainly affected by the size of the cell selector. For integration in the SCM context, one of most sought features is the possibility to act either on single cell domains (i.e., bit-alterability) as for DRAM or over an entire block of cells similar to the operation mode of a NAND Flash, while keeping the minimum area occupation of the cells. The NAND Flash technology has the greatest advantage in terms of integration density since the cell selector and the memory element are the same (i.e., the floating gate transistor), granting a cell area of 4 F^2 (F is the minimum lithographic feature size). The most common selectors for PCM are MOSFETs [34], [67], BJTs [68], [69], or diodes [70], [71]. MOSFETs severely limits the integration density due to the high area occupation (i.e., up to 22 F^2 in order to provide a reasonable RESET current) [60], [67], [72]. BJTs are the preferred solution in 1T-1R (i.e., one transistor-one resistor) architectures since they are able to provide acceptable current densities for the RESET operation at an area occupation expense of 5.5-8 F^2 if integrated vertically [68]. However, those parameters are still not suitable for high density integration in SCMs. Diode selectors are the best solution resulting in a 4 F^2 occupation that allows minimizing the PCM cell area as well for even larger arrays integration [22]. The quest for the best selector technology has been pursued by exploring also alternative technologies like Metal-Insulator-Transition (MIT) elements [73] or the Ovonic Threshold Switching (OTS) selector [74] that will help in the definition of stacked cross-point architectures for high density storage.

2) Technology demonstrators: the first technology demonstrators for PCM were targeted to replace NOR and DRAM Flash architectures resulting in a 128 Mb (256 Mb using multilevel operations) array manufactured with 90nm technology [58] (see Fig. 11) and a 1 Gb product in 45 nm technology [19]. Both memory chips demonstrated that PCM can outperform NOR Flash in terms of write and erase speed (i.e., 100-300 ns are needed for SET and RESET), power consumption (100 μA per operation), and area occupation (i.e., 5.5 F^2). Read speed is similar to that of a NOR Flash since the data transfer interface was kept as the legacy one. General reliability parameters like the endurance and data retention features have been proven similar to Flash on high-temperature tests.

A replacement for DRAM architectures has been pursued by the 8 Gb PCM demonstrator manufactured in 20 nm CMOS technology with a LPDDR2-NVM interface [22]. Given the operation speed of PCM technology, all the design activities were focused on the system cost-effectiveness. By using a diode selector, turning into a 4 F^2 cell area occupation, it is possible to occupy only 70% of a DRAM chip size manufactured at the same design rule with an offered write bandwidth of 133 MB/s. However, figures of merit of this technology are harder to benchmark against a DRAM, but once again are appealing for NOR Flash replacement. In [72], by using a novel multiple individual bank sensing/writing and a memory bank interleave design, it was demonstrated a DDR2 DRAM-like interface PCM. The write and read bandwidth on this chip are equal to 533 MB/s, and the random read latency is 37.5 ns, whereas the write latency is 11.25 ns.

The replacement of NAND Flash, both planar and 3D integrated, in storage applications like SSD requires PCM chips that are able to compete with such an integration density. The so-called 1S-1R (i.e., one selector-one resistor) architectures are not a cost-effective solution. Mainly, the cost ineffectiveness of 1S-1R architectures compared to the cross-point ones is due to the dimensions of the selector. Indeed, it is quite difficult to achieve a 4 F^2 footprint for a selection device (requirement for true cross-point architectures), while providing current densities in the range of 10-40 MA/cm^2 for reliable RESET operation. Parasitic leakage due to the selector integration schemes severely affects the achievable current density affecting the storage density of the PCM array. This yields to products with a capacity far below that of state-of-the-art NAND Flash. Therefore, the only possibility is to leverage the cross-point architecture This architecture integrates the memory element and the selection device in a 4 F^2 footprint that can be stacked even in the third dimension [27].

Researches in this context are represented by three array demonstrators. In [75] it was shown that is possible to create a cross-point PCM array by using a selection diode made of poly-Si with a high ON/OFF current ratio. PCM with a poly-Si diode allows fabricating memory arrays directly over a Si-substrate, and therefore, part of the peripheral circuit can be placed underneath the memory array. However, no details were provided about the maximum array size. A 64 Mb cross-point PCM chip has been manufactured and presented in [74]. The memory cell was built by layering a storage element and a selector. The storage element is a PCM cell and the selector is an OTS. Promising speed and reliability features could be obtained although no demonstration on larger densities has been provided so far. Finally, a high-programming-throughput 3D vertical chain-cell-type phase-change memory (VCCPCM) array was shown in [76]. This device inherits the same architecture of 3D NAND Flash where the PCM cell element is coupled with a MOSFET selector during the integration (see Fig. 12). Even in this case, despite the promised features, there are no indications on the maximum integrated array size.

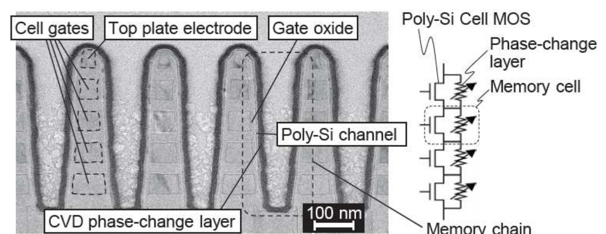


Fig. 12. Cross-sectional view of VCCPCM array and equivalent circuit of memory chain (reproduced with permission from [76]).

D. Benchmarking PCM with DRAM and NAND Flash

NAND Flash technology demonstrated to be capable of high density and low cost thanks to the moving into the third dimension of vertical integrations [77]. Moreover, its predicted scaling limitations continue to be overcome at each new technology node using both device level and architectural solutions, although being closer to serious threats [3], [78]. However, the growing latency gap between DRAM and increasingly huge non-volatile storage supports creates serious opportunities for PCM. This BEOL memory can represent a real compromise between performance and cost saving. In Table I we report the main performance of PCM technology compared to those of DRAM and NAND Flash. Programming speed in PCM, mainly limited by SET operation, is comparable to DRAM writing speed and it is much faster than in NAND Flash. Thanks to Fowler-Nordheim charge tunneling phenomenon used in programming operations, NAND Flash guarantees low current operations but at the expense of long write time (up to few milliseconds) and high write voltage. PCM fills the gap in terms of performances between DRAM and NAND Flash, providing lower voltage operations and higher endurance with respect to NAND Flash. In particular, the close-to-DRAM read latency of PCM can represent a great advantage to strongly increase system performance. It has been exploited in first PCM SSD demonstrators featuring 512-byte read operations in about 1-1.5μs and 3 millions of IOPS (i.e., Input/output operations per second) for queued reads, for a total throughput of 3.5 GB/s [79]. This result cannot be achieved with existing SSD based on NAND Flash memories, since this performance is orders of magnitude faster than existing Flash based SSDs, resulting in a new class of block storage devices. Moreover, innovative hybrid SSD architectures have been recently proposed to take advantage of PCM speed and non-volatility, in particular to improve the reliability of actual SSD based on NAND Flash [80], [81].

III. Spin-Transfer Torque Magnetic Memories

A. Materials and operation principles

The interest in magnetic random-access memory (MRAM) was renewed after the first successful attempts in 1995 to fabricate magnetic tunnel junctions (MTJs) that exhibit large tunneling magnetoresistance (TMR) amplitude of several tens of percent at room temperature using amorphous AlOx barriers. Besides their larger magnetoresistance amplitude, MTJ

TABLE I
COMPARISON OF DRAM, PCM AND NAND FLASH PERFORMANCE (DATA FROM [27], [82])

	DRAM	PCM	NAND Flash
Non-Volatile	No	Yes	Yes
Bit-alterable	Yes	Yes	No
Software complexity	Simple	Simple	Complex
Read Time	$\sim$ 20-50 ns	50-100 ns	25-125 μs
Read Energy	$\sim$ 0.1 nJ/b	$<<$1 nJ/b	$<<$1 nJ/b
Write Time	$\sim$ 20-50 ns	$\sim$ 1 μs	$\sim$ 1-5 ms
Write Energy	1.2 nJ/b	6 nJ/b	17.5 nJ/b
Write Voltage	2.5 V	3 V	15-20 V
Write bandwidth*	$\sim$ GB/s	50-100 MB/s	5-40 MB/s
Erase Time	N/A	N/A	$\sim$ 2-9 ms
Idle-Power	$\sim$ W/GB	$<<$ 0.1 W	$<<$ 0.1 W
Memory Endurance	10^{15}	$\sim 10^8$	10^3-10^5
Retention Time	64 ms	$>$ 10 years	min. 3 months
Cell Area	6 F^2	5 F^2-8 F^2	4 F^2
Density	1$\times$	2-4$\times$	4$\times$
Page size	64 B	64 B	4-16 KB

* (per die)

are more suitable than giant magnetoresistance (GMR) metallic structures for memory applications due to their larger impedance (adjustable to several kΩ) which allows an easier integration with CMOS components. Two other breakthroughs further boosted research and development in MRAM: the first was the discovery that MTJs based on crystalline MgO barriers associated with crystalline magnetic electrodes exhibit much larger TMR amplitude, in the range of 150-600% at room temperature, than their counterparts based on amorphous alumina tunnel barriers. This larger TMR provides a much improved read margin and faster read in memory devices, although it is difficult to achieve it for resistance values below kΩ. The second was the possibility to switch the magnetization of a magnetic nanostructure by a spin-polarized current thanks to the spin-transfer-torque (STT) effect [83]. This effect provided a new write scheme in MRAM with much better down-size scalability than in the first field write based generations of MRAM. Currently, most of research and development in MRAM are focused on STT-MRAM with perpendicular anisotropy (i.e., the magnetization in the ferromagnetic electrodes is oriented out of the plane of the layers) since STT-MRAM seems to be the most promising in terms of scalability down to and beyond the 16 nm technological node.

The MRAM technological evolution (see Fig. 13) of the last decade has benefited from the research in spintronics, exposing the TMR in MTJ based on MgO material [85], the STT [86], and the Spin Orbit Torque (SOT) phenomena [87]. A single MRAM cell consists of a MTJ made of two ferromagnetic layers and a dielectric barrier. The readout operation (i.e., determining the MTJ magnetic state) is performed by evaluating the MTJ resistance.

Between 1996 and 2004, most research and development focused on MRAM written by field. Until the discovery of STT switching and its gradual implementation in MTJ after 2006, the only known way to manipulate the MTJ storage layer was indeed with use of a magnetic field. Such a field is created by pulses of current flowing in conducting lines located below and above the MTJ.

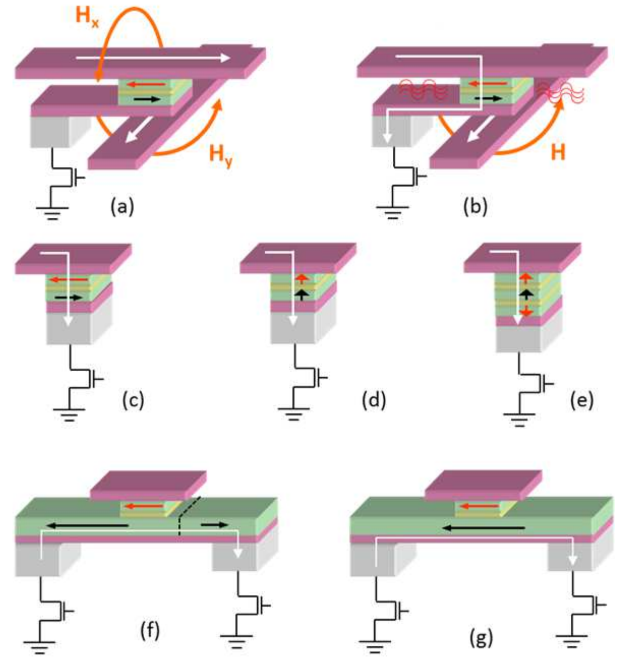


Fig. 13. Evolution of the MRAM technology in the last decade: (a) field-writing, (b) TAS, (c) planar STT-MRAM and (d) perpendicular p-STT-MRAM, (e) double barrier STT-MRAM, (f) 3-terminal MRAM based on domain wall propagation, and (g) SOT-MRAM (reproduced with permission from [84]. Copyright 2014 IOP Publishing Ltd).

A new concept stemming from the field written MRAM (Fig. 13a) is the Thermally Assisted MRAM concept (TAS-MRAM) (Fig. 13b) [88]. In TAS-MRAM, it is possible to write the memory element by combining the temporary heating of a selected cell produced by the tunneling current flowing through it with a single pulse of magnetic field. The power consumption to write these memory elements is significantly reduced compared to conventional field-written MRAM thanks to the possibility of using lower magnetic fields and to the sharing of each field pulse among several cells so as to write several bits at once. Field-written technology is robust and is already used in a variety of applications where reliability, endurance, and resistance to radiation are important features, such as in automotive and space applications. However, the down-size scalability provided by field-writing in conventional technology is limited to MTJ dimensions on the order of 60 nm $\times$ 120 nm due to electromigration in the conducting lines used to generate the field. In addition, in field-writing, the write field extends all along the conducting line where it is produced and decreases relatively gradually in space, inversely proportional to the distance to this line. As a result, unselected bits adjacent to selected bits may sense a significant fraction of the write field, which may yield accidental switching of these unselected bits.

Since the first observation of STT-induced switching in GMR metallic spin-valve pillars, the interest in using STT as a new write approach in MRAM has increased, motivated by the fact that STT-writing (Fig. 13c) is far down-size scalable

than field-writing as the write critical current proportionally decreases with the cell area constrained only by data retention concerns ($\sim$ 15 μA). Furthermore, STT provides very good write selectivity since the STT current flows only through the selected cells.

The interest in MRAM technology from SCM applications is now on perpendicularly magnetized STT-MRAM (i.e., p-STT-MRAM). These memories base on the perpendicular magnetic anisotropy (PMA) which exists at CoFeB/MgO interfaces (Fig. 13d) [89]. The p-STT-MRAM concept requires less current for the write operation with respect to the STT-MRAM counterpart for a given data retention constraint, while providing more stability of the stored data. Optimized p-STT-MRAM stacks will likely integrate a double tunneling barrier with antiparallel polarizing layers in order to maximize the anisotropy and the STT phenomenon efficiency (Fig. 13e). Several improvements have been proposed to increase the performance of this memory concept by combining different technological aspects like TAS and STT [90], [91].

A third category of MRAM under research and development is represented in the last row of Fig. 13. These are three-terminal MRAM cells. The purpose of these embodiments is to split read/write current, thereby increasing the memory reliabilty. Recently, a novel memory concept, called SOT-MRAM has been proposed and demonstrated [87]. A current flowing in the plane of a magnetic multi-layer with structural inversion asymmetry, such as Pt/Co(0.6nm)/AlOx, exerts a torque on the magnetization, due to the spin-orbit coupling. This torque can lead to magnetization reversal, with a switching time shorter than 500 ps and a writing energy one tenth that in current STT-MRAM. The SOT-MRAM solves several reliability issues associated to the MgO tunnel barrier that could potentially expand the memory endurance above the 10^{10} - 10^{12} range of the STT-MRAM, yet being limited by the electromigration phenomenon occurring in the bottom electrode metallic line of the cell. This new concept can be viewed as the ultimate evolution of STT-MRAM as it offers a scaling path for technological nodes below 22 nm, a lower power consumption, M-class-SCM-compatible performance, and largely improved reliability. This technology has several drawbacks that originates from the increased cell size due to the requirement of making two isolated contacts on top or bottom of each memory cell.

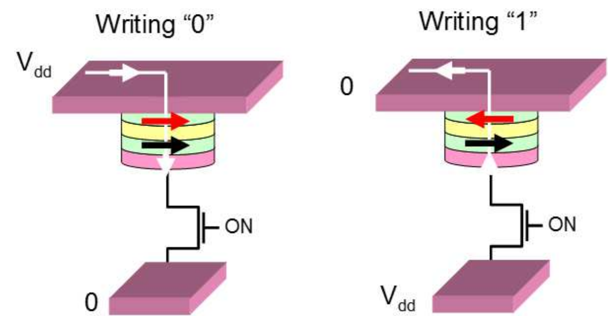


Fig. 14. Writing principle in STT-MRAM. Each STT-MRAM cell consists of an MTJ connected in series with a transistor. To write the parallel magnetic configuration, a current flow of density larger than J_c is sent through the MTJ from the storage layer (red arrow) to the pinned reference layer (black arrow) (i.e., electrons tunnel from the pinned reference layer to the free layer). To write the antiparallel magnetic configuration, the current flow density is sent through the MTJ from the reference layer to the storage layer.

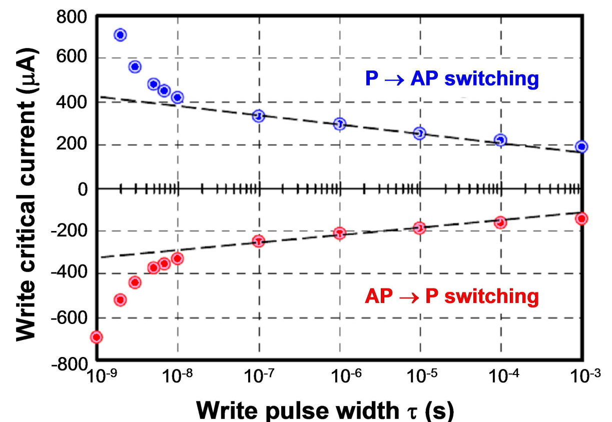


Fig. 15. Typical values of the critical write current density in STT-MRAM as a function of write pulse width (normalized with respect to J_{c0}).

B. Performance and reliability

1) Read/Write operations: the general principle of the read operation in MTJ-based MRAM consists in exploiting the change of resistance between Parallel (P) and Anti-Parallel (AP) magnetic configurations to determine the magnetic state of the junction and therefore the written information. During the operation, the read current is chosen so that the voltage across the MTJ is in the range between 0.1 V to 0.2 V. This choice is motivated by two reasons: *i)* in MTJs in general, and in MgO-based MTJ in particular, the TMR amplitude decreases with bias voltage. This behavior is explained by a reduction of the spin polarization as the bias voltage increases due to the fact that the spin filtering mechanism associated with the symmetry of the wave becomes less effective at higher voltage [87]. With read voltage in the range of 0.1 V to 0.2 V, the decrease of TMR compared to the maximum amplitude at very low voltage is no more than 10% in relative value; *ii)* the second reason for which the reading is performed at relatively low voltage is to avoid spin transfer torque disturbance of the storage layer magnetic state by the read current.

Concerning the write operation, when a spin-polarized current flows through a magnetic nanostructure, the STT results from the interaction between the spin of the conduction electrons and those responsible for the nanostructure magnetization. This torque is exerted on the local magnetization and tends to switch it towards a P or AP direction to that of the spin polarizing layer depending on the current direction. In STT-MRAM, the writing is performed with bipolar pulses of current. Writing a logical '0' (i.e., a P configuration of the magnetization in the storage and fixed layers) can be achieved by sending a current pulse through the stack with the electrons flowing from the fixed reference layer to the storage layer. Writing a logical '1' can be achieved by feeding a current pulse with opposite polarity. A major advantage of the STT write approach is the down-size scalability. Indeed, the critical

current for which the magnetization switches due to the STT influence is determined by a critical current density so that the total current required to write a memory cell scales as the area of the cell, assuming a constant free layer thickness. The possibility to use the STT to switch the magnetization of a free layer in a magnetoresistive stack was first demonstrated in metallic pillars called spin-valves [92] traversed by a current flowing perpendicular to the plane of the layers. A few years later, thanks to the progress made in the development of low RA (resistance×area product) magnetic tunnel junctions, magnetization switching induced by STT was also observed [86]. Interestingly, the current density required to write in MTJ was lower than in metallic pillars (in the range 2-6$\times 10^6$ A/cm^2 in MTJ) mainly due to a higher effective spin polarization in MTJ compared to spin-valves. Since then, the interest in STT in MTJs for STT-MRAM applications has kept on increasing. STT indeed provides a powerful write scheme in MRAM for several reasons:

- in STT-MRAM there is no need to create pulses of magnetic field. Each cell is directly written by the current flowing through the stack, as illustrated in Fig. 14;
- during write of a selected cell, the corresponding selection transistor in series with the MTJ is closed so that the write current flows only through the selected cell. This provides excellent write selectivity, much better than in field-written MRAM;
- in STT writing, the condition for magnetization switching is set by a critical current density J_c. The magnetization of the storage layer switches if the current density of proper direction exceeds J_c. This provides very good down-size scalability since the total current required to write scales like the cell area down to very small dimensions where it becomes limited by the thermal stability factor.

The relation between STT switching versus the current pulse width is shown in Fig. 15. As commonly observed in microelectronics, the larger the voltage (i.e., the current density), the faster the operation. Two different switching phenomena have been noticed, namely the thermal activation and the precessional switching [93], [94]. At a finite temperature, the thermal activation is the dominant factor in the switching current reduction for current pulses in a time regime greater than 10 ns. In the thermally-activated switching regime, the current depends on the pulse width τ and on a thermal stability factor $\Delta = K_u V / k_B T$ of the free layer [95], [96]:

$$J_c(\tau) = J_{c0} \left[1 - \frac{k_B T}{K_u V} ln \left(\frac{\tau}{\tau_0} \right) \right] \quad (1)$$

where $\tau_0 \sim$ 1ns is the attempt frequency inverse and $K_u V$ is the anisotropy energy. J_{c0} is the so-called critical current which corresponds to the linearly extrapolated value of the switching current density for a pulse duration of 1 ns. Typical write speeds in operation in STT-MRAM are around 5 to 10 ns, which corresponds to the intermediate regime between thermally activated and precessional switching.

2) Operation voltages: in conventional STT-MRAM, the write and read current paths are the same. In order to avoid write disturbance during read, the read voltage must be chosen low enough compared to the critical write voltage. There are therefore three voltage distributions in an MRAM chip which need to be well separated for proper functioning and reliability of the chip: the breakdown, write, and read distributions, respectively. This is schematically illustrated in Fig. 16.

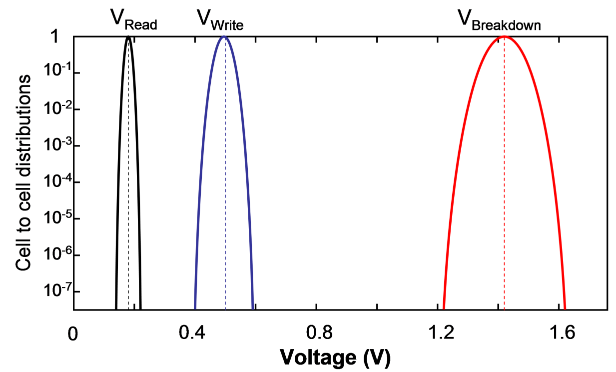


Fig. 16. Schematic representation of the three voltage distributions (i.e., read, write, and breakdown) specific for STT-MRAM functioning.

At each write event (and to lesser extend read event), the tunnel barrier is exposed to an electrical stress which may cause electrical breakdown. To avoid breakdown failure, the highest write voltage in the distribution must be sufficiently low compared to the weakest MTJ in terms of breakdown. By adjusting the MTJs stack composition and their RA, one tries to get this write voltage distribution centered around 0.5 V and be as narrow as possible (typical width as illustrated in Fig. 16). The distribution width mainly originates from fluctuations in the shape and particularly in edge defects associated with the patterning process.

The breakdown voltage distribution is related to the MTJ tunnel barrier that is a thin dielectric oxide layer (MgO $\sim$ 1 nm thick). When exposed to an excessively large voltage, this barrier may experience dielectric breakdown. The breakdown voltage in the MTJ depends on the voltage pulse duration, the number of pulses, and even on the delay between pulses [97]. Compared to CMOS dielectrics, these ultrathin MgO barriers are relatively resistant to breakdown. This mainly comes from the fact that the tunneling through the barrier is direct in normal working conditions, in contrast to Fowler-Nordheim tunneling as in Flash memories. As a result, upon cycling, less defects are generated in the MgO barrier than in CMOS oxides for Flash memory. For voltage pulse width in the range of 10 ns, the voltage breakdown is usually larger than 1.2 V even for RA $\sim 5\ \Omega \cdot \mu m^2$.

The read voltage distribution originates from the variation in the resistance of the selection transistor which is connected in series with the MTJ. The read voltage across the MTJ is typically in the range 0.1 V to 0.15 V. As explained earlier in the paper, this must be low enough compared to the write voltage in order to avoid any write disturbance during read caused by the STT from the read current. However, the lower the read voltage, the slower the read-out process. Therefore, a trade-off must be found.

3) Reliability and integration: endurance characteristics of an STT-MRAM have been demonstrated to sustain up to 10^{12} write cycles [98] and up to 10^{16} cycles when accelerated tests are exploited using manufacturing techniques that limit the trapping sites in the MgO barrier to reduce the mean-time-to-breakdown [97].

In MRAM, the information may get corrupted by an unintended switch in the magnetization of the storage layer due to thermal fluctuations. This is the primary source affecting STT-MRAM data retention capabilities. The failure rate in an MRAM chip of N bits in standby mode can be estimated as follows. The magnetic state of the storage layer of a memory cell can be described as a bistable system with the two stable states being separated by an energy barrier ΔE. ΔE is determined by the magnetic materials properties and the shape and dimensions of the magnetic element (i.e., the MTJ storage layer). At a temperature T, the characteristic thermally-activated switching time is given by an Arrhenius law:

$$\tau = \tau_0 \cdot exp\left(\frac{\Delta E}{k_B T}\right) \quad (2)$$

where k_B is the Boltzmann's constant and τ_0 is the time constant described in eq.(1). For a given bit, the probability of not having accidentally switched after a time t is:

$$P_{noswitch}(t) \propto exp(-t/\tau). \quad (3)$$

For N bits, the probability for the set of bits not having experienced any switching event after a time t is:

$$P^N_{noswitch}(t) \propto exp(-Nt/\tau). \quad (4)$$

Consequently, the probability of having experienced at least one switching event after a time t (i.e., the failure rate in standby mode) is given by:

$$F(t) = 1 - exp(-Nt/\tau) = 1 - exp\left[\frac{-Nt}{\tau_0} exp\left(-\frac{\Delta E}{k_B T}\right)\right]. \quad (5)$$

This expression clearly shows that the factor $\Delta = \Delta E/k_B T$, often called the thermal stability factor, plays a key role in the failure rate of MRAM chips in standby mode (i.e., memory retention failure). Fig. 17 shows the variation of the failure rate during 10 years in stand-by mode as a function of that factor for a 32 Mb and a 1 Gb MRAM chip. In order for the probability of experiencing one failure in time (FIT) during 10 years in stand-by mode to be below an acceptable level of 10^{-4} (this number depends whether the application is targeting S-class or M-class SCM, and on the possible use of ECC), the thermal stability factor must be greater than 67 for the 32 Mb chip and greater than 66 for the 1 Gb chip. The higher the memory capacity, the larger the thermal stability factor has to be.

The STT-MRAM appears today as one of the most credible candidate for M-class SCM especially for DRAM and cache replacement as it combines CMOS process compatibility, large endurance ($> 10^{15}$ write cycles), fast read/write time (1-30 ns), and adequate data retention. However, this technology is not yet fully mature, especially in ultra-scaled integration dimensions below 20 nm. Table II summarizes the features of DRAM and NAND Flash technologies compared to the STT-MRAM.

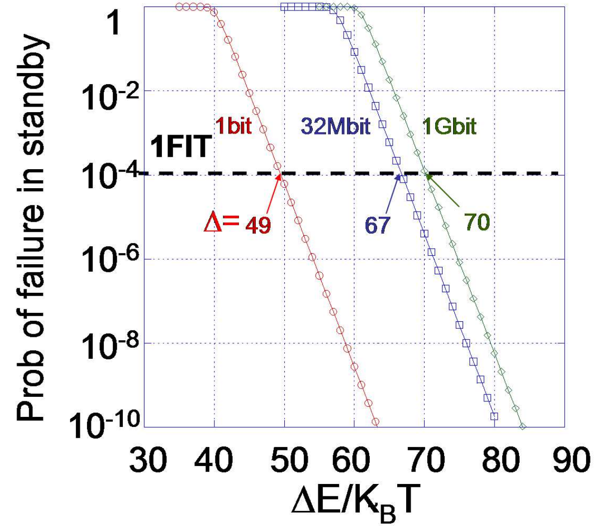


Fig. 17. Failure rate during 10 years in standby mode for a single STT-MRAM bit and chips sized 32 Mb or 1 Gb as a function of thermal stability factor.

Several reliability issues force this technology to require strengthening measures concerning the circuit design of the memory as well as the exploration of breakthrough architectures. To name a few, the high temperature range sensitivity, the cell-to-cell variability, and the accurate TMR control need to be accurately evaluated prior to the integration of an array product. The large parameters variability experienced in STT-MRAM cells is due to the patterning procedure of the MgO material. Edge defects are introduced during this process step leading to a variation of the typical tunneling barrier resistance, thus yielding to a modification of the TMR and of the data retention properties of the cells. The use of self-referenced sensing schemes could improve the robustness against those defects [99]. Concerning the p-STT-MRAM, there are several efforts in the optimization of the stack materials composition to improve the TMR, the operative temperature range, and to minimize the write current in order to reduce the overall memory power consumption. A solution could be represented by integrating double barrier MTJ (see Fig. 13) that should help in reaching the gigabit storage density for STT-MRAM [100].

The result of these activities materialized in the first 64 Mb STT-MRAM product with a DDR3 interface (see Fig. 18) [101], [102]. This memory is an M-class SCM compatible with state-of-the-art DDR3 memory controllers, therefore being easily integrable in SSD products [103].

TABLE II
COMPARISON OF DRAM, STT-MRAM AND NAND FLASH PERFORMANCE (DATA FROM [14], [82])

	DRAM	STT-MRAM	NAND Flash
Bit-alterable	Yes	Yes	No
Read Time	~ 20-50 ns	10 ns	25-125 μs
Write Time	~ 20-50 ns	10 ns	~ 1-5 ms
Write Energy per bit	2 pJ	0.02 pJ	10 nJ
Erase Time	N/A	N/A	~ 2-9 ms
Memory Endurance	10^{15}	~ $10^{1}5$	10^{3}-10^{5}
Retention Time	64 ms	> 10 years	min. 3 months
Cell Area	6 F^2	4 F^2	4 F^2
Integration density	64 Gb/chip	2 Gb/chip	1 Tb/chip

* (per die)

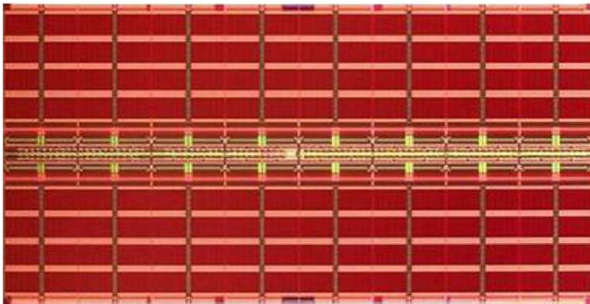


Fig. 18. Die photograph of the 64 Mb DDR3 STT-MRAM product from Everspin Technologies Inc. The die is organized in eight 8 Mb banks each one divided into eight sub-arrays (reproduced with permission from [104]).

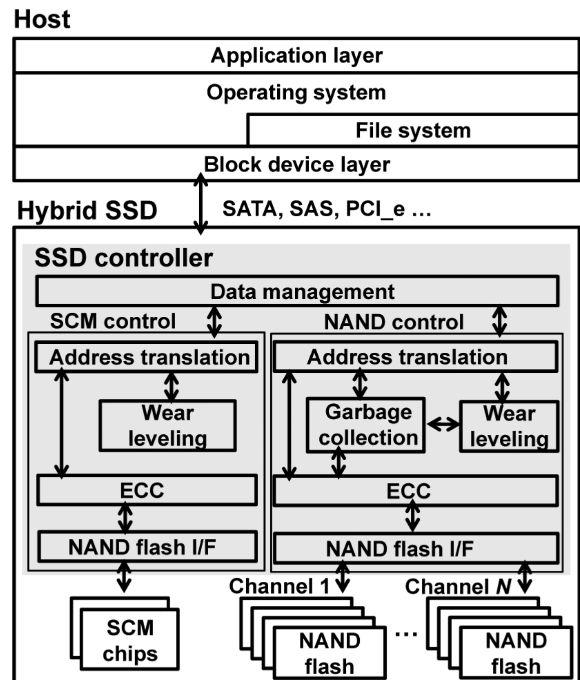


Fig. 19. Hybrid SSD system architecture for a generic SCM memory. PCM or STT-MRAM can be easily replaced in the design (reproduced with permission from [109]).

IV. SSD APPLICATIONS FOR PCM AND STT-MRAM

A. Outpacing NAND Flash limitations with Hybrid SSDs

NAND Flash memories are the storage core of an SSD. Both SLC and MLC technologies are widely used despite their well-known limitations introduced in Section I. Besides them, there is a functional requirement that forces the SSD firmware designers to develop proper measures in the Flash Translation Layer (FTL) [105], [106], namely the *erase-before-write* constraint [107]. NAND Flash cannot update the data by directly overwriting them, thus requiring a time-consuming erase operation before the overwrite. To complicate matters, the erase operation cannot be performed on a single data item, but only on large blocks whose dimension is few megabytes [108]. Finally, the number of erase operations per block must be spread across the whole SSD addressing space to avoid heavily worn spots in terms of endurance.

One key advantage of SCMs like PCM and STT-MRAM is the in-place data overwriting feature. These memories are indicated as bit-alterable but can be also written and erased using the same page size of NAND Flash for legacy applications. Since for these NVMs in-place updates are possible, frequently changed/accessed data (i.e., hot data) can be directed to those memories rather than Flash to improve system performance and longevity [109]. The hybrid memory/storage system idea then became a research subject. Examples of works tackling this topic mainly for PCM technology, yet not being limited to, are: [71], [108]–[110].

A *hybrid SSD* is a disk where NAND Flash and SCM like PCM or STT-MRAM share the same SSD controller (i.e., the brain of the SSD) although different functionalities are assigned to its sub-blocks depending on the data management strategies adopted by the disk [109]. Fig. 19 shows the architecture of a generic hybrid SSD controller. The data management module determines whether data should to be stored in SCM or in NAND flash memory based on the data activity and the memory device status. An address translation module, separated for each memory type, provides the logical interface between the host system and the SSD. The wear levelling module ensures to spread the wear-out among the entire addressable space of the disk to increase its lifetime separately for the SCM and for the NAND Flash. Additionally, the garbage collection module is mandatory to reclaim free space in the NAND Flash when their blocks are almost full for supporting the data overwriting. Finally, an ECC module is included for each memory to correct errors caused by endurance and data retention failures.

Hybrid SSD architectures could be beneficial in applications like on-line transaction processing (OLTP) or database management systems (DBMS), where a frequent data update is requested [111]. A dedicated technique to overcome NAND Flash limitations while avoiding performance and reliability loss in those scenario is devised in state-of-the-art enterprise SSDs, namely the in-place logging (IPL) [111]. Such an approach partitions NAND Flash blocks into: *i)* a data region to store regular data; *ii)* a log region to store the updates log of the data pages that request a content modification [110], [111]. With this technique the number of write and erase operations

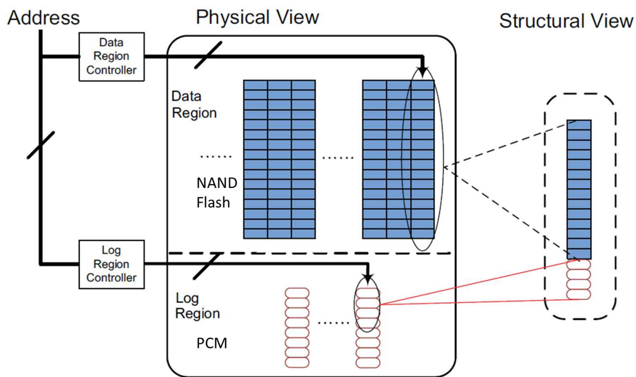


Fig. 20. Architectural description of a hybrid NAND Flash/PCM SSD for IPL methodology replacement (adapted and reproduced with permission from [110]).

is greatly reduced when used in conjunction with an on-board SSD DRAM. However, the IPL method can be insufficient for NAND Flash reliability improvement especially when a data item in a DBMS is repeatedly updated. Fig. 20 shows how a NAND Flash/PCM hybrid SSD could replace the IPL technique. NAND Flash memories are accessed via the Data Region controller, whereas the log updates requested by the application are redirected on a PCM through its Log Region controller. The controllers can be accessed in parallel to improve the total SSD access latency [111]. The hybrid SSD works as follows:

- when a read operation is issued, both NAND Flash and PCM are accessed. If log data in PCM exist for the associated data page they are transferred to the DRAM of the SSD along with the original data page;
- when a write operation is issued, the first thing that the SSD controller does is an existence check on the log sectors of the PCM associated to the data page to update in NAND Flash. Dependently on the check result a data update may occur either on an existing or on a new log sector of the PCM;
- when the log region management policies applied by the Log Region controller in the SSD (e.g., wear leveling, data update strategies, etc.) request a so-called *merge operation*, the new data are written to a new erased block of NAND Flash.

The log region of the PCM can be managed by statically associating a log page to a page or a group of pages in NAND Flash, or by dynamically changing the associations depending on the wear levelling and usage constraints of the SSD [110]. A simulation of this hybrid SSD has been performed with a synthetic DBMS workload constituted by a 1 GB database accessed by 100 users and with varying size of the SSD's DRAM buffer. Fig. 21 shows that the total write time of the DBMS transactions, the energy consumption of the disk, and its lifetime greatly improve (i.e., up to 5 times write time and power consumption reduction and up to 3 times lifetime enhancement) by using the hybrid solution instead of the IPL technique for an *all-Flash* SSD [110].

B. The power loss recovery case

During SSD operations the data are temporary stored in the internal DRAM cache to reduce the performance gap between the host system and the storage layer of the drive composed by slower NAND Flash. Faster systems like NVRAM cards use DRAM as the main storage backbone, leveraging on NAND Flash only for data backup purposes [112]. When the system issues a *power off* command to the SSD or to the NVRAM, there is a step to flush the content of the DRAM on the NAND Flash, update the user data, and finally the metadata used for describing the SSD/NVRAM state in terms of wear-out, invalid blocks, and so on. However, in case of a sudden power loss such as unplugging the system power or due to unexpected power outages, the flush operation cannot be completed correctly and since DRAM is a volatile memory it will lose all the data content yielding to severe device failures [113].

Many enterprise-class SSDs for data centers implement the so called Power Loss Protection (PLP) [114]. PLP circuitry is usually in the form of a microcontroller that generates a warning signal in case of power loss connected to a set of bulky aluminum or tantalum supercapacitors that maintain the SSD power for a sufficient time to finalize the data transfers from DRAM to NAND Flash [113]. A backup time of 20-40 ms can be achieved with 2 mF supercapacitors in large density SSDs up to the terabyte range [114]. Although this solution is effective against such issue, it lacks in compactness, it is very costly, and it is subjected to secondary reliability issues like the capacity degradation as a function of the temperature [115].

PCMs or STT-MRAMs can be integrated in hybrid SSDs to greatly help in the power loss protection and data recovery. In [80], two hybrid SSD architectures based on PCM were debated, although STT-MRAM could fit as well in the design with even superior characteristics. Fig. 22 shows the two architectures at a glance: in the first the PCM/STT-MRAM is used as a complete replacement of the SSD's DRAM cache, in the second the PCM/STT-MRAM is an auxiliary memory integrated along with the DRAM. Let us review the reliability in terms of time to recover from a power loss event, the performance, and the SSD lifetime improvement of the proposed architectures.

When the PCM/STT-MRAM is used as a main cache it stores the mapping tables including the logical address to physical NAND Flash address translation as well as the metadata containing information on the SSD blocks wear-out and availability. Moreover, temporary cached data, hot data, and the code of FTL routines like wear levelling and garbage collection runs on top of the cache memory. Upon a power fault event no data flush from PCM/STT-MRAM to NAND Flash is requested thanks to the non-volatility of the former memory, therefore the time needed for a flush operation is null. On the contrary, in state-of-the-art SSD architectures this time can be calculated as [80]:

$$T_{recovery} = (N_{data} + N_{map}) * (T_{NAND} + T_{FTL}) \qquad (6)$$

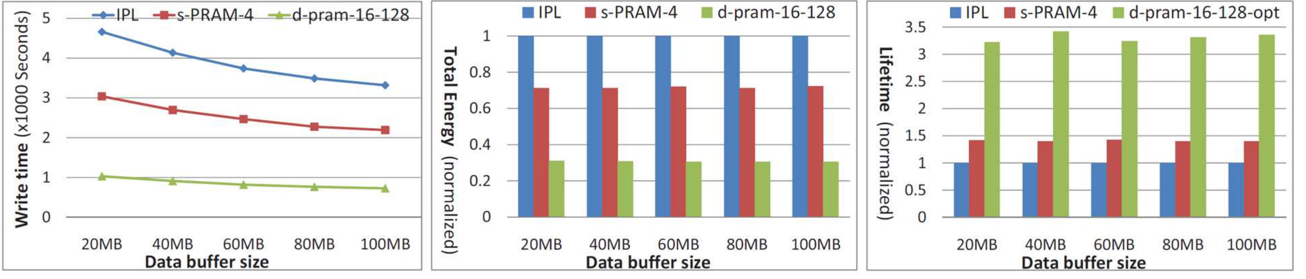


Fig. 21. Write time, total energy consumption, and lifetime as a function of the data buffer size (i.e., on-board SSD DRAM). The benchmarks are between state-of-the-art IPL techinque and different realizations of NAND Flash/PCM hybrid SSD (adapted and reproduced with permission from [110]).

where N_{data} is the amount of data cached in DRAM, N_{map} is the amount of FTL's metadata in DRAM, T_{NAND} is the time needed to write the cached data to NAND Flash, and T_{FTL} is the time requested by the FTL to compute where the data needs to be stored according to the wear-out and utilization statistics of the NAND Flash, respectively.

When the PCM/STT-MRAM is used as an auxiliary cache memory integrated in the disk along with the DRAM its role is to store the mapping tables and the FTL's metadata that will be flushed to DRAM at the system power on. In case of a power failure, the temporary data cached in DRAM are stored to PCM/STT-MRAM rather than NAND Flash. Compared to the first hybrid architecture, the FTL code will run on the DRAM. The recovery time for this architecture will be:

$$T_{recovery} = (N_{data} + N_{map}) * (T_{PCM/STT-MRAM}) \quad (7)$$

where $T_{PCM/STT-MRAM}$ is the time needed to write that memory. The recovery time calculated with (7) is longer than that of the first hybrid architecture, but comparing with that of state-of-the-art SSD it is found that by using fast M-class PCM like [72] or STT-MRAM like [116] such value could be up to ten or twenty times lower. In both cases the power loss reliability will be improved.

There are some differences concerning the performance of the two proposed architectures. In the first architecture, the PCM/STT-MRAM works as a DRAM, but because the read and write latencies of that memory (even considering their M-class realizations) are slower than volatile DRAM, the performance of the SSD will be slowed down. On the contrary, in the second architecture the PCM/STT-MRAM is accessed only upon a power fault and therefore the SSD performance will be that of a state-of-the-art system. STT-MRAM technology should be favored for this particular application thanks to the fastest access time compared to PCM.

The final concern of the proposed hybrid SSD architectures is the lifetime of the drive. This parameter is important to understand cost figures in data centers or computing facilities related to SSD deployment and maintenance [117]. The lifetime of an SSD with DRAM and NAND Flash, expressed in years, is calculated according to [118] as:

$$Lifetime = \frac{SSD_{Capacity} * NAND_{P/E} * \alpha}{\beta * 365} \quad (8)$$

where $SSD_{Capacity}$ is the storage density of the disk, $NAND_{P/E}$ is the endurance of NAND Flash blocks expressed in Program/Erase cycles, α is the actual NAND Flash utilization factor for storage, and β is a parameter accounting for the usage per day and the capacity rate of the disk, respectively. This equation holds true in the assumption of a perfect Wear Levelling scheme [118]. When a hybrid SSD architecture is considered, the $Lifetime$ can be extended by a multiplication factor γ that has been demonstrated in [80] to be:

$$\gamma = 1 + \frac{hyb_{Capacity} * hyb_{P/E} * \alpha_{hyb}}{NAND_{Capacity} * NAND_{P/E} * \alpha} \quad (9)$$

where $hyb_{Capacity}$ is the PCM/STT-MRAM capacity, $hyb_{P/E}$ is the endurance of the PCM/STT-MRAM expressed in Program/Erase cycles, and α_{hyb} is the utilization factor of the PCM/STT-MRAM the depends on the amount of hot data that are stored in memory along with other cached data. A 128 GB SSD using NAND Flash memories with and endurance up to 10^4 integrated along with 128 MB of PCM/STT-MRAM with an endurance up to 10^8 can achieve a γ equal to 6 when α_{hyb} is 0.5. Considering that the $Lifetime$ parameter of a state-of-the-art SSD is generally 5 years this turns into a deployment cost reduction for the SSD for additional 25 years. This result is similar for both hybrid architectures. The integration scheme where PCM/STT-MRAM is embedded as auxiliary memory will feature a slightly larger endurance since the FTL code does not run on top of it.

Analyzing the different reliability and performance metrics of each emerging NVM we can conclude that PCM and STT-MRAM offer similar advantages, although the latter technology seems to be favored in PLP applications thanks to the smaller power consumption, the fastest access time, and the longest endurance proven so far at a product level [104]. However, STT-MRAM integration density limitation poses some concerns about the amount of data that could be cached in memory in addition to the mapping tables and critical FTL metadata.

C. *Rethinking the storage backbone*

The advent of S-class demonstrators for PCM and STT-MRAM raised some concerns on the storage concept of the SSD. Emerging memories have been included in architectural analysis only from the hybrid viewpoint, coupling them with

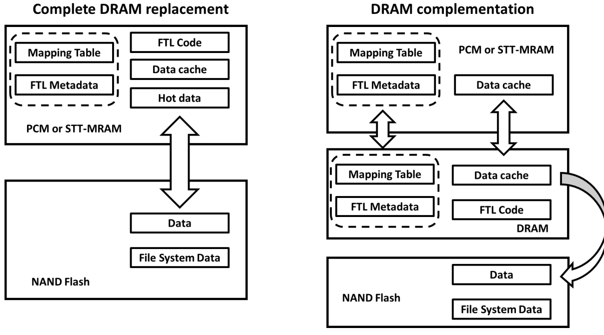


Fig. 22. Hybrid SSD architectures for power loss protection either using PCM or STT-MRAM as a full DRAM replacement or as auxiliary cache memories to complement DRAM (architecture idea taken from [80]).

existing NAND Flash or DRAM in the SSD. In this case, the figures of merit of SSDs like read/write latencies, throughput, etc. are similar to that of the slowest memory in the storage tier in worst case analysis. There is a call in changing the storage backbone by fully replacing the NAND Flash devices in the SSD with SCMs. Several architectures have been proposed either by simulations [119]–[121] or on product demonstrators that are however far from mass production [79], [122].

Fig. 23 shows an example of a SSD architecture where NAND Flash memories have been fully replaced by emerging non-volatile memories. The system is based on a controller that manages the data transfers with the host system through a PCIe 1.1 interface that allows theoretical throughput up to 4 GB/s. Moreover, a command scheduler to handle the read and write operations priority is implemented to accept commands from an Operating System (OS) that manages the data block transfers. Proper wear levelling schemes are adopted to enhance the lifetime of the disk [118]. A system prototype has been implemented on FPGA by emulating the latencies of PCM and STT-MRAM memories [119]. Such a system enables the comparison between several storage solutions like SSDs and traditional HDDs. The evaluated performance of an *all S-Class SCM* SSD shows that there is enormous potential for very low latencies (i.e., $< 30\ \mu s$) and high sustainable bandwidth close to the theoretical one offered by the PCIe 1.1 interface (see Fig. 24). However, even if those performance far outweigh those of state-of-the-art SSDs, there are some drawbacks in terms of OS complexity. The OS indeed, is responsible for more than 60% of the total SSD latency when a SCM is integrated in the disk [119], [121] since the latency bottleneck comes directly from the command scheduling operation rather than the memory itself.

The PCM technology is the favored one to be integrated in *all S-class SCM* SSDs since STT-MRAM still suffers from high density integration issues. However, before replacing NAND Flash in the storage backbone it is important to design the SSD controller to align the memory architecture (i.e., page size) with the OS requirements in order to avoid inefficiencies in the storage tier.

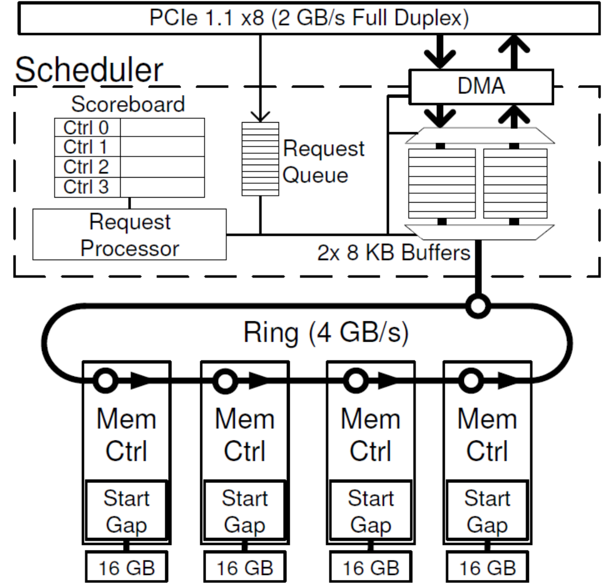


Fig. 23. SSD controller and storage backbone where NAND Flash has been fully replaced by SCMs like PCM or STT-MRAM (reproduced with permission from [119]).

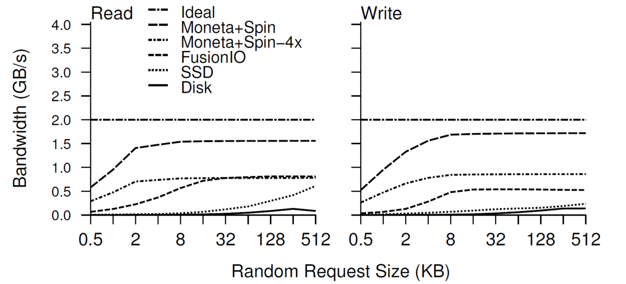


Fig. 24. SSD controller and storage backbone where NAND Flash has been fully replaced by SCMs like PCM or STT-MRAM (reproduced with permission from [119]).

D. In-storage processing

The final frontier for SSDs is the possibility to grant user applications to interact directly with is internal components. Recently, researchers have extended the idea about offloading the data analysis in bulk DBMS or On-Line Analytical Processing (OLAP) directly to the SSD controller and to the DRAM/NAND Flash memories constituting the disk [123]–[125]. As a matter of example let us consider a DBMS. Upon receiving a query for the data processing of some elements in the database stored in the SSD, a state-of-the-art computing architecture will to retrieve the data from the disk and then will execute the query on the machine hosting the storage platform. In new computing architectures like the one named *Smart SSD* [124], the disk fetches the data directly from NAND Flash chips to the SSD's internal DRAM, and then offload the query execution on the processors integrated in the SSD controller. In this case, only the results (expected to be much smaller than the raw data to be accessed in conventional architectures) are sent to the host machine. In this way, the traditional computing paradigm is changed to *in-storage processing*. Fast

M-class STT-MRAM might be beneficial for this particular application since the entire data processing could be performed in a relatively fast way (with latencies close to DRAM), with the advantage of a non-volatile storage medium that should be intrinsically resilient against power loss events. Indeed, this additional protection measure should avoid once again the usage of bulk supercapacitors to flush the memory content in case of a power failure during the processing of the data.

V. Conclusions

PCM and STT-MRAM technologies are good candidates for next generation SSDs. Their performance and reliability features are well placed in the SCMs context and seem to offer a viable solution for replacing NAND Flash and DRAM. PCMs technology demonstrators shown that these memories are easy to integrate in a fully compatible CMOS process with latencies, endurance, and data retention characteristics better than NAND Flash. Moreover, an accurate choice of the materials can easily toggle the memory behavior from S-class to M-class SCMs. Several issues still needs to be treated to improve the storage density further through multilevel approaches. PCMs are candidate in all SSD applications where a hybrid solution is sought for improving the disk performance in enterprise environments or as a complete storage backbone replacement for fast SSDs. Concerning STT-MRAM, their fast switching speed and relatively high endurance make this technology robust enough to outstand the typical NAND Flash limitations. However, their integration density is still limited due to reliability concerns related to the physics behind the switching process. In this case, M-class SCM better fits this memory technology. Their preferred application in SSDs could be as fast cache resilient to power loss failures or as an additional fast storage layer to be used in future in-storage processing platforms.

References

[1] A. Modelli, A. Visconti, and R. Bez, "Advanced Flash Memory Reliability," in *Int. Conf. on Integrated Circuit Design and Tech.*, 2004, pp. 211–218.

[2] Y. Park, J. Lee, S. S. Cho, G. Jin, and E. Jung, "Scaling and reliability of NAND flash devices," in *Int. Reliability Phys. Symp.*, 2014, pp. 2E.1.1–2E.1.4.

[3] E. Vatajelu, H. Aziza, and C. Zambelli, "Nonvolatile memories: Present and future challenges," in *Int. Design Test Symp.*, 2014, pp. 61–66.

[4] T. Parnell, C. Dunner, T. Mittelholzer, N. Papandreou, and H. Pozidis, "Endurance limits of MLC NAND flash," in *Int. Conf. on Communications*, Jun. 2015, pp. 376–381.

[5] Y. Cai, Y. Luo, E. F. Haratsch, K. Mai, and O. Mutlu, "Data retention in MLC NAND flash memory: Characterization, optimization, and recovery," in *Int. Symp. on High Perf. Comp. Arch.*, Feb. 2015, pp. 551–563.

[6] C. Zambelli, A. Chimenton, and P. Olivo, "Reliability issues of NAND Flash memories," in *Inside NAND Flash Memories*, R. Micheloni, L. Crippa, and A. Marelli, Eds. Springer Netherlands, 2010, pp. 89–113.

[7] Micron, "MT29F512G08EMCBBJ5-6 TLC NAND Flash Data sheet," 2015.

[8] L. Zuolo, C. Zambelli, R. Micheloni, D. Bertozzi, and P. Olivo, "Analysis of Reliability/Performance Trade-off in Solid State Drives," in *Int. Reliability Phys. Symp.*, Jun. 2014, pp. 4B.3.1–4B.3.5.

[9] A. Grossi, L. Zuolo, F. Restuccia, C. Zambelli, and P. Olivo, "Quality-of-Service Implications of Enhanced Program Algorithms for Charge-Trapping NAND in Future Solid-State Drives," *IEEE Trans. on Device and Mat. Reliability*, vol. 15, no. 3, pp. 363–369, 2015.

[10] W. Jeong, J. w. Im, D. H. Kim, S. W. Nam, D. K. Shim, M. H. Choi, H. J. Yoon, D. H. Kim, Y. S. Kim, H. W. Park, D. H. Kwak, S. W. Park, S. M. Yoon, W. G. Hahn, J. H. Ryu, S. W. Shim, K. T. Kang, J. D. Ihm, I. M. Kim, D. S. Lee, J. H. Cho, M. S. Kim, J. H. Jang, S. W. Hwang, D. S. Byeon, H. J. Yang, K. Park, K. H. Kyung, and J. H. Choi, "A 128 Gb 3b/cell V-NAND Flash Memory With 1 Gb/s I/O Rate," *IEEE J. of Solid-State Circ.*, vol. 51, no. 1, pp. 204–212, 2016.

[11] A. Grossi, C. Zambelli, and P. Olivo, "Reliability of 3D NAND Flash Memories," in *3D Flash Memories*, R. Micheloni, Ed. Springer Netherlands, 2016, pp. 29–62.

[12] R. F. Freitas and W. W. Wilcke, "Storage-class Memory: The Next Storage System Technology," *IBM J. Res. Dev.*, vol. 52, no. 4, pp. 439–447, 2008.

[13] G. W. Burr, M. J. Breitwisch, M. Franceschini, D. Garetto, K. Gopalakrishnan, B. Jackson, B. Kurdi, C. Lam, L. A. Lastras, A. Padilla, B. Rajendran, S. Raoux, and R. S. Shenoy, "Phase change memory technology," *J. of Vacuum Science & Tech. B*, vol. 28, no. 2, pp. 223–262, 2010.

[14] M. H. Kryder and C. S. Kim, "After Hard Drives - What Comes Next?" *IEEE Trans. on Magnetics*, vol. 45, no. 10, pp. 3406–3413, 2009.

[15] L. Perniola, G. Molas, G. Navarro, E. Nowak, V. Sousa, E. Vianello, and B. D. Salvo, "Universal Signatures from Non-Universal Memories: Clues for the Future..." in *Int. Memory Workshop*, May 2016, pp. 1–3.

[16] G. W. Burr, B. N. Kurdi, J. C. Scott, C. H. Lam, K. Gopalakrishnan, and R. S. Shenoy, "Overview of Candidate Device Technologies for Storage-class Memory," *IBM J. Res. Dev.*, vol. 52, no. 4, pp. 449–464, 2008.

[17] G. Navarro, M. Coue, A. Kiouseloglou, P. Noe, F. Fillot, V. Delaye, A. Persico, A. Roule, M. Bernard, C. Sabbione, D. Blachier, V. Sousa, L. Perniola, S. Maitrejean, A. Cabrini, G. Torelli, P. Zuliani, R. Annunziata, E. Palumbo, M. Borghi, G. Reimbold, and B. D. Salvo, "Trade-off between SET and data retention performance thanks to innovative materials for phase-change memory," in *Int. Electron Devices Meeting*, Dec. 2013, pp. 21.5.1–21.5.4.

[18] C. Zambelli, D. Bertozzi, A. Chimenton, and P. Olivo, "Nonvolatile Memory Partitioning Scheme for Technology-Based Performance-Reliability Tradeoff," *IEEE Embedded Sys. Lett.*, vol. 3, no. 1, pp. 13–15, 2011.

[19] G. Servalli, "A 45nm generation Phase Change Memory technology," in *Int. Electron Devices Meeting*, Dec. 2009, pp. 1–4.

[20] S. H. Lee, H. C. Park, M. S. Kim, H. W. Kim, M. R. Choi, H. G. Lee, J. W. Seo, S. C. Kim, S. G. Kim, S. B. Hong, S. Y. Lee, J. U. Lee, Y. S. Kim, K. S. Kim, J. I. Kim, M. Y. Lee, H. S. Shin, S. J. Chae, J. H. Song, H. S. Yoon, J. M. Oh, S. K. Min, H. M. Lee, K. R. Hong, J. T. Cheong, S. N. Park, J. C. Ku, Y. S. Sohn, S. K. Park, T. S. Kim, Y. K. Kim, K. W. Park, C. S. Han, W. Kim, H. J. Kim, K. S. Choi, J. H. Lee, and S. J. Hong, "Highly productive PCRAM technology platform and full chip operation: Based on 4F2 (84nm pitch) cell scheme for 1 Gb and beyond," in *Int. Electron Devices Meeting*, Dec. 2011, pp. 3.3.1–3.3.4.

[21] M. J. Kang, T. J. Park, Y. W. Kwon, D. H. Ahn, Y. S. Kang, H. Jeong, S. J. Ahn, Y. J. Song, B. C. Kim, S. W. Nam, H. K. Kang, G. T. Jeong, and C. H. Chung, "PRAM cell technology and characterization in 20nm node size," in *Int. Electron Devices Meeting*, Dec. 2011, pp. 3.1.1–3.1.4.

[22] Y. Choi, I. Song, M. H. Park, H. Chung, S. Chang, B. Cho, J. Kim, Y. Oh, D. Kwon, J. Sunwoo, J. Shin, Y. Rho, C. Lee, M. G. Kang, J. Lee, Y. Kwon, S. Kim, J. Kim, Y. J. Lee, Q. Wang, S. Cha, S. Ahn, H. Horii, J. Lee, K. Kim, H. Joo, K. Lee, Y. T. Lee, J. Yoo, and G. Jeong, "A 20nm 1.8V 8Gb PRAM with 40MB/s program bandwidth," in *Int. Solid-State Circ. Conf.*, Feb. 2012, pp. 46–48.

[23] EETimes, "Phase-change memory found in handset," [Online]. Available: http://www.eetimes.com/document.asp?doc_id=1258042, 2010.

[24] S. R. Ovshinsky, "Reversible electrical switching phenomena in disordered structures," *Phys. Rev. Lett*, vol. 21, pp. 1450–1453, 1968.

[25] N. Yamada, E. Ohno, N. Akahira, K. Nishiuchi, K. Nagata, and M. Takao, "High Speed Overwritable Phase Change Optical Disk Material," *Jap. J. of Appl. Phys.*, vol. 26, no. S4, p. 61, 1987.

[26] Ovonyx Inc., "Ovonic Unified Memory," [Online]. Available: http://www.ovonic.com, 1999.

[27] H. S. P. Wong, S. Raoux, S. Kim, J. Liang, J. P. Reifenberg, B. Rajendran, M. Asheghi, and K. E. Goodson, "Phase Change Memory," *Proc. of the IEEE*, vol. 98, no. 12, pp. 2201–2227, 2010.

[28] A. Fantini, L. Perniola, M. Armand, J. F. Nodin, V. Sousa, A. Persico, J. Cluzel, C. Jahan, S. Maitrejean, S. Lhostis, A. Roule, C. Dressler, G. Reimbold, B. D. Salvo, P. Mazoyer, D. Bensahel, and F. Boulanger,

"Comparative Assessment of GST and GeTe Materials for Application to Embedded Phase-Change Memory Devices," in *Int. Memory Workshop*, May 2009, pp. 1–2.

[29] D. Ielmini and Y. Zhang, "Analytical model for subthreshold conduction and threshold switching in chalcogenide-based memory devices," *J. of Appl. Phys.*, vol. 102, no. 5, p. 054517, 2007.

[30] A. Pirovano, A. L. Lacaita, F. Pellizzer, S. A. Kostylev, A. Benvenuti, and R. Bez, "Low-field amorphous state resistance and threshold voltage drift in chalcogenide materials," *IEEE Trans. on Electron Devices*, vol. 51, no. 5, pp. 714–719, 2004.

[31] A. Chimenton, C. Zambelli, P. Olivo, and A. Pirovano, "Set of Electrical Characteristic Parameters Suitable for Reliability Analysis of Multimegabit Phase Change Memory Arrays," in *Non-Volatile Semiconductor Memory Workshop*, 2008, pp. 49–51.

[32] A. Chimenton, C. Zambelli, and P. Olivo, "Impact of short SET pulse sequence on electronic switching in Phase Change Memory arrays," in *Non-Volatile Memory Tech. Symp.*, Nov. 2008, pp. 1–5.

[33] ——, "A new analytical model of the erasing operation in phase-change memories," *IEEE Electron Device Lett.*, vol. 31, pp. 198–200, 2010.

[34] S. Lai, "Current status of the phase change memory and its future," in *Int. Electron Devices Meeting*, Dec. 2003, pp. 10.1.1–10.1.4.

[35] G. Bruns, P. Merkelbach, C. Schlockermann, M. Salinga, M. Wuttig, T. D. Happ, J. B. Philipp, and M. Kund, "Nanosecond switching in gete phase change memory cells," *Appl. Phys. Lett.*, vol. 95, no. 4, p. 043108, 2009.

[36] A. V. Kolobov, P. Fons, A. I. Frenkel, A. L. Ankudinov, J. Tominaga, and T. Uruga, "Understanding the phase-change mechanism of rewritable optical media," *Nat. Mater.*, vol. 3, no. 10, pp. 703–708, 2004.

[37] M. Wuttig and N. Yamada, "Phase-change materials for rewriteable data storage," *Nat. Mater.*, vol. 6, no. 11, pp. 824–832, 2007.

[38] D. Lencer, M. Salinga, B. Grabowski, T. Hickel, J. Neugebauer, and M. Wuttig, "A map for phase-change materials," *Nat. Mater.*, vol. 7, no. 12, pp. 972–977, 2008.

[39] D. Mantegazza, D. Ielmini, A. Pirovano, B. Gleixner, A. L. Lacaita, E. Varesi, F. Pellizzer, and R. Bez, "Electrical characterization of anomalous cells in phase change memory arrays," in *Int. Electron Devices Meeting*, Dec. 2006, pp. 1–4.

[40] J. Sarkar and B. Gleixner, "Evolution of phase change memory characteristics with operating cycles," *Appl. Phys. Lett.*, vol. 91, p. 233506, 2007.

[41] S.-H. Hong and H. Lee, "Failure Analysis of Ge 2 Sb 2 Te 5 Based Phase Change Memory," *Jap. J. of Appl. Phys.*, vol. 47, no. 5R, p. 3372, 2008.

[42] S. Shin, K. M. Kim, J. Song, H. K. Kim, D. J. Choi, and H. H. Cho, "Thermal Stress Analysis of Ge1Sb4Te7-Based Phase-Change Memory Devices," *IEEE Trans. on Electron Devices*, vol. 58, no. 3, pp. 782–791, 2011.

[43] C. Zambelli, A. Chimenton, and P. Olivo, "Empirical investigation of SET seasoning effects in Phase Change Memory arrays," *Solid-State Electronics*, vol. 58, no. 1, pp. 23–27, 2011.

[44] ——, "Modeling of SET seasoning effects in phase change memory arrays," *Microelectronics Reliability*, vol. 52, no. 6, pp. 1060–1064, 2012.

[45] ——, "Statistical Modeling of Secondary Path During Erase Operation in Phase Change Memories," *IEEE Trans. on Electron Devices*, vol. 59, no. 3, pp. 813–818, 2012.

[46] A. Padilla, G. W. Burr, C. T. Rettner, T. Topuria, P. M. Rice, B. Jackson, K. Virwani, A. J. Kellock, D. Dupouy, A. Debunne, R. M. Shelby, K. Gopalakrishnan, R. S. Shenoy, and B. N. Kurdi, "Voltage polarity effects in Ge2Sb2Te5-based phase change memory devices," *J. of Appl. Phys.*, vol. 110, no. 5, 2011.

[47] Macronix International Co. Ltd., "Program/erase cycling endurance and data retention of macronix slc nand flash memories," [Online]. Available: http://www.macronix.com/Lists/ApplicationNote/Attachments/1611/AN0339V1-Endurance\%20and\%20Retention\%20of\%20NAND\%20Flash.pdf, 2014.

[48] U. Russo, D. Ielmini, A. Redaelli, and A. L. Lacaita, "Intrinsic Data Retention in Nanoscaled Phase-Change Memories - Part I: Monte Carlo Model for Crystallization and Percolation," *IEEE Trans. on Electron Devices*, vol. 53, no. 12, pp. 3032–3039, 2006.

[49] D. Ielmini, D. Sharma, S. Lavizzari, and A. L. Lacaita, "Reliability Impact of Chalcogenide-Structure Relaxation in Phase-Change Memory (PCM) Cells - Part I: Experimental Study," *IEEE Trans. on Electron Devices*, vol. 56, no. 5, pp. 1070–1077, 2009.

[50] N. Ciocchini, E. Palumbo, M. Borghi, P. Zuliani, R. Annunziata, and D. Ielmini, "Modeling Resistance Instabilities of Set and Reset States in Phase Change Memory With Ge-Rich GeSbTe," *IEEE Trans. on Electron Devices*, vol. 61, no. 6, pp. 2136–2144, 2014.

[51] R. G. D. Jeyasingh, M. A. Caldwell, D. J. Milliron, and H. S. P. Wong, "First demonstration of phase change memory device using solution processed GeTe nanoparticles," in *Proc. of the European Solid State Device Res. Conf.*, Sept. 2011, pp. 99–102.

[52] H. Y. Cheng, W. C. Chien, M. BrightSky, Y. H. Ho, Y. Zhu, A. Ray, R. Bruce, W. Kim, C. W. Yeh, H. L. Lung, and C. Lam, "Novel fast-switching and high-data retention phase-change memory based on new Ga-Sb-Ge material," in *Int. Electron Devices Meeting*, Dec. 2015, pp. 3.5.1–3.5.4.

[53] C. Zambelli, A. Chimenton, and P. Olivo, "Analysis and optimization of erasing waveform in phase change memory arrays," in *Proc. of the European Solid State Device Res. Conf.*, Sep. 2009, pp. 213–216.

[54] A. Kiouseloglou, E. Covi, G. Navarro, A. Cabrini, L. Perniola, and G. Torelli, "Optimal programming with voltage-controlled temperature profile to reduce SET state distribution dispersion in PCM," in *Int. Conf. on Electronics, Circ. and Sys.*, Dec. 2014, pp. 482–485.

[55] A. Athmanathan, M. Stanisavljevic, J. Cheon, S. Kang, C. Ahn, J. Yoon, M. Shin, T. Kim, N. Papandreou, H. Pozidis, and E. Eleftheriou, "A 6-bit drift-resilient readout scheme for multi-level Phase-Change Memory," in *Asian Solid-State Circ. Conf.*, Nov. 2014, pp. 137–140.

[56] K. Nakayama, M. Takata, T. Kasai, A. Kitagawa, and J. Akita, "Pulse number control of electrical resistance for multi-level storage based on phase change," *J. of Phys. D: Appl. Phys.*, vol. 40, no. 17, p. 5061, 2007.

[57] T. Nirschl, J. B. Philipp, T. D. Happ, G. W. Burr, B. Rajendran, M. H. Lee, A. Schrott, M. Yang, M. Breitwisch, C. F. Chen, E. Joseph, M. Lamorey, R. Cheek, S. H. Chen, S. Zaidi, S. Raoux, Y. C. Chen, Y. Zhu, R. Bergmann, H. L. Lung, and C. Lam, "Write Strategies for 2 and 4-bit Multi-Level Phase-Change Memory," in *Int. Electron Devices Meeting*, Dec. 2007, pp. 461–464.

[58] F. Bedeschi, R. Fackenthal, C. Resta, E. M. Donze, M. Jagasivamani, E. C. Buda, F. Pellizzer, D. W. Chow, A. Cabrini, G. M. A. Calvi, R. Faravelli, A. Fantini, G. Torelli, D. Mills, R. Gastaldi, and G. Casagrande, "A Bipolar-Selected Phase Change Memory Featuring Multi-Level Cell Storage," *IEEE J. of Solid-State Circ.*, vol. 44, no. 1, pp. 217–227, 2009.

[59] W. C. Chien, Y. H. Ho, H. Y. Cheng, M. BrightSky, C. J. Chen, C. W. Yeh, T. S. Chen, W. Kim, S. Kim, J. Y. Wu, A. Ray, R. Bruce, Y. Zhu, H. Y. Ho, H. L. Lung, and C. Lam, "A novel self-converging write scheme for 2-bits/cell phase change memory for Storage Class Memory (SCM) application," in *Symp. on VLSI Tech.*, Jun. 2015, pp. T100–T101.

[60] M. Stanisavljevic, H. Pozidis, A. Athmanathan, N. Papandreou, T. Mittelholzer, and E. Eleftheriou, "Demonstration of Reliable Triple-Level-Cell (TLC) Phase-Change Memory," in *Int. Memory Workshop*, May 2016, pp. 1–4.

[61] S. Kim, N. Sosa, M. BrightSky, D. Mori, W. Kim, Y. Zhu, K. Suu, and C. Lam, "A phase change memory cell with metallic surfactant layer as a resistance drift stabilizer," in *Int. Electron Devices Meeting*, Dec. 2013, pp. 30.7.1–30.7.4.

[62] M. Qiu, Z. Ming, J. Li, K. Gai, and Z. Zong, "Phase-Change Memory Optimization for Green Cloud with Genetic Algorithm," *IEEE Trans. on Comp.*, vol. 64, no. 12, pp. 3528–3540, 2015.

[63] A. Pirovano, A. L. Lacaita, A. Benvenuti, F. Pellizzer, S. Hudgens, and R. Bez, "Scaling analysis of phase-change memory technology," in *Int. Electron Devices Meeting*, Dec. 2003, pp. 29.6.1–29.6.4.

[64] A. Redaelli, M. Boniardi, A. Ghetti, U. Russo, C. Cupeta, S. Lavizzari, A. Pirovano, and G. Servalli, "Interface engineering for thermal disturb immune phase change memory technology," in *Int. Electron Devices Meeting*, Dec. 2013, pp. 30.4.1–30.4.4.

[65] J. Kluge, G. Navarro, V. Sousa, N. Castellani, S. Blonkowski, R. Annunziata, P. Zuliani, and L. Perniola, "High Operating Temperature Reliability of Optimized Ge-Rich GST Wall PCM Devices," in *Int. Memory Workshop*, May 2016, pp. 1–4.

[66] D. J. Wouters, R. Waser, and M. Wuttig, "Phase-Change and Redox-Based Resistive Switching Memories," *Proc. of the IEEE*, vol. 103, no. 8, pp. 1274–1288, 2015.

[67] L. Wei, J. Deng, L. W. Chang, K. Kim, C. T. Chuang, and H. S. P. Wong, "Selective Device Structure Scaling and Parasitics Engineering: A Way to Extend the Technology Roadmap," *IEEE Trans. on Electron Devices*, vol. 56, no. 2, pp. 312–320, 2009.

[68] F. Pellizzer, A. Benvenuti, B. Gleixner, Y. Kim, B. Johnson, M. Magistretti, T. Marangon, A. Pirovano, R. Bez, and G. Atwood, "A 90nm Phase Change Memory Technology for Stand-Alone Non-Volatile Memory Applications," in *Symp. on VLSI Tech.*, 2006, pp. 122–123.

[69] R. Bez, "Chalcogenide PCM: a memory technology for next decade," in *Int. Electron Devices Meeting*, Dec. 2009, pp. 1–4.

[70] J. H. Oh, J. H. Park, Y. S. Lim, H. S. Lim, Y. T. Oh, J. S. Kim, J. M. Shin, J. H. Park, Y. J. Song, K. C. Ryoo, D. W. Lim, S. S. Park, J. I. Kim, J. H. Kim, J. Yu, F. Yeung, C. W. Jeong, J. H. Kong, D. H. Kang, G. H. Koh, G. T. Jeong, H. S. Jeong, and K. Kim, "Full Integration of Highly Manufacturable 512Mb PRAM based on 90nm Technology," in *Int. Electron Devices Meeting*, Dec. 2006, pp. 1–4.

[71] J. K. Kim, H. G. Lee, S. Choi, and K. I. Bahng, "A PRAM and NAND Flash Hybrid Architecture for High-performance Embedded Storage Subsystems," in *Proc. of the ACM Int. Conf. on Embedded Soft.*, Oct. 2008, pp. 31–40.

[72] H. L. Lung, C. P. Miller, C. J. Chen, S. C. Lewis, J. Morrish, T. Perri, R. C. Jordan, H. Y. Ho, T. S. Chen, W. C. Chien, M. Drapa, T. Maffitt, J. Heath, Y. Nakamura, J. Okazawa, K. Hosokawa, M. BrightSky, R. Bruce, H. Y. Cheng, A. Ray, Y. H. Ho, C. W. Yeh, W. Kim, S. Kim, Y. Zhu, and C. Lam, "A Double-Data-Rate2 (DDR2) Interface Phase-Change Memory with 533MB/s Read -Write Data Rate and 37.5ns Access Latency for Memory-Type Storage Class Memory Applications," in *Int. Memory Workshop*, May 2016, pp. 1–5.

[73] M.-J. Lee, Y. Park, D.-S. Suh, E.-H. Lee, S. Seo, D.-C. Kim, R. Jung, B.-S. Kang, S.-E. Ahn, C. Lee, D. Seo, Y.-K. Cha, I.-K. Yoo, J.-S. Kim, and B. Park, "Two Series Oxide Resistors Applicable to High Speed and High Density Nonvolatile Memory," *Adv. Mater.*, vol. 19, no. 22, pp. 3919–3923, 2007.

[74] D. Kau, S. Tang, I. V. Karpov, R. Dodge, B. Klehn, J. A. Kalb, J. Strand, A. Diaz, N. Leung, J. Wu, S. Lee, T. Langtry, K.-W. Chang, C. Papagianni, J. Lee, J. Hirst, S. Erra, E. Flores, N. Righos, H. Castro, and G. Spadini, "A stackable cross point Phase Change Memory," in *Int. Electron Devices Meeting*, Dec. 2009, pp. 1–4.

[75] Y. Sasago, M. Kinoshita, T. Morikawa, K. Kurotsuchi, S. Hanzawa, T. Mine, A. Shima, Y. Fujisaki, H. Kume, H. Moriya, N. Takaura, and K. Torii, "Cross-point phase change memory with 4F2 cell size driven by low-contact-resistivity poly-Si diode," in *Symp. on VLSI Tech.*, Jun. 2009, pp. 24–25.

[76] K. Kurotsuchi, Y. Sasago, H. Yoshitake, H. Minemura, Y. Anzai, Y. Fujisaki, T. Takahama, T. Takahashi, T. Mine, A. Shima, K. Fujisaki, and T. Kobayashi, "2.8-GB/s-write and 670-MB/s-erase operations of a 3D vertical chain-cell-type phase-change-memory array," in *Symp. on VLSI Tech.*, Jun. 2015, pp. T92–T93.

[77] P. Cappelletti, "Non volatile memory evolution and revolution," in *Int. Electron Devices Meeting*, Dec. 2015, pp. 10.1.1–10.1.4.

[78] S. Lee, "Scaling Challenges in NAND Flash Device toward 10nm Technology," in *Int. Memory Workshop*, May 2012, pp. 1–4.

[79] HGST, "HGST Research Demonstrates World's Fastest SSD at Flash Memory Summit," [Online]. Available: https://www.hgst.com/company/media-room/press-releases/hgst-research-demonstrates-world-s-fastest-ssd-at-flash-memory-summit, 2014.

[80] Y. Liu, C. Zhou, and X. Cheng, "Hybrid SSD with PCM," in *Non-Volatile Memory Tech. Symp.*, Nov. 2011, pp. 1–5.

[81] M. Tarihi, H. Asadi, A. Haghdoost, M. Arjomand, and H. Sarbazi-Azad, "A Hybrid Non-Volatile Cache Design for Solid-State Drives Using Comprehensive I/O Characterization," *IEEE Trans. on Comp.*, vol. 65, no. 6, pp. 1678–1691, 2016.

[82] S. Eilert, M. Leinwander, and G. Crisenza, "Phase Change Memory: A New Memory Enables New Memory Usage Models," in *Int. Memory Workshop*, May 2009, pp. 1–2.

[83] Y. Huai, F. Albert, P. Nguyen, M. Pakala, and T. Valet, "Observation of spin-transfer switching in deep submicron-sized and low-resistance magnetic tunnel junctions," *Appl. Phys. Lett.*, vol. 84, no. 16, pp. 3118–3120, 2004.

[84] R. L. Stamps, S. Breitkreutz, J. kerman, A. V. Chumak, Y. Otani, G. E. W. Bauer, J.-U. Thiele, M. Bowen, S. A. Majetich, M. Klui, I. L. Prejbeanu, B. Dieny, N. M. Dempsey, and B. Hillebrands, "The 2014 Magnetism Roadmap," *J. of Phys. D: Appl. Phys.*, vol. 47, no. 33, p. 333001, 2014.

[85] S. Yuasa, T. Nagahama, A. Fukushima, Y. Suzuki, and K. Ando, "Giant room-temperature magnetoresistance in single-crystal Fe/MgO/Fe magnetic tunnel junctions," *Nat. Mater.*, vol. 3, no. 12, pp. 868–871, 2004.

[86] J. Slonczewski, "Current-driven excitation of magnetic multilayers," *J. of Magnetism and Magnetic Mater.*, vol. 159, no. 1, pp. L1–L7, 1996.

[87] I. M. Miron, K. Garello, G. Gaudin, P.-J. Zermatten, M. V. Costache, S. Auffret, S. Bandiera, B. Rodmacq, A. Schuhl, and P. Gambardella, "Perpendicular switching of a single ferromagnetic layer induced by in-plane current injection," *Nature*, vol. 476, no. 7359, pp. 189–193, 2011.

[88] I. L. Prejbeanu, W. Kula, K. Ounadjela, R. C. Sousa, O. Redon, B. Dieny, and J. P. Nozieres, "Thermally assisted switching in exchange-biased storage layer magnetic tunnel junctions," *IEEE Trans. on Magnetics*, vol. 40, no. 4, pp. 2625–2627, 2004.

[89] M. Gajek, J. J. Nowak, J. Z. Sun, P. L. Trouilloud, E. J. OSullivan, D. W. Abraham, M. C. Gaidis, G. Hu, S. Brown, Y. Zhu, R. P. Robertazzi, W. J. Gallagher, and D. C. Worledge, "Spin torque switching of 20 nm magnetic tunnel junctions with perpendicular anisotropy," *Appl. Phys. Lett.*, vol. 100, no. 13, 2012.

[90] S. Bandiera, R. C. Sousa, M. Marins de Castro, C. Ducruet, C. Portemont, S. Auffret, L. Vila, I. L. Prejbeanu, B. Rodmacq, and B. Dieny, "Spin transfer torque switching assisted by thermally induced anisotropy reorientation in perpendicular magnetic tunnel junctions," *Appl. Phys. Lett.*, vol. 99, no. 20, 2011.

[91] W.-G. Wang, M. Li, S. Hageman, and C. L. Chien, "Electric-field-assisted switching in magnetic tunnel junctions," *Nat. Mater.*, vol. 11, no. 1, pp. 64–68, 2012.

[92] S. S. P. Parkin, C. Kaiser, A. Panchula, P. M. Rice, B. Hughes, M. Samant, and S.-H. Yang, "Giant tunnelling magnetoresistance at room temperature with MgO (100) tunnel barriers," *Nat. Mater.*, vol. 3, no. 12, pp. 862–867, 2004.

[93] Z. Diao, Z. Li, S. Wang, Y. Ding, A. Panchula, E. Chen, L.-C. Wang, and Y. Huai, "Spin-transfer torque switching in magnetic tunnel junctions and spin-transfer torque random access memory," *J. of Phys.: Condensed Matter*, vol. 19, no. 16, p. 165209, 2007.

[94] A. A. Tulapurkar, T. Devolder, K. Yagami, P. Crozat, C. Chappert, A. Fukushima, and Y. Suzuki, "Subnanosecond magnetization reversal in magnetic nanopillars by spin angular momentum transfer," *Appl. Phys. Lett.*, vol. 85, no. 22, pp. 5358–5360, 2004.

[95] J. Z. Sun, "Spin-current interaction with a monodomain magnetic body: A model study," *Phys. Rev. B*, vol. 62, pp. 570–578, 2000.

[96] R. Heindl, W. H. Rippard, S. E. Russek, M. R. Pufall, and A. B. Kos, "Validity of the thermal activation model for spin-transfer torque switching in magnetic tunnel junctionsa)," *J. of Appl. Phys.*, vol. 109, no. 7, 2011.

[97] S. Amara-Dababi, R. C. Sousa, M. Chshiev, H. Ba, J. Alvarez-Hrault, L. Lombard, I. L. Prejbeanu, K. Mackay, and B. Dieny, "Charge trapping-detrapping mechanism of barrier breakdown in mgo magnetic tunnel junctions," *Appl. Phys. Lett.*, vol. 99, no. 8, 2011.

[98] T. Kawahara, R. Takemura, K. Miura, J. Hayakawa, S. Ikeda, Y. M. Lee, R. Sasaki, Y. Goto, K. Ito, T. Meguro, F. Matsukura, H. Takahashi, H. Matsuoka, and H. Ohno, "2 Mb SPRAM (SPin-Transfer Torque RAM) With Bit-by-Bit Bi-Directional Current Write and Parallelizing-Direction Current Read," *IEEE J. of Solid-State Circ.*, vol. 43, no. 1, pp. 109–120, 2008.

[99] Z. Li, B. Yan, L. Yang, W. Zhao, Y. Chen, and H. Li, "A new self-reference sensing scheme for TLC MRAM," in *Int. Symp. on Circ. and Sys.*, May 2015, pp. 593–596.

[100] H.-X. Liu, Y. Honda, T. Taira, K.-i. Matsuda, M. Arita, T. Uemura, and M. Yamamoto, "Giant tunneling magnetoresistance in epitaxial Co2MnSi/MgO/Co2MnSi magnetic tunnel junctions by half-metallicity of Co2MnSi and coherent tunneling," *Appl. Phys. Lett.*, vol. 101, no. 13, 2012.

[101] J. M. Slaughter, N. D. Rizzo, J. Janesky, R. Whig, F. B. Mancoff, D. Houssameddine, J. J. Sun, S. Aggarwal, K. Nagel, S. Deshpande, S. M. Alam, T. Andre, and P. LoPresti, "High density ST-MRAM technology," in *Int. Electron Devices Meeting*, Dec. 2012, pp. 29.3.1–29.3.4.

[102] N. D. Rizzo, D. Houssameddine, J. Janesky, R. Whig, F. B. Mancoff, M. L. Schneider, M. DeHerrera, J. J. Sun, K. Nagel, S. Deshpande, H. J. Chia, S. M. Alam, T. Andre, S. Aggarwal, and J. M. Slaughter, "A Fully Functional 64 Mb DDR3 ST-MRAM Built on 90 nm CMOS Technology," *IEEE Trans. on Magnetics*, vol. 49, no. 7, pp. 4441–4446, 2013.

[103] Everspin Technologies Inc., "Everspin Releases Highest Density MRAM Products to Create Fastest And Most Reliable Non-Volatile Storage Class Memory," [Online]. Available: https://www.everspin.com/file/965/download, 2016.

[104] D. Apalkov, B. Dieny, and J. M. Slaughter, "Magnetoresistive Random Access Memory," *Proc. of the IEEE*, vol. 104, no. 10, pp. 1796–1830, 2016.

[105] A. M. Caulfield, L. M. Grupp, and S. Swanson, "Gordon: Using Flash Memory to Build Fast, Power-efficient Clusters for Data-intensive Applications," *SIGARCH Comput. Archit. News*, vol. 37, no. 1, pp. 217–228, 2009.

[106] A. Gupta, Y. Kim, and B. Urgaonkar, "DFTL: A Flash Translation Layer Employing Demand-based Selective Caching of Page-level Address Mappings," *SIGARCH Comput. Archit. News*, vol. 37, no. 1, pp. 229–240, 2009.

[107] A. Leventhal, "Flash Storage Memory," *Commun. ACM*, vol. 51, no. 7, pp. 47–51, 2008.

[108] Y. Xie, "Modeling, Architecture, and Applications for Emerging Memory Technologies," *IEEE Design & Test of Comp.*, vol. 28, no. 1, pp. 44–51, 2011.

[109] C. Sun, T. O. Iwasaki, T. Onagi, K. Johguchi, and K. Takeuchi, "Cost, Capacity, and Performance Analyses for Hybrid SCM/NAND Flash SSD," *IEEE Trans. on Circ. and Sys. I: Regular Papers*, vol. 61, no. 8, pp. 2360–2369, Aug. 2014.

[110] G. Sun, Y. Joo, Y. Chen, D. Niu, Y. Xie, Y. Chen, and H. Li, "A hybrid solid-state storage architecture for the performance, energy consumption, and lifetime improvement," in *Int. Symp. on High Perf. Comp. Arch.*, Jan. 2010, pp. 1–12.

[111] S.-W. Lee and B. Moon, "Design of Flash-based DBMS: An In-page Logging Approach," in *Proc. ACM SIGMOD Int. Conf. on Management of Data*, Jun. 2007, pp. 55–66.

[112] Microsemi Corp., "Flashtec NVRAM Drives," [Online]. Available: http://www.microsemi.com/products/storage/flashtec-nvram-drives/flashtec-nvram-drives, 2016.

[113] C. Zambelli and P. Olivo, "Ssd reliability," in *Inside Solid State Drives (SSDs)*, R. Micheloni, A. Marelli, and K. Eshghi, Ed. Springer Netherlands, 2013, pp. 203–231.

[114] Samsung electronics Co., "Power loss protection (PLP) - Protect your data against sudden power loss," [Online]. Available: http://www.samsung.com/semiconductor/minisite/ssd/downloads/document/Samsung_SSD_845DC_05_Power_loss_protection_PLP.pdf, 2014.

[115] M. Ayadi, O. Briat, R. Lallemand, A. Eddahech, R. German, G. Coquery, and J. Vinassa, "Description of supercapacitor performance degradation rate during thermal cycling under constant voltage ageing test," *Microelectronics Reliability*, vol. 54, no. 9-10, pp. 1944–1948, 2014.

[116] K. Tsuchida, T. Inaba, K. Fujita, Y. Ueda, T. Shimizu, Y. Asao, T. Kajiyama, M. Iwayama, K. Sugiura, S. Ikegawa, T. Kishi, T. Kai, M. Amano, N. Shimomura, H. Yoda, and Y. Watanabe, "A 64Mb MRAM with clamped-reference and adequate-reference schemes," in *Int. Solid-State Circ. Conf.*, Feb. 2010, pp. 258–259.

[117] B. Schroeder and G. A. Gibson, "Understanding failures in petascale computers," *Journal of Physics: Conference Series*, vol. 78, no. 1, p. 012022, 2007.

[118] M. K. Qureshi, J. Karidis, M. Franceschini, V. Srinivasan, L. Lastras, and B. Abali, "Enhancing Lifetime and Security of PCM-based Main Memory with Start-gap Wear Leveling," in *Proc. Int. Symp. on Microarch.*, 2009, pp. 14–23.

[119] A. M. Caulfield, A. De, J. Coburn, T. I. Mollow, R. K. Gupta, and S. Swanson, "Moneta: A High-Performance Storage Array Architecture for Next-Generation, Non-volatile Memories," in *Proc. Int. Symp. on Microarch.*, 2010, pp. 385–395.

[120] L. Zuolo, C. Zambelli, R. Micheloni, S. Bates, and P. Olivo, "Design space exploration of latency and bandwidth in RRAM-based solid state drives," in *Non-Volatile Memory Tech. Symp.*, Oct. 2015, pp. 1–4.

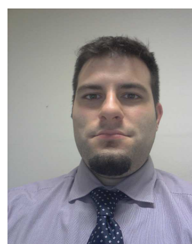
[121] L. Zuolo, C. Zambelli, A. Grossi, R. Micheloni, S. Bates, and P. Olivo, "Memory System Architecture Optimization for Enterprise All-RRAM Solid State Drives," in *Int. Memory Workshop*, May 2016, pp. 1–4.

[122] Micron Inc., "3D XPoint^{TM} technology," [Online]. Available: https://www.micron.com/about/emerging-technologies/3d-xpoint-technology, 2016.

[123] S. Seshadri, M. Gahagan, S. Bhaskaran, T. Bunker, A. De, Y. Jin, Y. Liu, and S. Swanson, "Willow: A User-programmable SSD," in *Proc. USENIX Conf. on Op. Sys. Design and Implementation*, 2014, pp. 67–80.

[124] J. Wang, D. Park, Y. Papakonstantinou, and S. Swanson, "SSD In-Storage Computing for Search Engines," *IEEE Trans. on Comp.*, 2016.

[125] J. Wang, D. Park, Y.-S. Kee, Y. Papakonstantinou, and S. Swanson, "SSD In-storage Computing for List Intersection," in *Proc. Int. Workshop on Data Management on New Hardware*, 2016, pp. 4:1–4:7.



Cristian Zambelli (SM'08-M'12) received the M.Sc., and the Ph.D. degrees in Electronic Engineering from Università degli Studi di Ferrara respectively in 2008, and 2012. Since 2015 he holds an Assistant Professor position with the Dipartimento di Ingegneria of the same institution. His main research interests are focused on the characterization, physics, and modeling of non-volatile memories reliability, and algorithmic solutions for reliability/performance trade-off exploitation in Solid State Drives. He is author of more than 65 papers published in international journals and proceedings of international conferences.

Gabriele Navarro received the Master degree in Microelectronic Engineering in 2007 and the Laurea degree in Physics in 2009 from the University of Padova (Italy). In 2013, he received the Ph.D. degree in Nanoelectronics from the Polytechnic Institute of Grenoble (France), with a work on the reliability analysis of embedded phase-change memories based on innovative materials. In 2014 he joined the Memory Devices Laboratory of CEA-LETI in Grenoble (France), and his research activities mainly involve the development, the fabrication and the characterization of innovative NVMs. His recent work focused on the reliability improvement of the Phase-Change Memory technology and on the development of innovative backend Selector devices, for both embedded and storage class applications. He is author/coauthor of more than 30 papers published in international journals and presented in international conferences.

Véronique Sousa graduated in 1994 from the Institut National Polytechnique de Grenoble (INPG) in the field of Materials Science and Engineering. During her PhD, which she received in 1997 from the INPG, she worked on the experimental and fundamental aspects of magnetic thin films with perpendicular anisotropy at CEA-INAC. Afterwards, she took a one-year post-doctoral position at INESC-Lisbon, and worked on various thin film materials used for magnetic data storage devices such as permanent magnets, spin valves or tunneling junctions. In October 1998, she joined the CEA-Leti-MINATEC-Campus, where she first focused on the development of advanced magneto-optical and phase change materials for optical data storage. Since then, she has led several projects aiming at the optimization of chalcogenide materials for various resistive memory technologies, including Current Bridging RAM and Phase Change Memories.

Luca Perniola was born in 1978 in Florence (Italy). He received the Laurea in nuclear engineering from the Politecnico di Milano (2002) and the Ph. D. degree from the University of Pisa and the Institut National Polytechnique de Grenoble (2005). In 2005 he was enrolled in the permanent staff of CEA-Leti, Grenoble, France. Since then he focused mainly on the electrical characterization and modeling of advanced Non-Volatile Memories (NVM) as Charge-Trap also in complex 3D device architectures (ie SONOS finfet and trigate), alternative to GST materials for phase-change memories and resistive RAM. Since 2013 he has been appointed head of the Advanced Memory Laboratory in Leti, mastering major NVM backend technologies, as RRAM, PCM and MRAM. Dr Perniola has published more than 100 papers on these topics. In the past he served as committee member of Memory Technology subcommittee at International Electron Device Meeting and currently he is committee member of the International Reliability Physics Symposium.

Ioan Lucian Prejbeanu has been conducting research on nanomagnetism and spintronics for more than 15 years. He holds a Physics degree from Babes Bolyai University in Cluj (Romania) and a PhD in Physics from Louis Pasteur University in Strasbourg where he pioneered the work on magnetic nanostructures. He then joined SPINTEC research laboratory in Grenoble, where he pioneered scientific work on thermally assisted MRAM, tackling the key long-standing problem of bits stable enough for long-term storage, yet still easy to write with small magnetic fields. Based on this proof-of-principle of the scientific concepts, Crocus Technology was founded in 2006 to develop and commercialize thermally assisted MRAM technology. Lucian joined Crocus Technology mid-2006 as R&D manager, where he made key contributions to the development and industrialization of thermally assisted MRAM for which he was awarded the SEE-IEEE Brillouin prize in 2012. In 2013, Lucian returns to Spintec as deputy director and became executive director as of January 1st, 2016, working on advanced STT-MRAM, hybrid CMOS-MRAM circuits and magnetic sensors. He holds 38 international patents on magnetic memories and has authored more than 70 scientific publications and book chapters on nanomagnetism and spintronics.